ADDENDUM
TMS320C54x, TMS320LC54x, TMS320VC54x DATA SHEET (SPRS039B)

This addendum provides current updated information regarding different speed performance versions and available derivative devices in the ’54x family.

This addendum provides changed dc characteristics and parameter data that apply to the 66 MIPS version of the TMS320LC541B8 devices only.

Data in the unshaded cells is new and applies only to the TMS320LC541B-66 device as indicated. The data in the shaded areas has not changed from that supplied in the current TMS320C54x, TMS320LC54x, TMS320VC54x datasheet (literature number SPRS039B). Please note the page numbers referenced apply to the SPRS039B datasheet.

switching characteristics over recommended operating conditions for a memory read ($\overline{\text{MSTRB}}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see Page 68)

PARAMETER		’54x-66		UNIT
		MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low§	– 2	4	ns
$t_{d(CLKH-A)}$	Delay time, address valid from CLKOUT high (transition)#	– 2	5	ns
$t_{d(CLKL-MSL)}$	Delay time, $\overline{\text{MSTRB}}$ low from CLKOUT low	– 2	3	ns
$t_{d(CLKL-MSH)}$	Delay time, $\overline{\text{MSTRB}}$ high from CLKOUT low	– 2	4	ns
$t_{h(CLKL-A)R}$	Hold time, address valid after CLKOUT low§	0	5¶	ns
$t_{h(CLKH-A)R}$	Hold time, address valid after CLKOUT high#	– 2	3¶	ns

timing requirements over recommended operating conditions for a memory read ($\overline{\text{MSTRB}}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see Page 69)

		’54x-66		UNIT
		MIN	MAX	
$t_{a(A)M}$	Access time, read data access from address valid		2H–9	ns
$t_{a(MSTRBL)}$	Access time, read data access from $\overline{\text{MSTRB}}$ low		2H–10	ns
$t_{su(D)R}$	Setup time, read data before CLKOUT low	5		ns
$t_{h(D)R}$	Hold time, read data after CLKOUT low	2		ns
$t_{h(A-D)R}$	Hold time, read data after address invalid	1		ns
$t_{h(D)MSTRBH}$	Hold time, read data after $\overline{\text{MSTRB}}$ high	0		ns

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switching characteristics over recommended operating conditions for a memory write ($\overline{MSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see Page 71)

PARAMETER		'54x-66		UNIT
		MIN	MAX	
$t_{d(CLKH-A)}$	Delay time, address valid from CLKOUT high§	– 2#	5	ns
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low¶	– 2	4	ns
$t_{d(CLKL-MSL)}$	Delay time, $\overline{MSTRB}$ low from CLKOUT low	– 2	3	ns
$t_{d(CLKL-D)W}$	Delay time, data valid from CLKOUT low	0#	6	ns
$t_{d(CLKL-MSH)}$	Delay time, $\overline{MSTRB}$ high from CLKOUT low	– 2	4	ns
$t_{d(CLKH-RWL)}$	Delay time, R/$\overline{W}$ low from CLKOUT high	– 2	3	ns
$t_{d(CLKH-RWH)}$	Delay time, R/$\overline{W}$ high from CLKOUT high	– 2	4	ns
$t_{d(RWL-MSTRBL)}$	Delay time, $\overline{MSTRB}$ low after R/$\overline{W}$ low#	H – 3	H + 2	ns
$t_{h(A)W}$	Hold time, address valid after CLKOUT high§	– 2	4	ns

switching characteristics over recommended operating conditions for a parallel I/O port read ($\overline{IOSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see Page 73)

PARAMETER		'54x-66		UNIT
		MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low	– 2	4	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, $\overline{IOSTRB}$ low from CLKOUT high	– 2	3	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, $\overline{IOSTRB}$ high from CLKOUT high	– 2	3	ns
$t_{h(A)IOR}$	Hold time, address after CLKOUT low	– 2	4	ns

timing requirements over recommended operating conditions for a parallel I/O port read ($\overline{IOSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see Page 74)

		'54x-66		UNIT
		MIN	MAX	
$t_{a(A)IO}$	Access time, read data access from address valid		3H–10	ns
$t_{a(ISTRBL)IO}$	Access time, read data access from $\overline{IOSTRB}$ low		2H–10	ns
$t_{su(D)IOR}$	Setup time, read data before CLKOUT high	5		ns
$t_{h(D)IOR}$	Hold time, read data after CLKOUT high	1		ns
$t_{h(ISTRBH-D)R}$	Hold time, read data after $\overline{IOSTRB}$ high	0		ns

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switching characteristics over recommended operating conditions for a parallel I/O port write ($\overline{IOSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$] (see Page 75)†

PARAMETER		’54x-66		UNIT
		MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low‡	– 2	4	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, $\overline{IOSTRB}$ low from CLKOUT high	–2	3	ns
$t_{d(CLKH-D)IOW}$	Delay time, write data valid from CLKOUT high	H–5§	H+8	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, $\overline{IOSTRB}$ high from CLKOUT high	–1	4	ns
$t_{d(CLKL-RWL)}$	Delay time, R/$\overline{W}$ low from CLKOUT low	– 2	3	ns
$t_{d(CLKL-RWH)}$	Delay time, R/$\overline{W}$ high from CLKOUT low	–2	5	ns
$t_{h(A)IOW}$	Hold time, address valid from CLKOUT low‡	– 2	4	ns
$t_{h(D)IOW}$	Hold time, write data after $\overline{IOSTRB}$ high	H–5	H+5§	ns
$t_{su(D)IOSTRBH}$	Setup time, write data before $\overline{IOSTRB}$ high	H–5	H	ns
$t_{su(A)IOSTRBL}$	Setup time, address valid before $\overline{IOSTRB}$ low§	H–5	H+5	ns

timing requirements over recommended operating conditions for externally generated wait states [H = 0.5 $t_{c(CO)}$]† (see Page 79)

		’54x-66		UNIT
		MIN	MAX	
$t_{su(RDY)}$	Setup time, READY before CLKOUT low	7		ns
$t_{h(RDY)}$	Hold time, READY after CLKOUT low	0		ns
$t_{v(RDY)MSTRB}$	Valid time, READY after $\overline{MSTRB}$ low§		4H–10	ns
$t_{h(RDY)MSTRB}$	Hold time, READY after $\overline{MSTRB}$ low§	4H		ns
$t_{v(RDY)IOSTRB}$	Valid time, READY after $\overline{IOSTRB}$ low§		5H–10	ns
$t_{h(RDY)IOSTRB}$	Hold time, READY after $\overline{IOSTRB}$ low§	5H		ns
$t_{v(MSCL)}$	Valid time, $\overline{MSC}$ low after CLKOUT low	–2	3	ns
$t_{v(MSCH)}$	Valid time, $\overline{MSC}$ high after CLKOUT low	–2‡	3	ns

switching characteristics over recommended operating conditions for $\overline{IAQ}$ and $\overline{IACK}$ [H = 0.5 $t_{c(CO)}$] (see Page 89)

PARAMETER		’54x-66		UNIT
		MIN	MAX	
$t_{d(CLKL-IAQL)}$	Delay time, $\overline{IAQ}$ low from CLKOUT low	– 1	5	ns
$t_{d(CLKL-IAQH)}$	Delay time, $\overline{IAQ}$ high from CLKOUT low	– 1	4	ns
$t_{d(A)IAQ}$	Delay time, address valid before $\overline{IAQ}$ low†		4	ns
$t_{d(CLKL-IACKL)}$	Delay time, $\overline{IACK}$ low from CLKOUT low	– 2	4	ns
$t_{d(CLKL-IACKH)}$	Delay time , $\overline{IACK}$ high from CLKOUT low	– 2†	4	ns
$t_{d(A)IACK}$	Delay time, address valid before $\overline{IACK}$ low†		3	ns
$t_{h(A)IAQ}$	Hold time, address valid after $\overline{IAQ}$ high†	– 4		ns
$t_{h(A)IACK}$	Hold time, address valid after $\overline{IACK}$ high†	– 3		ns
$t_{w(IAQL)}$	Pulse duration, $\overline{IAQ}$ low†	2H – 4		ns
$t_{w(IACKL)}$	Pulse duration, $\overline{IACK}$ low†	2H – 4		ns

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