Technical Reference Manual

J721E DRA829/TDA4VM/AM68P Processors Silicon Revision 1.1 Texas Instruments Families of Products

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1 System Interconnect Registers

1.1 QoS Registers

Table 1-2 through Table 1-28 list the memory-mapped QoS registers for the system interconnect initiators. All register offset addresses not listed in these tables should be considered as reserved locations and the register contents should not be modified.

Table 1-1. QoS Registers Instances

Instance	Base Address	CBASS_MAP_i Fields Availability
MCU_R5FSS0_CORE0_MEM_RD	45D1 0000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
MCU_R5FSS0_CORE0_MEM_WR	45D1 0400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
MCU_R5FSS0_CORE0_PER0	45D1 0800h	QOS, ORDERID, EPRIORITY
MCU_R5FSS0_CORE1_MEM_RD	45D1 1000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
MCU_R5FSS0_CORE1_MEM_WR	45D1 1400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
MCU_R5FSS0_CORE1_PER0	45D1 1800h	QOS, ORDERID, EPRIORITY
PRU_ICSSG0	45D8 0000h	ORDERID, EPRIORITY
PRU_ICSSG1	45D8 0400h	ORDERID, EPRIORITY
C66SS0_MDMA	45D8 1000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
C66SS1_MDMA	45D8 1400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
MMCSD1_RD	45D8 2000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
MMCSD1_WR	45D8 2400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
MMCSD2_RD	45D8 2800h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
MMCSD2_WR	45D8 2C00h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS0_CORE0_MEM_RD	45D8 4000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS0_CORE1_MEM_RD	45D8 4400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS0_CORE0_MEM_WR	45D8 4800h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS0_CORE1_MEM_WR	45D8 4C00h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS1_CORE0_MEM_RD	45D8 5000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS1_CORE1_MEM_RD	45D8 5400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS1_CORE0_MEM_WR	45D8 5800h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS1_CORE1_MEM_WR	45D8 5C00h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
COMPUTE_CLUSTER0_RD	45D8 6000h	QOS, ORDERID, EPRIORITY
COMPUTE_CLUSTER0_WR	45D8 6400h	QOS, ORDERID, EPRIORITY
C66SS0_CFG	45D8 7000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
C66SS1_CFG	45D8 7400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS0_CORE0_PER1_RD	45D8 9800h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS0_CORE1_PER1_RD	45D8 9C00h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS0_CORE0_PER1_WR	45D8 A000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS0_CORE1_PER1_WR	45D8 A400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS1_CORE0_PER1_RD	45D8 A800h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS1_CORE1_PER1_RD	45D8 AC00h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS1_CORE0_PER1_WR	45D8 B000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS1_CORE1_PER1_WR	45D8 B400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
VPFE0_DMA	45D8 C000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
PCIE0_RD_HP	45D9 0000h	QOS, ORDERID, EPRIORITY
PCIE0_RD_LP	45D9 0400h	QOS, ORDERID, EPRIORITY
PCIE0_WR_HP	45D9 0800h	QOS, ORDERID, EPRIORITY
PCIE0_WR_LP	45D9 0C00h	QOS, ORDERID, EPRIORITY
PCIE1_RD_HP	45D9 1000h	QOS, ORDERID, EPRIORITY
PCIE1_RD_LP	45D9 1400h	QOS, ORDERID, EPRIORITY

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Table 1-1. QoS Registers Instances (continued)

Instance	Base Address	CBASS_MAP_i Fields Availability
PCIE1_WR_HP	45D9 1800h	QOS, ORDERID, EPRIORITY
PCIE1_WR_LP	45D9 1C00h	QOS, ORDERID, EPRIORITY
PCIE2_RD_HP	45D9 2000h	QOS, ORDERID, EPRIORITY
PCIE2_RD_LP	45D9 2400h	QOS, ORDERID, EPRIORITY
PCIE2_WR_HP	45D9 2800h	QOS, ORDERID, EPRIORITY
PCIE2_WR_LP	45D9 2C00h	QOS, ORDERID, EPRIORITY
PCIE3_RD_HP	45D9 3000h	QOS, ORDERID, EPRIORITY
PCIE3_RD_LP	45D9 3400h	QOS, ORDERID, EPRIORITY
PCIE3_WR_HP	45D9 3800h	QOS, ORDERID, EPRIORITY
PCIE3_WR_LP	45D9 3C00h	QOS, ORDERID, EPRIORITY
USB3SS0_RD	45D9 8000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
USB3SS0_WR	45D9 8400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
USB3SS1_RD	45D9 8800h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
USB3SS1_WR	45D9 8C00h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
MLBSS0	45D9 9C00h	QOS, ORDERID, VIRTID, ATYPE
MMCSD0_RD	45D9 A000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
MMCSD0_WR	45D9 A400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
UFS0_RD	45D9 B000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
UFS0_WR	45D9 B400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
DEBUGSS0_RD	45DA 0000h	QOS, ORDERID, EPRIORITY
DEBUGSS0_WR	45DA 0400h	QOS, ORDERID, EPRIORITY
R5FSS0_CORE0_PER0	45DA 4000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS0_CORE1_PER0	45DA 4400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS1_CORE0_PER0	45DA 4800h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
R5FSS1_CORE1_PER0	45DA 4C00h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
DMPAC0_DATA	45DC 0000h	VIRTID, ATYPE
DECODER0_RD	45DC 0400h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
DECODER0_WR	45DC 0800h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
ENCODER0_RD	45DC 0C00h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
ENCODER0_WR	45DC 1000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
VPAC0_DATA0	45DC 1400h	VIRTID, ATYPE
VPAC0_DATA1	45DC 1800h	VIRTID, ATYPE
VPAC0_LDC0	45DC 1C00h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
DSS0_DMA	45DC 2000h	QOS, ORDERID, VIRTID, ATYPE
DSS0_FBDC	45DC 2400h	QOS, ORDERID, VIRTID, ATYPE
GPU0_M0_RD	45DC 5000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
GPU0_M0_WR	45DC 5800h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
GPU0_M1_RD	45DC 6000h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE
GPU0_M1_WR	45DC 6800h	QOS, ORDERID, EPRIORITY, VIRTID, ATYPE

Table 1-2. MCU_CBASS0 QoS Registers 1

Offset	Acronym	Register Name	MCU_R5FSS0_CORE0_MEM_RD Physical Address	MCU_R5FSS0_CORE0_MEM_WR Physical Address	MCU_R5FSS0_CORE0_PER0 Physical Address
0h + j*8	CBASS_GRP_MAP1_j	Group j Map Register 1	N/A	N/A	N/A
4h + j*8	CBASS_GRP_MAP2_j	Group j Map Register 2	N/A	N/A	N/A

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Table 1-2. MCU_CBASS0 QoS Registers 1 (continued)

Offset	Acronym	Register Name	MCU_R5FSS0_CORE0_MEM_RD Physical Address	MCU_R5FSS0_CORE0_MEM_WR Physical Address	MCU_R5FSS0_CORE0_PER0 Physical Address
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D1 0100h + i*4	45D1 0500h + i*4	45D1 0900h + i*4

(1) i = 0 for MCU_R5FSS0_CORE0_PER0
i = 0 for MCU_R5FSS0_CORE0_MEM_WR
i = 0 for MCU_R5FSS0_CORE0_MEM_RD

Table 1-3. MCU_CBASS0 QoS Registers 2

Offset	Acronym	Register Name	MCU_R5FSS0_CORE1_MEM_RD Physical Address	MCU_R5FSS0_CORE1_MEM_WR Physical Address	MCU_R5FSS0_CORE1_PER0 Physical Address
0h + j*8	CBASS_GRP_MAP1_j	Group j Map Register 1	N/A	N/A	N/A
4h + j*8	CBASS_GRP_MAP2_j	Group j Map Register 2	N/A	N/A	N/A
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D1 1100h + i*4	45D1 1500h + i*4	45D1 1900h + i*4

(1) i = 0 for MCU_R5FSS0_CORE1_MEM_RD
i = 0 for MCU_R5FSS0_CORE1_MEM_WR
i = 0 for MCU_R5FSS0_CORE1_PER0

Table 1-4. CBASS0 QoS Registers 1

Offset	Acronym	Register Name	PRU_ICSSG0 Physical Address	PRU_ICSSG1 Physical Address	C66SS0_MDMA Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D8 0000h + j*8	45D8 0400h + j*8	45D8 1000h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D8 0004h + j*8	45D8 0404h + j*8	45D8 1004h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D8 0100h + i*4	45D8 0500h + i*4	45D8 1100h + i*4

(1) j = 0 to 2 for C66SS0_MDMA, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for PRU_ICSSG0, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for PRU_ICSSG1, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
i = 0 for C66SS0_MDMA
i = 0 to 9 for PRU_ICSSG0
i = 0 to 9 for PRU_ICSSG1

Table 1-5. CBASS0 QoS Registers 2

Offset	Acronym	Register Name	C66SS1_MDMA Physical Address	MMCSD1_RD Physical Address	MMCSD1_WR Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D8 1400h + j*8	45D8 2000h + j*8	45D8 2400h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D8 1404h + j*8	45D8 2004h + j*8	45D8 2404h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D8 1500h + i*4	45D8 2100h + i*4	45D8 2500h + i*4

(1) j = 0 to 2 for MMCSD1_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for C66SS1_MDMA, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for MMCSD1_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
i = 0 for MMCSD1_WR
i = 0 for C66SS1_MDMA
i = 0 for MMCSD1_RD

Table 1-6. CBASS0 QoS Registers 3

Offset	Acronym	Register Name	MMCSD2_RD Physical Address	MMCSD2_WR Physical Address	R5FSS0_CORE0_MEM_RD Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D8 2800h + j*8	45D8 2C00h + j*8	45D8 4000h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D8 2804h + j*8	45D8 2C04h + j*8	45D8 4004h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D8 2900h + i*4	45D8 2D00h + i*4	45D8 4100h + i*4

(1) j = 0 to 2 for MMCSD2_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for MMCSD2_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR

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j = 0 to 2 for R5FSS0_CORE0_MEM_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
i = 0 for MMCSD2_RD
i = 0 for MMCSD2_WR
i = 0 for R5FSS0_CORE0_MEM_RD

Table 1-7. CBASS0 QoS Registers 4

Offset	Acronym	Register Name	R5FSS0_CORE1_MEM_RD Physical Address	R5FSS0_CORE0_MEM_WR Physical Address	R5FSS0_CORE1_MEM_WR Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D8 4400h + j*8	45D8 4800h + j*8	45D8 4C00h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D8 4404h + j*8	45D8 4804h + j*8	45D8 4C04h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D8 4500h + i*4	45D8 4900h + i*4	45D8 4D00h + i*4

(1) j = 0 to 2 for R5FSS0_CORE1_MEM_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for R5FSS0_CORE1_MEM_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for R5FSS0_CORE0_MEM_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
i = 0 for R5FSS0_CORE1_MEM_RD
i = 0 for R5FSS0_CORE1_MEM_WR
i = 0 for R5FSS0_CORE0_MEM_WR

Table 1-8. CBASS0 QoS Registers 5

Offset	Acronym	Register Name	R5FSS1_CORE0_MEM_RD Physical Address	R5FSS1_CORE1_MEM_RD Physical Address	R5FSS1_CORE0_MEM_WR Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D8 5000h + j*8	45D8 5400h + j*8	45D8 5800h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D8 5004h + j*8	45D8 5404h + j*8	45D8 5804h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D8 5100h + i*4	45D8 5500h + i*4	45D8 5900h + i*4

(1) j = 0 to 2 for R5FSS1_CORE1_MEM_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for R5FSS1_CORE0_MEM_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for R5FSS1_CORE0_MEM_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
i = 0 for R5FSS1_CORE1_MEM_RD
i = 0 for R5FSS1_CORE0_MEM_RD
i = 0 for R5FSS1_CORE0_MEM_WR

Table 1-9. CBASS0 QoS Registers 6

Offset	Acronym	Register Name	R5FSS1_CORE1_MEM_WR Physical Address	COMPUTE_CLUSTER0_RD Physical Address	COMPUTE_CLUSTER0_WR Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D8 5C00h + j*8	45D8 6000h + j*8	45D8 6400h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D8 5C04h + j*8	45D8 6004h + j*8	45D8 6404h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D8 5D00h + i*4	45D8 6100h + i*4	45D8 6500h + i*4

(1) j = 0 to 2 for R5FSS1_CORE1_MEM_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for COMPUTE_CLUSTER0_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for COMPUTE_CLUSTER0_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
i = 0 for R5FSS1_CORE1_MEM_WR
i = 0 for COMPUTE_CLUSTER0_WR
i = 0 for COMPUTE_CLUSTER0_RD

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Table 1-10. CBASS0 QoS Registers 7

Offset	Acronym	Register Name	C66SS0_CFG Physical Address	C66SS1_CFG Physical Address	R5FSS0_CORE0_PER1_RD Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D8 7000h + j*8	45D8 7400h + j*8	45D8 9800h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D8 7004h + j*8	45D8 7404h + j*8	45D8 9804h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D8 7100h + i*4	45D8 7500h + i*4	45D8 9900h + i*4

(1) j = 0 to 2 for C66SS1_CFG, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for C66SS0_CFG, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for R5FSS0_CORE0_PER1_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
i = 0 for C66SS1_CFG
i = 0 for C66SS0_CFG
i = 0 for R5FSS0_CORE0_PER1_RD

Table 1-11. CBASS0 QoS Registers 8

Offset	Acronym	Register Name	R5FSS0_CORE1_PER1_RD Physical Address	R5FSS0_CORE0_PER1_WR Physical Address	R5FSS0_CORE1_PER1_WR Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D8 9C00h + j*8	45D8 A000h + j*8	45D8 A400h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D8 9C04h + j*8	45D8 A004h + j*8	45D8 A404h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D8 9D00h + i*4	45D8 A100h + i*4	45D8 A500h + i*4

(1) j = 0 to 2 for R5FSS0_CORE1_PER1_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for R5FSS0_CORE0_PER1_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for R5FSS0_CORE1_PER1_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
i = 0 for R5FSS0_CORE1_PER1_RD
i = 0 for R5FSS0_CORE0_PER1_WR
i = 0 for R5FSS0_CORE1_PER1_WR

Table 1-12. CBASS0 QoS Registers 9

Offset	Acronym	Register Name	R5FSS1_CORE0_PER1_RD Physical Address	R5FSS1_CORE1_PER1_RD Physical Address	R5FSS1_CORE0_PER1_WR Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D8 A800h + j*8	45D8 AC00h + j*8	45D8 B000h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D8 A804h + j*8	45D8 AC04h + j*8	45D8 B004h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D8 A900h + i*4	45D8 AD00h + i*4	45D8 B100h + i*4

(1) j = 0 to 2 for R5FSS1_CORE1_PER1_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for R5FSS1_CORE0_PER1_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for R5FSS1_CORE0_PER1_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
i = 0 for R5FSS1_CORE1_PER1_RD
i = 0 for R5FSS1_CORE0_PER1_WR
i = 0 for R5FSS1_CORE0_PER1_RD

Table 1-13. CBASS0 QoS Registers 10

Offset	Acronym	Register Name	R5FSS1_CORE1_PER1_WR Physical Address	VPFE0_DMA Physical Address	PCIE0_RD_HP Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D8 B400h + j*8	45D8 C000h + j*8	45D9 0000h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D8 B404h + j*8	45D8 C004h + j*8	45D9 0004h + j*8

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Table 1-13. CBASS0 QoS Registers 10 (continued)

Offset	Acronym	Register Name	R5FSS1_CORE1_PER1_WR Physical Address	VPFE0_DMA Physical Address	PCIE0_RD_HP Physical Address
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D8 B500h + i*4	45D8 C100h + i*4	45D9 0100h + i*4

(1) j = 0 to 2 for VPFE0_DMA, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 2 for R5FSS1_CORE1_PER1_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_RC_TO_HC; 2 = group GR_NAVSS_DDR
j = 0 to 3 for PCIE0_RD_HP, where 0 = group GR_HC_TO_RC; 1 = group PCIE_SLV1; 2 = group PCIE_SLV2; 3 = group PCIE_SLV3
i = 0 for VPFE0_DMA
i = 0 for R5FSS1_CORE1_PER1_WR
i = 0 to 3 for PCIE0_RD_HP

Table 1-14. CBASS0 QoS Registers 11

Offset	Acronym	Register Name	PCIE0_RD_LP Physical Address	PCIE0_WR_HP Physical Address	PCIE0_WR_LP Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D9 0400h + j*8	45D9 0800h + j*8	45D9 0C00h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D9 0404h + j*8	45D9 0804h + j*8	45D9 0C04h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D9 0500h + i*4	45D9 0900h + i*4	45D9 0D00h + i*4

(1) j = 0 to 3 for PCIE0_RD_LP, where 0 = group GR_HC_TO_RC; 1 = group PCIE_SLV1; 2 = group PCIE_SLV2; 3 = group PCIE_SLV3
j = 0 to 3 for PCIE0_WR_LP, where 0 = group GR_HC_TO_RC; 1 = group PCIE_SLV1; 2 = group PCIE_SLV2; 3 = group PCIE_SLV3
j = 0 to 3 for PCIE0_WR_HP, where 0 = group GR_HC_TO_RC; 1 = group PCIE_SLV1; 2 = group PCIE_SLV2; 3 = group PCIE_SLV3
i = 0 to 3 for PCIE0_RD_LP
i = 0 to 3 for PCIE0_WR_LP
i = 0 to 3 for PCIE0_WR_HP

Table 1-15. CBASS0 QoS Registers 12

Offset	Acronym	Register Name	PCIE1_RD_HP Physical Address	PCIE1_RD_LP Physical Address	PCIE1_WR_HP Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D9 1000h + j*8	45D9 1400h + j*8	45D9 1800h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D9 1004h + j*8	45D9 1404h + j*8	45D9 1804h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D9 1100h + i*4	45D9 1500h + i*4	45D9 1900h + i*4

(1) j = 0 to 3 for PCIE1_RD_LP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV2; 3 = group PCIE_SLV3
j = 0 to 3 for PCIE1_WR_HP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV2; 3 = group PCIE_SLV3
j = 0 to 3 for PCIE1_RD_HP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV2; 3 = group PCIE_SLV3
i = 0 to 3 for PCIE1_RD_LP
i = 0 to 3 for PCIE1_WR_HP
i = 0 to 3 for PCIE1_RD_HP

Table 1-16. CBASS0 QoS Registers 13

Offset	Acronym	Register Name	PCIE1_WR_LP Physical Address	PCIE2_RD_HP Physical Address	PCIE2_RD_LP Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D9 1C00h + j*8	45D9 2000h + j*8	45D9 2400h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D9 1C04h + j*8	45D9 2004h + j*8	45D9 2404h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D9 1D00h + i*4	45D9 2100h + i*4	45D9 2500h + i*4

(1) j = 0 to 3 for PCIE2_RD_HP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV1; 3 = group PCIE_SLV3
j = 0 to 3 for PCIE2_RD_LP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV1; 3 = group PCIE_SLV3
j = 0 to 3 for PCIE1_WR_LP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV2; 3 = group PCIE_SLV3
i = 0 to 3 for PCIE2_RD_HP
i = 0 to 3 for PCIE2_RD_LP
i = 0 to 3 for PCIE1_WR_LP

Table 1-17. CBASS0 QoS Registers 14

Offset	Acronym	Register Name	PCIE2_WR_HP Physical Address	PCIE2_WR_LP Physical Address	PCIE3_RD_HP Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D9 2800h + j*8	45D9 2C00h + j*8	45D9 3000h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D9 2804h + j*8	45D9 2C04h + j*8	45D9 3004h + j*8

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Table 1-17. CBASS0 QoS Registers 14 (continued)

Offset	Acronym	Register Name	PCIE2_WR_HP Physical Address	PCIE2_WR_LP Physical Address	PCIE3_RD_HP Physical Address
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D9 2900h + i*4	45D9 2D00h + i*4	45D9 3100h + i*4

(1) j = 0 to 3 for PCIE2_WR_HP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV1; 3 = group PCIE_SLV3
j = 0 to 3 for PCIE3_RD_HP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV1; 3 = group PCIE_SLV2
j = 0 to 3 for PCIE2_WR_LP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV1; 3 = group PCIE_SLV3
i = 0 to 3 for PCIE2_WR_HP
i = 0 to 3 for PCIE3_RD_HP
i = 0 to 3 for PCIE2_WR_LP

Table 1-18. CBASS0 QoS Registers 15

Offset	Acronym	Register Name	PCIE3_RD_LP Physical Address	PCIE3_WR_HP Physical Address	PCIE3_WR_LP Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D9 3400h + j*8	45D9 3800h + j*8	45D9 3C00h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D9 3404h + j*8	45D9 3804h + j*8	45D9 3C04h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D9 3500h + i*4	45D9 3900h + i*4	45D9 3D00h + i*4

(1) j = 0 to 3 for PCIE3_WR_LP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV1; 3 = group PCIE_SLV2
j = 0 to 3 for PCIE3_WR_HP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV1; 3 = group PCIE_SLV2
j = 0 to 3 for PCIE3_RD_LP, where 0 = group PCIE_SLV0; 1 = group GR_HC_TO_RC; 2 = group PCIE_SLV1; 3 = group PCIE_SLV2
i = 0 to 3 for PCIE3_WR_LP
i = 0 to 3 for PCIE3_WR_HP
i = 0 to 3 for PCIE3_RD_LP

Table 1-19. CBASS0 QoS Registers 16

Offset	Acronym	Register Name	USB3SS0_RD Physical Address	USB3SS0_WR Physical Address	USB3SS1_RD Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D9 8000h + j*8	45D9 8400h + j*8	45D9 8800h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D9 8004h + j*8	45D9 8404h + j*8	45D9 8804h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D9 8100h + i*4	45D9 8500h + i*4	45D9 8900h + i*4

(1) j = 0 for USB3SS0_WR, where 0 = group GR_HC2_TO_HC
j = 0 for USB3SS1_RD, where 0 = group GR_HC2_TO_HC
j = 0 for USB3SS0_RD, where 0 = group GR_HC2_TO_HC
i = 0 to 7 for USB3SS0_WR
i = 0 to 7 for USB3SS1_RD
i = 0 to 7 for USB3SS0_RD

Table 1-20. CBASS0 QoS Registers 17

Offset	Acronym	Register Name	USB3SS1_WR Physical Address	MLBSS0 Physical Address	MMCSD0_RD Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D9 8C00h + j*8	45D9 9C00h + j*8	45D9 A000h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D9 8C04h + j*8	45D9 9C04h + j*8	45D9 A004h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D9 8D00h + i*4	45D9 9D00h + i*4	45D9 A100h + i*4

(1) j = 0 for MLBSS0, where 0 = group GR_HC2_TO_HC
j = 0 for MMCSD0_RD, where 0 = group GR_HC2_TO_HC
j = 0 for USB3SS1_WR, where 0 = group GR_HC2_TO_HC
i = 0 for MLBSS0
i = 0 for MMCSD0_RD
i = 0 to 7 for USB3SS1_WR

Table 1-21. CBASS0 QoS Registers 18

Offset	Acronym	Register Name	MMCSD0_WR Physical Address	UFS0_RD Physical Address	UFS0_WR Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45D9 A400h + j*8	45D9 B000h + j*8	45D9 B400h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45D9 A404h + j*8	45D9 B004h + j*8	45D9 B404h + j*8

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Table 1-21. CBASS0 QoS Registers 18 (continued)

Offset	Acronym	Register Name	MMCSD0_WR Physical Address	UFS0_RD Physical Address	UFS0_WR Physical Address
100h + i*4	CBASS_MAP_i (1)	Map Register i	45D9 A500h + i*4	45D9 B100h + i*4	45D9 B500h + i*4

(1) j = 0 for UFS0_WR, where 0 = group GR_HC2_TO_HC
j = 0 for UFS0_RD, where 0 = group GR_HC2_TO_HC
j = 0 for MMCSD0_WR, where 0 = group GR_HC2_TO_HC
i = 0 to 3 for UFS0_WR
i = 0 for UFS0_RD
i = 0 for MMCSD0_WR

Table 1-22. CBASS0 QoS Registers 19

Offset	Acronym	Register Name	DEBUGSS0_RD Physical Address	DEBUGSS0_WR Physical Address	R5FSS0_CORE0_PER0 Physical Address
0h + j*8	CBASS_GRP_MAP1_j	Group j Map Register 1	N/A	N/A	N/A
4h + j*8	CBASS_GRP_MAP2_j	Group j Map Register 2	N/A	N/A	N/A
100h + i*4	CBASS_MAP_i (1)	Map Register i	45DA 0100h + i*4	45DA 0500h + i*4	45DA 4100h + i*4

(1) i = 0 for DEBUGSS0_RD
i = 0 for DEBUGSS0_WR
i = 0 for R5FSS0_CORE0_PER0

Table 1-23. CBASS0 QoS Registers 20

Offset	Acronym	Register Name	R5FSS0_CORE1_PER0 Physical Address	R5FSS1_CORE0_PER0 Physical Address	R5FSS1_CORE1_PER0 Physical Address
0h + j*8	CBASS_GRP_MAP1_j	Group j Map Register 1	N/A	N/A	N/A
4h + j*8	CBASS_GRP_MAP2_j	Group j Map Register 2	N/A	N/A	N/A
100h + i*4	CBASS_MAP_i (1)	Map Register i	45DA 4500h + i*4	45DA 4900h + i*4	45DA 4D00h + i*4

(1) i = 0 for R5FSS0_CORE1_PER0
i = 0 for R5FSS1_CORE1_PER0
i = 0 for R5FSS1_CORE0_PER0

Table 1-24. CBASS0 QoS Registers 21

Offset	Acronym	Register Name	ENCODER0_WR Physical Address	DECODER0_RD Physical Address	DECODER0_WR Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45DC 1000h + j*8	45DC 0400h + j*8	45DC 0800h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45DC 1004h + j*8	45DC 0404h + j*8	45DC 0804h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45DC 1100h + i*4	45DC 0500h + i*4	45DC 0900h + i*4

(1) j = 0 to 1 for DECODER0_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
j = 0 to 1 for DECODER0_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
j = 0 to 1 for ENCODER0_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
i = 0 for DECODER0_RD
i = 0 for DECODER0_WR
i = 0 to 4 for ENCODER0_WR

Table 1-25. CBASS0 QoS Registers 22

Offset	Acronym	Register Name	VPAC0_DATA0 Physical Address	DMPAC0_DATA Physical Address	ENCODER0_RD Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	N/A	N/A	45DC 0C00h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	N/A	N/A	45DC 0C04h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45DC 1500h + i*4	45DC 0100h + i*4	45DC 0D00h + i*4

(1) j = 0 to 1 for ENCODER0_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
i = 0 to 4 for ENCODER0_RD
i = 0 to 31 for VPAC0_DATA0

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i = 0 to 31 for DMPAC0_DATA

Table 1-26. CBASS0 QoS Registers 23

Offset	Acronym	Register Name	VPAC0_DATA1 Physical Address	VPAC0_LDC0 Physical Address	DSS0_DMA Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	N/A	45DC 1C00h + j*8	45DC 2000h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	N/A	45DC 1C04h + j*8	45DC 2004h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45DC 1900h + i*4	45DC 1D00h + i*4	45DC 2100h + i*4

(1) j = 0 to 1 for DSS0_DMA, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
j = 0 to 1 for VPAC0_LDC0, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
i = 0 to 9 for DSS0_DMA
i = 0 to 63 for VPAC0_DATA1
i = 0 to 2 for VPAC0_LDC0

Table 1-27. CBASS0 QoS Registers 24

Offset	Acronym	Register Name	DSS0_FBDC Physical Address	GPU0_M0_RD Physical Address	GPU0_M0_WR Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45DC 2400h + j*8	45DC 5000h + j*8	45DC 5800h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45DC 2404h + j*8	45DC 5004h + j*8	45DC 5804h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45DC 2500h + i*4	45DC 5100h + i*4	45DC 5900h + i*4

(1) j = 0 to 1 for GPU0_M0_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
j = 0 to 1 for GPU0_M0_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
j = 0 to 1 for DSS0_FBDC, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
i = 0 to 47 for GPU0_M0_WR
i = 0 to 47 for GPU0_M0_RD
i = 0 to 9 for DSS0_FBDC

Table 1-28. CBASS0 QoS Registers 25

Offset	Acronym	Register Name	GPU0_M1_RD Physical Address	GPU0_M1_WR Physical Address
0h + j*8	CBASS_GRP_MAP1_j (1)	Group j Map Register 1	45DC 6000h + j*8	45DC 6800h + j*8
4h + j*8	CBASS_GRP_MAP2_j (1)	Group j Map Register 2	45DC 6004h + j*8	45DC 6804h + j*8
100h + i*4	CBASS_MAP_i (1)	Map Register i	45DC 6100h + i*4	45DC 6900h + i*4

(1) j = 0 to 1 for GPU0_M1_RD, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
j = 0 to 1 for GPU0_M1_WR, where 0 = group GR_NAVSS_SRAM; 1 = group GR_NAVSS_DDR
i = 0 to 47 for GPU0_M1_RD
i = 0 to 47 for GPU0_M1_WR

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1.1.1 CBASS_GRP_MAP1_j Register (Offset = 0h + j*8) [reset = 0h]

CBASS_GRP_MAP1_j is shown in Figure 1-1 and described in Table 1-30.

Return to Summary Table.

The Group Map Register 1 defines the final order ID for the initiator group j from input order ID values of 0 to 7.

Table 1-29. CBASS_GRP_MAP1_j Instances

Instance	Base Address
See Table 1-2 through Table 1-28	See Table 1-2 through Table 1-28

Figure 1-1. CBASS_GRP_MAP1_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ORDERID7				ORDERID6				ORDERID5				ORDERID4			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ORDERID3				ORDERID2				ORDERID1				ORDERID0			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-30. CBASS_GRP_MAP1_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	ORDERID7	R/W	0h	Final order ID value for initial order ID value of 7.
27-24	ORDERID6	R/W	0h	Final order ID value for initial order ID value of 6.
23-20	ORDERID5	R/W	0h	Final order ID value for initial order ID value of 5.
19-16	ORDERID4	R/W	0h	Final order ID value for initial order ID value of 4.
15-12	ORDERID3	R/W	0h	Final order ID value for initial order ID value of 3.
11-8	ORDERID2	R/W	0h	Final order ID value for initial order ID value of 2.
7-4	ORDERID1	R/W	0h	Final order ID value for initial order ID value of 1.
3-0	ORDERID0	R/W	0h	Final order ID value for initial order ID value of 0.

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1.1.2 CBASS_GRP_MAP2_j Register (Offset = 4h + j*8) [reset = 0h]

CBASS_GRP_MAP2_j is shown in Figure 1-2 and described in Table 1-32.

Return to Summary Table.

The Group Map Register 2 defines the final order ID for the initiator group j from input order ID values of 8 to 15.

Table 1-31. CBASS_GRP_MAP2_j Instances

Instance	Base Address
See Table 1-2 through Table 1-28	See Table 1-2 through Table 1-28

Figure 1-2. CBASS_GRP_MAP2_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ORDERID15				ORDERID14				ORDERID13				ORDERID12			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ORDERID11				ORDERID10				ORDERID9				ORDERID8			
R/W-0h				R/W-0h				R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-32. CBASS_GRP_MAP2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	ORDERID15	R/W	0h	Final order ID value for initial order ID value of 15.
27-24	ORDERID14	R/W	0h	Final order ID value for initial order ID value of 14.
23-20	ORDERID13	R/W	0h	Final order ID value for initial order ID value of 13.
19-16	ORDERID12	R/W	0h	Final order ID value for initial order ID value of 12.
15-12	ORDERID11	R/W	0h	Final order ID value for initial order ID value of 11.
11-8	ORDERID10	R/W	0h	Final order ID value for initial order ID value of 10.
7-4	ORDERID9	R/W	0h	Final order ID value for initial order ID value of 9.
3-0	ORDERID8	R/W	0h	Final order ID value for initial order ID value of 8.

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1.1.3 CBASS_MAP_i Register (Offset = 100h + i*4) [reset = X]

CBASS_MAP_i is shown in Figure 1-3 and described in Table 1-34.

Return to Summary Table.

The Map Register defines the fields for the initiator per channel.

Table 1-33. CBASS_MAP_i Instances

Instance	Base Address
See Table 1-2 through Table 1-28	See Table 1-2 through Table 1-28

Figure 1-3. CBASS_MAP_i Register

31	30	29	28	27	26	25	24
RESERVED		ATYPE		VIRTID			
R/W-X		R/W-0h		R/W-0h			
23	22	21	20	19	18	17	16
VIRTID							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	EPRIORITY			RESERVED			
R/W-X	R/W-7h			R/W-X			
7	6	5	4	3	2	1	0
ORDERID				RESERVED	QOS		
R/W-0h				R/W-X	R/W-0h		

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-34. CBASS_MAP_i Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R/W	X	
29-28	ATYPE(1)	R/W	0h	atype signal for channel "i". 0h = Not translated physical 1h = Intermediate 2h = Virtual 3h = Translated physical
27-16	VIRTID(1)	R/W	0h	virtid signal for channel "i".
15	RESERVED	R/W	X	
14-12	EPRIORITY(1)	R/W	7h	epriority signal for channel "i".
11-8	RESERVED	R/W	X	
7-4	ORDERID(1)	R/W	0h	orderid signal for channel "i".
3	RESERVED	R/W	X	
2-0	QOS(1)	R/W	0h	qos signal for channel "i".

(1) These fields are not available for all initiators. See column "**CBASS_MAP_i Fields Availability**" in Table 1-1 for more information.

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1.2 Firewall Exception Registers

Table 1-36 through Table 1-40 list the memory-mapped firewall exception registers for the system interconnect instances. All register offset addresses not listed in these tables should be considered as reserved locations and the register contents should not be modified.

Table 1-35. Firewall Exception Registers Instances

Instance	Base Address
CBASS_AC0_GLB	45B0 8000h
CBASS_INFRA0_GLB	45B0 C000h
CBASS_AASRC0_GLB	45B2 0000h
CBASS_CSI0_GLB	45B2 0400h
CBASS_DATADEBUG0_GLB	45B2 0800h
CBASS_HC0_GLB	45B2 0C00h
CBASS_HC_CFG0_GLB	45B2 1000h
CBASS_IPPHY0_GLB	45B2 1400h
CBASS_MCASP_G0_0_GLB	45B2 1800h
CBASS_MCASP_G1_0_GLB	45B2 1C00h
CBASS_RC0_GLB	45B2 2000h
CBASS_RC_CFG0_GLB	45B2 2400h
CBASS_HC2_0_GLB	45B2 2800h

Table 1-36. Firewall Exception Registers 1

Offset	Acronym	Register Name	CBASS_AC0_GLB Physical Address	CBASS_INFRA0_GLB Physical Address	CBASS_AASRC0_GLB Physical Address
0h	CBASS_PID	Revision Register	45B0 8000h	45B0 C000h	45B2 0000h
4h	CBASS_DESTINATION_ID	Destination ID Register	45B0 8004h	45B0 C004h	45B2 0004h
20h	CBASS_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	45B0 8020h	45B0 C020h	45B2 0020h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	45B0 8024h	45B0 C024h	45B2 0024h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	45B0 8028h	45B0 C028h	45B2 0028h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	45B0 802Ch	45B0 C02Ch	45B2 002Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	45B0 8030h	45B0 C030h	45B2 0030h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	45B0 8034h	45B0 C034h	45B2 0034h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	45B0 8038h	45B0 C038h	45B2 0038h
40h	CBASS_EXCEPTION_PEND_SET	Exception Logging Pending Set Register	45B0 8040h	45B0 C040h	45B2 0040h
44h	CBASS_EXCEPTION_PEND_CLEAR	Exception Logging Pending Clear Register	45B0 8044h	45B0 C044h	45B2 0044h

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Table 1-37. Firewall Exception Registers 2

Offset	Acronym	Register Name	CBASS_CSI0_GLB Physical Address	CBASS_DATADEBUG0_GLB Physical Address	CBASS_HC0_GLB Physical Address
0h	CBASS_PID	Revision Register	45B2 0400h	45B2 0800h	45B2 0C00h
4h	CBASS_DESTINATION_ID	Destination ID Register	45B2 0404h	45B2 0804h	45B2 0C04h
20h	CBASS_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	45B2 0420h	45B2 0820h	45B2 0C20h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	45B2 0424h	45B2 0824h	45B2 0C24h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	45B2 0428h	45B2 0828h	45B2 0C28h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	45B2 042Ch	45B2 082Ch	45B2 0C2Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	45B2 0430h	45B2 0830h	45B2 0C30h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	45B2 0434h	45B2 0834h	45B2 0C34h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	45B2 0438h	45B2 0838h	45B2 0C38h
40h	CBASS_EXCEPTION_PEND_SET	Exception Logging Pending Set Register	45B2 0440h	45B2 0840h	45B2 0C40h
44h	CBASS_EXCEPTION_PEND_CLEAR	Exception Logging Pending Clear Register	45B2 0444h	45B2 0844h	45B2 0C44h

Table 1-38. Firewall Exception Registers 3

Offset	Acronym	Register Name	CBASS_HC_CFG0_GLB Physical Address	CBASS_IPPHY0_GLB Physical Address	CBASS_MCASP_G0_0_GLB Physical Address
0h	CBASS_PID	Revision Register	45B2 1000h	45B2 1400h	45B2 1800h
4h	CBASS_DESTINATION_ID	Destination ID Register	45B2 1004h	45B2 1404h	45B2 1804h
20h	CBASS_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	45B2 1020h	45B2 1420h	45B2 1820h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	45B2 1024h	45B2 1424h	45B2 1824h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	45B2 1028h	45B2 1428h	45B2 1828h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	45B2 102Ch	45B2 142Ch	45B2 182Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	45B2 1030h	45B2 1430h	45B2 1830h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	45B2 1034h	45B2 1434h	45B2 1834h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	45B2 1038h	45B2 1438h	45B2 1838h
40h	CBASS_EXCEPTION_PEND_SET	Exception Logging Pending Set Register	45B2 1040h	45B2 1440h	45B2 1840h
44h	CBASS_EXCEPTION_PEND_CLEAR	Exception Logging Pending Clear Register	45B2 1044h	45B2 1444h	45B2 1844h

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Table 1-39. Firewall Exception Registers 4

Offset	Acronym	Register Name	CBASS_MCASP_G1_0_GLB Physical Address	CBASS_RC0_GLB Physical Address	CBASS_RC_CFG0_GLB Physical Address
0h	CBASS_PID	Revision Register	45B2 1C00h	45B2 2000h	45B2 2400h
4h	CBASS_DESTINATION_ID	Destination ID Register	45B2 1C04h	45B2 2004h	45B2 2404h
20h	CBASS_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	45B2 1C20h	45B2 2020h	45B2 2420h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	45B2 1C24h	45B2 2024h	45B2 2424h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	45B2 1C28h	45B2 2028h	45B2 2428h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	45B2 1C2Ch	45B2 202Ch	45B2 242Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	45B2 1C30h	45B2 2030h	45B2 2430h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	45B2 1C34h	45B2 2034h	45B2 2434h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	45B2 1C38h	45B2 2038h	45B2 2438h
40h	CBASS_EXCEPTION_PEND_SET	Exception Logging Pending Set Register	45B2 1C40h	45B2 2040h	45B2 2440h
44h	CBASS_EXCEPTION_PEND_CLEAR	Exception Logging Pending Clear Register	45B2 1C44h	45B2 2044h	45B2 2444h

Table 1-40. Firewall Exception Registers 5

Offset	Acronym	Register Name	CBASS_HC2_0_GLB Physical Address
0h	CBASS_PID	Revision Register	45B2 2800h
4h	CBASS_DESTINATION_ID	Destination ID Register	45B2 2804h
20h	CBASS_EXCEPTION_LOGGING_CONTROL	Exception Logging Control Register	45B2 2820h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	45B2 2824h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	45B2 2828h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	45B2 282Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	45B2 2830h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	45B2 2834h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	45B2 2838h
40h	CBASS_EXCEPTION_PEND_SET	Exception Logging Pending Set Register	45B2 2840h
44h	CBASS_EXCEPTION_PEND_CLEAR	Exception Logging Pending Clear Register	45B2 2844h

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1.2.1 CBASS_PID Register (Offset = 0h) [reset = X]

CBASS_PID is shown in Figure 1-4 and described in Table 1-42.

Return to Summary Table.

The Revision Register contains the major and minor revisions for the module.

Table 1-41. CBASS_PID Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 8000h
CBASS_INFRA0_GLB	45B0 C000h
CBASS_AASRC0_GLB	45B2 0000h
CBASS_CSI0_GLB	45B2 0400h
CBASS_DATADEBUG0_GLB	45B2 0800h
CBASS_HC0_GLB	45B2 0C00h
CBASS_HC_CFG0_GLB	45B2 1000h
CBASS_IPPHY0_GLB	45B2 1400h
CBASS_MCASP_G0_0_GLB	45B2 1800h
CBASS_MCASP_G1_0_GLB	45B2 1C00h
CBASS_RC0_GLB	45B2 2000h
CBASS_RC_CFG0_GLB	45B2 2400h
CBASS_HC2_0_GLB	45B2 2800h

Figure 1-4. CBASS_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 1-42. CBASS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	X	TI internal data.

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1.2.2 CBASS_DESTINATION_ID Register (Offset = 4h) [reset = X]

CBASS_DESTINATION_ID is shown in Figure 1-5 and described in Table 1-44.

Return to Summary Table.

The Destination ID Register defines the destination ID value for error messages.

Table 1-43. CBASS_DESTINATION_ID Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 8004h
CBASS_INFRA0_GLB	45B0 C004h
CBASS_AASRC0_GLB	45B2 0004h
CBASS_CSI0_GLB	45B2 0404h
CBASS_DATADEBUG0_GLB	45B2 0804h
CBASS_HC0_GLB	45B2 0C04h
CBASS_HC_CFG0_GLB	45B2 1004h
CBASS_IPPHY0_GLB	45B2 1404h
CBASS_MCASP_G0_0_GLB	45B2 1804h
CBASS_MCASP_G1_0_GLB	45B2 1C04h
CBASS_RC0_GLB	45B2 2004h
CBASS_RC_CFG0_GLB	45B2 2404h
CBASS_HC2_0_GLB	45B2 2804h

Figure 1-5. CBASS_DESTINATION_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEST_ID							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-44. CBASS_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DEST_ID	R/W	0h	The destination ID.

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1.2.3 CBASS_EXCEPTION_LOGGING_CONTROL Register (Offset = 20h) [reset = X]

CBASS_EXCEPTION_LOGGING_CONTROL is shown in Figure 1-6 and described in Table 1-46.

Return to Summary Table.

The Exception Logging Control Register controls the exception logging.

Table 1-45. CBASS_EXCEPTION_LOGGING_CONTROL Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 8020h
CBASS_INFRA0_GLB	45B0 C020h
CBASS_AASRC0_GLB	45B2 0020h
CBASS_CSI0_GLB	45B2 0420h
CBASS_DATADEBUG0_GLB	45B2 0820h
CBASS_HC0_GLB	45B2 0C20h
CBASS_HC_CFG0_GLB	45B2 1020h
CBASS_IPPHY0_GLB	45B2 1420h
CBASS_MCASP_G0_0_GLB	45B2 1820h
CBASS_MCASP_G1_0_GLB	45B2 1C20h
CBASS_RC0_GLB	45B2 2020h
CBASS_RC_CFG0_GLB	45B2 2420h
CBASS_HC2_0_GLB	45B2 2820h

Figure 1-6. CBASS_EXCEPTION_LOGGING_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						DISABLE_PEND	DISABLE_F
R/W-X						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-46. CBASS_EXCEPTION_LOGGING_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	DISABLE_PEND	R/W	0h	Disables logging pending when set.
0	DISABLE_F	R/W	0h	Disables logging when set.

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1.2.4 CBASS_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

CBASS_EXCEPTION_LOGGING_HEADER0 is shown in Figure 1-7 and described in Table 1-48.

Return to Summary Table.

The Exception Logging Header 0 Register contains the first word of the header.

Table 1-47. CBASS_EXCEPTION_LOGGING_HEADER0 Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 8024h
CBASS_INFRA0_GLB	45B0 C024h
CBASS_AASRC0_GLB	45B2 0024h
CBASS_CSI0_GLB	45B2 0424h
CBASS_DATADEBUG0_GLB	45B2 0824h
CBASS_HC0_GLB	45B2 0C24h
CBASS_HC_CFG0_GLB	45B2 1024h
CBASS_IPPHY0_GLB	45B2 1424h
CBASS_MCASP_G0_0_GLB	45B2 1824h
CBASS_MCASP_G1_0_GLB	45B2 1C24h
CBASS_RC0_GLB	45B2 2024h
CBASS_RC_CFG0_GLB	45B2 2424h
CBASS_HC2_0_GLB	45B2 2824h

Figure 1-7. CBASS_EXCEPTION_LOGGING_HEADER0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_F								SRC_ID																DEST_ID							
R-0h								R-0h																R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 1-48. CBASS_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type.
23-8	SRC_ID	R	0h	Source ID.
7-0	DEST_ID	R	0h	Destination ID.

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1.2.5 CBASS_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = X]

CBASS_EXCEPTION_LOGGING_HEADER1 is shown in Figure 1-8 and described in Table 1-50.

Return to Summary Table.

The Exception Logging Header 1 Register contains the second word of the header.

Table 1-49. CBASS_EXCEPTION_LOGGING_HEADER1 Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 8028h
CBASS_INFRA0_GLB	45B0 C028h
CBASS_AASRC0_GLB	45B2 0028h
CBASS_CSI0_GLB	45B2 0428h
CBASS_DATADEBUG0_GLB	45B2 0828h
CBASS_HC0_GLB	45B2 0C28h
CBASS_HC_CFG0_GLB	45B2 1028h
CBASS_IPPHY0_GLB	45B2 1428h
CBASS_MCASP_G0_0_GLB	45B2 1828h
CBASS_MCASP_G1_0_GLB	45B2 1C28h
CBASS_RC0_GLB	45B2 2028h
CBASS_RC_CFG0_GLB	45B2 2428h
CBASS_HC2_0_GLB	45B2 2828h

Figure 1-8. CBASS_EXCEPTION_LOGGING_HEADER1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP								CODE								RESERVED															
R-0h								R-0h								R-X															

LEGEND: R = Read Only; *-n* = value after reset

Table 1-50. CBASS_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group.
23-16	CODE	R	0h	Code.
15-0	RESERVED	R	X	

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1.2.6 CBASS_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

CBASS_EXCEPTION_LOGGING_DATA0 is shown in Figure 1-9 and described in Table 1-52.

Return to Summary Table.

The Exception Logging Data 0 Register contains the first word of the data.

Table 1-51. CBASS_EXCEPTION_LOGGING_DATA0 Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 802Ch
CBASS_INFRA0_GLB	45B0 C02Ch
CBASS_AASRC0_GLB	45B2 002Ch
CBASS_CSI0_GLB	45B2 042Ch
CBASS_DATADEBUG0_GLB	45B2 082Ch
CBASS_HC0_GLB	45B2 0C2Ch
CBASS_HC_CFG0_GLB	45B2 102Ch
CBASS_IPPHY0_GLB	45B2 142Ch
CBASS_MCASP_G0_0_GLB	45B2 182Ch
CBASS_MCASP_G1_0_GLB	45B2 1C2Ch
CBASS_RC0_GLB	45B2 202Ch
CBASS_RC_CFG0_GLB	45B2 242Ch
CBASS_HC2_0_GLB	45B2 282Ch

Figure 1-9. CBASS_EXCEPTION_LOGGING_DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_L																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 1-52. CBASS_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	Address lower 32 bits.

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1.2.7 CBASS_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = X]

CBASS_EXCEPTION_LOGGING_DATA1 is shown in Figure 1-10 and described in Table 1-54.

Return to Summary Table.

The Exception Logging Data 1 Register contains the second word of the data.

Table 1-53. CBASS_EXCEPTION_LOGGING_DATA1 Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 8030h
CBASS_INFRA0_GLB	45B0 C030h
CBASS_AASRC0_GLB	45B2 0030h
CBASS_CSI0_GLB	45B2 0430h
CBASS_DATADEBUG0_GLB	45B2 0830h
CBASS_HC0_GLB	45B2 0C30h
CBASS_HC_CFG0_GLB	45B2 1030h
CBASS_IPPHY0_GLB	45B2 1430h
CBASS_MCASP_G0_0_GLB	45B2 1830h
CBASS_MCASP_G1_0_GLB	45B2 1C30h
CBASS_RC0_GLB	45B2 2030h
CBASS_RC_CFG0_GLB	45B2 2430h
CBASS_HC2_0_GLB	45B2 2830h

Figure 1-10. CBASS_EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR_H															
R-X																R-0h															

LEGEND: R = Read Only; *-n* = value after reset

Table 1-54. CBASS_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ADDR_H	R	0h	Address upper 16 bits.

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1.2.8 CBASS_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = X]

CBASS_EXCEPTION_LOGGING_DATA2 is shown in Figure 1-11 and described in Table 1-56.

Return to Summary Table.

The Exception Logging Data 2 Register contains the third word of the data.

Table 1-55. CBASS_EXCEPTION_LOGGING_DATA2 Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 8034h
CBASS_INFRA0_GLB	45B0 C034h
CBASS_AASRC0_GLB	45B2 0034h
CBASS_CSI0_GLB	45B2 0434h
CBASS_DATADEBUG0_GLB	45B2 0834h
CBASS_HC0_GLB	45B2 0C34h
CBASS_HC_CFG0_GLB	45B2 1034h
CBASS_IPPHY0_GLB	45B2 1434h
CBASS_MCASP_G0_0_GLB	45B2 1834h
CBASS_MCASP_G1_0_GLB	45B2 1C34h
CBASS_RC0_GLB	45B2 2034h
CBASS_RC_CFG0_GLB	45B2 2434h
CBASS_HC2_0_GLB	45B2 2834h

Figure 1-11. CBASS_EXCEPTION_LOGGING_DATA2 Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
R-X				R-0h			
23	22	21	20	19	18	17	16
ROUTEID							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PRIV_ID							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 1-56. CBASS_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	ROUTEID	R	0h	Route ID.
15-14	RESERVED	R	X	
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.

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Table 1-56. CBASS_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SECURE	R	0h	Secure.
7-0	PRIV_ID	R	0h	Priv ID.

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1.2.9 CBASS_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = X]

CBASS_EXCEPTION_LOGGING_DATA3 is shown in Figure 1-12 and described in Table 1-58.

Return to Summary Table.

The Exception Logging Data 3 Register contains the fourth word of the data.

Table 1-57. CBASS_EXCEPTION_LOGGING_DATA3 Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 8038h
CBASS_INFRA0_GLB	45B0 C038h
CBASS_AASRC0_GLB	45B2 0038h
CBASS_CSI0_GLB	45B2 0438h
CBASS_DATADEBUG0_GLB	45B2 0838h
CBASS_HC0_GLB	45B2 0C38h
CBASS_HC_CFG0_GLB	45B2 1038h
CBASS_IPPHY0_GLB	45B2 1438h
CBASS_MCASP_G0_0_GLB	45B2 1838h
CBASS_MCASP_G1_0_GLB	45B2 1C38h
CBASS_RC0_GLB	45B2 2038h
CBASS_RC_CFG0_GLB	45B2 2438h
CBASS_HC2_0_GLB	45B2 2838h

Figure 1-12. CBASS_EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						BYTECNT									
R-X																						R-0h									

LEGEND: R = Read Only; *-n* = value after reset

Table 1-58. CBASS_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	BYTECNT	R	0h	Byte count.

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1.2.10 CBASS_EXCEPTION_PEND_SET Register (Offset = 40h) [reset = X]

CBASS_EXCEPTION_PEND_SET is shown in Figure 1-13 and described in Table 1-60.

Return to Summary Table.

The Exception Logging Pending Set Register allows to set the pend signal.

Table 1-59. CBASS_EXCEPTION_PEND_SET Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 8040h
CBASS_INFRA0_GLB	45B0 C040h
CBASS_AASRC0_GLB	45B2 0040h
CBASS_CSI0_GLB	45B2 0440h
CBASS_DATADEBUG0_GLB	45B2 0840h
CBASS_HC0_GLB	45B2 0C40h
CBASS_HC_CFG0_GLB	45B2 1040h
CBASS_IPPHY0_GLB	45B2 1440h
CBASS_MCASP_G0_0_GLB	45B2 1840h
CBASS_MCASP_G1_0_GLB	45B2 1C40h
CBASS_RC0_GLB	45B2 2040h
CBASS_RC_CFG0_GLB	45B2 2440h
CBASS_HC2_0_GLB	45B2 2840h

Figure 1-13. CBASS_EXCEPTION_PEND_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 1-60. CBASS_EXCEPTION_PEND_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_SET	R/W1S	0h	Write a 1 to set the exception pend signal.

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1.2.11 CBASS_EXCEPTION_PEND_CLEAR Register (Offset = 44h) [reset = X]

CBASS_EXCEPTION_PEND_CLEAR is shown in Figure 1-14 and described in Table 1-62.

Return to Summary Table.

The Exception Logging Pending Clear Register allows to clear the pend signal.

Table 1-61. CBASS_EXCEPTION_PEND_CLEAR Instances

Instance	Physical Address
CBASS_AC0_GLB	45B0 8044h
CBASS_INFRA0_GLB	45B0 C044h
CBASS_AASRC0_GLB	45B2 0044h
CBASS_CSI0_GLB	45B2 0444h
CBASS_DATADEBUG0_GLB	45B2 0844h
CBASS_HC0_GLB	45B2 0C44h
CBASS_HC_CFG0_GLB	45B2 1044h
CBASS_IPPHY0_GLB	45B2 1444h
CBASS_MCASP_G0_0_GLB	45B2 1844h
CBASS_MCASP_G1_0_GLB	45B2 1C44h
CBASS_RC0_GLB	45B2 2044h
CBASS_RC_CFG0_GLB	45B2 2444h
CBASS_HC2_0_GLB	45B2 2844h

Figure 1-14. CBASS_EXCEPTION_PEND_CLEAR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							PEND_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 1-62. CBASS_EXCEPTION_PEND_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	PEND_CLR	R/W1C	0h	Write a 1 to clear the exception pend signal.

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1.3 Firewall Region Registers

Table 1-84 through Table 1-168 list the memory-mapped firewall region registers for the system interconnect slaves. All register offset addresses not listed in these tables should be considered as reserved locations and the register contents should not be modified.

Table 1-63. Firewall Region Registers Instances

Instance	Base Address
INFRA_CBASS0	
PSRAM2KECC0_FW	4500 0400h
PSRAM2KECC0_ECCAGGR_FW	4500 0800h
PSC0_FW	4500 1400h
PLLCTRL0_FW	4500 1800h
GTC0_FW	4500 1C00h
PLL0_CFG_FW	4500 2000h
CTRL_MMR0_FW	4500 2400h
EFUSE0_FW	4500 2C00h
PBIST_INFRA0_CFG_FW	4500 3000h
GPIO0_FW	4500 4000h
GPIO1_FW	4500 4400h
GPIO2_FW	4500 4800h
GPIO3_FW	4500 4C00h
GPIO4_FW	4500 5000h
GPIO5_FW	4500 5400h
GPIO6_FW	4500 5800h
GPIO7_FW	4500 5C00h
ESM0_CFG_FW	4500 6000h
DCC0_FW	4500 8000h
DCC1_FW	4500 8400h
DCC2_FW	4500 8800h
DCC3_FW	4500 8C00h
DCC4_FW	4500 9000h
DCC5_FW	4500 9400h
DCC6_FW	4500 9800h
DCC7_FW	4500 9C00h
DCC8_FW	4500 A000h
DCC9_FW	4500 A400h
DCC10_FW	4500 A800h
DCC11_FW	4500 AC00h
DCC12_FW	4500 B000h
GPIOMUX_INTRTR0_CFG_FW	4500 E000h
MAIN2MCU_LVL_INTRTR0_CFG_FW	4500 E400h
MAIN2MCU_PLS_INTRTR0_CFG_FW	4500 E800h
CMPEVT_INTRTR0_CFG_FW	4500 EC00h
TIMESYNC_INTRTR0_CFG_FW	4500 F000h
MAIN_MCU1_INTROUTER0_FW	4500 F800h
MAIN_MCU0_INTROUTER0_FW	4500 FC00h
C66SS0_INTRTR0_CFG_FW	4501 0000h
C66SS0_INTRTR1_CFG_FW	4501 0400h
FW_CBASS0_ERR_FW	4501 2400h

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Table 1-63. Firewall Region Registers Instances (continued)

Instance	Base Address
INFRA_CBASS0_ERR_FW	4501 2800h
INFRA_ECC_AGGR0_CFG_FW	4501 4400h
PSRAMECC0_FW	4501 5000h
PSRAMECC0_ECCAGGR_FW	4501 5400h
WKUP_CBASS0	
WKUP_PSC0_FW	4502 0400h
WKUP_PLLCTRL0_FW	4502 0800h
WKUP_CTRL_MMR0_FW	4502 0C00h
WKUP_GPIO0_FW	4502 1000h
WKUP_ESM0_CFG_FW	4502 1400h
WKUP_VTM0_FW	4502 1C00h
WKUP_GPIO1_FW	4502 2400h
WKUP_I2C0_FW	4502 4000h
WKUP_UART0_FW	4502 8000h
WKUP_GPIOMUX_INTRTR0_CFG_FW	4502 A000h
WKUP_CBASS0_ERR_FW	4502 C000h
WKUP_FW_CBASS0_ERR_FW	4502 C400h
WKUP_ECC_AGGR0_CFG_FW	4502 C800h
MCU_CBASS0	
MCU_R5FSS0_CORE0_FW	4510 0000h
MCU_R5FSS0_CORE0_CFG_FW	4510 0400h
MCU_RTI0_FW	4510 0800h
MCU_R5FSS0_CORE1_FW	4510 1000h
MCU_R5FSS0_CORE1_CFG_FW	4510 1400h
MCU_RTI1_FW	4510 1800h
MCU_FSS0_CFG_FW	4510 2000h
MCU_FSS0_S1_FW	4510 2400h
MCU_FSS0_S0_FW	4510 3000h
MCU_PSROM0_FW	4510 6000h
MCU_MSRAM_1MB0_FW	4510 6800h
MCU_MSRAM_1MB0_CFG_FW	4510 6C00h
MCU_PSRAM0_FW	4510 7000h
MCU_TIMER0_FW	4510 8000h
MCU_TIMER1_FW	4510 8400h
MCU_TIMER2_FW	4510 8800h
MCU_TIMER3_FW	4510 8C00h
MCU_TIMER4_FW	4510 9000h
MCU_TIMER5_FW	4510 9400h
MCU_TIMER6_FW	4510 9800h
MCU_TIMER7_FW	4510 9C00h
MCU_TIMER8_FW	4510 A000h
MCU_TIMER9_FW	4510 A400h
MCU_SPI0_FW	4510 C000h
MCU_SPI1_FW	4510 C400h
MCU_SPI2_FW	4510 C800h
MCU_DCC0_FW	4511 0000h
MCU_DCC1_FW	4511 0400h

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Table 1-63. Firewall Region Registers Instances (continued)

Instance	Base Address
MCU_DCC2_FW	4511 0800h
MCU_ADC0_DMA_FW	4511 4000h
MCU_ADC0_CFG_FW	4511 4400h
MCU_ADC1_DMA_FW	4511 4800h
MCU_ADC1_CFG_FW	4511 4C00h
MCU_UART0_FW	4511 8000h
MCU_I2C0_FW	4512 0000h
MCU_I2C1_FW	4512 0400h
MCU_I3C0_FW	4512 2000h
MCU_I3C1_FW	4512 2400h
MCU_ESM0_CFG_FW	4512 4000h
MCU_MCAN0_FW	4512 8000h
MCU_MCAN1_FW	4512 8400h
MCU_CTRL_MMR0_FW	4512 C000h
MCU_PLL0_CFG_FW	4512 C400h
MCU_EFUSE0_FW	4512 E000h
MCU_PBIST0_CFG_FW	4512 F000h
MCU_PBIST_R5FSS0_CFG_FW	4512 F400h
MCU_CPSW0_FW	4513 1000h
MCU_CBASS0_ERR_FW	4513 7000h
MCU_FW_CBASS0_ERR_FW	4513 7800h
MCU_ECC_AGGR0_CFG_FW	4513 9400h
CBASS0	
EPWM0_FW	4520 0000h
HRPWM0_FW	4520 0400h
EPWM1_FW	4520 0800h
HRPWM1_FW	4520 0C00h
EPWM2_FW	4520 1000h
HRPWM2_FW	4520 1400h
EPWM3_FW	4520 1800h
HRPWM3_FW	4520 1C00h
EPWM4_FW	4520 2000h
HRPWM4_FW	4520 2400h
EPWM5_FW	4520 2800h
HRPWM5_FW	4520 2C00h
EQEP0_FW	4520 4000h
EQEP1_FW	4520 4400h
EQEP2_FW	4520 4800h
ECAP0_FW	4520 5000h
ECAP1_FW	4520 5400h
ECAP2_FW	4520 5800h
I2C0_FW	4520 6000h
I2C1_FW	4520 6400h
I2C2_FW	4520 6800h
I2C3_FW	4520 6C00h
I2C4_FW	4520 7000h
I2C5_FW	4520 7400h

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Table 1-63. Firewall Region Registers Instances (continued)

Instance	Base Address
I2C6_FW	4520 7800h
ATL0_FW	4520 8000h
I3C0_FW	4520 8800h
RTI0_FW	4520 9800h
RTI1_FW	4520 9C00h
RTI28_FW	4520 B800h
RTI29_FW	4520 BC00h
RTI30_FW	4520 C000h
RTI31_FW	4520 C400h
RTI16_FW	4520 D000h
RTI24_FW	4520 E000h
RTI25_FW	4520 E400h
RTI15_FW	4520 F000h
TIMER0_FW	4521 0000h
TIMER1_FW	4521 0400h
TIMER2_FW	4521 0800h
TIMER3_FW	4521 0C00h
TIMER4_FW	4521 1000h
TIMER5_FW	4521 1400h
TIMER6_FW	4521 1800h
TIMER7_FW	4521 1C00h
TIMER8_FW	4521 2000h
TIMER9_FW	4521 2400h
TIMER10_FW	4521 2800h
TIMER11_FW	4521 2C00h
TIMER12_FW	4521 3000h
TIMER13_FW	4521 3400h
TIMER14_FW	4521 3800h
TIMER15_FW	4521 3C00h
TIMER16_FW	4521 4000h
TIMER17_FW	4521 4400h
TIMER18_FW	4521 4800h
TIMER19_FW	4521 4C00h
SPI0_FW	4521 6000h
SPI1_FW	4521 6400h
SPI2_FW	4521 6800h
SPI3_FW	4521 6C00h
SPI4_FW	4521 7000h
SPI5_FW	4521 7400h
SPI6_FW	4521 7800h
SPI7_FW	4521 7C00h
UART0_FW	4521 9000h
UART1_FW	4521 9400h
UART2_FW	4521 9800h
UART3_FW	4521 9C00h
UART4_FW	4521 A000h
UART5_FW	4521 A400h

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Table 1-63. Firewall Region Registers Instances (continued)

Instance	Base Address
UART6_FW	4521 A800h
UART7_FW	4521 AC00h
UART8_FW	4521 B000h
UART9_FW	4521 B400h
MCAN0_FW	4521 C000h
MCAN1_FW	4521 C400h
MCAN2_FW	4521 C800h
MCAN3_FW	4521 CC00h
MCAN4_FW	4521 D000h
MCAN5_FW	4521 D400h
MCAN6_FW	4521 D800h
MCAN7_FW	4521 DC00h
MCAN8_FW	4521 E000h
MCAN9_FW	4521 E400h
MCAN10_FW	4521 E800h
MCAN11_FW	4521 EC00h
MCAN12_FW	4521 F000h
MCAN13_FW	4521 F400h
PDMA_MISC_PSIL0_CFG_FW	4522 2000h
PDMA_USART_PSIL0_CFG_FW	4522 2400h
CBASS_IPPHY0_ERR_FW	4523 FC00h
C66SS0_SRC_FW	4524 0000h
C66SS1_SRC_FW	4524 0400h
GPMC0_FW	4524 1800h
R5FSS0_CORE0_FW	4524 2800h
R5FSS0_CORE1_FW	4524 2C00h
R5FSS1_CORE0_FW	4524 3000h
R5FSS1_CORE1_FW	4524 3400h
R5FSS0_CORE0_CFG_FW	4525 0000h
R5FSS0_CORE1_CFG_FW	4525 0400h
R5FSS1_CORE0_CFG_FW	4525 0800h
R5FSS1_CORE1_CFG_FW	4525 0C00h
C66SS0_CFG_FW	4525 2000h
C66SS1_CFG_FW	4525 2400h
MMCSD1_CFG_FW	4525 3000h
MMCSD2_CFG_FW	4525 3400h
ELM0_FW	4525 4000h
PRU_ICSSG0_FW	4525 4800h
PRU_ICSSG1_FW	4525 4C00h
CPSW0_FW	4525 5800h
VPFE0_RATCFG_FW	4525 6800h
VPFE0_CFG_FW	4525 6C00h
NAVSS0_NBSS_CFG_FW	4525 7800h
COMPUTE_CLUSTER0_FW	4525 8000h
RCNAVSS11_ECC_AGGR_CFG_FW	4525 A000h
RC4_ECC_AGGR_CFG_FW	4525 A400h
RC_R500_ECC_AGGR_CFG_FW	4525 A800h

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Table 1-63. Firewall Region Registers Instances (continued)

Instance	Base Address
RC_R511_ECC_AGGR_CFG_FW	4525 AC00h
RCNAVSS10_ECC_AGGR_CFG_FW	4525 BC00h
PBIST_RC_NAVSS_CFG_FW	4525 C000h
PBIST_RC_NB_CFG_FW	4525 C400h
PBIST_RC_R5FSS0_CFG_FW	4525 C800h
PBIST_RC_R5FSS1_CFG_FW	4525 CC00h
CBASS_RC0_ERR_FW	4525 F800h
CBASS_RC_CFG0_ERR_FW	4525 FC00h
CSI_RX0_FW	4526 0000h
CSI_RX1_FW	4526 0400h
DPHY_RX0_FW	4526 1000h
DPHY_RX1_FW	4526 1400h
CSI_TX0_FW	4526 2000h
DPHY_TX0_FW	4526 2800h
CSI_PSIL0_CFG_FW	4526 3800h
CBASS_CSI0_ERR_FW	4526 7C00h
STM0_FW	4526 8000h
DEBUGSS0_CFG_FW	4526 8400h
MAIN_DEBUG_CELL0_FW	4526 8800h
CC_DEBUG_CELL0_FW	4526 8C00h
MAIN_DEBUG_CELL1_FW	4526 9000h
C66SS0_DEBUG_CELL_FW	4526 9400h
C66SS1_DEBUG_CELL_FW	4526 9800h
PDMA_DEBUG_PSIL0_CFG_FW	4526 A000h
CBASS_DATADEBUG0_ERR_FW	4526 FC00h
MCASP3_CFG_FW	4527 0000h
MCASP3_DMA_FW	4527 0400h
MCASP4_CFG_FW	4527 0800h
MCASP4_DMA_FW	4527 0C00h
MCASP5_CFG_FW	4527 1000h
MCASP5_DMA_FW	4527 1400h
MCASP6_CFG_FW	4527 1800h
MCASP6_DMA_FW	4527 1C00h
MCASP7_CFG_FW	4527 2000h
MCASP7_DMA_FW	4527 2400h
MCASP8_CFG_FW	4527 2800h
MCASP8_DMA_FW	4527 2C00h
MCASP9_CFG_FW	4527 3000h
MCASP9_DMA_FW	4527 3400h
MCASP10_CFG_FW	4527 3800h
MCASP10_DMA_FW	4527 3C00h
MCASP11_CFG_FW	4527 4000h
MCASP11_DMA_FW	4527 4400h
CBASS_MCASP_G1_0_ERR_FW	4527 7C00h
PCIE0_HP_FW	4527 8000h
PCIE0_LP_FW	4527 8400h
PCIE1_HP_FW	4527 8800h

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Table 1-63. Firewall Region Registers Instances (continued)

Instance	Base Address
PCIE1_LP_FW	4527 8C00h
PCIE2_HP_FW	4527 9000h
PCIE2_LP_FW	4527 9400h
PCIE3_HP_FW	4527 9800h
PCIE3_LP_FW	4527 9C00h
PCIE0_CFG_FW	4528 0000h
PCIE1_CFG_FW	4528 0400h
PCIE2_CFG_FW	4528 0800h
PCIE3_CFG_FW	4528 0C00h
USB3SS0_CORE_FW	4528 2000h
USB3SS0_USB2PHY_FW	4528 2400h
USB3SS1_CORE_FW	4528 2800h
USB3SS1_USB2PHY_FW	4528 2C00h
MMCSD0_CFG_FW	4528 4000h
MLBSS0_CFG_FW	4528 4800h
UFS0_CFG_FW	4528 5000h
HC5_ECC_AGGR_CFG_FW	4528 5C00h
SERDES0_FW	4528 6000h
SERDES1_FW	4528 6400h
SERDES2_FW	4528 6800h
SERDES3_FW	4528 6C00h
PBIST_HC0_CFG_FW	4528 7000h
CBASS_HC2_0_ERR_FW	4528 7400h
CBASS_HC0_ERR_FW	4528 7800h
CBASS_HC_CFG0_ERR_FW	4528 7C00h
MCASP0_CFG_FW	4528 8000h
MCASP0_DMA_FW	4528 8400h
MCASP1_CFG_FW	4528 8800h
MCASP1_DMA_FW	4528 8C00h
MCASP2_CFG_FW	4528 9000h
MCASP2_DMA_FW	4528 9400h
PDMA_AASRC_PSIL0_CFG_FW	4528 B800h
CBASS_MCASP_G0_0_ERR_FW	4528 BC00h
AASRC0_CFG_FW	4528 C000h
AASRC0_DATA_FW	4528 C400h
CBASS_AASRC0_ERR_FW	4528 FC00h

Table 1-64. Firewall Region Registers for INFRA_CBASS0 Slaves 1

Offset	Acronym	Register Name	PSRAM2KECC0_FW Physical Address	PSRAM2KECC0_ECCAGGR_FW Physical Address	PSC0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 0400h + formula	4500 0800h + formula	4500 1400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 0404h + formula	4500 0804h + formula	4500 1404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 0408h + formula	4500 0808h + formula	4500 1408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 040Ch + formula	4500 080Ch + formula	4500 140Ch + formula

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Table 1-64. Firewall Region Registers for INFRA_CBASS0 Slaves 1 (continued)

Offset	Acronym	Register Name	PSRAM2KECC0_FW Physical Address	PSRAM2KECC0_ECCAGGR_FW Physical Address	PSC0_FW Physical Address
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 0410h + formula	4500 0810h + formula	4500 1410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 0414h + formula	4500 0814h + formula	4500 1414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 0418h + formula	4500 0818h + formula	4500 1418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 041Ch + formula	4500 081Ch + formula	4500 141Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-65. Firewall Region Registers for INFRA_CBASS0 Slaves 2

Offset	Acronym	Register Name	PLLCTRL0_FW Physical Address	GTC0_FW Physical Address	PLL0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 1800h + formula	4500 1C00h + formula	4500 2000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 1804h + formula	4500 1C04h + formula	4500 2004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 1808h + formula	4500 1C08h + formula	4500 2008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 180Ch + formula	4500 1C0Ch + formula	4500 200Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 1810h + formula	4500 1C10h + formula	4500 2010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 1814h + formula	4500 1C14h + formula	4500 2014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 1818h + formula	4500 1C18h + formula	4500 2018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 181Ch + formula	4500 1C1Ch + formula	4500 201Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-66. Firewall Region Registers for INFRA_CBASS0 Slaves 3

Offset	Acronym	Register Name	CTRL_MMR0_FW Physical Address	EFUSE0_FW Physical Address	PBIST_INFRA0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 2400h + formula	4500 2C00h + formula	4500 3000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 2404h + formula	4500 2C04h + formula	4500 3004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 2408h + formula	4500 2C08h + formula	4500 3008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 240Ch + formula	4500 2C0Ch + formula	4500 300Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 2410h + formula	4500 2C10h + formula	4500 3010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 2414h + formula	4500 2C14h + formula	4500 3014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 2418h + formula	4500 2C18h + formula	4500 3018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 241Ch + formula	4500 2C1Ch + formula	4500 301Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-67. Firewall Region Registers for INFRA_CBASS0 Slaves 4

Offset	Acronym	Register Name	GPIO0_FW Physical Address	GPIO1_FW Physical Address	GPIO2_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 4000h + formula	4500 4400h + formula	4500 4800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 4004h + formula	4500 4404h + formula	4500 4804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 4008h + formula	4500 4408h + formula	4500 4808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 400Ch + formula	4500 440Ch + formula	4500 480Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 4010h + formula	4500 4410h + formula	4500 4810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 4014h + formula	4500 4414h + formula	4500 4814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 4018h + formula	4500 4418h + formula	4500 4818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 401Ch + formula	4500 441Ch + formula	4500 481Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-68. Firewall Region Registers for INFRA_CBASS0 Slaves 5

Offset	Acronym	Register Name	GPIO3_FW Physical Address	GPIO4_FW Physical Address	GPIO5_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 4C00h + formula	4500 5000h + formula	4500 5400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 4C04h + formula	4500 5004h + formula	4500 5404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 4C08h + formula	4500 5008h + formula	4500 5408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 4C0Ch + formula	4500 500Ch + formula	4500 540Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 4C10h + formula	4500 5010h + formula	4500 5410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 4C14h + formula	4500 5014h + formula	4500 5414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 4C18h + formula	4500 5018h + formula	4500 5418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 4C1Ch + formula	4500 501Ch + formula	4500 541Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-69. Firewall Region Registers for INFRA_CBASS0 Slaves 6

Offset	Acronym	Register Name	GPIO6_FW Physical Address	GPIO7_FW Physical Address	ESM0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 5800h + formula	4500 5C00h + formula	4500 6000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 5804h + formula	4500 5C04h + formula	4500 6004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 5808h + formula	4500 5C08h + formula	4500 6008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 580Ch + formula	4500 5C0Ch + formula	4500 600Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 5810h + formula	4500 5C10h + formula	4500 6010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 5814h + formula	4500 5C14h + formula	4500 6014h + formula

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Table 1-69. Firewall Region Registers for INFRA_CBASS0 Slaves 6 (continued)

Offset	Acronym	Register Name	GPIO6_FW Physical Address	GPIO7_FW Physical Address	ESM0_CFG_FW Physical Address
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 5818h + formula	4500 5C18h + formula	4500 6018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 581Ch + formula	4500 5C1Ch + formula	4500 601Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-70. Firewall Region Registers for INFRA_CBASS0 Slaves 7

Offset	Acronym	Register Name	DCC0_FW Physical Address	DCC1_FW Physical Address	DCC2_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 8000h + formula	4500 8400h + formula	4500 8800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 8004h + formula	4500 8404h + formula	4500 8804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 8008h + formula	4500 8408h + formula	4500 8808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 800Ch + formula	4500 840Ch + formula	4500 880Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 8010h + formula	4500 8410h + formula	4500 8810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 8014h + formula	4500 8414h + formula	4500 8814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 8018h + formula	4500 8418h + formula	4500 8818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 801Ch + formula	4500 841Ch + formula	4500 881Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-71. Firewall Region Registers for INFRA_CBASS0 Slaves 8

Offset	Acronym	Register Name	DCC3_FW Physical Address	DCC4_FW Physical Address	DCC5_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 8C00h + formula	4500 9000h + formula	4500 9400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 8C04h + formula	4500 9004h + formula	4500 9404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 8C08h + formula	4500 9008h + formula	4500 9408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 8C0Ch + formula	4500 900Ch + formula	4500 940Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 8C10h + formula	4500 9010h + formula	4500 9410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 8C14h + formula	4500 9014h + formula	4500 9414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 8C18h + formula	4500 9018h + formula	4500 9418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 8C1Ch + formula	4500 901Ch + formula	4500 941Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-72. Firewall Region Registers for INFRA_CBASS0 Slaves 9

Offset	Acronym	Register Name	DCC6_FW Physical Address	DCC7_FW Physical Address	DCC8_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 9800h + formula	4500 9C00h + formula	4500 A000h + formula

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Table 1-72. Firewall Region Registers for INFRA_CBASS0 Slaves 9 (continued)

Offset	Acronym	Register Name	DCC6_FW Physical Address	DCC7_FW Physical Address	DCC8_FW Physical Address
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 9804h + formula	4500 9C04h + formula	4500 A004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 9808h + formula	4500 9C08h + formula	4500 A008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 980Ch + formula	4500 9C0Ch + formula	4500 A00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 9810h + formula	4500 9C10h + formula	4500 A010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 9814h + formula	4500 9C14h + formula	4500 A014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 9818h + formula	4500 9C18h + formula	4500 A018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 981Ch + formula	4500 9C1Ch + formula	4500 A01Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-73. Firewall Region Registers for INFRA_CBASS0 Slaves 10

Offset	Acronym	Register Name	DCC9_FW Physical Address	DCC10_FW Physical Address	DCC11_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 A400h + formula	4500 A800h + formula	4500 AC00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 A404h + formula	4500 A804h + formula	4500 AC04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 A408h + formula	4500 A808h + formula	4500 AC08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 A40Ch + formula	4500 A80Ch + formula	4500 AC0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 A410h + formula	4500 A810h + formula	4500 AC10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 A414h + formula	4500 A814h + formula	4500 AC14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 A418h + formula	4500 A818h + formula	4500 AC18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 A41Ch + formula	4500 A81Ch + formula	4500 AC1Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-74. Firewall Region Registers for INFRA_CBASS0 Slaves 11

Offset	Acronym	Register Name	DCC12_FW Physical Address	GPIOMUX_INTRTR0_CFG_FW Physical Address	MAIN2MCU_LVL_INTRTR0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 B000h + formula	4500 E000h + formula	4500 E400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 B004h + formula	4500 E004h + formula	4500 E404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 B008h + formula	4500 E008h + formula	4500 E408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 B00Ch + formula	4500 E00Ch + formula	4500 E40Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 B010h + formula	4500 E010h + formula	4500 E410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 B014h + formula	4500 E014h + formula	4500 E414h + formula

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Table 1-74. Firewall Region Registers for INFRA_CBASS0 Slaves 11 (continued)

Offset	Acronym	Register Name	DCC12_FW Physical Address	GPIOMUX_INTRTR0_CFG_FW Physical Address	MAIN2MCU_LVL_INTRTR0_CFG_FW Physical Address
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 B018h + formula	4500 E018h + formula	4500 E418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 B01Ch + formula	4500 E01Ch + formula	4500 E41Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-75. Firewall Region Registers for INFRA_CBASS0 Slaves 12

Offset	Acronym	Register Name	MAIN2MCU_PLS_INTRTR0_CFG_FW Physical Address	CMPEVT_INTRTR0_CFG_FW Physical Address	TIMESYNC_INTRTR0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 E800h + formula	4500 EC00h + formula	4500 F000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 E804h + formula	4500 EC04h + formula	4500 F004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 E808h + formula	4500 EC08h + formula	4500 F008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 E80Ch + formula	4500 EC0Ch + formula	4500 F00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 E810h + formula	4500 EC10h + formula	4500 F010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 E814h + formula	4500 EC14h + formula	4500 F014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 E818h + formula	4500 EC18h + formula	4500 F018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 E81Ch + formula	4500 EC1Ch + formula	4500 F01Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-76. Firewall Region Registers for INFRA_CBASS0 Slaves 13

Offset	Acronym	Register Name	MAIN_MCU1_INTROUTER0_FW Physical Address	MAIN_MCU0_INTROUTER0_FW Physical Address	C66SS0_INTRTR0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4500 F800h + formula	4500 FC00h + formula	4501 0000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4500 F804h + formula	4500 FC04h + formula	4501 0004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4500 F808h + formula	4500 FC08h + formula	4501 0008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4500 F80Ch + formula	4500 FC0Ch + formula	4501 000Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4500 F810h + formula	4500 FC10h + formula	4501 0010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4500 F814h + formula	4500 FC14h + formula	4501 0014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4500 F818h + formula	4500 FC18h + formula	4501 0018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4500 F81Ch + formula	4500 FC1Ch + formula	4501 001Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-77. Firewall Region Registers for INFRA_CBASS0 Slaves 14

Offset	Acronym	Register Name	C66SS0_INTRTR1_CFG_FW Physical Address	FW_CBASS0_ERR_FW Physical Address	INFRA_CBASS0_ERR_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4501 0400h + formula	4501 2400h + formula	4501 2800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4501 0404h + formula	4501 2404h + formula	4501 2804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4501 0408h + formula	4501 2408h + formula	4501 2808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4501 040Ch + formula	4501 240Ch + formula	4501 280Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4501 0410h + formula	4501 2410h + formula	4501 2810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4501 0414h + formula	4501 2414h + formula	4501 2814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4501 0418h + formula	4501 2418h + formula	4501 2818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4501 041Ch + formula	4501 241Ch + formula	4501 281Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-78. Firewall Region Registers for INFRA_CBASS0 Slaves 15

Offset	Acronym	Register Name	INFRA_ECC_AGGR0_CFG_FW Physical Address	PSRAMECC0_FW Physical Address	PSRAMECC0_ECCAGGR_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4501 4400h + formula	4501 5000h + formula	4501 5400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4501 4404h + formula	4501 5004h + formula	4501 5404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4501 4408h + formula	4501 5008h + formula	4501 5408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4501 440Ch + formula	4501 500Ch + formula	4501 540Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4501 4410h + formula	4501 5010h + formula	4501 5410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4501 4414h + formula	4501 5014h + formula	4501 5414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4501 4418h + formula	4501 5018h + formula	4501 5418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4501 441Ch + formula	4501 501Ch + formula	4501 541Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-79. Firewall Region Registers for WKUP_CBASS0 Slaves 1

Offset	Acronym	Register Name	WKUP_PSC0_FW Physical Address	WKUP_PLLCTRL0_FW Physical Address	WKUP_CTRL_MMR0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4502 0400h + formula	4502 0800h + formula	4502 0C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4502 0404h + formula	4502 0804h + formula	4502 0C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4502 0408h + formula	4502 0808h + formula	4502 0C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4502 040Ch + formula	4502 080Ch + formula	4502 0C0Ch + formula

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Table 1-79. Firewall Region Registers for WKUP_CBASS0 Slaves 1 (continued)

Offset	Acronym	Register Name	WKUP_PSC0_FW Physical Address	WKUP_PLLCTRL0_FW Physical Address	WKUP_CTRL_MMR0_FW Physical Address
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4502 0410h + formula	4502 0810h + formula	4502 0C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4502 0414h + formula	4502 0814h + formula	4502 0C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4502 0418h + formula	4502 0818h + formula	4502 0C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4502 041Ch + formula	4502 081Ch + formula	4502 0C1Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-80. Firewall Region Registers for WKUP_CBASS0 Slaves 2

Offset	Acronym	Register Name	WKUP_GPIO0_FW Physical Address	WKUP_ESM0_CFG_FW Physical Address	WKUP_VTM0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4502 1000h + formula	4502 1400h + formula	4502 1C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4502 1004h + formula	4502 1404h + formula	4502 1C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4502 1008h + formula	4502 1408h + formula	4502 1C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4502 100Ch + formula	4502 140Ch + formula	4502 1C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4502 1010h + formula	4502 1410h + formula	4502 1C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4502 1014h + formula	4502 1414h + formula	4502 1C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4502 1018h + formula	4502 1418h + formula	4502 1C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4502 101Ch + formula	4502 141Ch + formula	4502 1C1Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-81. Firewall Region Registers for WKUP_CBASS0 Slaves 3

Offset	Acronym	Register Name	WKUP_GPIO1_FW Physical Address	WKUP_I2C0_FW Physical Address	WKUP_UART0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4502 2400h + formula	4502 4000h + formula	4502 8000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4502 2404h + formula	4502 4004h + formula	4502 8004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4502 2408h + formula	4502 4008h + formula	4502 8008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4502 240Ch + formula	4502 400Ch + formula	4502 800Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4502 2410h + formula	4502 4010h + formula	4502 8010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4502 2414h + formula	4502 4014h + formula	4502 8014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4502 2418h + formula	4502 4018h + formula	4502 8018h + formula

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Table 1-81. Firewall Region Registers for WKUP_CBASS0 Slaves 3 (continued)

Offset	Acronym	Register Name	WKUP_GPIO1_FW Physical Address	WKUP_I2C0_FW Physical Address	WKUP_UART0_FW Physical Address
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4502 241Ch + formula	4502 401Ch + formula	4502 801Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-82. Firewall Region Registers for WKUP_CBASS0 Slaves 4

Offset	Acronym	Register Name	WKUP_GPIOMUX_INTRTR0_CFG_FW Physical Address	WKUP_CBASS0_ERR_FW Physical Address	WKUP_FW_CBASS0_ERR_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4502 A000h + formula	4502 C000h + formula	4502 C400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4502 A004h + formula	4502 C004h + formula	4502 C404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4502 A008h + formula	4502 C008h + formula	4502 C408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4502 A00Ch + formula	4502 C00Ch + formula	4502 C40Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4502 A010h + formula	4502 C010h + formula	4502 C410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4502 A014h + formula	4502 C014h + formula	4502 C414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4502 A018h + formula	4502 C018h + formula	4502 C418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4502 A01Ch + formula	4502 C01Ch + formula	4502 C41Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-83. Firewall Region Registers for WKUP_CBASS0 Slaves 5

Offset	Acronym	Register Name	WKUP_ECC_AGGR0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4502 C800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4502 C804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4502 C808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4502 C80Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4502 C810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4502 C814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4502 C818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4502 C81Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-84. Firewall Region Registers for MCU_CBASS0 Slaves 1

Offset	Acronym	Register Name	MCU_R5FSS0_CORE0_FW Physical Address	MCU_R5FSS0_CORE0_CFG_FW Physical Address	MCU_RTI0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4510 0000h + formula	4510 0400h + formula	4510 0800h + formula

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Table 1-84. Firewall Region Registers for MCU_CBASS0 Slaves 1 (continued)

Offset	Acronym	Register Name	MCU_R5FSS0_CORE0_FW Physical Address	MCU_R5FSS0_CORE0_CFG_FW Physical Address	MCU_RTI0_FW Physical Address
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4510 0004h + formula	4510 0404h + formula	4510 0804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4510 0008h + formula	4510 0408h + formula	4510 0808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4510 000Ch + formula	4510 040Ch + formula	4510 080Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4510 0010h + formula	4510 0410h + formula	4510 0810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4510 0014h + formula	4510 0414h + formula	4510 0814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4510 0018h + formula	4510 0418h + formula	4510 0818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4510 001Ch + formula	4510 041Ch + formula	4510 081Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-85. Firewall Region Registers for MCU_CBASS0 Slaves 2

Offset	Acronym	Register Name	MCU_R5FSS0_CORE1_FW Physical Address	MCU_R5FSS0_CORE1_CFG_FW Physical Address	MCU_RTI1_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4510 1000h + formula	4510 1400h + formula	4510 1800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4510 1004h + formula	4510 1404h + formula	4510 1804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4510 1008h + formula	4510 1408h + formula	4510 1808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4510 100Ch + formula	4510 140Ch + formula	4510 180Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4510 1010h + formula	4510 1410h + formula	4510 1810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4510 1014h + formula	4510 1414h + formula	4510 1814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4510 1018h + formula	4510 1418h + formula	4510 1818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4510 101Ch + formula	4510 141Ch + formula	4510 181Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-86. Firewall Region Registers for MCU_CBASS0 Slaves 3

Offset	Acronym	Register Name	MCU_FSS0_CFG_FW Physical Address	MCU_FSS0_S1_FW Physical Address	MCU_FSS0_S0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4510 2000h + formula	4510 2400h + formula	4510 3000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4510 2004h + formula	4510 2404h + formula	4510 3004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4510 2008h + formula	4510 2408h + formula	4510 3008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4510 200Ch + formula	4510 240Ch + formula	4510 300Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4510 2010h + formula	4510 2410h + formula	4510 3010h + formula

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Table 1-86. Firewall Region Registers for MCU_CBASS0 Slaves 3 (continued)

Offset	Acronym	Register Name	MCU_FSS0_CFG_FW Physical Address	MCU_FSS0_S1_FW Physical Address	MCU_FSS0_S0_FW Physical Address
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4510 2014h + formula	4510 2414h + formula	4510 3014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4510 2018h + formula	4510 2418h + formula	4510 3018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4510 201Ch + formula	4510 241Ch + formula	4510 301Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-87. Firewall Region Registers for MCU_CBASS0 Slaves 4

Offset	Acronym	Register Name	MCU_PSROM0_FW Physical Address	MCU_MSRAM_1MB0_FW Physical Address	MCU_MSRAM_1MB0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4510 6000h + formula	4510 6800h + formula	4510 6C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4510 6004h + formula	4510 6804h + formula	4510 6C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4510 6008h + formula	4510 6808h + formula	4510 6C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4510 600Ch + formula	4510 680Ch + formula	4510 6C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4510 6010h + formula	4510 6810h + formula	4510 6C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4510 6014h + formula	4510 6814h + formula	4510 6C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4510 6018h + formula	4510 6818h + formula	4510 6C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4510 601Ch + formula	4510 681Ch + formula	4510 6C1Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-88. Firewall Region Registers for MCU_CBASS0 Slaves 5

Offset	Acronym	Register Name	MCU_PSRAM0_FW Physical Address	MCU_TIMER0_FW Physical Address	MCU_TIMER1_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4510 7000h + formula	4510 8000h + formula	4510 8400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4510 7004h + formula	4510 8004h + formula	4510 8404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4510 7008h + formula	4510 8008h + formula	4510 8408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4510 700Ch + formula	4510 800Ch + formula	4510 840Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4510 7010h + formula	4510 8010h + formula	4510 8410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4510 7014h + formula	4510 8014h + formula	4510 8414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4510 7018h + formula	4510 8018h + formula	4510 8418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4510 701Ch + formula	4510 801Ch + formula	4510 841Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-89. Firewall Region Registers for MCU_CBASS0 Slaves 6

Offset	Acronym	Register Name	MCU_TIMER2_FW Physical Address	MCU_TIMER3_FW Physical Address	MCU_TIMER4_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4510 8800h + formula	4510 8C00h + formula	4510 9000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4510 8804h + formula	4510 8C04h + formula	4510 9004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4510 8808h + formula	4510 8C08h + formula	4510 9008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4510 880Ch + formula	4510 8C0Ch + formula	4510 900Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4510 8810h + formula	4510 8C10h + formula	4510 9010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4510 8814h + formula	4510 8C14h + formula	4510 9014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4510 8818h + formula	4510 8C18h + formula	4510 9018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4510 881Ch + formula	4510 8C1Ch + formula	4510 901Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-90. Firewall Region Registers for MCU_CBASS0 Slaves 7

Offset	Acronym	Register Name	MCU_TIMER5_FW Physical Address	MCU_TIMER6_FW Physical Address	MCU_TIMER7_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4510 9400h + formula	4510 9800h + formula	4510 9C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4510 9404h + formula	4510 9804h + formula	4510 9C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4510 9408h + formula	4510 9808h + formula	4510 9C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4510 940Ch + formula	4510 980Ch + formula	4510 9C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4510 9410h + formula	4510 9810h + formula	4510 9C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4510 9414h + formula	4510 9814h + formula	4510 9C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4510 9418h + formula	4510 9818h + formula	4510 9C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4510 941Ch + formula	4510 981Ch + formula	4510 9C1Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-91. Firewall Region Registers for MCU_CBASS0 Slaves 8

Offset	Acronym	Register Name	MCU_TIMER8_FW Physical Address	MCU_TIMER9_FW Physical Address	MCU_SPI0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4510 A000h + formula	4510 A400h + formula	4510 C000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4510 A004h + formula	4510 A404h + formula	4510 C004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4510 A008h + formula	4510 A408h + formula	4510 C008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4510 A00Ch + formula	4510 A40Ch + formula	4510 C00Ch + formula

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Table 1-91. Firewall Region Registers for MCU_CBASS0 Slaves 8 (continued)

Offset	Acronym	Register Name	MCU_TIMER8_FW Physical Address	MCU_TIMER9_FW Physical Address	MCU_SPI0_FW Physical Address
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4510 A010h + formula	4510 A410h + formula	4510 C010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4510 A014h + formula	4510 A414h + formula	4510 C014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4510 A018h + formula	4510 A418h + formula	4510 C018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4510 A01Ch + formula	4510 A41Ch + formula	4510 C01Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-92. Firewall Region Registers for MCU_CBASS0 Slaves 9

Offset	Acronym	Register Name	MCU_SPI1_FW Physical Address	MCU_SPI2_FW Physical Address	MCU_DCC0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4510 C400h + formula	4510 C800h + formula	4511 0000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4510 C404h + formula	4510 C804h + formula	4511 0004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4510 C408h + formula	4510 C808h + formula	4511 0008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4510 C40Ch + formula	4510 C80Ch + formula	4511 000Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4510 C410h + formula	4510 C810h + formula	4511 0010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4510 C414h + formula	4510 C814h + formula	4511 0014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4510 C418h + formula	4510 C818h + formula	4511 0018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4510 C41Ch + formula	4510 C81Ch + formula	4511 001Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-93. Firewall Region Registers for MCU_CBASS0 Slaves 10

Offset	Acronym	Register Name	MCU_DCC1_FW Physical Address	MCU_DCC2_FW Physical Address	MCU_ADC0_DMA_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4511 0400h + formula	4511 0800h + formula	4511 4000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4511 0404h + formula	4511 0804h + formula	4511 4004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4511 0408h + formula	4511 0808h + formula	4511 4008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4511 040Ch + formula	4511 080Ch + formula	4511 400Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4511 0410h + formula	4511 0810h + formula	4511 4010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4511 0414h + formula	4511 0814h + formula	4511 4014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4511 0418h + formula	4511 0818h + formula	4511 4018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4511 041Ch + formula	4511 081Ch + formula	4511 401Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-94. Firewall Region Registers for MCU_CBASS0 Slaves 11

Offset	Acronym	Register Name	MCU_ADC0_CFG _FW Physical Address	MCU_ADC1_DMA _FW Physical Address	MCU_ADC1_CFG _FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4511 4400h + formula	4511 4800h + formula	4511 4C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4511 4404h + formula	4511 4804h + formula	4511 4C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4511 4408h + formula	4511 4808h + formula	4511 4C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4511 440Ch + formula	4511 480Ch + formula	4511 4C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4511 4410h + formula	4511 4810h + formula	4511 4C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4511 4414h + formula	4511 4814h + formula	4511 4C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4511 4418h + formula	4511 4818h + formula	4511 4C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4511 441Ch + formula	4511 481Ch + formula	4511 4C1Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-95. Firewall Region Registers for MCU_CBASS0 Slaves 12

Offset	Acronym	Register Name	MCU_UART0_FW Physical Address	MCU_I2C0_FW Physical Address	MCU_I2C1_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4511 8000h + formula	4512 0000h + formula	4512 0400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4511 8004h + formula	4512 0004h + formula	4512 0404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4511 8008h + formula	4512 0008h + formula	4512 0408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4511 800Ch + formula	4512 000Ch + formula	4512 040Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4511 8010h + formula	4512 0010h + formula	4512 0410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4511 8014h + formula	4512 0014h + formula	4512 0414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4511 8018h + formula	4512 0018h + formula	4512 0418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4511 801Ch + formula	4512 001Ch + formula	4512 041Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-96. Firewall Region Registers for MCU_CBASS0 Slaves 13

Offset	Acronym	Register Name	MCU_I3C0_FW Physical Address	MCU_I3C1_FW Physical Address	MCU_ESM0_CFG _FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4512 2000h + formula	4512 2400h + formula	4512 4000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4512 2004h + formula	4512 2404h + formula	4512 4004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4512 2008h + formula	4512 2408h + formula	4512 4008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4512 200Ch + formula	4512 240Ch + formula	4512 400Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4512 2010h + formula	4512 2410h + formula	4512 4010h + formula

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Table 1-96. Firewall Region Registers for MCU_CBASS0 Slaves 13 (continued)

Offset	Acronym	Register Name	MCU_I3C0_FW Physical Address	MCU_I3C1_FW Physical Address	MCU_ESM0_CFG_FW Physical Address
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4512 2014h + formula	4512 2414h + formula	4512 4014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4512 2018h + formula	4512 2418h + formula	4512 4018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4512 201Ch + formula	4512 241Ch + formula	4512 401Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-97. Firewall Region Registers for MCU_CBASS0 Slaves 14

Offset	Acronym	Register Name	MCU_MCAN0_FW Physical Address	MCU_MCAN1_FW Physical Address	MCU_CTRL_MMR0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4512 8000h + formula	4512 8400h + formula	4512 C000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4512 8004h + formula	4512 8404h + formula	4512 C004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4512 8008h + formula	4512 8408h + formula	4512 C008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4512 800Ch + formula	4512 840Ch + formula	4512 C00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4512 8010h + formula	4512 8410h + formula	4512 C010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4512 8014h + formula	4512 8414h + formula	4512 C014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4512 8018h + formula	4512 8418h + formula	4512 C018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4512 801Ch + formula	4512 841Ch + formula	4512 C01Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-98. Firewall Region Registers for MCU_CBASS0 Slaves 15

Offset	Acronym	Register Name	MCU_PLL0_CFG_FW Physical Address	MCU_EFUSE0_FW Physical Address	MCU_PBIST0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4512 C400h + formula	4512 E000h + formula	4512 F000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4512 C404h + formula	4512 E004h + formula	4512 F004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4512 C408h + formula	4512 E008h + formula	4512 F008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4512 C40Ch + formula	4512 E00Ch + formula	4512 F00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4512 C410h + formula	4512 E010h + formula	4512 F010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4512 C414h + formula	4512 E014h + formula	4512 F014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4512 C418h + formula	4512 E018h + formula	4512 F018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4512 C41Ch + formula	4512 E01Ch + formula	4512 F01Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-99. Firewall Region Registers for MCU_CBASS0 Slaves 16

Offset	Acronym	Register Name	MCU_PBIST_R5FSS0_CFG_FW Physical Address	MCU_CPSW0_FW Physical Address	MCU_CBASS0_ERR_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4512 F400h + formula	4513 1000h + formula	4513 7000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4512 F404h + formula	4513 1004h + formula	4513 7004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4512 F408h + formula	4513 1008h + formula	4513 7008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4512 F40Ch + formula	4513 100Ch + formula	4513 700Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4512 F410h + formula	4513 1010h + formula	4513 7010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4512 F414h + formula	4513 1014h + formula	4513 7014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4512 F418h + formula	4513 1018h + formula	4513 7018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4512 F41Ch + formula	4513 101Ch + formula	4513 701Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-100. Firewall Region Registers for MCU_CBASS0 Slaves 17

Offset	Acronym	Register Name	MCU_FW_CBASS0_ERR_FW Physical Address	MCU_ECC_AGGR0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4513 7800h + formula	4513 9400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4513 7804h + formula	4513 9404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4513 7808h + formula	4513 9408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4513 780Ch + formula	4513 940Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4513 7810h + formula	4513 9410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4513 7814h + formula	4513 9414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4513 7818h + formula	4513 9418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4513 781Ch + formula	4513 941Ch + formula

(1) See column "**Firewall Regions**" in for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-101. Firewall Region Registers for CBASS0 Slaves 1

Offset	Acronym	Register Name	EPWM0_FW Physical Address	HRPWM0_FW Physical Address	EPWM1_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 0000h + formula	4520 0400h + formula	4520 0800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 0004h + formula	4520 0404h + formula	4520 0804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 0008h + formula	4520 0408h + formula	4520 0808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 000Ch + formula	4520 040Ch + formula	4520 080Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 0010h + formula	4520 0410h + formula	4520 0810h + formula

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Table 1-101. Firewall Region Registers for CBASS0 Slaves 1 (continued)

Offset	Acronym	Register Name	EPWM0_FW Physical Address	HRPWM0_FW Physical Address	EPWM1_FW Physical Address
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 0014h + formula	4520 0414h + formula	4520 0814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 0018h + formula	4520 0418h + formula	4520 0818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 001Ch + formula	4520 041Ch + formula	4520 081Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-102. Firewall Region Registers for CBASS0 Slaves 2

Offset	Acronym	Register Name	HRPWM1_FW Physical Address	EPWM2_FW Physical Address	HRPWM2_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 0C00h + formula	4520 1000h + formula	4520 1400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 0C04h + formula	4520 1004h + formula	4520 1404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 0C08h + formula	4520 1008h + formula	4520 1408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 0C0Ch + formula	4520 100Ch + formula	4520 140Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 0C10h + formula	4520 1010h + formula	4520 1410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 0C14h + formula	4520 1014h + formula	4520 1414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 0C18h + formula	4520 1018h + formula	4520 1418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 0C1Ch + formula	4520 101Ch + formula	4520 141Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-103. Firewall Region Registers for CBASS0 Slaves 3

Offset	Acronym	Register Name	EPWM3_FW Physical Address	HRPWM3_FW Physical Address	EPWM4_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 1800h + formula	4520 1C00h + formula	4520 2000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 1804h + formula	4520 1C04h + formula	4520 2004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 1808h + formula	4520 1C08h + formula	4520 2008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 180Ch + formula	4520 1C0Ch + formula	4520 200Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 1810h + formula	4520 1C10h + formula	4520 2010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 1814h + formula	4520 1C14h + formula	4520 2014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 1818h + formula	4520 1C18h + formula	4520 2018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 181Ch + formula	4520 1C1Ch + formula	4520 201Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-104. Firewall Region Registers for CBASS0 Slaves 4

Offset	Acronym	Register Name	HRPWM4_FW Physical Address	EPWM5_FW Physical Address	HRPWM5_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 2400h + formula	4520 2800h + formula	4520 2C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 2404h + formula	4520 2804h + formula	4520 2C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 2408h + formula	4520 2808h + formula	4520 2C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 240Ch + formula	4520 280Ch + formula	4520 2C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 2410h + formula	4520 2810h + formula	4520 2C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 2414h + formula	4520 2814h + formula	4520 2C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 2418h + formula	4520 2818h + formula	4520 2C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 241Ch + formula	4520 281Ch + formula	4520 2C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-105. Firewall Region Registers for CBASS0 Slaves 5

Offset	Acronym	Register Name	EQEP0_FW Physical Address	EQEP1_FW Physical Address	EQEP2_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 4000h + formula	4520 4400h + formula	4520 4800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 4004h + formula	4520 4404h + formula	4520 4804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 4008h + formula	4520 4408h + formula	4520 4808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 400Ch + formula	4520 440Ch + formula	4520 480Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 4010h + formula	4520 4410h + formula	4520 4810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 4014h + formula	4520 4414h + formula	4520 4814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 4018h + formula	4520 4418h + formula	4520 4818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 401Ch + formula	4520 441Ch + formula	4520 481Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-106. Firewall Region Registers for CBASS0 Slaves 6

Offset	Acronym	Register Name	ECAP0_FW Physical Address	ECAP1_FW Physical Address	ECAP2_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 5000h + formula	4520 5400h + formula	4520 5800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 5004h + formula	4520 5404h + formula	4520 5804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 5008h + formula	4520 5408h + formula	4520 5808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 500Ch + formula	4520 540Ch + formula	4520 580Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 5010h + formula	4520 5410h + formula	4520 5810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 5014h + formula	4520 5414h + formula	4520 5814h + formula

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Table 1-106. Firewall Region Registers for CBASS0 Slaves 6 (continued)

Offset	Acronym	Register Name	ECAP0_FW Physical Address	ECAP1_FW Physical Address	ECAP2_FW Physical Address
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 5018h + formula	4520 5418h + formula	4520 5818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 501Ch + formula	4520 541Ch + formula	4520 581Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-107. Firewall Region Registers for CBASS0 Slaves 7

Offset	Acronym	Register Name	I2C0_FW Physical Address	I2C1_FW Physical Address	I2C2_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 6000h + formula	4520 6400h + formula	4520 6800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 6004h + formula	4520 6404h + formula	4520 6804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 6008h + formula	4520 6408h + formula	4520 6808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 600Ch + formula	4520 640Ch + formula	4520 680Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 6010h + formula	4520 6410h + formula	4520 6810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 6014h + formula	4520 6414h + formula	4520 6814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 6018h + formula	4520 6418h + formula	4520 6818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 601Ch + formula	4520 641Ch + formula	4520 681Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-108. Firewall Region Registers for CBASS0 Slaves 8

Offset	Acronym	Register Name	I2C3_FW Physical Address	I2C4_FW Physical Address	I2C5_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 6C00h + formula	4520 7000h + formula	4520 7400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 6C04h + formula	4520 7004h + formula	4520 7404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 6C08h + formula	4520 7008h + formula	4520 7408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 6C0Ch + formula	4520 700Ch + formula	4520 740Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 6C10h + formula	4520 7010h + formula	4520 7410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 6C14h + formula	4520 7014h + formula	4520 7414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 6C18h + formula	4520 7018h + formula	4520 7418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 6C1Ch + formula	4520 701Ch + formula	4520 741Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-109. Firewall Region Registers for CBASS0 Slaves 9

Offset	Acronym	Register Name	I2C6_FW Physical Address	ATL0_FW Physical Address	I3C0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 7800h + formula	4520 8000h + formula	4520 8800h + formula

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Table 1-109. Firewall Region Registers for CBASS0 Slaves 9 (continued)

Offset	Acronym	Register Name	I2C6_FW Physical Address	ATL0_FW Physical Address	I3C0_FW Physical Address
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 7804h + formula	4520 8004h + formula	4520 8804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 7808h + formula	4520 8008h + formula	4520 8808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 780Ch + formula	4520 800Ch + formula	4520 880Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 7810h + formula	4520 8010h + formula	4520 8810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 7814h + formula	4520 8014h + formula	4520 8814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 7818h + formula	4520 8018h + formula	4520 8818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 781Ch + formula	4520 801Ch + formula	4520 881Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-110. Firewall Region Registers for CBASS0 Slaves 10

Offset	Acronym	Register Name	RTI0_FW Physical Address	RTI1_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 9800h + formula	4520 9C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 9804h + formula	4520 9C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 9808h + formula	4520 9C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 980Ch + formula	4520 9C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 9810h + formula	4520 9C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 9814h + formula	4520 9C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 9818h + formula	4520 9C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 981Ch + formula	4520 9C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-111. Firewall Region Registers for CBASS0 Slaves 12

Offset	Acronym	Register Name	RTI28_FW Physical Address	RTI29_FW Physical Address	RTI30_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 B800h + formula	4520 BC00h + formula	4520 C000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 B804h + formula	4520 BC04h + formula	4520 C004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 B808h + formula	4520 BC08h + formula	4520 C008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 B80Ch + formula	4520 BC0Ch + formula	4520 C00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 B810h + formula	4520 BC10h + formula	4520 C010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 B814h + formula	4520 BC14h + formula	4520 C014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 B818h + formula	4520 BC18h + formula	4520 C018h + formula

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Table 1-111. Firewall Region Registers for CBASS0 Slaves 12 (continued)

Offset	Acronym	Register Name	RTI28_FW Physical Address	RTI29_FW Physical Address	RTI30_FW Physical Address
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 B81Ch + formula	4520 BC1Ch + formula	4520 C01Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-112. Firewall Region Registers for CBASS0 Slaves 13

Offset	Acronym	Register Name	RTI31_FW Physical Address	RTI16_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 C400h + formula	4520 D000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 C404h + formula	4520 D004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 C408h + formula	4520 D008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 C40Ch + formula	4520 D00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 C410h + formula	4520 D010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 C414h + formula	4520 D014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 C418h + formula	4520 D018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 C41Ch + formula	4520 D01Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-113. Firewall Region Registers for CBASS0 Slaves 14

Offset	Acronym	Register Name	RTI24_FW Physical Address	RTI25_FW Physical Address	RTI15_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4520 E000h + formula	4520 E400h + formula	4520 F000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4520 E004h + formula	4520 E404h + formula	4520 F004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4520 E008h + formula	4520 E408h + formula	4520 F008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4520 E00Ch + formula	4520 E40Ch + formula	4520 F00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4520 E010h + formula	4520 E410h + formula	4520 F010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4520 E014h + formula	4520 E414h + formula	4520 F014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4520 E018h + formula	4520 E418h + formula	4520 F018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4520 E01Ch + formula	4520 E41Ch + formula	4520 F01Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-114. Firewall Region Registers for CBASS0 Slaves 15

Offset	Acronym	Register Name	TIMER0_FW Physical Address	TIMER1_FW Physical Address	TIMER2_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 0000h + formula	4521 0400h + formula	4521 0800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 0004h + formula	4521 0404h + formula	4521 0804h + formula

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Table 1-114. Firewall Region Registers for CBASS0 Slaves 15 (continued)

Offset	Acronym	Register Name	TIMER0_FW Physical Address	TIMER1_FW Physical Address	TIMER2_FW Physical Address
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 0008h + formula	4521 0408h + formula	4521 0808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 000Ch + formula	4521 040Ch + formula	4521 080Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 0010h + formula	4521 0410h + formula	4521 0810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 0014h + formula	4521 0414h + formula	4521 0814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 0018h + formula	4521 0418h + formula	4521 0818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 001Ch + formula	4521 041Ch + formula	4521 081Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-115. Firewall Region Registers for CBASS0 Slaves 16

Offset	Acronym	Register Name	TIMER3_FW Physical Address	TIMER4_FW Physical Address	TIMER5_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 0C00h + formula	4521 1000h + formula	4521 1400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 0C04h + formula	4521 1004h + formula	4521 1404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 0C08h + formula	4521 1008h + formula	4521 1408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 0C0Ch + formula	4521 100Ch + formula	4521 140Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 0C10h + formula	4521 1010h + formula	4521 1410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 0C14h + formula	4521 1014h + formula	4521 1414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 0C18h + formula	4521 1018h + formula	4521 1418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 0C1Ch + formula	4521 101Ch + formula	4521 141Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-116. Firewall Region Registers for CBASS0 Slaves 17

Offset	Acronym	Register Name	TIMER6_FW Physical Address	TIMER7_FW Physical Address	TIMER8_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 1800h + formula	4521 1C00h + formula	4521 2000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 1804h + formula	4521 1C04h + formula	4521 2004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 1808h + formula	4521 1C08h + formula	4521 2008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 180Ch + formula	4521 1C0Ch + formula	4521 200Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 1810h + formula	4521 1C10h + formula	4521 2010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 1814h + formula	4521 1C14h + formula	4521 2014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 1818h + formula	4521 1C18h + formula	4521 2018h + formula

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Table 1-116. Firewall Region Registers for CBASS0 Slaves 17 (continued)

Offset	Acronym	Register Name	TIMER6_FW Physical Address	TIMER7_FW Physical Address	TIMER8_FW Physical Address
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 181Ch + formula	4521 1C1Ch + formula	4521 201Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-117. Firewall Region Registers for CBASS0 Slaves 18

Offset	Acronym	Register Name	TIMER9_FW Physical Address	TIMER10_FW Physical Address	TIMER11_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 2400h + formula	4521 2800h + formula	4521 2C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 2404h + formula	4521 2804h + formula	4521 2C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 2408h + formula	4521 2808h + formula	4521 2C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 240Ch + formula	4521 280Ch + formula	4521 2C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 2410h + formula	4521 2810h + formula	4521 2C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 2414h + formula	4521 2814h + formula	4521 2C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 2418h + formula	4521 2818h + formula	4521 2C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 241Ch + formula	4521 281Ch + formula	4521 2C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-118. Firewall Region Registers for CBASS0 Slaves 19

Offset	Acronym	Register Name	TIMER12_FW Physical Address	TIMER13_FW Physical Address	TIMER14_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 3000h + formula	4521 3400h + formula	4521 3800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 3004h + formula	4521 3404h + formula	4521 3804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 3008h + formula	4521 3408h + formula	4521 3808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 300Ch + formula	4521 340Ch + formula	4521 380Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 3010h + formula	4521 3410h + formula	4521 3810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 3014h + formula	4521 3414h + formula	4521 3814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 3018h + formula	4521 3418h + formula	4521 3818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 301Ch + formula	4521 341Ch + formula	4521 381Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-119. Firewall Region Registers for CBASS0 Slaves 20

Offset	Acronym	Register Name	TIMER15_FW Physical Address	TIMER16_FW Physical Address	TIMER17_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 3C00h + formula	4521 4000h + formula	4521 4400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 3C04h + formula	4521 4004h + formula	4521 4404h + formula

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Table 1-119. Firewall Region Registers for CBASS0 Slaves 20 (continued)

Offset	Acronym	Register Name	TIMER15_FW Physical Address	TIMER16_FW Physical Address	TIMER17_FW Physical Address
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 3C08h + formula	4521 4008h + formula	4521 4408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 3C0Ch + formula	4521 400Ch + formula	4521 440Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 3C10h + formula	4521 4010h + formula	4521 4410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 3C14h + formula	4521 4014h + formula	4521 4414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 3C18h + formula	4521 4018h + formula	4521 4418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 3C1Ch + formula	4521 401Ch + formula	4521 441Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-120. Firewall Region Registers for CBASS0 Slaves 21

Offset	Acronym	Register Name	TIMER18_FW Physical Address	TIMER19_FW Physical Address	SPI0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 4800h + formula	4521 4C00h + formula	4521 6000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 4804h + formula	4521 4C04h + formula	4521 6004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 4808h + formula	4521 4C08h + formula	4521 6008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 480Ch + formula	4521 4C0Ch + formula	4521 600Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 4810h + formula	4521 4C10h + formula	4521 6010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 4814h + formula	4521 4C14h + formula	4521 6014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 4818h + formula	4521 4C18h + formula	4521 6018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 481Ch + formula	4521 4C1Ch + formula	4521 601Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-121. Firewall Region Registers for CBASS0 Slaves 22

Offset	Acronym	Register Name	SPI1_FW Physical Address	SPI2_FW Physical Address	SPI3_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 6400h + formula	4521 6800h + formula	4521 6C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 6404h + formula	4521 6804h + formula	4521 6C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 6408h + formula	4521 6808h + formula	4521 6C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 640Ch + formula	4521 680Ch + formula	4521 6C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 6410h + formula	4521 6810h + formula	4521 6C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 6414h + formula	4521 6814h + formula	4521 6C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 6418h + formula	4521 6818h + formula	4521 6C18h + formula

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Table 1-121. Firewall Region Registers for CBASS0 Slaves 22 (continued)

Offset	Acronym	Register Name	SPI1_FW Physical Address	SPI2_FW Physical Address	SPI3_FW Physical Address
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 641Ch + formula	4521 681Ch + formula	4521 6C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-122. Firewall Region Registers for CBASS0 Slaves 23

Offset	Acronym	Register Name	SPI4_FW Physical Address	SPI5_FW Physical Address	SPI6_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 7000h + formula	4521 7400h + formula	4521 7800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 7004h + formula	4521 7404h + formula	4521 7804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 7008h + formula	4521 7408h + formula	4521 7808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 700Ch + formula	4521 740Ch + formula	4521 780Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 7010h + formula	4521 7410h + formula	4521 7810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 7014h + formula	4521 7414h + formula	4521 7814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 7018h + formula	4521 7418h + formula	4521 7818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 701Ch + formula	4521 741Ch + formula	4521 781Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-123. Firewall Region Registers for CBASS0 Slaves 24

Offset	Acronym	Register Name	SPI7_FW Physical Address	UART0_FW Physical Address	UART1_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 7C00h + formula	4521 9000h + formula	4521 9400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 7C04h + formula	4521 9004h + formula	4521 9404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 7C08h + formula	4521 9008h + formula	4521 9408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 7C0Ch + formula	4521 900Ch + formula	4521 940Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 7C10h + formula	4521 9010h + formula	4521 9410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 7C14h + formula	4521 9014h + formula	4521 9414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 7C18h + formula	4521 9018h + formula	4521 9418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 7C1Ch + formula	4521 901Ch + formula	4521 941Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-124. Firewall Region Registers for CBASS0 Slaves 25

Offset	Acronym	Register Name	UART2_FW Physical Address	UART3_FW Physical Address	UART4_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 9800h + formula	4521 9C00h + formula	4521 A000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 9804h + formula	4521 9C04h + formula	4521 A004h + formula

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Table 1-124. Firewall Region Registers for CBASS0 Slaves 25 (continued)

Offset	Acronym	Register Name	UART2_FW Physical Address	UART3_FW Physical Address	UART4_FW Physical Address
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 9808h + formula	4521 9C08h + formula	4521 A008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 980Ch + formula	4521 9C0Ch + formula	4521 A00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 9810h + formula	4521 9C10h + formula	4521 A010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 9814h + formula	4521 9C14h + formula	4521 A014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 9818h + formula	4521 9C18h + formula	4521 A018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 981Ch + formula	4521 9C1Ch + formula	4521 A01Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-125. Firewall Region Registers for CBASS0 Slaves 26

Offset	Acronym	Register Name	UART5_FW Physical Address	UART6_FW Physical Address	UART7_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 A400h + formula	4521 A800h + formula	4521 AC00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 A404h + formula	4521 A804h + formula	4521 AC04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 A408h + formula	4521 A808h + formula	4521 AC08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 A40Ch + formula	4521 A80Ch + formula	4521 AC0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 A410h + formula	4521 A810h + formula	4521 AC10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 A414h + formula	4521 A814h + formula	4521 AC14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 A418h + formula	4521 A818h + formula	4521 AC18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 A41Ch + formula	4521 A81Ch + formula	4521 AC1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-126. Firewall Region Registers for CBASS0 Slaves 27

Offset	Acronym	Register Name	UART8_FW Physical Address	UART9_FW Physical Address	MCAN0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 B000h + formula	4521 B400h + formula	4521 C000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 B004h + formula	4521 B404h + formula	4521 C004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 B008h + formula	4521 B408h + formula	4521 C008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 B00Ch + formula	4521 B40Ch + formula	4521 C00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 B010h + formula	4521 B410h + formula	4521 C010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 B014h + formula	4521 B414h + formula	4521 C014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 B018h + formula	4521 B418h + formula	4521 C018h + formula

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Table 1-126. Firewall Region Registers for CBASS0 Slaves 27 (continued)

Offset	Acronym	Register Name	UART8_FW Physical Address	UART9_FW Physical Address	MCAN0_FW Physical Address
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 B01Ch + formula	4521 B41Ch + formula	4521 C01Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-127. Firewall Region Registers for CBASS0 Slaves 28

Offset	Acronym	Register Name	MCAN1_FW Physical Address	MCAN2_FW Physical Address	MCAN3_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 C400h + formula	4521 C800h + formula	4521 CC00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 C404h + formula	4521 C804h + formula	4521 CC04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 C408h + formula	4521 C808h + formula	4521 CC08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 C40Ch + formula	4521 C80Ch + formula	4521 CC0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 C410h + formula	4521 C810h + formula	4521 CC10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 C414h + formula	4521 C814h + formula	4521 CC14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 C418h + formula	4521 C818h + formula	4521 CC18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 C41Ch + formula	4521 C81Ch + formula	4521 CC1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-128. Firewall Region Registers for CBASS0 Slaves 29

Offset	Acronym	Register Name	MCAN4_FW Physical Address	MCAN5_FW Physical Address	MCAN6_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 D000h + formula	4521 D400h + formula	4521 D800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 D004h + formula	4521 D404h + formula	4521 D804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 D008h + formula	4521 D408h + formula	4521 D808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 D00Ch + formula	4521 D40Ch + formula	4521 D80Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 D010h + formula	4521 D410h + formula	4521 D810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 D014h + formula	4521 D414h + formula	4521 D814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 D018h + formula	4521 D418h + formula	4521 D818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 D01Ch + formula	4521 D41Ch + formula	4521 D81Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-129. Firewall Region Registers for CBASS0 Slaves 30

Offset	Acronym	Register Name	MCAN7_FW Physical Address	MCAN8_FW Physical Address	MCAN9_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 DC00h + formula	4521 E000h + formula	4521 E400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 DC04h + formula	4521 E004h + formula	4521 E404h + formula

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Table 1-129. Firewall Region Registers for CBASS0 Slaves 30 (continued)

Offset	Acronym	Register Name	MCAN7_FW Physical Address	MCAN8_FW Physical Address	MCAN9_FW Physical Address
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 DC08h + formula	4521 E008h + formula	4521 E408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 DC0Ch + formula	4521 E00Ch + formula	4521 E40Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 DC10h + formula	4521 E010h + formula	4521 E410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 DC14h + formula	4521 E014h + formula	4521 E414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 DC18h + formula	4521 E018h + formula	4521 E418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 DC1Ch + formula	4521 E01Ch + formula	4521 E41Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-130. Firewall Region Registers for CBASS0 Slaves 31

Offset	Acronym	Register Name	MCAN10_FW Physical Address	MCAN11_FW Physical Address	MCAN12_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 E800h + formula	4521 EC00h + formula	4521 F000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 E804h + formula	4521 EC04h + formula	4521 F004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 E808h + formula	4521 EC08h + formula	4521 F008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 E80Ch + formula	4521 EC0Ch + formula	4521 F00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 E810h + formula	4521 EC10h + formula	4521 F010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 E814h + formula	4521 EC14h + formula	4521 F014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 E818h + formula	4521 EC18h + formula	4521 F018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 E81Ch + formula	4521 EC1Ch + formula	4521 F01Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-131. Firewall Region Registers for CBASS0 Slaves 32

Offset	Acronym	Register Name	MCAN13_FW Physical Address	PDMA_MISC_PSIL0_CFG_FW Physical Address	PDMA_USART_PSIL0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4521 F400h + formula	4522 2000h + formula	4522 2400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4521 F404h + formula	4522 2004h + formula	4522 2404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4521 F408h + formula	4522 2008h + formula	4522 2408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4521 F40Ch + formula	4522 200Ch + formula	4522 240Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4521 F410h + formula	4522 2010h + formula	4522 2410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4521 F414h + formula	4522 2014h + formula	4522 2414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4521 F418h + formula	4522 2018h + formula	4522 2418h + formula

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Table 1-131. Firewall Region Registers for CBASS0 Slaves 32 (continued)

Offset	Acronym	Register Name	MCAN13_FW Physical Address	PDMA_MISC_PSIL0_CFG_FW Physical Address	PDMA_USART_PSIL0_CFG_FW Physical Address
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4521 F41Ch + formula	4522 201Ch + formula	4522 241Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-132. Firewall Region Registers for CBASS0 Slaves 33

Offset	Acronym	Register Name	CBASS_IPPHY0_ERR_FW Physical Address	C66SS0_SRC_FW Physical Address	C66SS1_SRC_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4523 FC00h + formula	4524 0000h + formula	4524 0400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4523 FC04h + formula	4524 0004h + formula	4524 0404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4523 FC08h + formula	4524 0008h + formula	4524 0408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4523 FC0Ch + formula	4524 000Ch + formula	4524 040Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4523 FC10h + formula	4524 0010h + formula	4524 0410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4523 FC14h + formula	4524 0014h + formula	4524 0414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4523 FC18h + formula	4524 0018h + formula	4524 0418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4523 FC1Ch + formula	4524 001Ch + formula	4524 041Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-133. Firewall Region Registers for CBASS0 Slaves 34

Offset	Acronym	Register Name	GPMC0_FW Physical Address	R5FSS0_CORE0_FW Physical Address	R5FSS0_CORE1_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4524 1800h + formula	4524 2800h + formula	4524 2C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4524 1804h + formula	4524 2804h + formula	4524 2C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4524 1808h + formula	4524 2808h + formula	4524 2C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4524 180Ch + formula	4524 280Ch + formula	4524 2C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4524 1810h + formula	4524 2810h + formula	4524 2C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4524 1814h + formula	4524 2814h + formula	4524 2C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4524 1818h + formula	4524 2818h + formula	4524 2C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4524 181Ch + formula	4524 281Ch + formula	4524 2C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-134. Firewall Region Registers for CBASS0 Slaves 35

Offset	Acronym	Register Name	R5FSS1_CORE0_FW Physical Address	R5FSS1_CORE1_FW Physical Address	R5FSS0_CORE0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4524 3000h + formula	4524 3400h + formula	4525 0000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4524 3004h + formula	4524 3404h + formula	4525 0004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4524 3008h + formula	4524 3408h + formula	4525 0008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4524 300Ch + formula	4524 340Ch + formula	4525 000Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4524 3010h + formula	4524 3410h + formula	4525 0010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4524 3014h + formula	4524 3414h + formula	4525 0014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4524 3018h + formula	4524 3418h + formula	4525 0018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4524 301Ch + formula	4524 341Ch + formula	4525 001Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-135. Firewall Region Registers for CBASS0 Slaves 36

Offset	Acronym	Register Name	R5FSS0_CORE1_CFG_FW Physical Address	R5FSS1_CORE0_CFG_FW Physical Address	R5FSS1_CORE1_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4525 0400h + formula	4525 0800h + formula	4525 0C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4525 0404h + formula	4525 0804h + formula	4525 0C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4525 0408h + formula	4525 0808h + formula	4525 0C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4525 040Ch + formula	4525 080Ch + formula	4525 0C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4525 0410h + formula	4525 0810h + formula	4525 0C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4525 0414h + formula	4525 0814h + formula	4525 0C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4525 0418h + formula	4525 0818h + formula	4525 0C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4525 041Ch + formula	4525 081Ch + formula	4525 0C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-136. Firewall Region Registers for CBASS0 Slaves 37

Offset	Acronym	Register Name	C66SS0_CFG_FW Physical Address	C66SS1_CFG_FW Physical Address	MMCSD1_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4525 2000h + formula	4525 2400h + formula	4525 3000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4525 2004h + formula	4525 2404h + formula	4525 3004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4525 2008h + formula	4525 2408h + formula	4525 3008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4525 200Ch + formula	4525 240Ch + formula	4525 300Ch + formula

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Table 1-136. Firewall Region Registers for CBASS0 Slaves 37 (continued)

Offset	Acronym	Register Name	C66SS0_CFG_FW Physical Address	C66SS1_CFG_FW Physical Address	MMCSD1_CFG_FW Physical Address
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4525 2010h + formula	4525 2410h + formula	4525 3010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4525 2014h + formula	4525 2414h + formula	4525 3014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4525 2018h + formula	4525 2418h + formula	4525 3018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4525 201Ch + formula	4525 241Ch + formula	4525 301Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-137. Firewall Region Registers for CBASS0 Slaves 38

Offset	Acronym	Register Name	MMCSD2_CFG_FW Physical Address	ELM0_FW Physical Address	PRU_ICSSG0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4525 3400h + formula	4525 4000h + formula	4525 4800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4525 3404h + formula	4525 4004h + formula	4525 4804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4525 3408h + formula	4525 4008h + formula	4525 4808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4525 340Ch + formula	4525 400Ch + formula	4525 480Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4525 3410h + formula	4525 4010h + formula	4525 4810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4525 3414h + formula	4525 4014h + formula	4525 4814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4525 3418h + formula	4525 4018h + formula	4525 4818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4525 341Ch + formula	4525 401Ch + formula	4525 481Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-138. Firewall Region Registers for CBASS0 Slaves 39

Offset	Acronym	Register Name	PRU_ICSSG1_FW Physical Address	CPSW0_FW Physical Address	VPFE0_RATCFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4525 4C00h + formula	4525 5800h + formula	4525 6800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4525 4C04h + formula	4525 5804h + formula	4525 6804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4525 4C08h + formula	4525 5808h + formula	4525 6808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4525 4C0Ch + formula	4525 580Ch + formula	4525 680Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4525 4C10h + formula	4525 5810h + formula	4525 6810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4525 4C14h + formula	4525 5814h + formula	4525 6814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4525 4C18h + formula	4525 5818h + formula	4525 6818h + formula

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Table 1-138. Firewall Region Registers for CBASS0 Slaves 39 (continued)

Offset	Acronym	Register Name	PRU_ICSSG1_FW Physical Address	CPSW0_FW Physical Address	VPFE0_RATCFG_FW Physical Address
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4525 4C1Ch + formula	4525 581Ch + formula	4525 681Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-139. Firewall Region Registers for CBASS0 Slaves 40

Offset	Acronym	Register Name	VPFE0_CFG_FW Physical Address	NAVSS0_NBSS_CFG_FW Physical Address	COMPUTE_CLUSTER0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4525 6C00h + formula	4525 7800h + formula	4525 8000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4525 6C04h + formula	4525 7804h + formula	4525 8004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4525 6C08h + formula	4525 7808h + formula	4525 8008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4525 6C0Ch + formula	4525 780Ch + formula	4525 800Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4525 6C10h + formula	4525 7810h + formula	4525 8010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4525 6C14h + formula	4525 7814h + formula	4525 8014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4525 6C18h + formula	4525 7818h + formula	4525 8018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4525 6C1Ch + formula	4525 781Ch + formula	4525 801Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-140. Firewall Region Registers for CBASS0 Slaves 41

Offset	Acronym	Register Name	RCNAVSS11_ECC_AGGR_CFG_FW Physical Address	RC4_ECC_AGGR_CFG_FW Physical Address	RC_R500_ECC_AGGR_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4525 A000h + formula	4525 A400h + formula	4525 A800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4525 A004h + formula	4525 A404h + formula	4525 A804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4525 A008h + formula	4525 A408h + formula	4525 A808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4525 A00Ch + formula	4525 A40Ch + formula	4525 A80Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4525 A010h + formula	4525 A410h + formula	4525 A810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4525 A014h + formula	4525 A414h + formula	4525 A814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4525 A018h + formula	4525 A418h + formula	4525 A818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4525 A01Ch + formula	4525 A41Ch + formula	4525 A81Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-141. Firewall Region Registers for CBASS0 Slaves 42

Offset	Acronym	Register Name	RC_R511_ECC_AGGR_CFG_FW Physical Address	RCNAVSS10_ECC_AGGR_CFG_FW Physical Address	PBIST_RC_NAVSS_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4525 AC00h + formula	4525 BC00h + formula	4525 C000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4525 AC04h + formula	4525 BC04h + formula	4525 C004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4525 AC08h + formula	4525 BC08h + formula	4525 C008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4525 AC0Ch + formula	4525 BC0Ch + formula	4525 C00Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4525 AC10h + formula	4525 BC10h + formula	4525 C010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4525 AC14h + formula	4525 BC14h + formula	4525 C014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4525 AC18h + formula	4525 BC18h + formula	4525 C018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4525 AC1Ch + formula	4525 BC1Ch + formula	4525 C01Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-142. Firewall Region Registers for CBASS0 Slaves 43

Offset	Acronym	Register Name	PBIST_RC_NB_CFG_FW Physical Address	PBIST_RC_R5FSS0_CFG_FW Physical Address	PBIST_RC_R5FSS1_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4525 C400h + formula	4525 C800h + formula	4525 CC00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4525 C404h + formula	4525 C804h + formula	4525 CC04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4525 C408h + formula	4525 C808h + formula	4525 CC08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4525 C40Ch + formula	4525 C80Ch + formula	4525 CC0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4525 C410h + formula	4525 C810h + formula	4525 CC10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4525 C414h + formula	4525 C814h + formula	4525 CC14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4525 C418h + formula	4525 C818h + formula	4525 CC18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4525 C41Ch + formula	4525 C81Ch + formula	4525 CC1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-143. Firewall Region Registers for CBASS0 Slaves 44

Offset	Acronym	Register Name	CBASS_RC0_ERR_FW Physical Address	CBASS_RC_CFG0_ERR_FW Physical Address	CSI_RX0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4525 F800h + formula	4525 FC00h + formula	4526 0000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4525 F804h + formula	4525 FC04h + formula	4526 0004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4525 F808h + formula	4525 FC08h + formula	4526 0008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4525 F80Ch + formula	4525 FC0Ch + formula	4526 000Ch + formula

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Table 1-143. Firewall Region Registers for CBASS0 Slaves 44 (continued)

Offset	Acronym	Register Name	CBASS_RC0_ERR_FW Physical Address	CBASS_RC_CFG0_ERR_FW Physical Address	CSI_RX0_FW Physical Address
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4525 F810h + formula	4525 FC10h + formula	4526 0010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4525 F814h + formula	4525 FC14h + formula	4526 0014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4525 F818h + formula	4525 FC18h + formula	4526 0018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4525 F81Ch + formula	4525 FC1Ch + formula	4526 001Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-144. Firewall Region Registers for CBASS0 Slaves 45

Offset	Acronym	Register Name	CSI_RX1_FW Physical Address	DPHY_RX0_FW Physical Address	DPHY_RX1_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4526 0400h + formula	4526 1000h + formula	4526 1400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4526 0404h + formula	4526 1004h + formula	4526 1404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4526 0408h + formula	4526 1008h + formula	4526 1408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4526 040Ch + formula	4526 100Ch + formula	4526 140Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4526 0410h + formula	4526 1010h + formula	4526 1410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4526 0414h + formula	4526 1014h + formula	4526 1414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4526 0418h + formula	4526 1018h + formula	4526 1418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4526 041Ch + formula	4526 101Ch + formula	4526 141Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-145. Firewall Region Registers for CBASS0 Slaves 46

Offset	Acronym	Register Name	CSI_TX0_FW Physical Address	DPHY_TX0_FW Physical Address	CSI_PSIL0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4526 2000h + formula	4526 2800h + formula	4526 3800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4526 2004h + formula	4526 2804h + formula	4526 3804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4526 2008h + formula	4526 2808h + formula	4526 3808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4526 200Ch + formula	4526 280Ch + formula	4526 380Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4526 2010h + formula	4526 2810h + formula	4526 3810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4526 2014h + formula	4526 2814h + formula	4526 3814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4526 2018h + formula	4526 2818h + formula	4526 3818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4526 201Ch + formula	4526 281Ch + formula	4526 381Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-146. Firewall Region Registers for CBASS0 Slaves 47

Offset	Acronym	Register Name	CBASS_CSI0_ERR_FW Physical Address	STM0_FW Physical Address	DEBUGSS0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4526 7C00h + formula	4526 8000h + formula	4526 8400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4526 7C04h + formula	4526 8004h + formula	4526 8404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4526 7C08h + formula	4526 8008h + formula	4526 8408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4526 7C0Ch + formula	4526 800Ch + formula	4526 840Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4526 7C10h + formula	4526 8010h + formula	4526 8410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4526 7C14h + formula	4526 8014h + formula	4526 8414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4526 7C18h + formula	4526 8018h + formula	4526 8418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4526 7C1Ch + formula	4526 801Ch + formula	4526 841Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-147. Firewall Region Registers for CBASS0 Slaves 48

Offset	Acronym	Register Name	MAIN_DEBUG_CELL0_FW Physical Address	CC_DEBUG_CELL0_FW Physical Address	MAIN_DEBUG_CELL1_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4526 8800h + formula	4526 8C00h + formula	4526 9000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4526 8804h + formula	4526 8C04h + formula	4526 9004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4526 8808h + formula	4526 8C08h + formula	4526 9008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4526 880Ch + formula	4526 8C0Ch + formula	4526 900Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4526 8810h + formula	4526 8C10h + formula	4526 9010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4526 8814h + formula	4526 8C14h + formula	4526 9014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4526 8818h + formula	4526 8C18h + formula	4526 9018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4526 881Ch + formula	4526 8C1Ch + formula	4526 901Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-148. Firewall Region Registers for CBASS0 Slaves 49

Offset	Acronym	Register Name	C66SS0_DEBUG_CELL_FW Physical Address	C66SS1_DEBUG_CELL_FW Physical Address	PDMA_DEBUG_PSIL0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4526 9400h + formula	4526 9800h + formula	4526 A000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4526 9404h + formula	4526 9804h + formula	4526 A004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4526 9408h + formula	4526 9808h + formula	4526 A008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4526 940Ch + formula	4526 980Ch + formula	4526 A00Ch + formula

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Table 1-148. Firewall Region Registers for CBASS0 Slaves 49 (continued)

Offset	Acronym	Register Name	C66SS0_DEBUG_CELL_FW Physical Address	C66SS1_DEBUG_CELL_FW Physical Address	PDMA_DEBUG_PSIL0_CFG_FW Physical Address
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4526 9410h + formula	4526 9810h + formula	4526 A010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4526 9414h + formula	4526 9814h + formula	4526 A014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4526 9418h + formula	4526 9818h + formula	4526 A018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4526 941Ch + formula	4526 981Ch + formula	4526 A01Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-149. Firewall Region Registers for CBASS0 Slaves 50

Offset	Acronym	Register Name	CBASS_DATADEBUG0_ERR_FW Physical Address	MCASP3_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4526 FC00h + formula	4527 0000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4526 FC04h + formula	4527 0004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4526 FC08h + formula	4527 0008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4526 FC0Ch + formula	4527 000Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4526 FC10h + formula	4527 0010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4526 FC14h + formula	4527 0014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4526 FC18h + formula	4527 0018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4526 FC1Ch + formula	4527 001Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-150. Firewall Region Registers for CBASS0 Slaves 51

Offset	Acronym	Register Name	MCASP3_DMA_FW Physical Address	MCASP4_CFG_FW Physical Address	MCASP4_DMA_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4527 0400h + formula	4527 0800h + formula	4527 0C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4527 0404h + formula	4527 0804h + formula	4527 0C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4527 0408h + formula	4527 0808h + formula	4527 0C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4527 040Ch + formula	4527 080Ch + formula	4527 0C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4527 0410h + formula	4527 0810h + formula	4527 0C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4527 0414h + formula	4527 0814h + formula	4527 0C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4527 0418h + formula	4527 0818h + formula	4527 0C18h + formula

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Table 1-150. Firewall Region Registers for CBASS0 Slaves 51 (continued)

Offset	Acronym	Register Name	MCASP3_DMA_FW Physical Address	MCASP4_CFG_FW Physical Address	MCASP4_DMA_FW Physical Address
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4527 041Ch + formula	4527 081Ch + formula	4527 0C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-151. Firewall Region Registers for CBASS0 Slaves 52

Offset	Acronym	Register Name	MCASP5_CFG_FW Physical Address	MCASP5_DMA_FW Physical Address	MCASP6_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4527 1000h + formula	4527 1400h + formula	4527 1800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4527 1004h + formula	4527 1404h + formula	4527 1804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4527 1008h + formula	4527 1408h + formula	4527 1808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4527 100Ch + formula	4527 140Ch + formula	4527 180Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4527 1010h + formula	4527 1410h + formula	4527 1810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4527 1014h + formula	4527 1414h + formula	4527 1814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4527 1018h + formula	4527 1418h + formula	4527 1818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4527 101Ch + formula	4527 141Ch + formula	4527 181Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-152. Firewall Region Registers for CBASS0 Slaves 53

Offset	Acronym	Register Name	MCASP6_DMA_FW Physical Address	MCASP7_CFG_FW Physical Address	MCASP7_DMA_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4527 1C00h + formula	4527 2000h + formula	4527 2400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4527 1C04h + formula	4527 2004h + formula	4527 2404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4527 1C08h + formula	4527 2008h + formula	4527 2408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4527 1C0Ch + formula	4527 200Ch + formula	4527 240Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4527 1C10h + formula	4527 2010h + formula	4527 2410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4527 1C14h + formula	4527 2014h + formula	4527 2414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4527 1C18h + formula	4527 2018h + formula	4527 2418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4527 1C1Ch + formula	4527 201Ch + formula	4527 241Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-153. Firewall Region Registers for CBASS0 Slaves 54

Offset	Acronym	Register Name	MCASP8_CFG_FW Physical Address	MCASP8_DMA_FW Physical Address	MCASP9_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4527 2800h + formula	4527 2C00h + formula	4527 3000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4527 2804h + formula	4527 2C04h + formula	4527 3004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4527 2808h + formula	4527 2C08h + formula	4527 3008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4527 280Ch + formula	4527 2C0Ch + formula	4527 300Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4527 2810h + formula	4527 2C10h + formula	4527 3010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4527 2814h + formula	4527 2C14h + formula	4527 3014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4527 2818h + formula	4527 2C18h + formula	4527 3018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4527 281Ch + formula	4527 2C1Ch + formula	4527 301Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-154. Firewall Region Registers for CBASS0 Slaves 55

Offset	Acronym	Register Name	MCASP9_DMA_FW Physical Address	MCASP10_CFG_FW Physical Address	MCASP10_DMA_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4527 3400h + formula	4527 3800h + formula	4527 3C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4527 3404h + formula	4527 3804h + formula	4527 3C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4527 3408h + formula	4527 3808h + formula	4527 3C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4527 340Ch + formula	4527 380Ch + formula	4527 3C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4527 3410h + formula	4527 3810h + formula	4527 3C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4527 3414h + formula	4527 3814h + formula	4527 3C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4527 3418h + formula	4527 3818h + formula	4527 3C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4527 341Ch + formula	4527 381Ch + formula	4527 3C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-155. Firewall Region Registers for CBASS0 Slaves 56

Offset	Acronym	Register Name	MCASP11_CFG_FW Physical Address	MCASP11_DMA_FW Physical Address	CBASS_MCASP_G1_0_ERR_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4527 4000h + formula	4527 4400h + formula	4527 7C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4527 4004h + formula	4527 4404h + formula	4527 7C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4527 4008h + formula	4527 4408h + formula	4527 7C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4527 400Ch + formula	4527 440Ch + formula	4527 7C0Ch + formula

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Table 1-155. Firewall Region Registers for CBASS0 Slaves 56 (continued)

Offset	Acronym	Register Name	MCASP11_CFG_ FW Physical Address	MCASP11_DMA_ FW Physical Address	CBASS_MCASP_ G1_0_ERR_FW Physical Address
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4527 4010h + formula	4527 4410h + formula	4527 7C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4527 4014h + formula	4527 4414h + formula	4527 7C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4527 4018h + formula	4527 4418h + formula	4527 7C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4527 401Ch + formula	4527 441Ch + formula	4527 7C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-156. Firewall Region Registers for CBASS0 Slaves 57

Offset	Acronym	Register Name	PCIE0_HP_FW Physical Address	PCIE0_LP_FW Physical Address	PCIE1_HP_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4527 8000h + formula	4527 8400h + formula	4527 8800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4527 8004h + formula	4527 8404h + formula	4527 8804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4527 8008h + formula	4527 8408h + formula	4527 8808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4527 800Ch + formula	4527 840Ch + formula	4527 880Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4527 8010h + formula	4527 8410h + formula	4527 8810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4527 8014h + formula	4527 8414h + formula	4527 8814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4527 8018h + formula	4527 8418h + formula	4527 8818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4527 801Ch + formula	4527 841Ch + formula	4527 881Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-157. Firewall Region Registers for CBASS0 Slaves 58

Offset	Acronym	Register Name	PCIE1_LP_FW Physical Address	PCIE2_HP_FW Physical Address	PCIE2_LP_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4527 8C00h + formula	4527 9000h + formula	4527 9400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4527 8C04h + formula	4527 9004h + formula	4527 9404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4527 8C08h + formula	4527 9008h + formula	4527 9408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4527 8C0Ch + formula	4527 900Ch + formula	4527 940Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4527 8C10h + formula	4527 9010h + formula	4527 9410h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4527 8C14h + formula	4527 9014h + formula	4527 9414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4527 8C18h + formula	4527 9018h + formula	4527 9418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4527 8C1Ch + formula	4527 901Ch + formula	4527 941Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-158. Firewall Region Registers for CBASS0 Slaves 59

Offset	Acronym	Register Name	PCIE3_HP_FW Physical Address	PCIE3_LP_FW Physical Address	PCIE0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4527 9800h + formula	4527 9C00h + formula	4528 0000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4527 9804h + formula	4527 9C04h + formula	4528 0004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4527 9808h + formula	4527 9C08h + formula	4528 0008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4527 980Ch + formula	4527 9C0Ch + formula	4528 000Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4527 9810h + formula	4527 9C10h + formula	4528 0010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4527 9814h + formula	4527 9C14h + formula	4528 0014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4527 9818h + formula	4527 9C18h + formula	4528 0018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4527 981Ch + formula	4527 9C1Ch + formula	4528 001Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-159. Firewall Region Registers for CBASS0 Slaves 60

Offset	Acronym	Register Name	PCIE1_CFG_FW Physical Address	PCIE2_CFG_FW Physical Address	PCIE3_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4528 0400h + formula	4528 0800h + formula	4528 0C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4528 0404h + formula	4528 0804h + formula	4528 0C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4528 0408h + formula	4528 0808h + formula	4528 0C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4528 040Ch + formula	4528 080Ch + formula	4528 0C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4528 0410h + formula	4528 0810h + formula	4528 0C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4528 0414h + formula	4528 0814h + formula	4528 0C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4528 0418h + formula	4528 0818h + formula	4528 0C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4528 041Ch + formula	4528 081Ch + formula	4528 0C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-160. Firewall Region Registers for CBASS0 Slaves 61

Offset	Acronym	Register Name	USB3SS0_CORE_FW Physical Address	USB3SS0_USB2PHY_FW Physical Address	USB3SS1_CORE_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4528 2000h + formula	4528 2400h + formula	4528 2800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4528 2004h + formula	4528 2404h + formula	4528 2804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4528 2008h + formula	4528 2408h + formula	4528 2808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4528 200Ch + formula	4528 240Ch + formula	4528 280Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4528 2010h + formula	4528 2410h + formula	4528 2810h + formula

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Table 1-160. Firewall Region Registers for CBASS0 Slaves 61 (continued)

Offset	Acronym	Register Name	USB3SS0_CORE_FW Physical Address	USB3SS0_USB2PHY_FW Physical Address	USB3SS1_CORE_FW Physical Address
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4528 2014h + formula	4528 2414h + formula	4528 2814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4528 2018h + formula	4528 2418h + formula	4528 2818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4528 201Ch + formula	4528 241Ch + formula	4528 281Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-161. Firewall Region Registers for CBASS0 Slaves 62

Offset	Acronym	Register Name	USB3SS1_USB2PHY_FW Physical Address	MMCSD0_CFG_FW Physical Address	MLBSS0_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4528 2C00h + formula	4528 4000h + formula	4528 4800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4528 2C04h + formula	4528 4004h + formula	4528 4804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4528 2C08h + formula	4528 4008h + formula	4528 4808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4528 2C0Ch + formula	4528 400Ch + formula	4528 480Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4528 2C10h + formula	4528 4010h + formula	4528 4810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4528 2C14h + formula	4528 4014h + formula	4528 4814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4528 2C18h + formula	4528 4018h + formula	4528 4818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4528 2C1Ch + formula	4528 401Ch + formula	4528 481Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-162. Firewall Region Registers for CBASS0 Slaves 63

Offset	Acronym	Register Name	UFS0_CFG_FW Physical Address	HC5_ECC_AGGR_CFG_FW Physical Address	SERDES0_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4528 5000h + formula	4528 5C00h + formula	4528 6000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4528 5004h + formula	4528 5C04h + formula	4528 6004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4528 5008h + formula	4528 5C08h + formula	4528 6008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4528 500Ch + formula	4528 5C0Ch + formula	4528 600Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4528 5010h + formula	4528 5C10h + formula	4528 6010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4528 5014h + formula	4528 5C14h + formula	4528 6014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4528 5018h + formula	4528 5C18h + formula	4528 6018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4528 501Ch + formula	4528 5C1Ch + formula	4528 601Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-163. Firewall Region Registers for CBASS0 Slaves 64

Offset	Acronym	Register Name	SERDES1_FW Physical Address	SERDES2_FW Physical Address	SERDES3_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4528 6400h + formula	4528 6800h + formula	4528 6C00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4528 6404h + formula	4528 6804h + formula	4528 6C04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4528 6408h + formula	4528 6808h + formula	4528 6C08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4528 640Ch + formula	4528 680Ch + formula	4528 6C0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4528 6410h + formula	4528 6810h + formula	4528 6C10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4528 6414h + formula	4528 6814h + formula	4528 6C14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4528 6418h + formula	4528 6818h + formula	4528 6C18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4528 641Ch + formula	4528 681Ch + formula	4528 6C1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-164. Firewall Region Registers for CBASS0 Slaves 65

Offset	Acronym	Register Name	PBIST_HC0_CFG_FW Physical Address	CBASS_HC2_0_ERR_FW Physical Address	CBASS_HC0_ERR_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4528 7000h + formula	4528 7400h + formula	4528 7800h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4528 7004h + formula	4528 7404h + formula	4528 7804h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4528 7008h + formula	4528 7408h + formula	4528 7808h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4528 700Ch + formula	4528 740Ch + formula	4528 780Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4528 7010h + formula	4528 7410h + formula	4528 7810h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4528 7014h + formula	4528 7414h + formula	4528 7814h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4528 7018h + formula	4528 7418h + formula	4528 7818h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4528 701Ch + formula	4528 741Ch + formula	4528 781Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-165. Firewall Region Registers for CBASS0 Slaves 66

Offset	Acronym	Register Name	CBASS_HC_CFG0_ERR_FW Physical Address	MCASP0_CFG_FW Physical Address	MCASP0_DMA_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4528 7C00h + formula	4528 8000h + formula	4528 8400h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4528 7C04h + formula	4528 8004h + formula	4528 8404h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4528 7C08h + formula	4528 8008h + formula	4528 8408h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4528 7C0Ch + formula	4528 800Ch + formula	4528 840Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4528 7C10h + formula	4528 8010h + formula	4528 8410h + formula

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Table 1-165. Firewall Region Registers for CBASS0 Slaves 66 (continued)

Offset	Acronym	Register Name	CBASS_HC_CFG0_ERR_FW Physical Address	MCASP0_CFG_FW Physical Address	MCASP0_DMA_FW Physical Address
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4528 7C14h + formula	4528 8014h + formula	4528 8414h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4528 7C18h + formula	4528 8018h + formula	4528 8418h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4528 7C1Ch + formula	4528 801Ch + formula	4528 841Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-166. Firewall Region Registers for CBASS0 Slaves 67

Offset	Acronym	Register Name	MCASP1_CFG_FW Physical Address	MCASP1_DMA_FW Physical Address	MCASP2_CFG_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4528 8800h + formula	4528 8C00h + formula	4528 9000h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4528 8804h + formula	4528 8C04h + formula	4528 9004h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4528 8808h + formula	4528 8C08h + formula	4528 9008h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4528 880Ch + formula	4528 8C0Ch + formula	4528 900Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4528 8810h + formula	4528 8C10h + formula	4528 9010h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4528 8814h + formula	4528 8C14h + formula	4528 9014h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4528 8818h + formula	4528 8C18h + formula	4528 9018h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4528 881Ch + formula	4528 8C1Ch + formula	4528 901Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

Table 1-167. Firewall Region Registers for CBASS0 Slaves 68

Offset	Acronym	Register Name	MCASP2_DMA_FW Physical Address	PDMA_AASRC_PSIL0_CFG_FW Physical Address	CBASS_MCASP_G0_0_ERR_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4528 9400h + formula	4528 B800h + formula	4528 BC00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4528 9404h + formula	4528 B804h + formula	4528 BC04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4528 9408h + formula	4528 B808h + formula	4528 BC08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4528 940Ch + formula	4528 B80Ch + formula	4528 BC0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4528 9410h + formula	4528 B810h + formula	4528 BC10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4528 9414h + formula	4528 B814h + formula	4528 BC14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4528 9418h + formula	4528 B818h + formula	4528 BC18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4528 941Ch + formula	4528 B81Ch + formula	4528 BC1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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Table 1-168. Firewall Region Registers for CBASS0 Slaves 69

Offset	Acronym	Register Name	AASRC0_CFG_FW Physical Address	AASRC0_DATA_FW Physical Address	CBASS_AASRC0_ERR_FW Physical Address
0h + formula	CBASS_FW_REGION_i_CONTROL (1)	Firewall Region i Control Register	4528 C000h + formula	4528 C400h + formula	4528 FC00h + formula
4h + formula	CBASS_FW_REGION_i_PERMISSION_0 (1)	Firewall Region i Permission 0 Register	4528 C004h + formula	4528 C404h + formula	4528 FC04h + formula
8h + formula	CBASS_FW_REGION_i_PERMISSION_1 (1)	Firewall Region i Permission 1 Register	4528 C008h + formula	4528 C408h + formula	4528 FC08h + formula
Ch + formula	CBASS_FW_REGION_i_PERMISSION_2 (1)	Firewall Region i Permission 2 Register	4528 C00Ch + formula	4528 C40Ch + formula	4528 FC0Ch + formula
10h + formula	CBASS_FW_REGION_i_START_ADDRESS_L (1)	Firewall Region i Start Address Low Register	4528 C010h + formula	4528 C410h + formula	4528 FC10h + formula
14h + formula	CBASS_FW_REGION_i_START_ADDRESS_H (1)	Firewall Region i Start Address High Register	4528 C014h + formula	4528 C414h + formula	4528 FC14h + formula
18h + formula	CBASS_FW_REGION_i_END_ADDRESS_L (1)	Firewall Region i End Address Low Register	4528 C018h + formula	4528 C418h + formula	4528 FC18h + formula
1Ch + formula	CBASS_FW_REGION_i_END_ADDRESS_H (1)	Firewall Region i End Address High Register	4528 C01Ch + formula	4528 C41Ch + formula	4528 FC1Ch + formula

(1) See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value.

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1.3.1 CBASS_FW_REGION_i_CONTROL Register (Offset = 0h + formula) [reset = X]

CBASS_FW_REGION_i_CONTROL is shown in Figure 1-15 and described in Table 1-170.

Return to Summary Table.

The Firewall Region i Control Register defines the control fields for the slave module (see Table 1-63) region i firewall.

Offset = 0h + (i * 20h). See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value. For example, if "Firewall Regions" = 4, therefore i = 0 to 3.

Table 1-169. CBASS_FW_REGION_i_CONTROL Instances

Instance	Physical Address
See Table 1-64 through Table 1-168.	See Table 1-64 through Table 1-168.

Figure 1-15. CBASS_FW_REGION_i_CONTROL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED						CACHE_MODE	BACKGROUND
R/W-X						R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			LOCK	ENABLE			
R/W-X			R/W1S-0h	R/W-0h			

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 1-170. CBASS_FW_REGION_i_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9	CACHE_MODE	R/W	0h	Cache mode for region. Set to 1 to check cache permissions. Set to 0 to ignore cache permissions.
8	BACKGROUND	R/W	0h	Background enable for region. There can be one background region per firewall and foreground regions can have overlapping addresses only with the background region.
7-5	RESERVED	R/W	X	
4	LOCK	R/W1S	0h	Lock region. Once set region values cannot be modified.
3-0	ENABLE	R/W	0h	Enable region. A value of 0xA enables, others disable.

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1.3.2 CBASS_FW_REGION_i_PERMISSION_0 Register (Offset = 4h + formula) [reset = X]

CBASS_FW_REGION_i_PERMISSION_0 is shown in Figure 1-16 and described in Table 1-172.

Return to Summary Table.

The Firewall Region i Permission 0 Register defines the permissions for the slave module (see Table 1-63) region i firewall.

Offset = 4h + (i * 20h). See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value. For example, if "Firewall Regions" = 4, therefore i = 0 to 3.

Table 1-171. CBASS_FW_REGION_i_PERMISSION_0 Instances

Instance	Physical Address
See Table 1-64 through Table 1-168.	See Table 1-64 through Table 1-168.

Figure 1-16. CBASS_FW_REGION_i_PERMISSION_0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-172. CBASS_FW_REGION_i_PERMISSION_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.

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Table 1-172. CBASS_FW_REGION_i_PERMISSION_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

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1.3.3 CBASS_FW_REGION_i_PERMISSION_1 Register (Offset = 8h + formula) [reset = X]

CBASS_FW_REGION_i_PERMISSION_1 is shown in Figure 1-17 and described in Table 1-174.

Return to Summary Table.

The Firewall Region i Permission 1 Register defines the permissions for the slave module (see Table 1-63) region i firewall.

Offset = 8h + (i * 20h). See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value. For example, if "Firewall Regions" = 4, therefore i = 0 to 3.

Table 1-173. CBASS_FW_REGION_i_PERMISSION_1 Instances

Instance	Physical Address
See Table 1-64 through Table 1-168.	See Table 1-64 through Table 1-168.

Figure 1-17. CBASS_FW_REGION_i_PERMISSION_1 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-174. CBASS_FW_REGION_i_PERMISSION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.

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Table 1-174. CBASS_FW_REGION_i_PERMISSION_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

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1.3.4 CBASS_FW_REGION_i_PERMISSION_2 Register (Offset = Ch + formula) [reset = X]

CBASS_FW_REGION_i_PERMISSION_2 is shown in Figure 1-18 and described in Table 1-176.

Return to Summary Table.

The Firewall Region i Permission 2 Register defines the permissions for the module (see Table 1-63) region i firewall.

Offset = Ch + (i * 20h). See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value. For example, if "Firewall Regions" = 4, therefore i = 0 to 3.

Table 1-175. CBASS_FW_REGION_i_PERMISSION_2 Instances

Instance	Physical Address
See Table 1-64 through Table 1-168.	See Table 1-64 through Table 1-168.

Figure 1-18. CBASS_FW_REGION_i_PERMISSION_2 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
PRIV_ID							
R/W-0h							
15	14	13	12	11	10	9	8
NONSEC_USER_DEBUG	NONSEC_USER_CACHEABLE	NONSEC_USER_READ	NONSEC_USER_WRITE	NONSEC_SUPV_DEBUG	NONSEC_SUPV_CACHEABLE	NONSEC_SUPV_READ	NONSEC_SUPV_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SEC_USER_DEBUG	SEC_USER_CACHEABLE	SEC_USER_READ	SEC_USER_WRITE	SEC_SUPV_DEBUG	SEC_SUPV_CACHEABLE	SEC_SUPV_READ	SEC_SUPV_WRITE
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-176. CBASS_FW_REGION_i_PERMISSION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	PRIV_ID	R/W	0h	Allowed privid.
15	NONSEC_USER_DEBUG	R/W	0h	Non-secure user debug allowed.
14	NONSEC_USER_CACHEABLE	R/W	0h	Non-secure user cacheable allowed.
13	NONSEC_USER_READ	R/W	0h	Non-secure user read allowed.
12	NONSEC_USER_WRITE	R/W	0h	Non-secure user write allowed.
11	NONSEC_SUPV_DEBUG	R/W	0h	Non-secure supervisor debug allowed.
10	NONSEC_SUPV_CACHEABLE	R/W	0h	Non-secure supervisor cacheable allowed.
9	NONSEC_SUPV_READ	R/W	0h	Non-secure supervisor read allowed.
8	NONSEC_SUPV_WRITE	R/W	0h	Non-secure supervisor write allowed.
7	SEC_USER_DEBUG	R/W	0h	Secure user debug allowed.
6	SEC_USER_CACHEABLE	R/W	0h	Secure user cacheable allowed.

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Table 1-176. CBASS_FW_REGION_i_PERMISSION_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	SEC_USER_READ	R/W	0h	Secure user read allowed.
4	SEC_USER_WRITE	R/W	0h	Secure user write allowed.
3	SEC_SUPV_DEBUG	R/W	0h	Secure supervisor debug allowed.
2	SEC_SUPV_CACHEABLE	R/W	0h	Secure supervisor cacheable allowed.
1	SEC_SUPV_READ	R/W	0h	Secure supervisor read allowed.
0	SEC_SUPV_WRITE	R/W	0h	Secure supervisor write allowed.

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1.3.5 CBASS_FW_REGION_i_START_ADDRESS_L Register (Offset = 10h + formula) [reset = X]

CBASS_FW_REGION_i_START_ADDRESS_L is shown in Figure 1-19 and described in Table 1-178.

Return to Summary Table.

The Firewall Region i Start Address Low Register defines the start address bits 31 to 0 for the slave module (see Table 1-63) region i firewall.

Offset = 10h + (i * 20h). See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value. For example, if "Firewall Regions" = 4, therefore i = 0 to 3.

Table 1-177. CBASS_FW_REGION_i_START_ADDRESS_L Instances

Instance	Physical Address
See Table 1-64 through Table 1-168.	See Table 1-64 through Table 1-168.

Figure 1-19. CBASS_FW_REGION_i_START_ADDRESS_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
START_ADDRESS_L															
R/W-X															
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
START_ADDRESS_L				START_ADDRESS_LSB											
R/W-X				R-0h											

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 1-178. CBASS_FW_REGION_i_START_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	START_ADDRESS_L	R/W	X	Start address bits 31 to 12. Lowest 12 bits are forced to 0 as address must be 4KB aligned.
11-0	START_ADDRESS_LSB	R	0h	Start address bits 11 to 0 are forced to 0 as address must be 4KB aligned.

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1.3.6 CBASS_FW_REGION_i_START_ADDRESS_H Register (Offset = 14h + formula) [reset = X]

CBASS_FW_REGION_i_START_ADDRESS_H is shown in Figure 1-20 and described in Table 1-180.

Return to Summary Table.

The Firewall Region i Start Address High Register defines the start address bits 47 to 32 for the slave module (see Table 1-63) region i firewall.

Offset = 14h + (i * 20h). See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value. For example, if "Firewall Regions" = 4, therefore i = 0 to 3.

Table 1-179. CBASS_FW_REGION_i_START_ADDRESS_H Instances

Instance	Physical Address
See Table 1-64 through Table 1-168.	See Table 1-64 through Table 1-168.

Figure 1-20. CBASS_FW_REGION_i_START_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																START_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-180. CBASS_FW_REGION_i_START_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	START_ADDRESS_H	R/W	0h	Start address bits 47 to 32.

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1.3.7 CBASS_FW_REGION_i_END_ADDRESS_L Register (Offset = 18h + formula) [reset = X]

CBASS_FW_REGION_i_END_ADDRESS_L is shown in Figure 1-21 and described in Table 1-182.

Return to Summary Table.

The Firewall Region i End Address Low Register defines the end address bits 31 to 0 to include for the slave module (see Table 1-63) region i firewall.

Offset = 18h + (i * 20h). See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value. For example, if "Firewall Regions" = 4, therefore i = 0 to 3.

Table 1-181. CBASS_FW_REGION_i_END_ADDRESS_L Instances

Instance	Physical Address
See Table 1-64 through Table 1-168.	See Table 1-64 through Table 1-168.

Figure 1-21. CBASS_FW_REGION_i_END_ADDRESS_L Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
END_ADDRESS_L															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
END_ADDRESS_L				END_ADDRESS_LSB											
R/W-X				R-FFFh											

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 1-182. CBASS_FW_REGION_i_END_ADDRESS_L Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	END_ADDRESS_L	R/W	X	End address bits 31 to 12 to include in the match. Lowest 12 bits are forced to 1s as address must be 4KB aligned.
11-0	END_ADDRESS_LSB	R	FFFh	End address bits 11 to 0 are forced to 1s as address must be 4KB aligned minus 1.

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1.3.8 CBASS_FW_REGION_i_END_ADDRESS_H Register (Offset = 1Ch + formula) [reset = X]

CBASS_FW_REGION_i_END_ADDRESS_H is shown in Figure 1-22 and described in Table 1-184.

Return to Summary Table.

The Firewall Region i End Address High Register defines the end address bits 47 to 32 to include for the slave module (see Table 1-63) region i firewall.

Offset = 1Ch + (i * 20h). See column "**Firewall Regions**" in through for the "i" values associated with each slave. Decrement by 1 the value of this column to get the max "i" value. For example, if "Firewall Regions" = 4, therefore i = 0 to 3.

Table 1-183. CBASS_FW_REGION_i_END_ADDRESS_H Instances

Instance	Physical Address
See Table 1-64 through Table 1-168.	See Table 1-64 through Table 1-168.

Figure 1-22. CBASS_FW_REGION_i_END_ADDRESS_H Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																END_ADDRESS_H															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-184. CBASS_FW_REGION_i_END_ADDRESS_H Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	END_ADDRESS_H	R/W	0h	End address bits 47 to 32 to include in the match.

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1.4 Null Error Reporting Registers

Table 1-186 through Table 1-192 list the memory-mapped interconnect null error reporting registers. All register offset addresses not listed in these tables should be considered as reserved locations and the register contents should not be modified.

Table 1-185. Null Error Reporting Registers Instances

Instance	Base Address
CBASS_INFRA0_ERR	00B0 0000h
CBASS_FW0_ERR	00B0 8000h
CBASS_HC2_0_ERR	02A8 3000h
CBASS_AC0_ERR	02A8 5000h
CBASS_DATADEBUG0_ERR	02A8 6000h
CBASS_HC0_ERR	02A8 7000h
CBASS_CSI0_ERR	02A8 8000h
CBASS_HC_CFG0_ERR	02A8 9000h
CBASS_MCASP_G0_0_ERR	02A8 A000h
CBASS_MCASP_G1_0_ERR	02A8 B000h
CBASS_RC0_ERR	02A8 C000h
CBASS_RC_CFG0_ERR	02A8 D000h
CBASS_AASRC0_ERR	02A8 E000h
CBASS_IPPHY0_ERR	02A8 F000h
WKUP_CBASS_FW0_ERR	4240 4000h
MCU_CBASS_FW0_ERR	4710 8000h

Table 1-186. Null Error Reporting Registers 1

Offset	Acronym	Register Name	CBASS_INFRA0_ERR Physical Address	CBASS_FW0_ERR Physical Address
0h	CBASS_PID	Revision Register	00B0 0000h	00B0 8000h
4h	CBASS_DESTINATION_ID	Destination ID Register	00B0 0004h	00B0 8004h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	00B0 0024h	00B0 8024h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	00B0 0028h	00B0 8028h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	00B0 002Ch	00B0 802Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	00B0 0030h	00B0 8030h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	00B0 0034h	00B0 8034h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	00B0 0038h	00B0 8038h
50h	CBASS_ERR_INTR_RAW_STAT	Global Interrupt Raw Status Register	00B0 0050h	00B0 8050h
54h	CBASS_ERR_INTR_ENABLED_STAT	Global Interrupt Enabled Status Register	00B0 0054h	00B0 8054h
58h	CBASS_ERR_INTR_ENABLE_SET	Interrupt Enable Set Register	00B0 0058h	00B0 8058h
5Ch	CBASS_ERR_INTR_ENABLE_CLR	Interrupt Enable Clear Register	00B0 005Ch	00B0 805Ch
60h	CBASS_EOI	End of Interrupt Register	00B0 0060h	00B0 8060h

Table 1-187. Null Error Reporting Registers 2

Offset	Acronym	Register Name	CBASS_HC2_0_ERR Physical Address	CBASS_AC0_ERR Physical Address
0h	CBASS_PID	Revision Register	02A8 3000h	02A8 5000h
4h	CBASS_DESTINATION_ID	Destination ID Register	02A8 3004h	02A8 5004h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	02A8 3024h	02A8 5024h

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Table 1-187. Null Error Reporting Registers 2 (continued)

Offset	Acronym	Register Name	CBASS_HC2_0_ERR Physical Address	CBASS_AC0_ERR Physical Address
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	02A8 3028h	02A8 5028h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	02A8 302Ch	02A8 502Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	02A8 3030h	02A8 5030h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	02A8 3034h	02A8 5034h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	02A8 3038h	02A8 5038h
50h	CBASS_ERR_INTR_RAW_STAT	Global Interrupt Raw Status Register	02A8 3050h	02A8 5050h
54h	CBASS_ERR_INTR_ENABLED_STAT	Global Interrupt Enabled Status Register	02A8 3054h	02A8 5054h
58h	CBASS_ERR_INTR_ENABLE_SET	Interrupt Enable Set Register	02A8 3058h	02A8 5058h
5Ch	CBASS_ERR_INTR_ENABLE_CLR	Interrupt Enable Clear Register	02A8 305Ch	02A8 505Ch
60h	CBASS_EOI	End of Interrupt Register	02A8 3060h	02A8 5060h

Table 1-188. Null Error Reporting Registers 3

Offset	Acronym	Register Name	CBASS_DATADEBUG0_ERR Physical Address	CBASS_HC0_ERR Physical Address	CBASS_CSI0_ERR Physical Address
0h	CBASS_PID	Revision Register	02A8 6000h	02A8 7000h	02A8 8000h
4h	CBASS_DESTINATION_ID	Destination ID Register	02A8 6004h	02A8 7004h	02A8 8004h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	02A8 6024h	02A8 7024h	02A8 8024h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	02A8 6028h	02A8 7028h	02A8 8028h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	02A8 602Ch	02A8 702Ch	02A8 802Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	02A8 6030h	02A8 7030h	02A8 8030h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	02A8 6034h	02A8 7034h	02A8 8034h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	02A8 6038h	02A8 7038h	02A8 8038h
50h	CBASS_ERR_INTR_RAW_STAT	Global Interrupt Raw Status Register	02A8 6050h	02A8 7050h	02A8 8050h
54h	CBASS_ERR_INTR_ENABLED_STAT	Global Interrupt Enabled Status Register	02A8 6054h	02A8 7054h	02A8 8054h
58h	CBASS_ERR_INTR_ENABLE_SET	Interrupt Enable Set Register	02A8 6058h	02A8 7058h	02A8 8058h
5Ch	CBASS_ERR_INTR_ENABLE_CLR	Interrupt Enable Clear Register	02A8 605Ch	02A8 705Ch	02A8 805Ch
60h	CBASS_EOI	End of Interrupt Register	02A8 6060h	02A8 7060h	02A8 8060h

Table 1-189. Null Error Reporting Registers 4

Offset	Acronym	Register Name	CBASS_HC_CFG0_ERR Physical Address	CBASS_MCASP_G0_0_ERR Physical Address	CBASS_MCASP_G1_0_ERR Physical Address
0h	CBASS_PID	Revision Register	02A8 9000h	02A8 A000h	02A8 B000h

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Table 1-189. Null Error Reporting Registers 4 (continued)

Offset	Acronym	Register Name	CBASS_HC_CFG0_ERR Physical Address	CBASS_MCASP_G0_0_ERR Physical Address	CBASS_MCASP_G1_0_ERR Physical Address
4h	CBASS_DESTINATION_ID	Destination ID Register	02A8 9004h	02A8 A004h	02A8 B004h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	02A8 9024h	02A8 A024h	02A8 B024h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	02A8 9028h	02A8 A028h	02A8 B028h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	02A8 902Ch	02A8 A02Ch	02A8 B02Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	02A8 9030h	02A8 A030h	02A8 B030h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	02A8 9034h	02A8 A034h	02A8 B034h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	02A8 9038h	02A8 A038h	02A8 B038h
50h	CBASS_ERR_INTR_RAW_STAT	Global Interrupt Raw Status Register	02A8 9050h	02A8 A050h	02A8 B050h
54h	CBASS_ERR_INTR_ENABLED_STAT	Global Interrupt Enabled Status Register	02A8 9054h	02A8 A054h	02A8 B054h
58h	CBASS_ERR_INTR_ENABLE_SET	Interrupt Enable Set Register	02A8 9058h	02A8 A058h	02A8 B058h
5Ch	CBASS_ERR_INTR_ENABLE_CLR	Interrupt Enable Clear Register	02A8 905Ch	02A8 A05Ch	02A8 B05Ch
60h	CBASS_EOI	End of Interrupt Register	02A8 9060h	02A8 A060h	02A8 B060h

Table 1-190. Null Error Reporting Registers 5

Offset	Acronym	Register Name	CBASS_RC0_ERR Physical Address	CBASS_RC_CFG0_ERR Physical Address	CBASS_AASRC0_ERR Physical Address
0h	CBASS_PID	Revision Register	02A8 C000h	02A8 D000h	02A8 E000h
4h	CBASS_DESTINATION_ID	Destination ID Register	02A8 C004h	02A8 D004h	02A8 E004h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	02A8 C024h	02A8 D024h	02A8 E024h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	02A8 C028h	02A8 D028h	02A8 E028h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	02A8 C02Ch	02A8 D02Ch	02A8 E02Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	02A8 C030h	02A8 D030h	02A8 E030h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	02A8 C034h	02A8 D034h	02A8 E034h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	02A8 C038h	02A8 D038h	02A8 E038h
50h	CBASS_ERR_INTR_RAW_STAT	Global Interrupt Raw Status Register	02A8 C050h	02A8 D050h	02A8 E050h
54h	CBASS_ERR_INTR_ENABLED_STAT	Global Interrupt Enabled Status Register	02A8 C054h	02A8 D054h	02A8 E054h
58h	CBASS_ERR_INTR_ENABLE_SET	Interrupt Enable Set Register	02A8 C058h	02A8 D058h	02A8 E058h

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Table 1-190. Null Error Reporting Registers 5 (continued)

Offset	Acronym	Register Name	CBASS_RC0_ERR Physical Address	CBASS_RC_CFG0_ERR Physical Address	CBASS_AASRC0_ERR Physical Address
5Ch	CBASS_ERR_INTR_ENABLE_CLR	Interrupt Enable Clear Register	02A8 C05Ch	02A8 D05Ch	02A8 E05Ch
60h	CBASS_EOI	End of Interrupt Register	02A8 C060h	02A8 D060h	02A8 E060h

Table 1-191. Null Error Reporting Registers 6

Offset	Acronym	Register Name	CBASS_IPPHY0_ERR Physical Address	WKUP_CBASS_FW0_ERR Physical Address
0h	CBASS_PID	Revision Register	02A8 F000h	4240 4000h
4h	CBASS_DESTINATION_ID	Destination ID Register	02A8 F004h	4240 4004h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	02A8 F024h	4240 4024h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	02A8 F028h	4240 4028h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	02A8 F02Ch	4240 402Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	02A8 F030h	4240 4030h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	02A8 F034h	4240 4034h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	02A8 F038h	4240 4038h
50h	CBASS_ERR_INTR_RAW_STAT	Global Interrupt Raw Status Register	02A8 F050h	4240 4050h
54h	CBASS_ERR_INTR_ENABLED_STAT	Global Interrupt Enabled Status Register	02A8 F054h	4240 4054h
58h	CBASS_ERR_INTR_ENABLE_SET	Interrupt Enable Set Register	02A8 F058h	4240 4058h
5Ch	CBASS_ERR_INTR_ENABLE_CLR	Interrupt Enable Clear Register	02A8 F05Ch	4240 405Ch
60h	CBASS_EOI	End of Interrupt Register	02A8 F060h	4240 4060h

Table 1-192. Null Error Reporting Registers 7

Offset	Acronym	Register Name	MCU_CBASS_FW0_ERR Physical Address
0h	CBASS_PID	Revision Register	4710 8000h
4h	CBASS_DESTINATION_ID	Destination ID Register	4710 8004h
24h	CBASS_EXCEPTION_LOGGING_HEADER0	Exception Logging Header 0 Register	4710 8024h
28h	CBASS_EXCEPTION_LOGGING_HEADER1	Exception Logging Header 1 Register	4710 8028h
2Ch	CBASS_EXCEPTION_LOGGING_DATA0	Exception Logging Data 0 Register	4710 802Ch
30h	CBASS_EXCEPTION_LOGGING_DATA1	Exception Logging Data 1 Register	4710 8030h
34h	CBASS_EXCEPTION_LOGGING_DATA2	Exception Logging Data 2 Register	4710 8034h
38h	CBASS_EXCEPTION_LOGGING_DATA3	Exception Logging Data 3 Register	4710 8038h
50h	CBASS_ERR_INTR_RAW_STAT	Global Interrupt Raw Status Register	4710 8050h
54h	CBASS_ERR_INTR_ENABLED_STAT	Global Interrupt Enabled Status Register	4710 8054h
58h	CBASS_ERR_INTR_ENABLE_SET	Interrupt Enable Set Register	4710 8058h
5Ch	CBASS_ERR_INTR_ENABLE_CLR	Interrupt Enable Clear Register	4710 805Ch
60h	CBASS_EOI	End of Interrupt Register	4710 8060h

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1.4.1 CBASS_PID Register (Offset = 0h) [reset = X]

CBASS_PID is shown in Figure 1-23 and described in Table 1-194.

Return to Summary Table.

The Revision Register contains the major and minor revisions for the module.

Table 1-193. CBASS_PID Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0000h
CBASS_FW0_ERR	00B0 8000h
CBASS_HC2_0_ERR	02A8 3000h
CBASS_AC0_ERR	02A8 5000h
CBASS_DATADEBUG0_ERR	02A8 6000h
CBASS_HC0_ERR	02A8 7000h
CBASS_CSI0_ERR	02A8 8000h
CBASS_HC_CFG0_ERR	02A8 9000h
CBASS_MCASP_G0_0_ERR	02A8 A000h
CBASS_MCASP_G1_0_ERR	02A8 B000h
CBASS_RC0_ERR	02A8 C000h
CBASS_RC_CFG0_ERR	02A8 D000h
CBASS_AASRC0_ERR	02A8 E000h
CBASS_IPPHY0_ERR	02A8 F000h
WKUP_CBASS_FW0_ERR	4240 4000h
MCU_CBASS_FW0_ERR	4710 8000h

Figure 1-23. CBASS_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 1-194. CBASS_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	REV	R	X	TI internal data.

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1.4.2 CBASS_DESTINATION_ID Register (Offset = 4h) [reset = X]

CBASS_DESTINATION_ID is shown in Figure 1-24 and described in Table 1-196.

Return to Summary Table.

The Destination ID Register defines the destination ID value for error messages.

Table 1-195. CBASS_DESTINATION_ID Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0004h
CBASS_FW0_ERR	00B0 8004h
CBASS_HC2_0_ERR	02A8 3004h
CBASS_AC0_ERR	02A8 5004h
CBASS_DATADEBUG0_ERR	02A8 6004h
CBASS_HC0_ERR	02A8 7004h
CBASS_CSI0_ERR	02A8 8004h
CBASS_HC_CFG0_ERR	02A8 9004h
CBASS_MCASP_G0_0_ERR	02A8 A004h
CBASS_MCASP_G1_0_ERR	02A8 B004h
CBASS_RC0_ERR	02A8 C004h
CBASS_RC_CFG0_ERR	02A8 D004h
CBASS_AASRC0_ERR	02A8 E004h
CBASS_IPPHY0_ERR	02A8 F004h
WKUP_CBASS_FW0_ERR	4240 4004h
MCU_CBASS_FW0_ERR	4710 8004h

Figure 1-24. CBASS_DESTINATION_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								DEST_ID							
R/W-X																								R/W-0h							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-196. CBASS_DESTINATION_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	DEST_ID	R/W	0h	The destination ID.

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1.4.3 CBASS_EXCEPTION_LOGGING_HEADER0 Register (Offset = 24h) [reset = 0h]

CBASS_EXCEPTION_LOGGING_HEADER0 is shown in Figure 1-25 and described in Table 1-198.

Return to Summary Table.

The Exception Logging Header 0 Register contains the first word of the header.

Table 1-197. CBASS_EXCEPTION_LOGGING_HEADER0 Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0024h
CBASS_FW0_ERR	00B0 8024h
CBASS_HC2_0_ERR	02A8 3024h
CBASS_AC0_ERR	02A8 5024h
CBASS_DATADEBUG0_ERR	02A8 6024h
CBASS_HC0_ERR	02A8 7024h
CBASS_CSI0_ERR	02A8 8024h
CBASS_HC_CFG0_ERR	02A8 9024h
CBASS_MCASP_G0_0_ERR	02A8 A024h
CBASS_MCASP_G1_0_ERR	02A8 B024h
CBASS_RC0_ERR	02A8 C024h
CBASS_RC_CFG0_ERR	02A8 D024h
CBASS_AASRC0_ERR	02A8 E024h
CBASS_IPPHY0_ERR	02A8 F024h
WKUP_CBASS_FW0_ERR	4240 4024h
MCU_CBASS_FW0_ERR	4710 8024h

Figure 1-25. CBASS_EXCEPTION_LOGGING_HEADER0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE_F								SRC_ID																DEST_ID							
R-0h								R-0h																R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 1-198. CBASS_EXCEPTION_LOGGING_HEADER0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TYPE_F	R	0h	Type. 7 = CBASS.
23-8	SRC_ID	R	0h	Source ID. Always 0.
7-0	DEST_ID	R	0h	Destination ID.

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1.4.4 CBASS_EXCEPTION_LOGGING_HEADER1 Register (Offset = 28h) [reset = X]

CBASS_EXCEPTION_LOGGING_HEADER1 is shown in Figure 1-26 and described in Table 1-200.

Return to Summary Table.

The Exception Logging Header 1 Register contains the second word of the header.

Table 1-199. CBASS_EXCEPTION_LOGGING_HEADER1 Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0028h
CBASS_FW0_ERR	00B0 8028h
CBASS_HC2_0_ERR	02A8 3028h
CBASS_AC0_ERR	02A8 5028h
CBASS_DATADEBUG0_ERR	02A8 6028h
CBASS_HC0_ERR	02A8 7028h
CBASS_CSI0_ERR	02A8 8028h
CBASS_HC_CFG0_ERR	02A8 9028h
CBASS_MCASP_G0_0_ERR	02A8 A028h
CBASS_MCASP_G1_0_ERR	02A8 B028h
CBASS_RC0_ERR	02A8 C028h
CBASS_RC_CFG0_ERR	02A8 D028h
CBASS_AASRC0_ERR	02A8 E028h
CBASS_IPPHY0_ERR	02A8 F028h
WKUP_CBASS_FW0_ERR	4240 4028h
MCU_CBASS_FW0_ERR	4710 8028h

Figure 1-26. CBASS_EXCEPTION_LOGGING_HEADER1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GROUP								CODE								RESERVED															
R-0h								R-0h								R-X															

LEGEND: R = Read Only; *-n* = value after reset

Table 1-200. CBASS_EXCEPTION_LOGGING_HEADER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	GROUP	R	0h	Group. Always 0.
23-16	CODE	R	0h	Code. 0 = CBASS decode error.
15-0	RESERVED	R	X	

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1.4.5 CBASS_EXCEPTION_LOGGING_DATA0 Register (Offset = 2Ch) [reset = 0h]

CBASS_EXCEPTION_LOGGING_DATA0 is shown in Figure 1-27 and described in Table 1-202.

Return to Summary Table.

The Exception Logging Data 0 Register contains the first word of the data.

Table 1-201. CBASS_EXCEPTION_LOGGING_DATA0 Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 002Ch
CBASS_FW0_ERR	00B0 802Ch
CBASS_HC2_0_ERR	02A8 302Ch
CBASS_AC0_ERR	02A8 502Ch
CBASS_DATADEBUG0_ERR	02A8 602Ch
CBASS_HC0_ERR	02A8 702Ch
CBASS_CSI0_ERR	02A8 802Ch
CBASS_HC_CFG0_ERR	02A8 902Ch
CBASS_MCASP_G0_0_ERR	02A8 A02Ch
CBASS_MCASP_G1_0_ERR	02A8 B02Ch
CBASS_RC0_ERR	02A8 C02Ch
CBASS_RC_CFG0_ERR	02A8 D02Ch
CBASS_AASRC0_ERR	02A8 E02Ch
CBASS_IPPHY0_ERR	02A8 F02Ch
WKUP_CBASS_FW0_ERR	4240 402Ch
MCU_CBASS_FW0_ERR	4710 802Ch

Figure 1-27. CBASS_EXCEPTION_LOGGING_DATA0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_L																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 1-202. CBASS_EXCEPTION_LOGGING_DATA0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDR_L	R	0h	Address lower 32 bits.

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1.4.6 CBASS_EXCEPTION_LOGGING_DATA1 Register (Offset = 30h) [reset = X]

CBASS_EXCEPTION_LOGGING_DATA1 is shown in Figure 1-28 and described in Table 1-204.

Return to Summary Table.

The Exception Logging Data 1 Register contains the second word of the data.

Table 1-203. CBASS_EXCEPTION_LOGGING_DATA1 Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0030h
CBASS_FW0_ERR	00B0 8030h
CBASS_HC2_0_ERR	02A8 3030h
CBASS_AC0_ERR	02A8 5030h
CBASS_DATADEBUG0_ERR	02A8 6030h
CBASS_HC0_ERR	02A8 7030h
CBASS_CSI0_ERR	02A8 8030h
CBASS_HC_CFG0_ERR	02A8 9030h
CBASS_MCASP_G0_0_ERR	02A8 A030h
CBASS_MCASP_G1_0_ERR	02A8 B030h
CBASS_RC0_ERR	02A8 C030h
CBASS_RC_CFG0_ERR	02A8 D030h
CBASS_AASRC0_ERR	02A8 E030h
CBASS_IPPHY0_ERR	02A8 F030h
WKUP_CBASS_FW0_ERR	4240 4030h
MCU_CBASS_FW0_ERR	4710 8030h

Figure 1-28. CBASS_EXCEPTION_LOGGING_DATA1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																ADDR_H															
R-X																R-0h															

LEGEND: R = Read Only; *-n* = value after reset

Table 1-204. CBASS_EXCEPTION_LOGGING_DATA1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-0	ADDR_H	R	0h	Address upper 16 bits.

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1.4.7 CBASS_EXCEPTION_LOGGING_DATA2 Register (Offset = 34h) [reset = X]

CBASS_EXCEPTION_LOGGING_DATA2 is shown in Figure 1-29 and described in Table 1-206.

Return to Summary Table.

The Exception Logging Data 2 Register contains the third word of the data.

Table 1-205. CBASS_EXCEPTION_LOGGING_DATA2 Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0034h
CBASS_FW0_ERR	00B0 8034h
CBASS_HC2_0_ERR	02A8 3034h
CBASS_AC0_ERR	02A8 5034h
CBASS_DATADEBUG0_ERR	02A8 6034h
CBASS_HC0_ERR	02A8 7034h
CBASS_CSI0_ERR	02A8 8034h
CBASS_HC_CFG0_ERR	02A8 9034h
CBASS_MCASP_G0_0_ERR	02A8 A034h
CBASS_MCASP_G1_0_ERR	02A8 B034h
CBASS_RC0_ERR	02A8 C034h
CBASS_RC_CFG0_ERR	02A8 D034h
CBASS_AASRC0_ERR	02A8 E034h
CBASS_IPPHY0_ERR	02A8 F034h
WKUP_CBASS_FW0_ERR	4240 4034h
MCU_CBASS_FW0_ERR	4710 8034h

Figure 1-29. CBASS_EXCEPTION_LOGGING_DATA2 Register

31	30	29	28	27	26	25	24
RESERVED				ROUTEID			
R-X				R-0h			
23	22	21	20	19	18	17	16
ROUTEID							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		WRITE	READ	DEBUG	CACHEABLE	PRIV	SECURE
R-X		R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PRIV_ID							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 1-206. CBASS_EXCEPTION_LOGGING_DATA2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	ROUTEID	R	0h	Route ID.
15-14	RESERVED	R	X	
13	WRITE	R	0h	Write.
12	READ	R	0h	Read.

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Table 1-206. CBASS_EXCEPTION_LOGGING_DATA2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	DEBUG	R	0h	Debug.
10	CACHEABLE	R	0h	Cacheable.
9	PRIV	R	0h	Priv.
8	SECURE	R	0h	Secure.
7-0	PRIV_ID	R	0h	Priv ID.

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1.4.8 CBASS_EXCEPTION_LOGGING_DATA3 Register (Offset = 38h) [reset = X]

CBASS_EXCEPTION_LOGGING_DATA3 is shown in Figure 1-30 and described in Table 1-208.

Return to Summary Table.

The Exception Logging Data 3 Register contains the fourth word of the data.

Table 1-207. CBASS_EXCEPTION_LOGGING_DATA3 Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0038h
CBASS_FW0_ERR	00B0 8038h
CBASS_HC2_0_ERR	02A8 3038h
CBASS_AC0_ERR	02A8 5038h
CBASS_DATADEBUG0_ERR	02A8 6038h
CBASS_HC0_ERR	02A8 7038h
CBASS_CSI0_ERR	02A8 8038h
CBASS_HC_CFG0_ERR	02A8 9038h
CBASS_MCASP_G0_0_ERR	02A8 A038h
CBASS_MCASP_G1_0_ERR	02A8 B038h
CBASS_RC0_ERR	02A8 C038h
CBASS_RC_CFG0_ERR	02A8 D038h
CBASS_AASRC0_ERR	02A8 E038h
CBASS_IPPHY0_ERR	02A8 F038h
WKUP_CBASS_FW0_ERR	4240 4038h
MCU_CBASS_FW0_ERR	4710 8038h

Figure 1-30. CBASS_EXCEPTION_LOGGING_DATA3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						BYTECNT									
R-X																						R-0h									

LEGEND: R = Read Only; *-n* = value after reset

Table 1-208. CBASS_EXCEPTION_LOGGING_DATA3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	X	
9-0	BYTECNT	R	0h	Byte count.

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1.4.9 CBASS_ERR_INTR_RAW_STAT Register (Offset = 50h) [reset = X]

CBASS_ERR_INTR_RAW_STAT is shown in Figure 1-31 and described in Table 1-210.

Return to Summary Table.

Global Interrupt Raw Status Register

Table 1-209. CBASS_ERR_INTR_RAW_STAT Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0050h
CBASS_FW0_ERR	00B0 8050h
CBASS_HC2_0_ERR	02A8 3050h
CBASS_AC0_ERR	02A8 5050h
CBASS_DATADEBUG0_ERR	02A8 6050h
CBASS_HC0_ERR	02A8 7050h
CBASS_CSI0_ERR	02A8 8050h
CBASS_HC_CFG0_ERR	02A8 9050h
CBASS_MCASP_G0_0_ERR	02A8 A050h
CBASS_MCASP_G1_0_ERR	02A8 B050h
CBASS_RC0_ERR	02A8 C050h
CBASS_RC_CFG0_ERR	02A8 D050h
CBASS_AASRC0_ERR	02A8 E050h
CBASS_IPPHY0_ERR	02A8 F050h
WKUP_CBASS_FW0_ERR	4240 4050h
MCU_CBASS_FW0_ERR	4710 8050h

Figure 1-31. CBASS_ERR_INTR_RAW_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							INTR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 1-210. CBASS_ERR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	INTR	R/W1S	0h	Level Interrupt status

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1.4.10 CBASS_ERR_INTR_ENABLED_STAT Register (Offset = 54h) [reset = X]

CBASS_ERR_INTR_ENABLED_STAT is shown in Figure 1-32 and described in Table 1-212.

Return to Summary Table.

Global Interrupt Enabled Status Register

Table 1-211. CBASS_ERR_INTR_ENABLED_STAT Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0054h
CBASS_FW0_ERR	00B0 8054h
CBASS_HC2_0_ERR	02A8 3054h
CBASS_AC0_ERR	02A8 5054h
CBASS_DATADEBUG0_ERR	02A8 6054h
CBASS_HC0_ERR	02A8 7054h
CBASS_CSI0_ERR	02A8 8054h
CBASS_HC_CFG0_ERR	02A8 9054h
CBASS_MCASP_G0_0_ERR	02A8 A054h
CBASS_MCASP_G1_0_ERR	02A8 B054h
CBASS_RC0_ERR	02A8 C054h
CBASS_RC_CFG0_ERR	02A8 D054h
CBASS_AASRC0_ERR	02A8 E054h
CBASS_IPPHY0_ERR	02A8 F054h
WKUP_CBASS_FW0_ERR	4240 4054h
MCU_CBASS_FW0_ERR	4710 8054h

Figure 1-32. CBASS_ERR_INTR_ENABLED_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ENABLED_INTR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 1-212. CBASS_ERR_INTR_ENABLED_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ENABLED_INTR	R/W1C	0h	Level Enabled Interrupt status

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1.4.11 CBASS_ERR_INTR_ENABLE_SET Register (Offset = 58h) [reset = X]

CBASS_ERR_INTR_ENABLE_SET is shown in Figure 1-33 and described in Table 1-214.

Return to Summary Table.

Interrupt Enable Set Register

Table 1-213. CBASS_ERR_INTR_ENABLE_SET Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0058h
CBASS_FW0_ERR	00B0 8058h
CBASS_HC2_0_ERR	02A8 3058h
CBASS_AC0_ERR	02A8 5058h
CBASS_DATADEBUG0_ERR	02A8 6058h
CBASS_HC0_ERR	02A8 7058h
CBASS_CSI0_ERR	02A8 8058h
CBASS_HC_CFG0_ERR	02A8 9058h
CBASS_MCASP_G0_0_ERR	02A8 A058h
CBASS_MCASP_G1_0_ERR	02A8 B058h
CBASS_RC0_ERR	02A8 C058h
CBASS_RC_CFG0_ERR	02A8 D058h
CBASS_AASRC0_ERR	02A8 E058h
CBASS_IPPHY0_ERR	02A8 F058h
WKUP_CBASS_FW0_ERR	4240 4058h
MCU_CBASS_FW0_ERR	4710 8058h

Figure 1-33. CBASS_ERR_INTR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_SET
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 1-214. CBASS_ERR_INTR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	INTR_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register

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1.4.12 CBASS_ERR_INTR_ENABLE_CLR Register (Offset = 5Ch) [reset = X]

CBASS_ERR_INTR_ENABLE_CLR is shown in Figure 1-34 and described in Table 1-216.

Return to Summary Table.

Interrupt Enable Clear Register

Table 1-215. CBASS_ERR_INTR_ENABLE_CLR Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 005Ch
CBASS_FW0_ERR	00B0 805Ch
CBASS_HC2_0_ERR	02A8 305Ch
CBASS_AC0_ERR	02A8 505Ch
CBASS_DATADEBUG0_ERR	02A8 605Ch
CBASS_HC0_ERR	02A8 705Ch
CBASS_CSI0_ERR	02A8 805Ch
CBASS_HC_CFG0_ERR	02A8 905Ch
CBASS_MCASP_G0_0_ERR	02A8 A05Ch
CBASS_MCASP_G1_0_ERR	02A8 B05Ch
CBASS_RC0_ERR	02A8 C05Ch
CBASS_RC_CFG0_ERR	02A8 D05Ch
CBASS_AASRC0_ERR	02A8 E05Ch
CBASS_IPPHY0_ERR	02A8 F05Ch
WKUP_CBASS_FW0_ERR	4240 405Ch
MCU_CBASS_FW0_ERR	4710 805Ch

Figure 1-34. CBASS_ERR_INTR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							INTR_ENABLE_CLR
R/W-X							R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 1-216. CBASS_ERR_INTR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	INTR_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register

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1.4.13 CBASS_EOI Register (Offset = 60h) [reset = X]

CBASS_EOI is shown in Figure 1-35 and described in Table 1-218.

Return to Summary Table.

End of Interrupt Register

Table 1-217. CBASS_EOI Instances

Instance	Physical Address
CBASS_INFRA0_ERR	00B0 0060h
CBASS_FW0_ERR	00B0 8060h
CBASS_HC2_0_ERR	02A8 3060h
CBASS_AC0_ERR	02A8 5060h
CBASS_DATADEBUG0_ERR	02A8 6060h
CBASS_HC0_ERR	02A8 7060h
CBASS_CSI0_ERR	02A8 8060h
CBASS_HC_CFG0_ERR	02A8 9060h
CBASS_MCASP_G0_0_ERR	02A8 A060h
CBASS_MCASP_G1_0_ERR	02A8 B060h
CBASS_RC0_ERR	02A8 C060h
CBASS_RC_CFG0_ERR	02A8 D060h
CBASS_AASRC0_ERR	02A8 E060h
CBASS_IPPHY0_ERR	02A8 F060h
WKUP_CBASS_FW0_ERR	4240 4060h
MCU_CBASS_FW0_ERR	4710 8060h

Figure 1-35. CBASS_EOI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																WR															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 1-218. CBASS_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	WR	R/W	0h	End of Interrupt Register

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2 WKUP_CTRL_MMR0 Registers

Table 2-2 lists the memory-mapped registers for the WKUP_CTRL_MMR0. All register offset addresses not listed in Table 2-2 should be considered as reserved locations and the register contents should not be modified.

Table 2-1. WKUP_CTRL_MMR0 Instances

Instance	Base Address
WKUP_CTRL_MMR0	4300 0000h

Table 2-2. WKUP_CTRL_MMR0 Registers

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	WKUP_CTRL_MMR0 Proxy0 Physical Address	WKUP_CTRL_MMR0 Proxy1 Physical Address
0h	2000h	CTRLMMR_WKUP_PID	Peripheral Identification Register	4300 0000h	4300 2000h
8h	2008h	CTRLMMR_WKUP_MMR_CFG1	Configuration register 1	4300 0008h	4300 2008h
14h	2014h	CTRLMMR_WKUP_JTAGID	JTAG / DEVICE ID Register	4300 0014h	4300 2014h
18h	2018h	Section 2.3	JTAG User Code ID Register	4300 0018h	4300 2018h
20h	2020h	CTRLMMR_WKUP_DIE_ID0	Die ID Register 0	4300 0020h	4300 2020h
24h	2024h	CTRLMMR_WKUP_DIE_ID1	Die ID Register 1	4300 0024h	4300 2024h
28h	2028h	CTRLMMR_WKUP_DIE_ID2	Die ID Register 2	4300 0028h	4300 2028h
2Ch	202Ch	CTRLMMR_WKUP_DIE_ID3	Die ID Register 3	4300 002Ch	4300 202Ch
30h	2030h	CTRLMMR_WKUP_DEVSTAT	WKUP Domain Device Status Register	4300 0030h	4300 2030h
34h	2034h	CTRLMMR_WKUP_BOOTCFG	WKUP Domain Boot Configuration Register	4300 0034h	4300 2034h
38h	2038h	CTRLMMR_WKUP_POST_SEL_STAT	Power-on Self Test Selection Status Register	4300 0038h	4300 2038h
3Ch	203Ch	CTRLMMR_WKUP_POST_OPT	Power-on Self Test Options Register	4300 003Ch	4300 203Ch
50h	2050h	CTRLMMR_WKUP_RESET_SRC_STAT	Reset Status Register	4300 0050h	4300 2050h
60h	2060h	CTRLMMR_WKUP_DEVICE_FEATURE0	Device Feature Register 0	4300 0060h	4300 2060h
64h	2064h	CTRLMMR_WKUP_DEVICE_FEATURE1	Device Feature Register 1	4300 0064h	4300 2064h
68h	2068h	CTRLMMR_WKUP_DEVICE_FEATURE2	Device Feature Register 2	4300 0068h	4300 2068h
6Ch	206Ch	CTRLMMR_WKUP_DEVICE_FEATURE3	Device Feature Register 3	4300 006Ch	4300 206Ch
70h	2070h	CTRLMMR_WKUP_DEVICE_FEATURE4	Device Feature Register 4	4300 0070h	4300 2070h
74h	2074h	CTRLMMR_WKUP_DEVICE_FEATURE5	Device Feature Register 5	4300 0074h	4300 2074h
78h	2078h	CTRLMMR_WKUP_DEVICE_FEATURE6	Device Feature Register 6	4300 0078h	4300 2078h
1008h	3008h	CTRLMMR_WKUP_LOCK0_KICK0	Partition 0 Lock Key 0 Register	4300 1008h	4300 3008h

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Table 2-2. WKUP_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	WKUP_CTRL_MMR0 Proxy0 Physical Address	WKUP_CTRL_MMR0 Proxy1 Physical Address
100Ch	300Ch	CTRLMMR_WKUP_LOCK0_KICK1	Partition 0 Lock Key 1 Register	4300 100Ch	4300 300Ch
1010h	3010h	CTRLMMR_WKUP_INTR_RAW_STAT	Interrupt Raw Status Register	4300 1010h	4300 3010h
1014h	3014h	CTRLMMR_WKUP_INTR_STAT_CLR	Interrupt Status and Clear Register	4300 1014h	4300 3014h
1018h	3018h	CTRLMMR_WKUP_INTR_EN_SET	Interrupt Enable Set Register	4300 1018h	4300 3018h
101Ch	301Ch	CTRLMMR_WKUP_INTR_EN_CLR	Interrupt Enable Clear Register	4300 101Ch	4300 301Ch
1020h	3020h	CTRLMMR_WKUP_EOI	End of Interrupt Register	4300 1020h	4300 3020h
1024h	3024h	CTRLMMR_WKUP_FAULT_ADDR	Fault Address Register	4300 1024h	4300 3024h
1028h	3028h	CTRLMMR_WKUP_FAULT_TYPE	Fault Type Register	4300 1028h	4300 3028h
102Ch	302Ch	CTRLMMR_WKUP_FAULT_ATTR	Fault Attribute Register	4300 102Ch	4300 302Ch
1030h	3030h	CTRLMMR_WKUP_FAULT_CLR	Fault Clear Register	4300 1030h	4300 3030h
1100h	3100h	CTRLMMR_WKUP_P0_CLAIM0	Partition 0 Claim Register 0	4300 1100h	4300 3100h
1104h	3104h	CTRLMMR_WKUP_P0_CLAIM1	Partition 0 Claim Register 1	4300 1104h	4300 3104h
1108h	3108h	CTRLMMR_WKUP_P0_CLAIM2	Partition 0 Claim Register 2	4300 1108h	4300 3108h
110Ch	310Ch	CTRLMMR_WKUP_P0_CLAIM3	Partition 0 Claim Register 3	4300 110Ch	4300 310Ch
1110h	3110h	CTRLMMR_WKUP_P0_CLAIM4	Partition 0 Claim Register 4	4300 1110h	4300 3110h
1114h	3114h	CTRLMMR_WKUP_P0_CLAIM5	Partition 0 Claim Register 5	4300 1114h	4300 3114h
1118h	3118h	CTRLMMR_WKUP_P0_CLAIM6	Partition 0 Claim Register 6	4300 1118h	4300 3118h
4004h	6004h	CTRLMMR_WKUP_MAIN_PWR_CTRL	MAIN Voltage Domain Power Control Register	4300 4004h	4300 6004h
4020h	6020h	CTRLMMR_WKUP_GPIO_CTRL	WKUP GPIO Control Register	4300 4020h	4300 6020h
4030h	6030h	CTRLMMR_WKUP_I2C0_CTRL	WKUP I2C0 Control Register	4300 4030h	4300 6030h
4084h	6084h	CTRLMMR_WKUP_DBOUNCE_CFG1	Debounce Config Register	4300 4084h	4300 6084h
4088h	6088h	CTRLMMR_WKUP_DBOUNCE_CFG2	Debounce Config Register	4300 4088h	4300 6088h
408Ch	608Ch	CTRLMMR_WKUP_DBOUNCE_CFG3	Debounce Config Register	4300 408Ch	4300 608Ch
4090h	6090h	CTRLMMR_WKUP_DBOUNCE_CFG4	Debounce Config Register	4300 4090h	4300 6090h
4094h	6094h	CTRLMMR_WKUP_DBOUNCE_CFG5	Debounce Config Register	4300 4094h	4300 6094h
4098h	6098h	CTRLMMR_WKUP_DBOUNCE_CFG6	Debounce Config Register	4300 4098h	4300 6098h

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Table 2-2. WKUP_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	WKUP_CTRL_MMR0 Proxy0 Physical Address	WKUP_CTRL_MMR0 Proxy1 Physical Address
5008h	7008h	CTRLMMR_WKUP_LOCK1_KICK0	Partition 1 Lock Key 0 Register	4300 5008h	4300 7008h
500Ch	700Ch	CTRLMMR_WKUP_LOCK1_KICK1	Partition 1 Lock Key 1 Register	4300 500Ch	4300 700Ch
5100h	7100h	CTRLMMR_WKUP_P1_CLAIM0	Partition 1 Claim Register 0	4300 5100h	4300 7100h
5104h	7104h	CTRLMMR_WKUP_P1_CLAIM1	Partition 1 Claim Register 1	4300 5104h	4300 7104h
5108h	7108h	CTRLMMR_WKUP_P1_CLAIM2	Partition 1 Claim Register 2	4300 5108h	4300 7108h
8000h	A000h	CTRLMMR_WKUP_MCU_OBSCLK_CTRL	Observe Clock Output Control Register	4300 8000h	4300 A000h
8014h	A014	Section 2.54	Oscillator1 Control Register	4300 8014h	4300 A014h
8030h	A030h	CTRLMMR_WKUP_LFXOSC_CTRL	Low Frequency Oscillator Control Register	4300 8030h	4300 A030h
8034h	A034h	CTRLMMR_WKUP_LFXOSC_TRIM	Low Frequency Oscillator Trim Register	4300 8034h	4300 A034h
8050h	A050h	CTRLMMR_WKUP_MCU_PLL_CLKSEL	MCU PLL Source Clock Select Register	4300 8050h	4300 A050h
8060h	A060h	CTRLMMR_WKUP_PER_CLKSEL	WKUP Peripheral Clock Select Register	4300 8060h	4300 A060h
8064h	A064h	CTRLMMR_WKUP_USART_CLKSEL	CTRLMMR_WKUP_POK_VDDR_MCU_OV_CTRL	4300 8064h	4300 A064h
8070h	A070h	CTRLMMR_WKUP_GPIO_CLKSEL	WKUP GPIO Clock Select Register	4300 8070h	4300 A070h
8080h	A080h	CTRLMMR_WKUP_MAIN_PLL0_CLKSEL	MAIN PLL0 Source Clock Select Register	4300 8080h	4300 A080h
8084h	A084h	CTRLMMR_WKUP_MAIN_PLL1_CLKSEL	MAIN PLL1 Source Clock Select Register	4300 8084h	4300 A084h
8088h	A088h	CTRLMMR_WKUP_MAIN_PLL2_CLKSEL	MAIN PLL2 Source Clock Select Register	4300 8088h	4300 A088h
808Ch	A08Ch	CTRLMMR_WKUP_MAIN_PLL3_CLKSEL	MAIN PLL3 Source Clock Select Register	4300 808Ch	4300 A08Ch
8090h	A090h	CTRLMMR_WKUP_MAIN_PLL4_CLKSEL	MAIN PLL4 Source Clock Select Register	4300 8090h	4300 A090h
8094h	A094h	CTRLMMR_WKUP_MAIN_PLL5_CLKSEL	MAIN PLL5 Source Clock Select Register	4300 8094h	4300 A094h
8098h	A098h	CTRLMMR_WKUP_MAIN_PLL6_CLKSEL	MAIN PLL6 Source Clock Select Register	4300 8098h	4300 A098h
809Ch	A09Ch	CTRLMMR_WKUP_MAIN_PLL7_CLKSEL	MAIN PLL7 Source Clock Select Register	4300 809Ch	4300 A09Ch
80A0h	A0A0h	CTRLMMR_WKUP_MAIN_PLL8_CLKSEL	MAIN PLL8 Source Clock Select Register	4300 80A0h	4300 A0A0h
80B0h	A0B0h	CTRLMMR_WKUP_MAIN_PLL12_CLKSEL	MAIN PLL12 Source Clock Select Register	4300 80B0h	4300 A0B0h
80B4h	A0B4h	CTRLMMR_WKUP_MAIN_PLL13_CLKSEL	MAIN PLL13 Source Clock Select Register	4300 80B4h	4300 A0B4h
80B8h	A0B8h	CTRLMMR_WKUP_MAIN_PLL14_CLKSEL	MAIN PLL14 Source Clock Select Register	4300 80B8h	4300 A0B8h
80BCh	A0BCh	CTRLMMR_WKUP_MAIN_PLL15_CLKSEL	MAIN PLL15 Source Clock Select Register	4300 80BCh	4300 A0BCh

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Table 2-2. WKUP_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	WKUP_CTRL_MMR0 Proxy0 Physical Address	WKUP_CTRL_MMR0 Proxy1 Physical Address
80C0h	A0C0h	CTRLMMR_WKUP_MAIN_PLL16_CLKSEL	MAIN PLL16 Source Clock Select Register	4300 80C0h	4300 A0C0h
80C4h	A0C4h	CTRLMMR_WKUP_MAIN_PLL17_CLKSEL	MAIN PLL17 Source Clock Select Register	4300 80C4h	4300 A0C4h
80C8h	A0C8h	CTRLMMR_WKUP_MAIN_PLL18_CLKSEL	MAIN PLL18 Source Clock Select Register	4300 80C8h	4300 A0C8h
80CCh	A0CCh	CTRLMMR_WKUP_MAIN_PLL19_CLKSEL	MAIN PLL19 Source Clock Select Register	4300 80CCh	4300 A0CCh
80DCh	A0DCh	CTRLMMR_WKUP_MAIN_PLL23_CLKSEL	MAIN PLL23 Source Clock Select Register	4300 80DCh	4300 A0DCh
80E0h	A0E0h	CTRLMMR_WKUP_MAIN_PLL24_CLKSEL	MAIN PLL24 Source Clock Select Register	4300 80E0h	4300 A0E0h
80E4h	A0E4h	CTRLMMR_WKUP_MAIN_PLL25_CLKSEL	MAIN PLL25 Source Clock Select Register	4300 80E4h	4300 A0E4h
8100h	A100h	CTRLMMR_WKUP_MAIN_SYSCLK_CTRL	MAIN System Clock Control Register	4300 8100h	4300 A100h
8110h	A110h	CTRLMMR_WKUP_MCU_SPI0_CLKSEL	MCU_SPI Clock Select Register	4300 8110h	4300 A110h
8114h	A114h	CTRLMMR_WKUP_MCU_SPI1_CLKSEL	MCU_SPI Clock Select Register	4300 8114h	4300 A114h
9008h	B008h	CTRLMMR_WKUP_LOCK2_KICK0	Partition 2 Lock Key 0 Register	4300 9008h	4300 B008h
900Ch	B00Ch	CTRLMMR_WKUP_LOCK2_KICK1	Partition 2 Lock Key 1 Register	4300 900Ch	4300 B00Ch
9100h	B100h	CTRLMMR_WKUP_P2_CLAIM0	Partition 2 Claim Register 0	4300 9100h	4300 B100h
9104h	B104h	CTRLMMR_WKUP_P2_CLAIM1	Partition 2 Claim Register 1	4300 9104h	4300 B104h
9108h	B108h	CTRLMMR_WKUP_P2_CLAIM2	Partition 2 Claim Register 2	4300 9108h	4300 B108h
C280h	E280h	CTRLMMR_WKUP_DMSC_LBIST_SIG	DMSC Logic BIST MISR Signature Register	4300 C280h	4300 E280h
C2C0h	E2C0h	CTRLMMR_WKUP_POST_STAT	WKUP Power-On Self Test Status Register	4300 C2C0h	4300 E2C0h
C320h	E320h	CTRLMMR_WKUP_FUSE_CRC_STAT	WKUP eFuse CRC Status Register	4300 C320h	4300 E320h
D008h	F008h	CTRLMMR_WKUP_LOCK3_KICK0	Partition 3 Lock Key 0 Register	4300 D008h	4300 F008h
D00Ch	F00Ch	CTRLMMR_WKUP_LOCK3_KICK1	Partition 3 Lock Key 1 Register	4300 D00Ch	4300 F00Ch
D100h	F100h	CTRLMMR_WKUP_P3_CLAIM0	Partition 3 Claim Register 0	4300 D100h	4300 F100h
D104h	F104h	CTRLMMR_WKUP_P3_CLAIM1	Partition 3 Claim Register 1	4300 D104h	4300 F104h
D108h	F108h	CTRLMMR_WKUP_P3_CLAIM2	Partition 3 Claim Register 2	4300 D108h	4300 F108h
D10Ch	F10Ch	CTRLMMR_WKUP_P3_CLAIM3	Partition 3 Claim Register 3	4300 D10Ch	4300 F10Ch
D110h	F110h	CTRLMMR_WKUP_P3_CLAIM4	Partition 3 Claim Register 4	4300 D110h	4300 F110h
D114h	F114h	CTRLMMR_WKUP_P3_CLAIM5	Partition 3 Claim Register 5	4300 D114h	4300 F114h

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Table 2-2. WKUP_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	WKUP_CTRL_MMR0 Proxy0 Physical Address	WKUP_CTRL_MMR0 Proxy1 Physical Address
D118h	F118h	CTRLMMR_WKUP_P3_CLAIM6	Partition 3 Claim Register 6	4300 D118h	4300 F118h
18000h	1A000h	CTRLMMR_WKUP_POR_CTRL	Power-On Reset Module Control Register	4301 8000h	4301 A000h
18004h	1A004h	CTRLMMR_WKUP_POR_STAT	Power-On Reset Module Status Register	4301 8004h	4301 A004h
18008h	1A008h	CTRLMMR_WKUP_PRG0_CTRL	WKUP PRG0 Control Register	4301 8008h	4301 A008h
1800Ch	1A00Ch	CTRLMMR_WKUP_PRG0_STAT	WKUP PRG0 Status and Clear Register	4301 800Ch	4301 A00Ch
18010h	1A010h	CTRLMMR_WKUP_POK_VDDA_PMIC_IN_CTRL	VDDA_PMIC_IN Power-OK Control Register	4301 8010h	4301 A010h
18014h	1A014h	CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_UV_CTRL	3P3_VDDA_MCU Undervoltage Power-OK Control Register	4301 8014h	4301 A014h
18018h	1A018h	CTRLMMR_WKUP_POK_VDDR_MCU_UV_CTRL	VDDR_MCU Undervoltage Power-OK Control Register	4301 8018h	4301 A018h
18020h	1A020h	CTRLMMR_WKUP_POK_VDD_MCU_OV_CTRL	VDD_MCU Overvoltage Power-OK Control Register	4301 8020h	4301 A020h
18024h	1A024h	CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_OV_CTRL	3P3_VDDA_MCU Overvoltage Power-OK Control Register	4301 8024h	4301 A024h
18028h	1A028h	CTRLMMR_WKUP_POK_VDDR_MCU_OV_CTRL	VDDR_MCU Overvoltage Power-OK Control Register	4301 8028h	4301 A028h
18058h	1A058h	CTRLMMR_WKUP_PRG1_CTRL	WKUP PRG1 Control Register	4301 8058h	4301 A058h
1805Ch	1A05Ch	CTRLMMR_WKUP_PRG1_STAT	WKUP PRG1 Status and Clear Register	4301 805Ch	4301 A05Ch
18070h	1A070h	CTRLMMR_WKUP_MAIN_VDOM_CTRL	MAIN Voltage Domain Control Register	4301 8070h	4301 A070h
18080h	1A080h	CTRLMMR_WKUP_POR_POKHV_UV_CTRL	1.8V VDDA_MCU undervoltage POK Control Register	4301 8080h	4301 A080h
18084h	1A084h	CTRLMMR_WKUP_POR_POKLV_UV_CTRL	VDD_MCU undervoltage POK Control Register	4301 8084h	4301 A084h
18088h	1A088h	CTRLMMR_WKUP_POR_POKHV_OV_CTRL	1.8V VDDA_MCU overvoltage POK Control Register	4301 8088h	4301 A088h
1808Ch	1A08Ch	CTRLMMR_WKUP_POR_BANDGAP_CTRL	Bandgap Control Register	4301 808Ch	4301 A08Ch
180A0h	1A0A0h	CTRLMMR_WKUP_TEMP_DIODE_TRIM	Temperature Diode Trim Register	4301 80A0h	4301 A0A0h
180B0h	1A0B0h	CTRLMMR_WKUP_IO_VOLTAGE_STAT	I/O Voltage Status Register	4301 80B0h	4301 A0B0h
18104h	1A104h	CTRLMMR_WKUP_MAIN_POR_TO_CTRL	MAIN PORz Reset Timeout Register	4301 8104h	4301 A104h
18108h	1A108h	CTRLMMR_WKUP_MAIN_PRG_CTRL	MAIN PRG Control Register	4301 8108h	4301 A108h
1810Ch	1A10Ch	CTRLMMR_WKUP_MAIN_PRG_STAT	MAIN PRG Status Register	4301 810Ch	4301 A10Ch
18110h	1A110h	CTRLMMR_WKUP_POK_VDD_CORE_UV_CTRL	VDD_CORE Undervoltage Power-OK Control Register	4301 8110h	4301 A110h
18114h	1A114h	CTRLMMR_WKUP_POK_VDD_CPU_UV_CTRL	VDD_CPU Undervoltage Power-OK Control Register	4301 8114h	4301 A114h
18118h	1A118h	CTRLMMR_WKUP_POK_VMON_EXT_UV_CTRL	1P8_VDDA_SOC Undervoltage Power-OK Control Register	4301 8118h	4301 A118h

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Table 2-2. WKUP_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	WKUP_CTRL_MMR0 Proxy0 Physical Address	WKUP_CTRL_MMR0 Proxy1 Physical Address
1811Ch	1A11Ch	CTRLMMR_WKUP_POK_VDDR_CORE_UV_CTRL	VDDR_CORE Undervoltage Power-OK Control Register	4301 811Ch	4301 A11Ch
18120h	1A120h	CTRLMMR_WKUP_POK_VDD_CORE_OV_CTRL	VDD_CORE Overvoltage Power-OK Control Register	4301 8120h	4301 A120h
18124h	1A124h	CTRLMMR_WKUP_POK_VDD_CPU_OV_CTRL	VDD_CPU Overvoltage Power-OK Control Register	4301 8124h	4301 A124h
18128h	1A128h	CTRLMMR_WKUP_POK_VMON_EXT_OV_CTRL	1P8_VDDA_SOC Overvoltage Power-OK Control Register	4301 8128h	4301 A128h
1812Ch	1A12Ch	CTRLMMR_WKUP_POK_VDDR_CORE_OV_CTRL	VDDR_CORE Overvoltage Power-OK Control Register	4301 812Ch	4301 A12Ch
18160h	1A160h	CTRLMMR_WKUP_DEEPSLEEP_CTRL	Deep Sleep Control Register	4301 8160h	4301 A160h
18170h	1A170h	CTRLMMR_WKUP_POR_RST_CTRL	PowerOn Reset Control Register	4301 8170h	4301 A170h
18174h	1A174h	CTRLMMR_WKUP_MAIN_WARM_RST_CTRL	MAIN Domain Warm Reset Control Register	4301 8174h	4301 A174h
18178h	1A178h	CTRLMMR_WKUP_RST_STAT	Reset Status Register	4301 8178h	4301 A178h
1817Ch	1A17Ch	CTRLMMR_WKUP_MCU_WARM_RST_CTRL	MCU Domain Warm Reset Control Register	4301 817Ch	4301 A17Ch
18180h	1A180h	CTRLMMR_WKUP_VDD_CPU_GLDTC_CTRL	CPU Voltage Glitch Detect Control Register	4301 8180h	4301 A180h
18190h	1A190h	CTRLMMR_WKUP_VDD_CORE_GLDTC_CTRL	Core Voltage Glitch Detect Control Register	4301 8190h	4301 A190h
18194h	1A194h	CTRLMMR_WKUP_VDDR_CPU_GLDTC_CTRL	CPU SRAM Voltage Glitch Detect Control Register	4301 8194h	4301 A194h
18198h	1A198h	CTRLMMR_WKUP_VDDR_CORE_GLDTC_CTRL	Core SRAM Voltage Glitch Detect Control Register	4301 8198h	4301 A198h
181A0h	1A1A0h	CTRLMMR_WKUP_VDD_CPU_GLDTC_STAT	CPU Voltage Glitch Detect Status Register	4301 81A0h	4301 A1A0h
181B0h	1A1B0h	CTRLMMR_WKUP_VDD_CORE_GLDTC_STAT	Core Voltage Core Glitch Detect Status Register	4301 81B0h	4301 A1B0h
181B4h	1A1B4h	CTRLMMR_WKUP_VDDR_CPU_GLDTC_STAT	CPU SRAM Voltage Glitch Detect Status Register	4301 81B4h	4301 A1B4h
181B8h	1A1B8h	CTRLMMR_WKUP_VDDR_CORE_GLDTC_STAT	Core SRAM Voltage Glitch Detect Status Register	4301 81B8h	4301 A1B8h
181C0h	1A1C0h	CTRLMMR_WKUP_VDD_MCU_GLDTC_CTRL	MCU Voltage Glitch Detect Control Register	4301 81C0h	4301 A1C0h
181C4h	1A1C4h	CTRLMMR_WKUP_VDDR_MCU_GLDTC_CTRL	MCU SRAM Glitch Detect Control Register	4301 81C4h	4301 A1C4h
181D0h	1A1D0h	CTRLMMR_WKUP_VDD_MCU_GLDTC_STAT	MCU Voltage Glitch Detect Status Register	4301 81D0h	4301 A1D0h
181D4h	1A1D4h	CTRLMMR_WKUP_VDDR_MCU_GLDTC_STAT	MCU SRAM Glitch Detect Status Register	4301 81D4h	4301 A1D4h
19008h	1B008h	CTRLMMR_WKUP_LOCK6_KICK0	Partition 6 Lock Key 0 Register	4301 9008h	4301 B008h
1900Ch	1B00Ch	CTRLMMR_WKUP_LOCK6_KICK1	Partition 6 Lock Key 1 Register	4301 900Ch	4301 B00Ch
19100h	1B100h	CTRLMMR_WKUP_P6_CLAIM0	Partition 6 Claim Register 0	4301 9100h	4301 B100h
19104h	1B104h	CTRLMMR_WKUP_P6_CLAIM1	Partition 6 Claim Register 1	4301 9104h	4301 B104h

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Table 2-2. WKUP_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	WKUP_CTRL_MMR0 Proxy0 Physical Address	WKUP_CTRL_MMR0 Proxy1 Physical Address
19108h	1B108h	CTRLMMR_WKUP_P6_CLAIM2	Partition 6 Claim Register 2	4301 9108h	4301 B108h
1910Ch	1B10Ch	CTRLMMR_WKUP_P6_CLAIM3	Partition 6 Claim Register 3	4301 910Ch	4301 B10Ch
1C000h	1E000h	CTRLMMR_WKUP_PADCONFIG0	PAD Configuration Register 0	4301 C000h	4301 E000h
1C004h	1E004h	CTRLMMR_WKUP_PADCONFIG1	PAD Configuration Register 1	4301 C004h	4301 E004h
1C008h	1E008h	CTRLMMR_WKUP_PADCONFIG2	PAD Configuration Register 2	4301 C008h	4301 E008h
1C00Ch	1E00Ch	CTRLMMR_WKUP_PADCONFIG3	PAD Configuration Register 3	4301 C00Ch	4301 E00Ch
1C010h	1E010h	CTRLMMR_WKUP_PADCONFIG4	PAD Configuration Register 4	4301 C010h	4301 E010h
1C014h	1E014h	CTRLMMR_WKUP_PADCONFIG5	PAD Configuration Register 5	4301 C014h	4301 E014h
1C018h	1E018h	CTRLMMR_WKUP_PADCONFIG6	PAD Configuration Register 6	4301 C018h	4301 E018h
1C01Ch	1E01Ch	CTRLMMR_WKUP_PADCONFIG7	PAD Configuration Register 7	4301 C01Ch	4301 E01Ch
1C020h	1E020h	CTRLMMR_WKUP_PADCONFIG8	PAD Configuration Register 8	4301 C020h	4301 E020h
1C024h	1E024h	CTRLMMR_WKUP_PADCONFIG9	PAD Configuration Register 9	4301 C024h	4301 E024h
1C028h	1E028h	CTRLMMR_WKUP_PADCONFIG10	PAD Configuration Register 10	4301 C028h	4301 E028h
1C02Ch	1E02Ch	CTRLMMR_WKUP_PADCONFIG11	PAD Configuration Register 11	4301 C02Ch	4301 E02Ch
1C030h	1E030h	CTRLMMR_WKUP_PADCONFIG12	PAD Configuration Register 12	4301 C030h	4301 E030h
1C034h	1E034h	CTRLMMR_WKUP_PADCONFIG13	PAD Configuration Register 13	4301 C034h	4301 E034h
1C038h	1E038h	CTRLMMR_WKUP_PADCONFIG14	PAD Configuration Register 14	4301 C038h	4301 E038h
1C03Ch	1E03Ch	CTRLMMR_WKUP_PADCONFIG15	PAD Configuration Register 15	4301 C03Ch	4301 E03Ch
1C040h	1E040h	CTRLMMR_WKUP_PADCONFIG16	PAD Configuration Register 16	4301 C040h	4301 E040h
1C044h	1E044h	CTRLMMR_WKUP_PADCONFIG17	PAD Configuration Register 17	4301 C044h	4301 E044h
1C048h	1E048h	CTRLMMR_WKUP_PADCONFIG18	PAD Configuration Register 18	4301 C048h	4301 E048h
1C04Ch	1E04Ch	CTRLMMR_WKUP_PADCONFIG19	PAD Configuration Register 19	4301 C04Ch	4301 E04Ch
1C050h	1E050h	CTRLMMR_WKUP_PADCONFIG20	PAD Configuration Register 20	4301 C050h	4301 E050h
1C054h	1E054h	CTRLMMR_WKUP_PADCONFIG21	PAD Configuration Register 21	4301 C054h	4301 E054h
1C058h	1E058h	CTRLMMR_WKUP_PADCONFIG22	PAD Configuration Register 22	4301 C058h	4301 E058h
1C05Ch	1E05Ch	CTRLMMR_WKUP_PADCONFIG23	PAD Configuration Register 23	4301 C05Ch	4301 E05Ch

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Table 2-2. WKUP_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	WKUP_CTRL_MMR0 Proxy0 Physical Address	WKUP_CTRL_MMR0 Proxy1 Physical Address
1C060h	1E060h	CTRLMMR_WKUP_PADCONFIG24	PAD Configuration Register 24	4301 C060h	4301 E060h
1C064h	1E064h	CTRLMMR_WKUP_PADCONFIG25	PAD Configuration Register 25	4301 C064h	4301 E064h
1C068h	1E068h	CTRLMMR_WKUP_PADCONFIG26	PAD Configuration Register 26	4301 C068h	4301 E068h
1C06Ch	1E06Ch	CTRLMMR_WKUP_PADCONFIG27	PAD Configuration Register 27	4301 C06Ch	4301 E06Ch
1C070h	1E070h	CTRLMMR_WKUP_PADCONFIG28	PAD Configuration Register 28	4301 C070h	4301 E070h
1C074h	1E074h	CTRLMMR_WKUP_PADCONFIG29	PAD Configuration Register 29	4301 C074h	4301 E074h
1C078h	1E078h	CTRLMMR_WKUP_PADCONFIG30	PAD Configuration Register 30	4301 C078h	4301 E078h
1C07Ch	1E07Ch	CTRLMMR_WKUP_PADCONFIG31	PAD Configuration Register 31	4301 C07Ch	4301 E07Ch
1C080h	1E080h	CTRLMMR_WKUP_PADCONFIG32	PAD Configuration Register 32	4301 C080h	4301 E080h
1C084h	1E084h	CTRLMMR_WKUP_PADCONFIG33	PAD Configuration Register 33	4301 C084h	4301 E084h
1C088h	1E088h	CTRLMMR_WKUP_PADCONFIG34	PAD Configuration Register 34	4301 C088h	4301 E088h
1C08Ch	1E08Ch	CTRLMMR_WKUP_PADCONFIG35	PAD Configuration Register 35	4301 C08Ch	4301 E08Ch
1C090h	1E090h	CTRLMMR_WKUP_PADCONFIG36	PAD Configuration Register 36	4301 C090h	4301 E090h
1C094h	1E094h	CTRLMMR_WKUP_PADCONFIG37	PAD Configuration Register 37	4301 C094h	4301 E094h
1C098h	1E098h	CTRLMMR_WKUP_PADCONFIG38	PAD Configuration Register 38	4301 C098h	4301 E098h
1C09Ch	1E09Ch	CTRLMMR_WKUP_PADCONFIG39	PAD Configuration Register 39	4301 C09Ch	4301 E09Ch
1C0A0h	1E0A0h	CTRLMMR_WKUP_PADCONFIG40	PAD Configuration Register 40	4301 C0A0h	4301 E0A0h
1C0A4h	1E0A4h	CTRLMMR_WKUP_PADCONFIG41	PAD Configuration Register 41	4301 C0A4h	4301 E0A4h
1C0A8h	1E0A8h	CTRLMMR_WKUP_PADCONFIG42	PAD Configuration Register 42	4301 C0A8h	4301 E0A8h
1C0ACh	1E0ACh	CTRLMMR_WKUP_PADCONFIG43	PAD Configuration Register 43	4301 C0ACh	4301 E0ACh
1C0B0h	1E0B0h	CTRLMMR_WKUP_PADCONFIG44	PAD Configuration Register 44	4301 C0B0h	4301 E0B0h
1C0B4h	1E0B4h	CTRLMMR_WKUP_PADCONFIG45	PAD Configuration Register 45	4301 C0B4h	4301 E0B4h
1C0B8h	1E0B8h	CTRLMMR_WKUP_PADCONFIG46	PAD Configuration Register 46	4301 C0B8h	4301 E0B8h
1C0BCh	1E0BCh	CTRLMMR_WKUP_PADCONFIG47	PAD Configuration Register 47	4301 C0BCh	4301 E0BCh
1C0C0h	1E0C0h	CTRLMMR_WKUP_PADCONFIG48	PAD Configuration Register 48	4301 C0C0h	4301 E0C0h
1C0C4h	1E0C4h	CTRLMMR_WKUP_PADCONFIG49	PAD Configuration Register 49	4301 C0C4h	4301 E0C4h

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Table 2-2. WKUP_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	WKUP_CTRL_MMR0 Proxy0 Physical Address	WKUP_CTRL_MMR0 Proxy1 Physical Address
1C0C8h	1E0C8h	CTRLMMR_WKUP_PADCONFIG50	PAD Configuration Register 50	4301 C0C8h	4301 E0C8h
1C0CCh	1E0CCh	CTRLMMR_WKUP_PADCONFIG51	PAD Configuration Register 51	4301 C0CCh	4301 E0CCh
1C0D0h	1E0D0h	CTRLMMR_WKUP_PADCONFIG52	PAD Configuration Register 52	4301 C0D0h	4301 E0D0h
1C0D4h	1E0D4h	CTRLMMR_WKUP_PADCONFIG53	PAD Configuration Register 53	4301 C0D4h	4301 E0D4h
1C0D8h	1E0D8h	CTRLMMR_WKUP_PADCONFIG54	PAD Configuration Register 54	4301 C0D8h	4301 E0D8h
1C0DCh	1E0DCh	CTRLMMR_WKUP_PADCONFIG55	PAD Configuration Register 55	4301 C0DCh	4301 E0DCh
1C0E0h	1E0E0h	CTRLMMR_WKUP_PADCONFIG56	PAD Configuration Register 56	4301 C0E0h	4301 E0E0h
1C0E4h	1E0E4h	CTRLMMR_WKUP_PADCONFIG57	PAD Configuration Register 57	4301 C0E4h	4301 E0E4h
1C0E8h	1E0E8h	CTRLMMR_WKUP_PADCONFIG58	PAD Configuration Register 58	4301 C0E8h	4301 E0E8h
1C0ECh	1E0ECh	CTRLMMR_WKUP_PADCONFIG59	PAD Configuration Register 59	4301 C0ECh	4301 E0ECh
1C0F0h	1E0F0h	CTRLMMR_WKUP_PADCONFIG60	PAD Configuration Register 60	4301 C0F0h	4301 E0F0h
1C0F4h	1E0F4h	CTRLMMR_WKUP_PADCONFIG61	PAD Configuration Register 61	4301 C0F4h	4301 E0F4h
1C0F8h	1E0F8h	CTRLMMR_WKUP_PADCONFIG62	PAD Configuration Register 62	4301 C0F8h	4301 E0F8h
1C0FCh	1E0FCh	CTRLMMR_WKUP_PADCONFIG63	PAD Configuration Register 63	4301 C0FCh	4301 E0FCh
1C100h	1E100h	CTRLMMR_WKUP_PADCONFIG64	PAD Configuration Register 64	4301 C100h	4301 E100h
1C104h	1E104h	CTRLMMR_WKUP_PADCONFIG65	PAD Configuration Register 65	4301 C104h	4301 E104h
1C108h	1E108h	CTRLMMR_WKUP_PADCONFIG66	PAD Configuration Register 66	4301 C108h	4301 E108h
1C10Ch	1E10Ch	CTRLMMR_WKUP_PADCONFIG67	PAD Configuration Register 67	4301 C10Ch	4301 E10Ch
1C110h	1E110h	CTRLMMR_WKUP_PADCONFIG68	PAD Configuration Register 68	4301 C110h	4301 E110h
1C114h	1E114h	CTRLMMR_WKUP_PADCONFIG69	PAD Configuration Register 69	4301 C114h	4301 E114h
1C118h	1E118h	CTRLMMR_WKUP_PADCONFIG70	PAD Configuration Register 70	4301 C118h	4301 E118h
1C11Ch	1E11Ch	CTRLMMR_WKUP_PADCONFIG71	PAD Configuration Register 71	4301 C11Ch	4301 E11Ch
1C120h	1E120h	CTRLMMR_WKUP_PADCONFIG72	PAD Configuration Register 72	4301 C120h	4301 E120h
1C124h	1E124h	CTRLMMR_WKUP_PADCONFIG73	PAD Configuration Register 73	4301 C124h	4301 E124h
1C128h	1E128h	CTRLMMR_WKUP_PADCONFIG74	PAD Configuration Register 74	4301 C128h	4301 E128h
1C12Ch	1E12Ch	CTRLMMR_WKUP_PADCONFIG75	PAD Configuration Register 75	4301 C12Ch	4301 E12Ch

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Table 2-2. WKUP_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	WKUP_CTRL_MMR0 Proxy0 Physical Address	WKUP_CTRL_MMR0 Proxy1 Physical Address
1C130h	1E130h	CTRLMMR_WKUP_PADCONFIG76	PAD Configuration Register 76	4301 C130h	4301 E130h
1C134h	1E134h	CTRLMMR_WKUP_PADCONFIG77	PAD Configuration Register 77	4301 C134h	4301 E134h
1C138h	1E138h	CTRLMMR_WKUP_PADCONFIG78	PAD Configuration Register 78	4301 C138h	4301 E138h
1C13Ch	1E13Ch	CTRLMMR_WKUP_PADCONFIG79	PAD Configuration Register 79	4301 C13Ch	4301 E13Ch
1C140h	1E140h	CTRLMMR_WKUP_PADCONFIG80	PAD Configuration Register 80	4301 C140h	4301 E140h
1C144h	1E144h	CTRLMMR_WKUP_PADCONFIG81	PAD Configuration Register 81	4301 C144h	4301 E144h
1C148h	1E148h	CTRLMMR_WKUP_PADCONFIG82	PAD Configuration Register 82	4301 C148h	4301 E148h
1C14Ch	1E14Ch	CTRLMMR_WKUP_PADCONFIG83	PAD Configuration Register 83	4301 C14Ch	4301 E14Ch
1C150h	1E150h	CTRLMMR_WKUP_PADCONFIG84	PAD Configuration Register 84	4301 C150h	4301 E150h
1C154h	1E154h	CTRLMMR_WKUP_PADCONFIG85	PAD Configuration Register 85	4301 C154h	4301 E154h
1C158h	1E158h	CTRLMMR_WKUP_PADCONFIG86	PAD Configuration Register 86	4301 C158h	4301 E158h
1C15Ch	1E15Ch	CTRLMMR_WKUP_PADCONFIG87	PAD Configuration Register 87	4301 C15Ch	4301 E15Ch
1C160h	1E160h	CTRLMMR_WKUP_PADCONFIG88	PAD Configuration Register 88	4301 C160h	4301 E160h
1C164h	1E164h	CTRLMMR_WKUP_PADCONFIG89	PAD Configuration Register 89	4301 C164h	4301 E164h
1C168h	1E168h	CTRLMMR_WKUP_PADCONFIG90	PAD Configuration Register 90	4301 C168h	4301 E168h
1C16Ch	1E16Ch	CTRLMMR_WKUP_PADCONFIG91	PAD Configuration Register 91	4301 C16Ch	4301 E16Ch
1C170h	1E170h	CTRLMMR_WKUP_PADCONFIG92	PAD Configuration Register 92	4301 C170h	4301 E170h
1C174h	1E174h	CTRLMMR_WKUP_PADCONFIG93	PAD Configuration Register 93	4301 C174h	4301 E174h
1D008h	1F008h	CTRLMMR_WKUP_LOCK7_KICK0	Partition 7 Lock Key 0 Register	4301 D008h	4301 F008h
1D00Ch	1F00Ch	CTRLMMR_WKUP_LOCK7_KICK1	Partition 7 Lock Key 1 Register	4301 D00Ch	4301 F00Ch
1D100h	1F100h	CTRLMMR_WKUP_P7_CLAIM0	Partition 7 Claim Register 0	4301 D100h	4301 F100h
1D104h	1F104h	CTRLMMR_WKUP_P7_CLAIM1	Partition 7 Claim Register 1	4301 D104h	4301 F104h
1D108h	1F108h	CTRLMMR_WKUP_P7_CLAIM2	Partition 7 Claim Register 2	4301 D108h	4301 F108h

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2.1 CTRLMMR_WKUP_PID Register (Proxy0 Offset = 0h; Proxy1 Offset = 2000h) [reset = 61800800h]

CTRLMMR_WKUP_PID is shown in Figure 2-1 and described in Table 2-4.

Return to Summary Table.

Peripheral release details.

Table 2-3. CTRLMMR_WKUP_PID Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0000h	4300 2000h

Figure 2-1. CTRLMMR_WKUP_PID Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R-1h		R-2h		R-180h			

23	22	21	20	19	18	17	16
FUNC							
R-180h							

15	14	13	12	11	10	9	8
R_RTL					X_MAJOR		
R-1h					R-0h		

7	6	5	4	3	2	1	0
CUSTOM		Y_MINOR					
R-0h		R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 2-4. CTRLMMR_WKUP_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business unit
27-16	FUNC	R	180h	Module functional identifier
15-11	R_RTL	R	1h	RTL revision
10-8	X_MAJOR	R	0h	Major revision
7-6	CUSTOM	R	0h	Custom revision
5-0	Y_MINOR	R	0h	Minor revision

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2.2 CTRLMMR_WKUP_MMR_CFG1 Register (Proxy0 Offset = 8h; Proxy1 Offset = 2008h) [reset = 800000DFh]

CTRLMMR_WKUP_MMR_CFG1 is shown in Figure 2-2 and described in Table 2-6.

Return to Summary Table.

Indicates the MMR configuration.

Table 2-5. CTRLMMR_WKUP_MMR_CFG1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0008h	4300 2008h

Figure 2-2. CTRLMMR_WKUP_MMR_CFG1 Register

31	30	29	28	27	26	25	24
PROXY_EN	RESERVED						
R-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
PARTITIONS							
R-DFh							

LEGEND: R = Read Only; *-n* = value after reset

Table 2-6. CTRLMMR_WKUP_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PROXY_EN	R	1h	Proxy addressing enabled
30-8	RESERVED	R	0h	Reserved
7-0	PARTITIONS	R	DFh	Indicates present partitions

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2.3 CTRLMMR_WKUP_JTAG_USER_ID Register (Proxy0 Offset = 18h; Proxy1 Offset = 2014h) [reset = BB6402Fh]

Return to Summary Table.

This register must be readable by the configuration bus so that this can be accessed via the JTAG and CPU. In Boundary Scan mode, this ID should also be readable with only TCLK present. This means without a valid CPU clock running and also implies that Fusefarm scan is not necessary. The Variant field should be set in the top metal mask so that this may be changed if a future PG is necessary. All other fields may be hard coded.

Table 2-7. CTRLMMR_WKUP_JTAG_USER_ID Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0018h	4300 2018h

Figure 2-3. CTRLMMR_WKUP_JTAG_USER_ID Register

31	30	29	28	27	26	25	24
DEVICE_ID							
R-0h							
23	22	21	20	19	18	17	16
DEVICE_ID							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 2-8. CTRLMMR_WKUP_JTAG_USER_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DEVICE_ID	R	0h	Base part number See device comparison table in the device-specific data sheet for details.
15-0	Reserved			

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2.4 CTRLMMR_WKUP_DIE_ID0 Register (Proxy0 Offset = 20h; Proxy1 Offset = 2020h) [reset = X]

CTRLMMR_WKUP_DIE_ID0 is shown in Figure 2-4 and described in Table 2-10.

Return to Summary Table.

Contains information to identify this particular die.

Table 2-9. CTRLMMR_WKUP_DIE_ID0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0020h	4300 2020h

Figure 2-4. CTRLMMR_WKUP_DIE_ID0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIEID																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 2-10. CTRLMMR_WKUP_DIE_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIEID	R	X	Contains individual die information

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2.5 CTRLMMR_WKUP_DIE_ID1 Register (Proxy0 Offset = 24h; Proxy1 Offset = 2024h) [reset = X]

CTRLMMR_WKUP_DIE_ID1 is shown in Figure 2-5 and described in Table 2-12.

Return to Summary Table.

Contains information to identify this particular die.

Table 2-11. CTRLMMR_WKUP_DIE_ID1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0024h	4300 2024h

Figure 2-5. CTRLMMR_WKUP_DIE_ID1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIEID																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 2-12. CTRLMMR_WKUP_DIE_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIEID	R	X	Contains individual die information

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2.6 CTRLMMR_WKUP_DIE_ID2 Register (Proxy0 Offset = 28h; Proxy1 Offset = 2028h) [reset = X]

CTRLMMR_WKUP_DIE_ID2 is shown in Figure 2-6 and described in Table 2-14.

Return to Summary Table.

Contains information to identify this particular die.

Table 2-13. CTRLMMR_WKUP_DIE_ID2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0028h	4300 2028h

Figure 2-6. CTRLMMR_WKUP_DIE_ID2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIEID																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 2-14. CTRLMMR_WKUP_DIE_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIEID	R	X	Contains individual die information

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2.7 CTRLMMR_WKUP_DIE_ID3 Register (Proxy0 Offset = 2Ch; Proxy1 Offset = 202Ch) [reset = X]

CTRLMMR_WKUP_DIE_ID3 is shown in Figure 2-7 and described in Table 2-16.

Return to Summary Table.

Contains information to identify this particular die.

Table 2-15. CTRLMMR_WKUP_DIE_ID3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 002Ch	4300 202Ch

Figure 2-7. CTRLMMR_WKUP_DIE_ID3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIEID																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 2-16. CTRLMMR_WKUP_DIE_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DIEID	R	X	Contains individual die information

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2.8 CTRLMMR_WKUP_DEVSTAT Register (Proxy0 Offset = 30h; Proxy1 Offset = 2030h) [reset = X]

CTRLMMR_WKUP_DEVSTAT is shown in Figure 2-8 and described in Table 2-18.

Return to Summary Table.

Indicates MCU bootstrap selection. The default value of this register is determined by the MCU bootstrap pins when the por_boot_cfg_srst_n input is de-asserted.

Table 2-17. CTRLMMR_WKUP_DEVSTAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0030h	4300 2030h

Figure 2-8. CTRLMMR_WKUP_DEVSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						BOOTMODE									
R-0h																						R/W-X									

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-18. CTRLMMR_WKUP_DEVSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BOOTMODE	R/W	X	Indicates MCU bootstrap selection. The default value of this register is determined by the MCU bootstrap pins when the por_boot_cfg_srst_n input is de-asserted. However, this register can be written before a warm boot to invoke a different boot mode than that latched from the BOOTMODE pins. Bits 9:8 - Power-on Self Test mode (if CTRLMMR_WKUP_POST_SEL_STAT = 0h) 0h - POST mode 1 (See POST_OPT_opt1_xxx bitfields) 1h - POST mode 2 (See POST_OPT_opt2_xxx bitfields) 2h - POST mode 3 (See POST_OPT_opt3_xxx bitfields) 3h - Bypass POST Bits 7:3 - MCU primary and secondary boot source Bits 2:0 - WKUP_HFOSC0 frequency selection 0h - 19.2 MHz 1h - 20.0 MHz 2h - 24.0 MHz 3h - 25.0 MHz 4h - 26.0 MHz 5h - 27.0 MHz 6h - Reserved for device test 7h - No PLL configuration

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2.9 CTRLMMR_WKUP_BOOTCFG Register (Proxy0 Offset = 34h; Proxy1 Offset = 2034h) [reset = X]

CTRLMMR_WKUP_BOOTCFG is shown in Figure 2-9 and described in Table 2-20.

Return to Summary Table.

Indicates MCU bootstrap selection latched at power-on reset by PORz. The default value of this register is determined by the MCU bootstrap pins when the por_boot_cfg_srst_n input is de-asserted and will remain until the MCU bootstrap pins are re-latched on a subsequent por_boot_cfg_srst_n rising edge.

Table 2-19. CTRLMMR_WKUP_BOOTCFG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0034h	4300 2034h

Figure 2-9. CTRLMMR_WKUP_BOOTCFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						BOOTMODE									
R-0h																						R-X									

LEGEND: R = Read Only; *-n* = value after reset

Table 2-20. CTRLMMR_WKUP_BOOTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R	0h	Reserved
9-0	BOOTMODE	R	X	Indicates MCU boot mode as latched at power-on reset. These bits always contain the values latched. Bits 9:8 - Power-on Self Test mode (if CTRLMMR_WKUP_POST_SEL_STAT = 0h) 0h - POST mode 1 (See POST_OPT_opt1_xxx bitfields) 1h - POST mode 2 (See POST_OPT_opt2_xxx bitfields) 2h - POST mode 3 (See POST_OPT_opt3_xxx bitfields) 3h - Bypass POST Bits 7:3 - MCU primary and secondary boot source Bits 2:0 - WKUP_HFOSC0 frequency selection 0h - 19.2 MHz 1h - 20.0 MHz 2h - 24.0 MHz 3h - 25.0 MHz 4h - 26.0 MHz 5h - 27.0 MHz 6h - Reserved for device test 7h - No PLL configuration

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2.10 CTRLMMR_WKUP_POST_SEL_STAT Register (Proxy0 Offset = 38h; Proxy1 Offset = 2038h) [reset = X]

CTRLMMR_WKUP_POST_SEL_STAT is shown in Figure 2-10 and described in Table 2-22.

Return to Summary Table.

Indicates which power-on self test option was performed.

Table 2-21. CTRLMMR_WKUP_POST_SEL_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0038h	4300 2038h

Figure 2-10. CTRLMMR_WKUP_POST_SEL_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						POST_SEL_STAT	
R-0h						R-X	

LEGEND: R = Read Only; *-n* = value after reset

Table 2-22. CTRLMMR_WKUP_POST_SEL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	POST_SEL_STAT	R	X	Indicates which POST option was selected at power-up

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2.11 CTRLMMR_WKUP_POST_OPT Register (Proxy0 Offset = 3Ch; Proxy1 Offset = 203Ch) [reset = X]

CTRLMMR_WKUP_POST_OPT is shown in Figure 2-11 and described in Table 2-24.

Return to Summary Table.

Indicates the 3 available power-on self test (POST) options:
Bits 3:0 - POST Option 1
Bits 11:8 - POST Option 2
Bits 19:16 - POST Option 3

Table 2-23. CTRLMMR_WKUP_POST_OPT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 003Ch	4300 203Ch

Figure 2-11. CTRLMMR_WKUP_POST_OPT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED				OPT3_MCU_PBIST_EN	OPT3_MCU_LBIST_EN	OPT3_DMSC_LBIST_EN	OPT3_PARALLEL_EN
R-0h				R-X	R-X	R-X	R-X
15	14	13	12	11	10	9	8
RESERVED				OPT2_MCU_PBIST_EN	OPT2_MCU_LBIST_EN	OPT2_DMSC_LBIST_EN	OPT2_PARALLEL_EN
R-0h				R-X	R-X	R-X	R-X
7	6	5	4	3	2	1	0
RESERVED				OPT1_MCU_PBIST_EN	OPT1_MCU_LBIST_EN	OPT1_DMSC_LBIST_EN	OPT1_PARALLEL_EN
R-0h				R-X	R-X	R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-24. CTRLMMR_WKUP_POST_OPT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19	OPT3_MCU_PBIST_EN	R	X	MCU R5 PBIST enabled
18	OPT3_MCU_LBIST_EN	R	X	MCU R5 LBIST enabled
17	OPT3_DMSC_LBIST_EN	R	X	DMSC LBIST enabled
16	OPT3_PARALLEL_EN	R	X	Selects DMSC/MCU R5 LBIST sequencing 0h - Serial (DMSC LBIST performed first) 1h - Parallel
15-12	RESERVED	R	0h	Reserved
11	OPT2_MCU_PBIST_EN	R	X	MCU R5 PBIST enabled
10	OPT2_MCU_LBIST_EN	R	X	MCU R5 LBIST enabled
9	OPT2_DMSC_LBIST_EN	R	X	DMSC LBIST enabled
8	OPT2_PARALLEL_EN	R	X	Selects DMSC/MCU R5 LBIST sequencing 0h - Serial (DMSC LBIST performed first) 1h - Parallel
7-4	RESERVED	R	0h	Reserved

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Table 2-24. CTRLMMR_WKUP_POST_OPT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	OPT1_MCU_PBIST_EN	R	X	MCU R5 PBIST enabled
2	OPT1_MCU_LBIST_EN	R	X	MCU R5 LBIST enabled
1	OPT1_DMSC_LBIST_EN	R	X	DMSC LBIST enabled
0	OPT1_PARALLEL_EN	R	X	Selects DMSC/MCU R5 LBIST sequencing 0h - Serial (DMSC LBIST performed first) 1h - Parallel

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2.12 CTRLMMR_WKUP_RESET_SRC_STAT Register (Proxy0 Offset = 50h; Proxy1 Offset = 2050h) [reset = 0h]

CTRLMMR_WKUP_RESET_SRC_STAT is shown in Figure 2-12 and described in Table 2-26.

Return to Summary Table.

Indicates source of last device reset.

Table 2-25. CTRLMMR_WKUP_RESET_SRC_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0050h	4300 2050h

Figure 2-12. CTRLMMR_WKUP_RESET_SRC_STAT Register

31	30	29	28	27	26	25	24
RESERVED							THERMAL_RST
R-0h							REC-0h
23	22	21	20	19	18	17	16
RESERVED			DBUGSS_RST	COLD_OUT_RST	RESERVED		WARM_OUT_RST
R-0h			FEC-0h	FEC-0h	R-0h		FEC-0h
15	14	13	12	11	10	9	8
RESERVED				PORZ_PIN	RESERVED	RESET_REQZ_PIN	MCU_RSTZ_PIN
R-0h				FEC-0h	R-0h	FEC-0h	FEC-0h
7	6	5	4	3	2	1	0
RESERVED				SW_MAIN_POR	RESERVED	SW_MAIN_WARMRST	SW_MCU_WARMRST
R-0h				FEC-0h	R-0h	FEC-0h	FEC-0h

LEGEND: FEC = Falling Edge Capture; R = Read Only; REC = Rising Edge Capture-*n* = value after reset

Table 2-26. CTRLMMR_WKUP_RESET_SRC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	THERMAL_RST	REC	0h	When set, indicates that a VTM Max Temp Thermal reset occurred. Write 1 to clear this bit.
23-21	RESERVED	R	0h	Reserved
20	DBUGSS_RST	FEC	0h	When set, indicates that a Debug reset occurred. Write 1 to clear this bit.
19	COLD_OUT_RST	FEC	0h	When set, indicates that a DMSC Cold reset occurred. Write 1 to clear this bit.
18-17	RESERVED	R	0h	Reserved
16	WARM_OUT_RST	FEC	0h	When set, indicates that a DSMC Warm reset occured. Write 1 to clear this bit.
15-12	RESERVED	R	0h	Reserved
11	PORZ_PIN	FEC	0h	When set indicates that a PORz pin reset occurred. Write 1 to clear this bit.
10	RESERVED	R	0h	Reserved

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Table 2-26. CTRLMMR_WKUP_RESET_SRC_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	RESET_REQZ_PIN	FEC	0h	When set indicates that a RESET_REQz pin reset occurred. Write 1 to clear this bit.
8	MCU_RSTZ_PIN	FEC	0h	When set indicates that a MCU_RESETz pin reset occurred. Write 1 to clear this bit.
7-4	RESERVED	R	0h	Reserved
3	SW_MAIN_POR	FEC	0h	When set, indicates that a Software MAIN Power-on reset occurred. Write 1 to clear this bit.
2	RESERVED	R	0h	Reserved
1	SW_MAIN_WARMRST	FEC	0h	When set indicates that a Software MAIN Warm reset occurred. Write 1 to clear this bit.
0	SW_MCU_WARMRST	FEC	0h	When set indicates that a Software MCU Warm reset occurred. Write 1 to clear this bit.

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2.13 CTRLMMR_WKUP_DEVICE_FEATURE0 Register (Proxy0 Offset = 60h; Proxy1 Offset = 2060h) [reset = X]

CTRLMMR_WKUP_DEVICE_FEATURE0 is shown in Figure 2-13 and described in Table 2-28.

Return to Summary Table.

Indicates enabled MPU processing elements on the device.

Table 2-27. CTRLMMR_WKUP_DEVICE_FEATURE0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0060h	4300 2060h

Figure 2-13. CTRLMMR_WKUP_DEVICE_FEATURE0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED		RESERVED	RESERVED	RESERVED		MPU_CLUSTER0_CORE1	MPU_CLUSTER0_CORE0
R-0h		R-X	R-X	R-0h		R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-28. CTRLMMR_WKUP_DEVICE_FEATURE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5	RESERVED	R	X	Reserved
4	RESERVED	R	X	Reserved
3-2	RESERVED	R	0h	Reserved
1	MPU_CLUSTER0_CORE1	R	X	MPU Cluster0 Core 1 is enabled when set
0	MPU_CLUSTER0_CORE0	R	X	MPU Cluster0 Core 0 is enabled when set

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2.14 CTRLMMR_WKUP_DEVICE_FEATURE1 Register (Proxy0 Offset = 64h; Proxy1 Offset = 2064h) [reset = X]

CTRLMMR_WKUP_DEVICE_FEATURE1 is shown in Figure 2-14 and described in Table 2-30.

Return to Summary Table.

Indicates enabled non-MPU processing elements on the device.

Table 2-29. CTRLMMR_WKUP_DEVICE_FEATURE1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0064h	4300 2064h

Figure 2-14. CTRLMMR_WKUP_DEVICE_FEATURE1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED						RESERVED	C71_CORE0
R-0h						R-X	R-X

15	14	13	12	11	10	9	8
RESERVED			GPU	RESERVED		C66_CORE1	C66_CORE0
R-0h			R-X	R-0h		R-X	R-X

7	6	5	4	3	2	1	0
RESERVED				MCU_CLUSTER1_CORE1	MCU_CLUSTER1_CORE0	MCU_CLUSTER0_CORE1	MCU_CLUSTER0_CORE0
R-0h				R-X	R-X	R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-30. CTRLMMR_WKUP_DEVICE_FEATURE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	RESERVED	R	X	Reserved
16	C71_CORE0	R	X	C71 Core0 is enabled when set
15-13	RESERVED	R	0h	Reserved
12	GPU	R	X	GPU is enabled when set
11-10	RESERVED	R	0h	Reserved
9	C66_CORE1	R	X	C66 Core1 is enabled when set
8	C66_CORE0	R	X	C66 Core0 is enabled when set
7-4	RESERVED	R	0h	Reserved
3	MCU_CLUSTER1_CORE1	R	X	MAIN MCU Cluster1 Core1 is enabled when set
2	MCU_CLUSTER1_CORE0	R	X	MAIN MCU Cluster1 Core0 is enabled when set
1	MCU_CLUSTER0_CORE1	R	X	MAIN MCU Cluster0 Core1 is enabled when set
0	MCU_CLUSTER0_CORE0	R	X	MAIN MCU Cluster0 Core0 is enabled when set

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2.15 CTRLMMR_WKUP_DEVICE_FEATURE2 Register (Proxy0 Offset = 68h; Proxy1 Offset = 2068h) [reset = X]

CTRLMMR_WKUP_DEVICE_FEATURE2 is shown in Figure 2-15 and described in Table 2-32.

Return to Summary Table.

Indicates enabled MCU domain interface elements on the device.

Table 2-31. CTRLMMR_WKUP_DEVICE_FEATURE2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0068h	4300 2068h

Figure 2-15. CTRLMMR_WKUP_DEVICE_FEATURE2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					CRYPTO_PKA_EN	CRYPTO_ENCR_EN	CRYPTO_SHA_EN
R-0h					R-X	R-X	R-X
7	6	5	4	3	2	1	0
AES_AUTH_EN	HYPERBUS	OSPI1	OSPI0	MCU_MCAN1	RESERVED	MCU_MCAN0	MCU_MCAN_FD_MODE
R-X	R-X	R-X	R-X	R-X	R-0h	R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-32. CTRLMMR_WKUP_DEVICE_FEATURE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10	CRYPTO_PKA_EN	R	X	MCU SA2_UL Crypto Module PKA enabled
9	CRYPTO_ENCR_EN	R	X	MCU SA2_UL Crypto Module AES/3DES/DBRG enabled
8	CRYPTO_SHA_EN	R	X	MCU SA2_UL Crypto Module SHA/MD5 enabled
7	AES_AUTH_EN	R	X	AES authentication is enabled in MCU_FlashSS and DMSC when set
6	HYPERBUS	R	X	MCU_FSS0_HPB0 is enabled when set
5	OSPI1	R	X	MCU_OSPI1 is enabled when set
4	OSPI0	R	X	MCU_OSPI0 is enabled when set
3	MCU_MCAN1	R	X	MCU_MCAN1 is enabled when set
2	RESERVED	R	0h	Reserved
1	MCU_MCAN0	R	X	MCU_MCAN0 is enabled when set
0	MCU_MCAN_FD_MODE	R	X	FD mode is supported on MCU_MCAN[1:0] when set

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2.16 CTRLMMR_WKUP_DEVICE_FEATURE3 Register (Proxy0 Offset = 6Ch; Proxy1 Offset = 206Ch) [reset = X]

CTRLMMR_WKUP_DEVICE_FEATURE3 is shown in Figure 2-16 and described in Table 2-34.

Return to Summary Table.

Indicates enabled MAIN domain interface elements on the device.

Table 2-33. CTRLMMR_WKUP_DEVICE_FEATURE3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 006Ch	4300 206Ch

Figure 2-16. CTRLMMR_WKUP_DEVICE_FEATURE3 Register

31	30	29	28	27	26	25	24
RESERVED		RESERVED	EMIF0	RESERVED			
R-0h		R-X	R-X	R-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	RESERVED	MMC_4B0	MMC_8B	RESERVED		ICSS_G1	ICSS_G0
R-0h	R-X	R-X	R-X	R-0h		R-X	R-X
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED		RESERVED	SERDES4	SERDES3	SERDES2	SERDES1	SERDES0
R-0h		R-X	R-X	R-X	R-X	R-X	R-X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PCIE3	PCIE2	PCIE1	PCIE0	RESERVED	RESERVED	USB1	USB0
R-X	R-X	R-X	R-X	R-0h	R-X	R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-34. CTRLMMR_WKUP_DEVICE_FEATURE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	RESERVED	R	X	Reserved
28	EMIF0	R	X	EMIF0 is enabled when set
27-23	RESERVED	R	0h	Reserved
22	RESERVED	R	X	Reserved
21	MMC_4B0	R	X	4-bit MMCSD1 is enabled when set
20	MMC_8B	R	X	8-bit MMCSD0 is enabled when set
19-18	RESERVED	R	0h	Reserved
17	ICSS_G1	R	X	ICSS_G1 is enabled when set
16	ICSS_G0	R	X	ICSS_G0 is enabled when set
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R	X	Reserved
12	SERDES4	R	X	10G SERDES4 is enabled when set
11	SERDES3	R	X	16G SERDES3 is enabled when set
10	SERDES2	R	X	16G SERDES2 is enabled when set
9	SERDES1	R	X	16G SERDES1 is enabled when set

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Table 2-34. CTRLMMR_WKUP_DEVICE_FEATURE3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	SERDES0	R	X	16G SERDES0 is enabled when set
7	PCIE3	R	X	PCIe3 is enabled when set
6	PCIE2	R	X	PCIe2 is enabled when set
5	PCIE1	R	X	PCIe1 is enabled when set
4	PCIE0	R	X	PCIe0 is enabled when set
3	RESERVED	R	0h	Reserved
2	RESERVED	R	X	Reserved
1	USB1	R	X	USB1 is enabled when set
0	USB0	R	X	USB0 is enabled when set

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2.17 CTRLMMR_WKUP_DEVICE_FEATURE4 Register (Proxy0 Offset = 70h; Proxy1 Offset = 2070h) [reset = X]

CTRLMMR_WKUP_DEVICE_FEATURE4 is shown in Figure 2-17 and described in Table 2-36.

Return to Summary Table.

Indicates enabled MAIN domain interface elements on the device.

Table 2-35. CTRLMMR_WKUP_DEVICE_FEATURE4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0070h	4300 2070h

Figure 2-17. CTRLMMR_WKUP_DEVICE_FEATURE4 Register

31	30	29	28	27	26	25	24
RESERVED						DECODER	ENCODER
R-0h						R-X	R-X
23	22	21	20	19	18	17	16
RESERVED			VPFE	VPE	VPAC	SDE	DMPAC
R-0h			R-X	R-X	R-X	R-X	R-X
15	14	13	12	11	10	9	8
RESERVED		RESERVED	EDP0	RESERVED			CSITX0
R-0h		R-X	R-X	R-0h			R-X
7	6	5	4	3	2	1	0
RESERVED	RESERVED	CSIRX1	CSIRX0	RESERVED	DSI	RESERVED	DSS
R-0h	R-X	R-X	R-X	R-0h	R-X	R-0h	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-36. CTRLMMR_WKUP_DEVICE_FEATURE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25	DECODER	R	X	Video decoder is enabled when set
24	ENCODER	R	X	Video encoder is enabled when set
23-21	RESERVED	R	0h	Reserved
20	VPFE	R	X	VPFE is enabled when set
19	VPE	R	X	Video processing engine is enabled when set
18	VPAC	R	X	VPAC is enabled when set
17	SDE	R	X	DMPAC Stereo Disparity Engine is enabled when set
16	DMPAC	R	X	DMPAC is enabled when set
15-14	RESERVED	R	0h	Reserved
13	RESERVED	R	X	Reserved
12	EDP0	R	X	Embedded display port 0 is enabled when set
11-9	RESERVED	R	0h	Reserved
8	CSITX0	R	X	CSI_TX0 is enabled when set
7	RESERVED	R	0h	Reserved
6	RESERVED	R	X	Reserved

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Table 2-36. CTRLMMR_WKUP_DEVICE_FEATURE4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CSIRX1	R	X	CSI_RX1 is enabled when set
4	CSIRX0	R	X	CSI_RX0 is enabled when set
3	RESERVED	R	0h	Reserved
2	DSI	R	X	DSI is enabled when set
1	RESERVED	R	0h	Reserved
0	DSS	R	X	DSS is enabled when set

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2.18 CTRLMMR_WKUP_DEVICE_FEATURE5 Register (Proxy0 Offset = 74h; Proxy1 Offset = 2074h) [reset = X]

CTRLMMR_WKUP_DEVICE_FEATURE5 is shown in Figure 2-18 and described in Table 2-38.

Return to Summary Table.

Indicates enabled MAIN domain interface elements on the device.

Table 2-37. CTRLMMR_WKUP_DEVICE_FEATURE5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0074h	4300 2074h

Figure 2-18. CTRLMMR_WKUP_DEVICE_FEATURE5 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED		MCAN13	MCAN12	MCAN11	MCAN10	MCAN9	MCAN8
R-0h		R-X	R-X	R-X	R-X	R-X	R-X
7	6	5	4	3	2	1	0
MCAN7	MCAN6	MCAN5	MCAN4	MCAN3	MCAN2	MCAN1	MCAN0
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-38. CTRLMMR_WKUP_DEVICE_FEATURE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13	MCAN13	R	X	MCAN13 is enabled when set
12	MCAN12	R	X	MCAN12 is enabled when set
11	MCAN11	R	X	MCAN11 is enabled when set
10	MCAN10	R	X	MCAN10 is enabled when set
9	MCAN9	R	X	MCAN9 is enabled when set
8	MCAN8	R	X	MCAN8 is enabled when set
7	MCAN7	R	X	MCAN7 is enabled when set
6	MCAN6	R	X	MCAN6 is enabled when set
5	MCAN5	R	X	MCAN5 is enabled when set
4	MCAN4	R	X	MCAN4 is enabled when set
3	MCAN3	R	X	MCAN3 is enabled when set
2	MCAN2	R	X	MCAN2 is enabled when set
1	MCAN1	R	X	MCAN1 is enabled when set
0	MCAN0	R	X	MCAN0 is enabled when set

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2.19 CTRLMMR_WKUP_DEVICE_FEATURE6 Register (Proxy0 Offset = 78h; Proxy1 Offset = 2078h) [reset = X]

CTRLMMR_WKUP_DEVICE_FEATURE6 is shown in Figure 2-19 and described in Table 2-40.

Return to Summary Table.

Indicates enabled MAIN domain interface elements on the device.

Table 2-39. CTRLMMR_WKUP_DEVICE_FEATURE6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 0078h	4300 2078h

Figure 2-19. CTRLMMR_WKUP_DEVICE_FEATURE6 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED		RESERVED	RESERVED
R-0h	R-X	R-X	R-X	R-0h		R-X	R-X
15	14	13	12	11	10	9	8
RESERVED						I3C	MOTOR_PER
R-0h						R-X	R-X
7	6	5	4	3	2	1	0
ATL	MLB	SA2_UL	CPSW9G	RESERVED		RESERVED	UFS0
R-X	R-X	R-X	R-X	R-0h		R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-40. CTRLMMR_WKUP_DEVICE_FEATURE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-23	RESERVED	R	0h	Reserved
22	RESERVED	R	X	Reserved
21	RESERVED	R	X	Reserved
20	RESERVED	R	X	Reserved
19-18	RESERVED	R	0h	Reserved
17	RESERVED	R	X	Reserved
16	RESERVED	R	X	Reserved
15-10	RESERVED	R	0h	Reserved
9	I3C	R	X	MAIN domain I3C is enabled when set
8	MOTOR_PER	R	X	Motor control peripherals (eCAP, eQEP, eHRPWM) are enabled when set
7	ATL	R	X	Audio tracking logic is enabled when set
6	MLB	R	X	Media local bus is enabled when set
5	SA2_UL	R	X	MAIN domain security accelerator is enabled when set
4	CPSW9G	R	X	8 Channel Q/SGMII Ethernet switch enabled when set
3-2	RESERVED	R	0h	Reserved
1	RESERVED	R	X	Reserved

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Table 2-40. CTRLMMR_WKUP_DEVICE_FEATURE6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	UFS0	R	X	UFS interface 0 is enabled when set

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2.20 CTRLMMR_WKUP_LOCK0_KICK0 Register (Proxy0 Offset = 1008h; Proxy1 Offset = 3008h) [reset = 0h]

CTRLMMR_WKUP_LOCK0_KICK0 is shown in Figure 2-20 and described in Table 2-42.

Return to Summary Table.

Lower 32-bits of Partition0 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_WKUP_LOCK0_KICK1 with its key value before write-protected Partition 0 registers can be written.

Table 2-41. CTRLMMR_WKUP_LOCK0_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1008h	4300 3008h

Figure 2-20. CTRLMMR_WKUP_LOCK0_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-42. CTRLMMR_WKUP_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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2.21 CTRLMMR_WKUP_LOCK0_KICK1 Register (Proxy0 Offset = 100Ch; Proxy1 Offset = 300Ch) [reset = 0h]

CTRLMMR_WKUP_LOCK0_KICK1 is shown in Figure 2-21 and described in Table 2-44.

Return to Summary Table.

Upper 32-bits of Partition 0 write lock key. This register must be written with the designated key value after a write to CTRLMMR_WKUP_LOCK0_KICK0 with its key value before write-protected Partition 0 registers can be written.

Table 2-43. CTRLMMR_WKUP_LOCK0_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 100Ch	4300 300Ch

Figure 2-21. CTRLMMR_WKUP_LOCK0_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-44. CTRLMMR_WKUP_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers

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2.22 CTRLMMR_WKUP_INTR_RAW_STAT Register (Proxy0 Offset = 1010h; Proxy1 Offset = 3010h) [reset = 0h]

CTRLMMR_WKUP_INTR_RAW_STAT is shown in Figure 2-22 and described in Table 2-46.

Return to Summary Table.

Shows the interrupt status (before enabling) and allows setting of the interrupt status (for test).

Table 2-45. CTRLMMR_WKUP_INTR_RAW_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1010h	4300 3010h

Figure 2-22. CTRLMMR_WKUP_INTR_RAW_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	LOCK_ERR	ADDR_ERR	PROT_ERR
R-0h				W1TS-0h	W1TS-0h	W1TS-0h	W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 2-46. CTRLMMR_WKUP_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PROXY_ERR	W1TS	0h	Proxy violation occurred (attempt to write a Proxy1 claimed register through its Proxy0 address) Write 1 to set the status bit (for test) Writing 0 has no effect.
2	LOCK_ERR	W1TS	0h	Lock violation occurred (attempt to write a write-locked register with partition locked) Write 1 to set the status bit (for test) Writing 0 has no effect.
1	ADDR_ERR	W1TS	0h	Address violation occurred (attempt to read or write an invalid register address) Write 1 to set the status bit (for test) Writing 0 has no effect.
0	PROT_ERR	W1TS	0h	Protection violation occurred (attempt to read or write a register with insufficient security or privilege access rights) Write 1 to set the status bit (for test) Writing 0 has no effect.

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2.23 CTRLMMR_WKUP_INTR_STAT_CLR Register (Proxy0 Offset = 1014h; Proxy1 Offset = 3014h) [reset = 0h]

CTRLMMR_WKUP_INTR_STAT_CLR is shown in Figure 2-23 and described in Table 2-48.

Return to Summary Table.

Shows the enabled interrupt status and allows the interrupt to be cleared.

Table 2-47. CTRLMMR_WKUP_INTR_STAT_CLR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1014h	4300 3014h

Figure 2-23. CTRLMMR_WKUP_INTR_STAT_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				EN_PROXY_ERR	EN_LOCK_ERR	EN_ADDR_ERR	EN_PROT_ERR
R-0h				W1TC-0h	W1TC-0h	W1TC-0h	W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 2-48. CTRLMMR_WKUP_INTR_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	EN_PROXY_ERR	W1TC	0h	Enabled proxy interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
2	EN_LOCK_ERR	W1TC	0h	Enabled lock interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
1	EN_ADDR_ERR	W1TC	0h	Enabled address interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
0	EN_PROT_ERR	W1TC	0h	Enabled protection interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.

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2.24 CTRLMMR_WKUP_INTR_EN_SET Register (Proxy0 Offset = 1018h; Proxy1 Offset = 3018h) [reset = 0h]

CTRLMMR_WKUP_INTR_EN_SET is shown in Figure 2-24 and described in Table 2-50.

Return to Summary Table.

Allows interrupt enables to be set.

Table 2-49. CTRLMMR_WKUP_INTR_EN_SET Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1018h	4300 3018h

Figure 2-24. CTRLMMR_WKUP_INTR_EN_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_SET	LOCK_ERR_EN_SET	ADDR_ERR_EN_SET	PROT_ERR_EN_SET
R-0h				W1TS-0h	W1TS-0h	W1TS-0h	W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 2-50. CTRLMMR_WKUP_INTR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PROXY_ERR_EN_SET	W1TS	0h	Proxy interrupt enable Write 1 to enable proxy interrupt events Writing 0 has no effect.
2	LOCK_ERR_EN_SET	W1TS	0h	Lock interrupt enable Write 1 to enable lock interrupt events Writing 0 has no effect.
1	ADDR_ERR_EN_SET	W1TS	0h	Address interrupt enable Write 1 to enable address interrupt events Writing 0 has no effect.
0	PROT_ERR_EN_SET	W1TS	0h	Protection interrupt enable Write 1 to enable protection interrupt events Writing 0 has no effect.

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2.25 CTRLMMR_WKUP_INTR_EN_CLR Register (Proxy0 Offset = 101Ch; Proxy1 Offset = 301Ch) [reset = 0h]

CTRLMMR_WKUP_INTR_EN_CLR is shown in Figure 2-25 and described in Table 2-52.

Return to Summary Table.

Allows interrupt enables to be cleared.

Table 2-51. CTRLMMR_WKUP_INTR_EN_CLR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 101Ch	4300 301Ch

Figure 2-25. CTRLMMR_WKUP_INTR_EN_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	LOCK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
R-0h				W1TC-0h	W1TC-0h	W1TC-0h	W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 2-52. CTRLMMR_WKUP_INTR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PROXY_ERR_EN_CLR	W1TC	0h	Proxy interrupt disable Write 1 to disable proxy interrupt events Writing 0 has no effect.
2	LOCK_ERR_EN_CLR	W1TC	0h	Lock interrupt disable Write 1 to disable lock interrupt events Writing 0 has no effect.
1	ADDR_ERR_EN_CLR	W1TC	0h	Address interrupt disable Write 1 to disable address interrupt events Writing 0 has no effect.
0	PROT_ERR_EN_CLR	W1TC	0h	Protection interrupt disable Write 1 to disable protection interrupt events Writing 0 has no effect.

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2.26 CTRLMMR_WKUP_EOI Register (Proxy0 Offset = 1020h; Proxy1 Offset = 3020h) [reset = 0h]

CTRLMMR_WKUP_EOI is shown in Figure 2-26 and described in Table 2-54.

Return to Summary Table.

EOI Vector value. This register should be written with interrupt distribution value required by the device architecture to indicate service completion of the MMR interrupt.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 2-53. CTRLMMR_WKUP_EOI Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1020h	4300 3020h

Figure 2-26. CTRLMMR_WKUP_EOI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VECTOR							
R-0h																								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-54. CTRLMMR_WKUP_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VECTOR	R/W	0h	EOI vector value

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2.27 CTRLMMR_WKUP_FAULT_ADDR Register (Proxy0 Offset = 1024h; Proxy1 Offset = 3024h) [reset = 0h]

CTRLMMR_WKUP_FAULT_ADDR is shown in Figure 2-27 and described in Table 2-56.

Return to Summary Table.

Indicates the address of the first transfer that caused a fault to occur.

Table 2-55. CTRLMMR_WKUP_FAULT_ADDR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1024h	4300 3024h

Figure 2-27. CTRLMMR_WKUP_FAULT_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 2-56. CTRLMMR_WKUP_FAULT_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	Address of the faulted access

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2.28 CTRLMMR_WKUP_FAULT_TYPE Register (Proxy0 Offset = 1028h; Proxy1 Offset = 3028h) [reset = 0h]

CTRLMMR_WKUP_FAULT_TYPE is shown in Figure 2-28 and described in Table 2-58.

Return to Summary Table.

Indicates the access type of the first transfer that caused a fault to occur.

Table 2-57. CTRLMMR_WKUP_FAULT_TYPE Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1028h	4300 3028h

Figure 2-28. CTRLMMR_WKUP_FAULT_TYPE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										TYPE					
R-0h																										R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 2-58. CTRLMMR_WKUP_FAULT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	TYPE	R	0h	Type of access which faulted 0h - No fault 1h - User execute access 2h - User write access 4h - User read access 8h - Supervisor execute access 10h - Supervisor write access 20h - Supervisor read access

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2.29 CTRLMMR_WKUP_FAULT_ATTR Register (Proxy0 Offset = 102Ch; Proxy1 Offset = 302Ch) [reset = 0h]

CTRLMMR_WKUP_FAULT_ATTR is shown in Figure 2-29 and described in Table 2-60.

Return to Summary Table.

Indicates the attributes of the first transfer that caused a fault to occur.

Table 2-59. CTRLMMR_WKUP_FAULT_ATTR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 102Ch	4300 302Ch

Figure 2-29. CTRLMMR_WKUP_FAULT_ATTR Register

31	30	29	28	27	26	25	24
XID							
R-0h							
23	22	21	20	19	18	17	16
XID				ROUTEID			
R-0h				R-0h			
15	14	13	12	11	10	9	8
ROUTEID							
R-0h							
7	6	5	4	3	2	1	0
PRIVID							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 2-60. CTRLMMR_WKUP_FAULT_ATTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	XID	R	0h	Transaction ID
19-8	ROUTEID	R	0h	Route ID
7-0	PRIVID	R	0h	Privilege ID

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2.30 CTRLMMR_WKUP_FAULT_CLR Register (Proxy0 Offset = 1030h; Proxy1 Offset = 3030h) [reset = 0h]

CTRLMMR_WKUP_FAULT_CLR is shown in Figure 2-30 and described in Table 2-62.

Return to Summary Table.

Allows software to clear the current fault. Clearing the current fault allows the CTRLMMR_WKUP_FAULT_ADDR, CTRLMMR_WKUP_FAULT_TYPE, and CTRLMMR_WKUP_FAULT_ATTR registers to latch the attributes of the next fault that occurs. This does not affect the fault interrupt event itself. The interrupt must be cleared using the appropriate INTR_STATUS_CLR register bits.

Table 2-61. CTRLMMR_WKUP_FAULT_CLR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1030h	4300 3030h

Figure 2-30. CTRLMMR_WKUP_FAULT_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLEAR
R-0h							W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 2-62. CTRLMMR_WKUP_FAULT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLEAR	W1TC	0h	Fault clear Write 1 to clear the current fault Writing 0 has no effect

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2.31 CTRLMMR_WKUP_P0_CLAIM0 Register (Proxy0 Offset = 1100h; Proxy1 Offset = 3100h) [reset = 0h]

CTRLMMR_WKUP_P0_CLAIM0 is shown in Figure 2-31 and described in Table 2-64.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 2-63. CTRLMMR_WKUP_P0_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1100h	4300 3100h

Figure 2-31. CTRLMMR_WKUP_P0_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-64. CTRLMMR_WKUP_P0_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (0 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (0 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.32 CTRLMMR_WKUP_P0_CLAIM1 Register (Proxy0 Offset = 1104h; Proxy1 Offset = 3104h) [reset = 0h]

CTRLMMR_WKUP_P0_CLAIM1 is shown in Figure 2-32 and described in Table 2-66.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 2-65. CTRLMMR_WKUP_P0_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1104h	4300 3104h

Figure 2-32. CTRLMMR_WKUP_P0_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-66. CTRLMMR_WKUP_P0_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (1 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (1 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.33 CTRLMMR_WKUP_P0_CLAIM2 Register (Proxy0 Offset = 1108h; Proxy1 Offset = 3108h) [reset = 0h]

CTRLMMR_WKUP_P0_CLAIM2 is shown in Figure 2-33 and described in Table 2-68.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 2-67. CTRLMMR_WKUP_P0_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1108h	4300 3108h

Figure 2-33. CTRLMMR_WKUP_P0_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-68. CTRLMMR_WKUP_P0_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (2 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (2 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.34 CTRLMMR_WKUP_P0_CLAIM3 Register (Proxy0 Offset = 110Ch; Proxy1 Offset = 310Ch) [reset = 0h]

CTRLMMR_WKUP_P0_CLAIM3 is shown in Figure 2-34 and described in Table 2-70.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 2-69. CTRLMMR_WKUP_P0_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 110Ch	4300 310Ch

Figure 2-34. CTRLMMR_WKUP_P0_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-70. CTRLMMR_WKUP_P0_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (3 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (3 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.35 CTRLMMR_WKUP_P0_CLAIM4 Register (Proxy0 Offset = 1110h; Proxy1 Offset = 3110h) [reset = 0h]

CTRLMMR_WKUP_P0_CLAIM4 is shown in Figure 2-35 and described in Table 2-72.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 2-71. CTRLMMR_WKUP_P0_CLAIM4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1110h	4300 3110h

Figure 2-35. CTRLMMR_WKUP_P0_CLAIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-72. CTRLMMR_WKUP_P0_CLAIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (4 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (4 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.36 CTRLMMR_WKUP_P0_CLAIM5 Register (Proxy0 Offset = 1114h; Proxy1 Offset = 3114h) [reset = 0h]

CTRLMMR_WKUP_P0_CLAIM5 is shown in Figure 2-36 and described in Table 2-74.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 2-73. CTRLMMR_WKUP_P0_CLAIM5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1114h	4300 3114h

Figure 2-36. CTRLMMR_WKUP_P0_CLAIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-74. CTRLMMR_WKUP_P0_CLAIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (5 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (5 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.37 CTRLMMR_WKUP_P0_CLAIM6 Register (Proxy0 Offset = 1118h; Proxy1 Offset = 3118h) [reset = 0h]

CTRLMMR_WKUP_P0_CLAIM6 is shown in Figure 2-37 and described in Table 2-76.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 2-75. CTRLMMR_WKUP_P0_CLAIM6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 1118h	4300 3118h

Figure 2-37. CTRLMMR_WKUP_P0_CLAIM6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-76. CTRLMMR_WKUP_P0_CLAIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (6 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (6 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.38 CTRLMMR_WKUP_MAIN_PWR_CTRL Register (Proxy0 Offset = 4004h; Proxy1 Offset = 6004h) [reset = 1h]

CTRLMMR_WKUP_MAIN_PWR_CTRL is shown in Figure 2-38 and described in Table 2-78.

Return to Summary Table.

Controls power options for the MAIN voltage domain.

Table 2-77. CTRLMMR_WKUP_MAIN_PWR_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 4004h	4300 6004h

Figure 2-38. CTRLMMR_WKUP_MAIN_PWR_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							PWR_EN
R-0h							R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-78. CTRLMMR_WKUP_MAIN_PWR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	PWR_EN	R/W	1h	When set, drives the PMIC_POWER_EN1 output pin causing PMIC to turn on the MAIN voltage domain

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2.39 CTRLMMR_WKUP_GPIO_CTRL Register (Proxy0 Offset = 4020h; Proxy1 Offset = 6020h) [reset = 0h]

CTRLMMR_WKUP_GPIO_CTRL is shown in Figure 2-39 and described in Table 2-80.

Return to Summary Table.

Controls operation of the WKUP_GPIO module.

Table 2-79. CTRLMMR_WKUP_GPIO_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 4020h	4300 6020h

Figure 2-39. CTRLMMR_WKUP_GPIO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							WAKEN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-80. CTRLMMR_WKUP_GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	WAKEN	R/W	0h	Enables WKUP_GPIO wakeup event operation by controling the WKUP_GPIO LPSC clockstop_ack behavior. 0h - No WKUP_GPIO wakeup support. WKUP_GPIO vbus clock is gated on clkstop_ack from WKUP_GPIO to LPSC 1h - WKUP_GPIO wakeup enabled. WKUP_GPIO vbus clock is NOT gated on LPSC clockstop_req. WKUP_GPIO LPSC clkstop_ack input is driven by clkstop_req output.

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2.40 CTRLMMR_WKUP_I2C0_CTRL Register (Proxy0 Offset = 4030h; Proxy1 Offset = 6030h) [reset = 0h]

CTRLMMR_WKUP_I2C0_CTRL is shown in Figure 2-40 and described in Table 2-82.

Return to Summary Table.

Controls WKUP_I2C0 operation.

Table 2-81. CTRLMMR_WKUP_I2C0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 4030h	4300 6030h

Figure 2-40. CTRLMMR_WKUP_I2C0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							HS_MCS_EN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-82. CTRLMMR_WKUP_I2C0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HS_MCS_EN	R/W	0h	HS Mode master current source enable. When set, enables the current-source pull-up on the SCL output. Only one master on the I2C bus should enable SCL current sourcing.

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2.41 CTRLMMR_WKUP_DBOUNCE_CFG1 Register (Proxy0 Offset = 4084h; Proxy1 Offset = 6084h) [reset = 0h]

CTRLMMR_WKUP_DBOUNCE_CFG1 is shown in Figure 2-41 and described in Table 2-84.

Return to Summary Table.

Configures IO debounce selections.

Table 2-83. CTRLMMR_WKUP_DBOUNCE_CFG1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 4084h	4300 6084h

Figure 2-41. CTRLMMR_WKUP_DBOUNCE_CFG1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DB_CFG					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-84. CTRLMMR_WKUP_DBOUNCE_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with DEBOUNCE_SEL set to 1h.

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2.42 CTRLMMR_WKUP_DBOUNCE_CFG2 Register (Proxy0 Offset = 4088h; Proxy1 Offset = 6088h) [reset = 0h]

CTRLMMR_WKUP_DBOUNCE_CFG2 is shown in Figure 2-42 and described in Table 2-86.

Return to Summary Table.

Configures IO debounce selections.

Table 2-85. CTRLMMR_WKUP_DBOUNCE_CFG2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 4088h	4300 6088h

Figure 2-42. CTRLMMR_WKUP_DBOUNCE_CFG2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DB_CFG					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-86. CTRLMMR_WKUP_DBOUNCE_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with DEBOUNCE_SEL set to 2h.

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2.43 CTRLMMR_WKUP_DBOUNCE_CFG3 Register (Proxy0 Offset = 408Ch; Proxy1 Offset = 608Ch) [reset = 0h]

CTRLMMR_WKUP_DBOUNCE_CFG3 is shown in Figure 2-43 and described in Table 2-88.

Return to Summary Table.

Configures IO debounce selections.

Table 2-87. CTRLMMR_WKUP_DBOUNCE_CFG3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 408Ch	4300 608Ch

Figure 2-43. CTRLMMR_WKUP_DBOUNCE_CFG3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DB_CFG					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-88. CTRLMMR_WKUP_DBOUNCE_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with DEBOUNCE_SEL set to 3h.

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2.44 CTRLMMR_WKUP_DBOUNCE_CFG4 Register (Proxy0 Offset = 4090h; Proxy1 Offset = 6090h) [reset = 0h]

CTRLMMR_WKUP_DBOUNCE_CFG4 is shown in Figure 2-44 and described in Table 2-90.

Return to Summary Table.

Configures IO debounce selections.

Table 2-89. CTRLMMR_WKUP_DBOUNCE_CFG4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 4090h	4300 6090h

Figure 2-44. CTRLMMR_WKUP_DBOUNCE_CFG4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DB_CFG					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-90. CTRLMMR_WKUP_DBOUNCE_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with DEBOUNCE_SEL set to 4h.

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2.45 CTRLMMR_WKUP_DBOUNCE_CFG5 Register (Proxy0 Offset = 4094h; Proxy1 Offset = 6094h) [reset = 0h]

CTRLMMR_WKUP_DBOUNCE_CFG5 is shown in Figure 2-45 and described in Table 2-92.

Return to Summary Table.

Configures IO debounce selections.

Table 2-91. CTRLMMR_WKUP_DBOUNCE_CFG5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 4094h	4300 6094h

Figure 2-45. CTRLMMR_WKUP_DBOUNCE_CFG5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DB_CFG					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-92. CTRLMMR_WKUP_DBOUNCE_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with DEBOUNCE_SEL set to 5h.

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2.46 CTRLMMR_WKUP_DBOUNCE_CFG6 Register (Proxy0 Offset = 4098h; Proxy1 Offset = 6098h) [reset = 0h]

CTRLMMR_WKUP_DBOUNCE_CFG6 is shown in Figure 2-46 and described in Table 2-94.

Return to Summary Table.

Configures IO debounce selections.

Table 2-93. CTRLMMR_WKUP_DBOUNCE_CFG6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 4098h	4300 6098h

Figure 2-46. CTRLMMR_WKUP_DBOUNCE_CFG6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										DB_CFG					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-94. CTRLMMR_WKUP_DBOUNCE_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	DB_CFG	R/W	0h	Configures the debounce period used for I/Os with DEBOUNCE_SEL set to 6h.

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2.47 CTRLMMR_WKUP_LOCK1_KICK0 Register (Proxy0 Offset = 5008h; Proxy1 Offset = 7008h) [reset = 0h]

CTRLMMR_WKUP_LOCK1_KICK0 is shown in Figure 2-47 and described in Table 2-96.

Return to Summary Table.

Lower 32-bits of Partition1 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_WKUP_LOCK1_KICK1 with its key value before write-protected Partition 1 registers can be written.

Table 2-95. CTRLMMR_WKUP_LOCK1_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 5008h	4300 7008h

Figure 2-47. CTRLMMR_WKUP_LOCK1_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-96. CTRLMMR_WKUP_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition1 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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2.48 CTRLMMR_WKUP_LOCK1_KICK1 Register (Proxy0 Offset = 500Ch; Proxy1 Offset = 700Ch) [reset = 0h]

CTRLMMR_WKUP_LOCK1_KICK1 is shown in Figure 2-48 and described in Table 2-98.

Return to Summary Table.

Upper 32-bits of Partition 1 write lock key. This register must be written with the designated key value after a write to CTRLMMR_WKUP_LOCK1_KICK0 with its key value before write-protected Partition 1 registers can be written.

Table 2-97. CTRLMMR_WKUP_LOCK1_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 500Ch	4300 700Ch

Figure 2-48. CTRLMMR_WKUP_LOCK1_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-98. CTRLMMR_WKUP_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition1 registers

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2.49 CTRLMMR_WKUP_P1_CLAIM0 Register (Proxy0 Offset = 5100h; Proxy1 Offset = 7100h) [reset = 0h]

CTRLMMR_WKUP_P1_CLAIM0 is shown in Figure 2-49 and described in Table 2-100.

Return to Summary Table.

Claim bits for Partition 1 Registers.

Table 2-99. CTRLMMR_WKUP_P1_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 5100h	4300 7100h

Figure 2-49. CTRLMMR_WKUP_P1_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-100. CTRLMMR_WKUP_P1_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 4000h + (0 x 80h) + (b x 4h) and register Proxy1 address of: 6000h + (0 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.50 CTRLMMR_WKUP_P1_CLAIM1 Register (Proxy0 Offset = 5104h; Proxy1 Offset = 7104h) [reset = 0h]

CTRLMMR_WKUP_P1_CLAIM1 is shown in Figure 2-50 and described in Table 2-102.

Return to Summary Table.

Claim bits for Partition 1 Registers.

Table 2-101. CTRLMMR_WKUP_P1_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 5104h	4300 7104h

Figure 2-50. CTRLMMR_WKUP_P1_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-102. CTRLMMR_WKUP_P1_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 4000h + (1 x 80h) + (b x 4h) and register Proxy1 address of: 6000h + (1 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.51 CTRLMMR_WKUP_P1_CLAIM2 Register (Proxy0 Offset = 5108h; Proxy1 Offset = 7108h) [reset = 0h]

CTRLMMR_WKUP_P1_CLAIM2 is shown in Figure 2-51 and described in Table 2-104.

Return to Summary Table.

Claim bits for Partition 1 Registers.

Table 2-103. CTRLMMR_WKUP_P1_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 5108h	4300 7108h

Figure 2-51. CTRLMMR_WKUP_P1_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-104. CTRLMMR_WKUP_P1_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 4000h + (2 x 80h) + (b x 4h) and register Proxy1 address of: 6000h + (2 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.52 CTRLMMR_WKUP_MCU_OBSCLK_CTRL Register (Proxy0 Offset = 8000h; Proxy1 Offset = A000h) [reset = 0h]

CTRLMMR_WKUP_MCU_OBSCLK_CTRL is shown in Figure 2-52 and described in Table 2-106.

Return to Summary Table.

Controls which internal clock is made observable on the MCU_OBSCLK output pin.

Table 2-105. CTRLMMR_WKUP_MCU_OBSCLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8000h	4300 A000h

Figure 2-52. CTRLMMR_WKUP_MCU_OBSCLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							OUT_MUX_SEL
R-0h							R/W-0h
23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED				CLK_DIV			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				CLK_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-106. CTRLMMR_WKUP_MCU_OBSCLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	OUT_MUX_SEL	R/W	0h	MCU_OBSCLK pin output mux selection. Note, when WKUP_HFOSC0_CLK is selected (1h) the CLK_SEL field must be programmed to 1h. 0h - The output of the MCU_OBSCLK output divider is output on the pin 1h - WKUP_HFOSC0_CLK is output on the pin
23-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the OBSCLK divider value. This bit can be cleared but must not be set in the same write cycle in which the CLK_DIV value is changed.
15-12	RESERVED	R	0h	Reserved
11-8	CLK_DIV	R/W	0h	MCU_OBSCLK pin clock selection output divider Output clock is divided by CLK_DIV+1
7-4	RESERVED	R	0h	Reserved

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Table 2-106. CTRLMMR_WKUP_MCU_OBSCLK_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	CLK_SEL	R/W	0h	MCU_OBSCLK pin clock selection 0h - CLK_12M_RC 1h - "0" 2h - MCU_PLL0_HSDIV0_CLKOUT 3h - MCU_PLLCTL_OBSCLK 4h - MCU_PLL1_HSDIV1_CLKOUT 5h - MCU_PLL1_HSDIV2_CLKOUT 6h - MCU_PLL1_HSDIV3_CLKOUT 7h - MCU_PLL1_HSDIV4_CLKOUT 8h - MCU_PLL2_HSDIV0_CLKOUT 9h - CLK_32K Ah - MCU_PLL2_HSDIV1_CLKOUT Bh - MCU_PLL2_HSDIV2_CLKOUT Ch - MCU_PLL2_HSDIV3_CLKOUT Dh - MCU_PLL2_HSDIV4_CLKOUT Eh - WKUP_HFOSC0_CLKOUT Fh - WKUP_LFOSC0_CLKOUT

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2.53 CTRLMMR_WKUP_LFXOSC_CTRL Register (Proxy0 Offset = 8030h; Proxy1 Offset = A030h) [reset = 80h]

CTRLMMR_WKUP_LFXOSC_CTRL is shown in Figure 2-53 and described in Table 2-108.

Return to Summary Table.

Controls the operation of the low frequency oscillator.

Table 2-107. CTRLMMR_WKUP_LFXOSC_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8030h	4300 A030h

Figure 2-53. CTRLMMR_WKUP_LFXOSC_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
PD_C	RESERVED		BP_C	RESERVED			
R/W-1h	R-0h		R/W-0h	R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-108. CTRLMMR_WKUP_LFXOSC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	PD_C	R/W	1h	Oscillator powerdown control. When set, oscillator is disabled.
6-5	RESERVED	R	0h	Reserved
4	BP_C	R/W	0h	Oscillator bypass control. When set, oscillator is in bypass mode.
3-0	RESERVED	R	0h	Reserved

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2.54 HFOSC1_CTRL - Oscillator1 Control Register (Proxy0 Offset = 8014h; Proxy1 Offset = A014h) [reset = 80h]

HFOSC1_CTRL is described in Table 2-109.

Return to Summary Table.

Controls the operation of the low frequency oscillator.

Table 2-109. HFOSC1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	PD_C	R/W	1h	Oscillator powerdown control. When set, oscillator is disabled. Oscillator output is tristated if bp_c=0
6-5	RESERVED	R	0h	Reserved
4	BP_C	R/W	0h	Oscillator bypass control. When set oscillator is in bypass mode
3-0	RESERVED	R	0h	Reserved

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2.55 CTRLMMR_WKUP_LFXOSC_TRIM Register (Proxy0 Offset = 8034h; Proxy1 Offset = A034h) [reset = X]

CTRLMMR_WKUP_LFXOSC_TRIM is shown in Figure 2-54 and described in Table 2-111.

Return to Summary Table.

Provides frequency trimming for the low frequency oscillator module.

Table 2-110. CTRLMMR_WKUP_LFXOSC_TRIM Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8034h	4300 A034h

Figure 2-54. CTRLMMR_WKUP_LFXOSC_TRIM Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED		RESERVED		RESERVED	I_MULT		
R-0h		R/W-X		R-0h	R/W-X		

15	14	13	12	11	10	9	8
RESERVED		RESERVED					
R-0h		R/W-X					

7	6	5	4	3	2	1	0
RESERVED				RESERVED			
R/W-X				R/W-X			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-111. CTRLMMR_WKUP_LFXOSC_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21-20	RESERVED	R/W	X	Reserved
19	RESERVED	R	0h	Reserved
18-16	I_MULT	R/W	X	AGC AMP current multiplication gain 0h - 3x AMP_AGC IBIAS 1h - 4x AMP_AGC IBIAS 2h - 5x AMP_AGC IBIAS 3h - 6x AMP_AGC IBIAS 4h - 7x AMP_AGC IBIAS 5h - 8x AMP_AGC IBIAS 6h - 9x AMP_AGC IBIAS 7h - 10x AMP_AGC IBIAS
15-14	RESERVED	R	0h	Reserved
13-8	RESERVED	R/W	X	Reserved
7-4	RESERVED	R/W	X	Reserved
3-0	RESERVED	R/W	X	Reserved

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2.56 CTRLMMR_WKUP_MCU_PLL_CLKSEL Register (Proxy0 Offset = 8050h; Proxy1 Offset = A050h) [reset = 800000h]

CTRLMMR_WKUP_MCU_PLL_CLKSEL is shown in Figure 2-55 and described in Table 2-113.

Return to Summary Table.

Controls the clock source for MCU voltage domain PLL[2:0].

Table 2-112. CTRLMMR_WKUP_MCU_PLL_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8050h	4300 A050h

Figure 2-55. CTRLMMR_WKUP_MCU_PLL_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							CLKLOSS_SWTCH_EN
R-0h							R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-113. CTRLMMR_WKUP_MCU_PLL_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a mcu_reset_z for MCU PLL[2:0]. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when an MCU warm reset occurs and will keep MCU PLL[2:0] in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MCU PLL[2:0]_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-9	RESERVED	R	0h	Reserved
8	CLKLOSS_SWTCH_EN	R/W	0h	When set, enables automatic switching of MCU PLL[2:0] clock source to CLK_12M_RC if WKUP_HFOSC0 clock loss is detected

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Table 2-113. CTRLMMR_WKUP_MCU_PLL_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

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2.57 CTRLMMR_WKUP_PER_CLKSEL Register (Proxy0 Offset = 8060h; Proxy1 Offset = A060h) [reset = 0h]

CTRLMMR_WKUP_PER_CLKSEL is shown in Figure 2-56 and described in Table 2-115.

Return to Summary Table.

Controls the wakeup peripheral functional clock source. Allows the main oscillator to be used as the functional clock source for the WKUP_USART and WKUP_I2C when PLLs are powered down.

Table 2-114. CTRLMMR_WKUP_PER_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8060h	4300 A060h

Figure 2-56. CTRLMMR_WKUP_PER_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							MCUPLL_BYPASS
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-115. CTRLMMR_WKUP_PER_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MCUPLL_BYPASS	R/W	0h	Select the main oscillator clock rather than the PLL generated clock as the functional clock (PLL BYPASS mode). 0h - WKUP_I2C functional clock is MCU_PLL1_HSDIV3_CLKOUT WKUP_USART functional clock is MCU_PLL1_HSDIV3_CLKOUT or MAIN_PLL_HSDIV5_CLKOUT as selected by CTRLMMR_WKUP_USART_CLKSEL.clk_sel 1h - WKUP_I2C functional clock is WKUP_HFOSC0_CLKOUT WKUP_USART functional clock is WKUP_HFOSC0_CLKOUT

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2.58 CTRLMMR_WKUP_USART_CLKSEL Register (Proxy0 Offset = 8064h; Proxy1 Offset = A064h) [reset = 0h]

CTRLMMR_WKUP_USART_CLKSEL is shown in Figure 2-57 and described in Table 2-117.

Return to Summary Table.

Controls the functional clock source for WKUP_USART0.

Table 2-116. CTRLMMR_WKUP_USART_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8064h	4300 A064h

Figure 2-57. CTRLMMR_WKUP_USART_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-117. CTRLMMR_WKUP_USART_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	WKUP_USART0 FCLK selection 0h - MCU_PLL1_HSDIV3_CLKOUT 1h - MAIN_PLL_HSDIV5_CLKOUT

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2.59 CTRLMMR_WKUP_GPIO_CLKSEL Register (Proxy0 Offset = 8070h; Proxy1 Offset = A070h) [reset = 0h]

CTRLMMR_WKUP_GPIO_CLKSEL is shown in Figure 2-58 and described in Table 2-119.

Return to Summary Table.

Controls the functional clock source for WKUP_GPIO.

Table 2-118. CTRLMMR_WKUP_GPIO_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8070h	4300 A070h

Figure 2-58. CTRLMMR_WKUP_GPIO_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						WAKE_CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-119. CTRLMMR_WKUP_GPIO_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	WAKE_CLK_SEL	R/W	0h	WKUP_GPIO clock selection. Must be set to MCU_SYSCLK0/6 whenever WKUP_GPIO VBUS interface is enabled. Other clock source may be selected as a wake up clock for DeepSleep modes after WKUP_GPIO is gated off through LPSC. 0h - MCU_SYSCLK0 / 6 1h - MCU_SYSCLK0 / 6 2h - CLK_32K 3h - CLK_12M_RC

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2.60 CTRLMMR_WKUP_MAIN_PLL0_CLKSEL Register (Proxy0 Offset = 8080h; Proxy1 Offset = A080h) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL0_CLKSEL is shown in Figure 2-59 and described in Table 2-121.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL0.

Table 2-120. CTRLMMR_WKUP_MAIN_PLL0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8080h	4300 A080h

Figure 2-59. CTRLMMR_WKUP_MAIN_PLL0_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-121. CTRLMMR_WKUP_MAIN_PLL0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL0. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL0 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL0_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL0 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.61 CTRLMMR_WKUP_MAIN_PLL1_CLKSEL Register (Proxy0 Offset = 8084h; Proxy1 Offset = A084h) [reset = 0h]

CTRLMMR_WKUP_MAIN_PLL1_CLKSEL is shown in Figure 2-60 and described in Table 2-123.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL1.

Table 2-122. CTRLMMR_WKUP_MAIN_PLL1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8084h	4300 A084h

Figure 2-60. CTRLMMR_WKUP_MAIN_PLL1_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-0h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-123. CTRLMMR_WKUP_MAIN_PLL1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL1 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. This bit is cleared to 0h when a MAIN warm reset occurs which will cause MAIN PLL1 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL1 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL1 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.62 CTRLMMR_WKUP_MAIN_PLL2_CLKSEL Register (Proxy0 Offset = 8088h; Proxy1 Offset = A088h) [reset = 0h]

CTRLMMR_WKUP_MAIN_PLL2_CLKSEL is shown in Figure 2-61 and described in Table 2-125.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL2.

Table 2-124. CTRLMMR_WKUP_MAIN_PLL2_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8088h	4300 A088h

Figure 2-61. CTRLMMR_WKUP_MAIN_PLL2_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-0h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-125. CTRLMMR_WKUP_MAIN_PLL2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL2 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. This bit is cleared to 0h when a MAIN warm reset occurs which will cause MAIN PLL2 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL2 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL2 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.63 CTRLMMR_WKUP_MAIN_PLL3_CLKSEL Register (Proxy0 Offset = 808Ch; Proxy1 Offset = A08Ch) [reset = 0h]

CTRLMMR_WKUP_MAIN_PLL3_CLKSEL is shown in Figure 2-62 and described in Table 2-127.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL3.

Table 2-126. CTRLMMR_WKUP_MAIN_PLL3_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 808Ch	4300 A08Ch

Figure 2-62. CTRLMMR_WKUP_MAIN_PLL3_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
BYP_WARM_RST	RESERVED						
R/W-0h	R-0h						

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-127. CTRLMMR_WKUP_MAIN_PLL3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL3 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. This bit is cleared to 0h when a MAIN warm reset occurs which will cause MAIN PLL3 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL3 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL3 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.64 CTRLMMR_WKUP_MAIN_PLL4_CLKSEL Register (Proxy0 Offset = 8090h; Proxy1 Offset = A090h) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL4_CLKSEL is shown in Figure 2-63 and described in Table 2-129.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL4.

Table 2-128. CTRLMMR_WKUP_MAIN_PLL4_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8090h	4300 A090h

Figure 2-63. CTRLMMR_WKUP_MAIN_PLL4_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED			XREF_SEL	RESERVED			CLK_SEL
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-129. CTRLMMR_WKUP_MAIN_PLL4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL4. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL4 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL4_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-5	RESERVED	R	0h	Reserved
4	XREF_SEL	R/W	0h	Selects the alternate clock source for MAIN PLL4 0h - Use WKUP_HFOSC0_CLKOUT or HFOSC1 CLKOUT as selected by clk_sel bit 1h - Use EXT_REFCLK1

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Table 2-129. CTRLMMR_WKUP_MAIN_PLL4_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL4 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.65 CTRLMMR_WKUP_MAIN_PLL5_CLKSEL Register (Proxy0 Offset = 8094h; Proxy1 Offset = A094h) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL5_CLKSEL is shown in Figure 2-64 and described in Table 2-131.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL5.

Table 2-130. CTRLMMR_WKUP_MAIN_PLL5_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8094h	4300 A094h

Figure 2-64. CTRLMMR_WKUP_MAIN_PLL5_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-131. CTRLMMR_WKUP_MAIN_PLL5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL5. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL5 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL5_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL5 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.66 CTRLMMR_WKUP_MAIN_PLL6_CLKSEL Register (Proxy0 Offset = 8098h; Proxy1 Offset = A098h) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL6_CLKSEL is shown in Figure 2-65 and described in Table 2-133.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL6.

Table 2-132. CTRLMMR_WKUP_MAIN_PLL6_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8098h	4300 A098h

Figure 2-65. CTRLMMR_WKUP_MAIN_PLL6_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-133. CTRLMMR_WKUP_MAIN_PLL6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL6. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL6 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL6_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL6 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.67 CTRLMMR_WKUP_MAIN_PLL7_CLKSEL Register (Proxy0 Offset = 809Ch; Proxy1 Offset = A09Ch) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL7_CLKSEL is shown in Figure 2-66 and described in Table 2-135.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL7.

Table 2-134. CTRLMMR_WKUP_MAIN_PLL7_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 809Ch	4300 A09Ch

Figure 2-66. CTRLMMR_WKUP_MAIN_PLL7_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-135. CTRLMMR_WKUP_MAIN_PLL7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL7. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL7 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL7_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL7 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.68 CTRLMMR_WKUP_MAIN_PLL8_CLKSEL Register (Proxy0 Offset = 80A0h; Proxy1 Offset = A0A0h) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL8_CLKSEL is shown in Figure 2-67 and described in Table 2-137.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL8.

Table 2-136. CTRLMMR_WKUP_MAIN_PLL8_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80A0h	4300 A0A0h

Figure 2-67. CTRLMMR_WKUP_MAIN_PLL8_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-137. CTRLMMR_WKUP_MAIN_PLL8_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL8. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL8 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL8_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL8 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.69 CTRLMMR_WKUP_MAIN_PLL12_CLKSEL Register (Proxy0 Offset = 80B0h; Proxy1 Offset = A0B0h) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL12_CLKSEL is shown in Figure 2-68 and described in Table 2-139.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL12.

Table 2-138. CTRLMMR_WKUP_MAIN_PLL12_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80B0h	4300 A0B0h

Figure 2-68. CTRLMMR_WKUP_MAIN_PLL12_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-139. CTRLMMR_WKUP_MAIN_PLL12_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL12. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL12 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL12_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-1	RESERVED	R	0h	Reserved

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Table 2-139. CTRLMMR_WKUP_MAIN_PLL12_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL12 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.70 CTRLMMR_WKUP_MAIN_PLL13_CLKSEL Register (Proxy0 Offset = 80B4h; Proxy1 Offset = A0B4h) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL13_CLKSEL is shown in Figure 2-69 and described in Table 2-141.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL13.

Table 2-140. CTRLMMR_WKUP_MAIN_PLL13_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80B4h	4300 A0B4h

Figure 2-69. CTRLMMR_WKUP_MAIN_PLL13_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-141. CTRLMMR_WKUP_MAIN_PLL13_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL13. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL13 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL13_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-1	RESERVED	R	0h	Reserved

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Table 2-141. CTRLMMR_WKUP_MAIN_PLL13_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL13 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.71 CTRLMMR_WKUP_MAIN_PLL14_CLKSEL Register (Proxy0 Offset = 80B8h; Proxy1 Offset = A0B8h) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL14_CLKSEL is shown in Figure 2-70 and described in Table 2-143.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL14.

Table 2-142. CTRLMMR_WKUP_MAIN_PLL14_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80B8h	4300 A0B8h

Figure 2-70. CTRLMMR_WKUP_MAIN_PLL14_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-143. CTRLMMR_WKUP_MAIN_PLL14_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL14. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL14 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL14_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-1	RESERVED	R	0h	Reserved

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Table 2-143. CTRLMMR_WKUP_MAIN_PLL14_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL14 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.72 CTRLMMR_WKUP_MAIN_PLL15_CLKSEL Register (Proxy0 Offset = 80BCh; Proxy1 Offset = A0BCh) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL15_CLKSEL is shown in Figure 2-71 and described in Table 2-145.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL15.

Table 2-144. CTRLMMR_WKUP_MAIN_PLL15_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80BCh	4300 A0BCh

Figure 2-71. CTRLMMR_WKUP_MAIN_PLL15_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED			XREF_SEL	RESERVED			CLK_SEL
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-145. CTRLMMR_WKUP_MAIN_PLL15_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL15. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL15 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL15_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-5	RESERVED	R	0h	Reserved

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Table 2-145. CTRLMMR_WKUP_MAIN_PLL15_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	XREF_SEL	R/W	0h	Selects the alternate clock source for MAIN PLL15 0h - Use WKUP_HFOSC0_CLKOUT or HFOSC1 CLKOUT as selected by clk_sel bit 1h - Use EXT_REFCLK1
3-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL15 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.73 CTRLMMR_WKUP_MAIN_PLL16_CLKSEL Register (Proxy0 Offset = 80C0h; Proxy1 Offset = A0C0h) [reset = 0h]

CTRLMMR_WKUP_MAIN_PLL16_CLKSEL is shown in Figure 2-72 and described in Table 2-147.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL16.

Table 2-146. CTRLMMR_WKUP_MAIN_PLL16_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80C0h	4300 A0C0h

Figure 2-72. CTRLMMR_WKUP_MAIN_PLL16_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
BYP_WARM_RST	RESERVED						
R/W-0h	R-0h						

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-147. CTRLMMR_WKUP_MAIN_PLL16_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL16 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. This bit is cleared to 0h when a MAIN warm reset occurs which will cause MAIN PLL16 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL16 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL16 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.74 CTRLMMR_WKUP_MAIN_PLL17_CLKSEL Register (Proxy0 Offset = 80C4h; Proxy1 Offset = A0C4h) [reset = 0h]

CTRLMMR_WKUP_MAIN_PLL17_CLKSEL is shown in Figure 2-73 and described in Table 2-149.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL17.

Table 2-148. CTRLMMR_WKUP_MAIN_PLL17_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80C4h	4300 A0C4h

Figure 2-73. CTRLMMR_WKUP_MAIN_PLL17_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-0h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-149. CTRLMMR_WKUP_MAIN_PLL17_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL17 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. This bit is cleared to 0h when a MAIN warm reset occurs which will cause MAIN PLL17 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL17 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL17 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.75 CTRLMMR_WKUP_MAIN_PLL18_CLKSEL Register (Proxy0 Offset = 80C8h; Proxy1 Offset = A0C8h) [reset = 0h]

CTRLMMR_WKUP_MAIN_PLL18_CLKSEL is shown in Figure 2-74 and described in Table 2-151.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL18.

Table 2-150. CTRLMMR_WKUP_MAIN_PLL18_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80C8h	4300 A0C8h

Figure 2-74. CTRLMMR_WKUP_MAIN_PLL18_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-0h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-151. CTRLMMR_WKUP_MAIN_PLL18_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL18 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. This bit is cleared to 0h when a MAIN warm reset occurs which will cause MAIN PLL18 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL18 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL18 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.76 CTRLMMR_WKUP_MAIN_PLL19_CLKSEL Register (Proxy0 Offset = 80CCh; Proxy1 Offset = A0CCh) [reset = 0h]

CTRLMMR_WKUP_MAIN_PLL19_CLKSEL is shown in Figure 2-75 and described in Table 2-153.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL19.

Table 2-152. CTRLMMR_WKUP_MAIN_PLL19_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80CCh	4300 A0CCh

Figure 2-75. CTRLMMR_WKUP_MAIN_PLL19_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-0h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-153. CTRLMMR_WKUP_MAIN_PLL19_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL19 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. This bit is cleared to 0h when a MAIN warm reset occurs which will cause MAIN PLL19 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL19 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL19 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.77 CTRLMMR_WKUP_MAIN_PLL23_CLKSEL Register (Proxy0 Offset = 80DCh; Proxy1 Offset = A0DCh) [reset = 0h]

CTRLMMR_WKUP_MAIN_PLL23_CLKSEL is shown in Figure 2-76 and described in Table 2-155.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL23.

Table 2-154. CTRLMMR_WKUP_MAIN_PLL23_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80DCh	4300 A0DCh

Figure 2-76. CTRLMMR_WKUP_MAIN_PLL23_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
BYP_WARM_RST	RESERVED						
R/W-0h	R-0h						

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-155. CTRLMMR_WKUP_MAIN_PLL23_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override This bit has no effect on PLL operation as MAIN PLL23 is reset isolated and exit from bypass mode (in the case of a Thermal reset) is always hardware controlled.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	0h	PLL bypass mode after warm reset. This bit is cleared to 0h when a MAIN warm reset occurs which will cause MAIN PLL23 to exit bypass mode after reset exit. Setting this bit will have no effect on PLL behaviot. Because MAIN PLL23 is warm reset insensitive, bypass mode will only be entered (and exited) in the case of a Thermal reset event.
22-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL23 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.78 CTRLMMR_WKUP_MAIN_PLL24_CLKSEL Register (Proxy0 Offset = 80E0h; Proxy1 Offset = A0E0h) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL24_CLKSEL is shown in Figure 2-77 and described in Table 2-157.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL24.

Table 2-156. CTRLMMR_WKUP_MAIN_PLL24_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80E0h	4300 A0E0h

Figure 2-77. CTRLMMR_WKUP_MAIN_PLL24_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-157. CTRLMMR_WKUP_MAIN_PLL24_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL24. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL24 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL24_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-1	RESERVED	R	0h	Reserved

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Table 2-157. CTRLMMR_WKUP_MAIN_PLL24_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL24 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use MLBP_IO_CLK

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2.79 CTRLMMR_WKUP_MAIN_PLL25_CLKSEL Register (Proxy0 Offset = 80E4h; Proxy1 Offset = A0E4h) [reset = 800000h]

CTRLMMR_WKUP_MAIN_PLL25_CLKSEL is shown in Figure 2-78 and described in Table 2-159.

Return to Summary Table.

Controls the clock source for MAIN voltage domain PLL25.

Table 2-158. CTRLMMR_WKUP_MAIN_PLL25_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 80E4h	4300 A0E4h

Figure 2-78. CTRLMMR_WKUP_MAIN_PLL25_CLKSEL Register

31	30	29	28	27	26	25	24
BYPASS_SW_OVRD	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BYP_WARM_RST	RESERVED						
R/W-1h	R-0h						
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-159. CTRLMMR_WKUP_MAIN_PLL25_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_SW_OVRD	R/W	0h	PLL Bypass warm reset software override When set, enables software control of exit from bypass mode on a main_reset_z for MAIN PLL25. This bit must not be set until after the corresponding byp_warm_rst bit has been cleared or the PLL will immediately enter bypass mode.
30-24	RESERVED	R	0h	Reserved
23	BYP_WARM_RST	R/W	1h	PLL bypass mode after warm reset. This bit is only valid when bypass_sw_ovrd is set to 1h to enable bypass software override. This bit is set (1h) when a MAIN warm reset occurs and will keep MAIN PLL25 in bypass mode after reset exit until cleared by software. 0h - Exit bypass mode (based on MAIN PLL25_CTRL_bypass_en bit value) 1h - Maintain bypass mode.
22-1	RESERVED	R	0h	Reserved

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Table 2-159. CTRLMMR_WKUP_MAIN_PLL25_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLK_SEL	R/W	0h	Selects the clock source for MAIN PLL25 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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2.80 CTRLMMR_WKUP_MAIN_SYSCLK_CTRL Register (Proxy0 Offset = 8100h; Proxy1 Offset = A100h) [reset = 0h]

CTRLMMR_WKUP_MAIN_SYSCLK_CTRL is shown in Figure 2-79 and described in Table 2-161.

Return to Summary Table.

Controls clock gating of the MAIN PLL Controller SYSCLK outputs.

Table 2-160. CTRLMMR_WKUP_MAIN_SYSCLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8100h	4300 A100h

Figure 2-79. CTRLMMR_WKUP_MAIN_SYSCLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							SYSCLK1_GATE
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							SYSCLK0_GATE
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-161. CTRLMMR_WKUP_MAIN_SYSCLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	SYSCLK1_GATE	R/W	0h	When set, gates off SYSCLK1 output of the MAIN PLL Controller
7-1	RESERVED	R	0h	Reserved
0	SYSCLK0_GATE	R/W	0h	When set, gates off SYSCLK0 (MCLK1) output of the MAIN PLL Controller

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2.81 CTRLMMR_WKUP_MCU_SPI0_CLKSEL Register (Proxy0 Offset = 8110h; Proxy1 Offset = A110h) [reset = 0h]

CTRLMMR_WKUP_MCU_SPI0_CLKSEL is shown in Figure 2-80 and described in Table 2-163.

Return to Summary Table.

MCU_SPI0 clock control.

Table 2-162. CTRLMMR_WKUP_MCU_SPI0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8110h	4300 A110h

Figure 2-80. CTRLMMR_WKUP_MCU_SPI0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-163. CTRLMMR_WKUP_MCU_SPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

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2.82 CTRLMMR_WKUP_MCU_SPI1_CLKSEL Register (Proxy0 Offset = 8114h; Proxy1 Offset = A114h) [reset = 0h]

CTRLMMR_WKUP_MCU_SPI1_CLKSEL is shown in Figure 2-81 and described in Table 2-165.

Return to Summary Table.

MCU_SPI1 clock control.

Table 2-164. CTRLMMR_WKUP_MCU_SPI1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 8114h	4300 A114h

Figure 2-81. CTRLMMR_WKUP_MCU_SPI1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-165. CTRLMMR_WKUP_MCU_SPI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

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2.83 CTRLMMR_WKUP_LOCK2_KICK0 Register (Proxy0 Offset = 9008h; Proxy1 Offset = B008h) [reset = 0h]

CTRLMMR_WKUP_LOCK2_KICK0 is shown in Figure 2-82 and described in Table 2-167.

Return to Summary Table.

Lower 32-bits of Partition2 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_WKUP_LOCK2_KICK1 with its key value before write-protected Partition 2 registers can be written.

Table 2-166. CTRLMMR_WKUP_LOCK2_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 9008h	4300 B008h

Figure 2-82. CTRLMMR_WKUP_LOCK2_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-167. CTRLMMR_WKUP_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition2 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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2.84 CTRLMMR_WKUP_LOCK2_KICK1 Register (Proxy0 Offset = 900Ch; Proxy1 Offset = B00Ch) [reset = 0h]

CTRLMMR_WKUP_LOCK2_KICK1 is shown in Figure 2-83 and described in Table 2-169.

Return to Summary Table.

Upper 32-bits of Partition 2 write lock key. This register must be written with the designated key value after a write to CTRLMMR_WKUP_LOCK2_KICK0 with its key value before write-protected Partition 2 registers can be written.

Table 2-168. CTRLMMR_WKUP_LOCK2_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 900Ch	4300 B00Ch

Figure 2-83. CTRLMMR_WKUP_LOCK2_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-169. CTRLMMR_WKUP_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition2 registers

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2.85 CTRLMMR_WKUP_P2_CLAIM0 Register (Proxy0 Offset = 9100h; Proxy1 Offset = B100h) [reset = 0h]

CTRLMMR_WKUP_P2_CLAIM0 is shown in Figure 2-84 and described in Table 2-171.

Return to Summary Table.

Claim bits for Partition 2 Registers.

Table 2-170. CTRLMMR_WKUP_P2_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 9100h	4300 B100h

Figure 2-84. CTRLMMR_WKUP_P2_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-171. CTRLMMR_WKUP_P2_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 8000h + (0 x 80h) + (b x 4h) and register Proxy1 address of: A000h + (0 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.86 CTRLMMR_WKUP_P2_CLAIM1 Register (Proxy0 Offset = 9104h; Proxy1 Offset = B104h) [reset = 0h]

CTRLMMR_WKUP_P2_CLAIM1 is shown in Figure 2-85 and described in Table 2-173.

Return to Summary Table.

Claim bits for Partition 2 Registers.

Table 2-172. CTRLMMR_WKUP_P2_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 9104h	4300 B104h

Figure 2-85. CTRLMMR_WKUP_P2_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-173. CTRLMMR_WKUP_P2_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 8000h + (1 x 80h) + (b x 4h) and register Proxy1 address of: A000h + (1 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.87 CTRLMMR_WKUP_P2_CLAIM2 Register (Proxy0 Offset = 9108h; Proxy1 Offset = B108h) [reset = 0h]

CTRLMMR_WKUP_P2_CLAIM2 is shown in Figure 2-86 and described in Table 2-175.

Return to Summary Table.

Claim bits for Partition 2 Registers.

Table 2-174. CTRLMMR_WKUP_P2_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 9108h	4300 B108h

Figure 2-86. CTRLMMR_WKUP_P2_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-175. CTRLMMR_WKUP_P2_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 8000h + (2 x 80h) + (b x 4h) and register Proxy1 address of: A000h + (2 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.88 CTRLMMR_WKUP_DMSC_LBIST_SIG Register (Proxy0 Offset = C280h; Proxy1 Offset = E280h) [reset = X]

CTRLMMR_WKUP_DMSC_LBIST_SIG is shown in Figure 2-87 and described in Table 2-177.

Return to Summary Table.

Contains expected MISR output value.

Table 2-176. CTRLMMR_WKUP_DMSC_LBIST_SIG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 C280h	4300 E280h

Figure 2-87. CTRLMMR_WKUP_DMSC_LBIST_SIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_SIG																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 2-177. CTRLMMR_WKUP_DMSC_LBIST_SIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_SIG	R	X	MISR signature

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2.89 CTRLMMR_WKUP_POST_STAT Register (Proxy0 Offset = C2C0h; Proxy1 Offset = E2C0h) [reset = X]

CTRLMMR_WKUP_POST_STAT is shown in Figure 2-88 and described in Table 2-179.

Return to Summary Table.

Contains the result of power-on self tests.

Table 2-178. CTRLMMR_WKUP_POST_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 C2C0h	4300 E2C0h

Figure 2-88. CTRLMMR_WKUP_POST_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED						FPOST_PLL_LOCK_TIMEOUT	FPOST_PLL_LOCKLOSS
R-0h						R-X	R-X

15	14	13	12	11	10	9	8
POST_MCU_PBIST_FAIL	RESERVED					POST_MCU_PBIST_TIMEOUT	POST_MCU_PBIST_DONE
R-X	R-0h					R-X	R-X

7	6	5	4	3	2	1	0
RESERVED		POST_MCU_LBIST_TIMEOUT	POST_DMSC_LBIST_TIMEOUT	RESERVED		POST_MCU_LBIST_DONE	POST_DMSC_LBIST_DONE
R-0h		R-X	R-X	R-0h		R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-179. CTRLMMR_WKUP_POST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17	FPOST_PLL_LOCK_TIMEOUT	R	X	Indicates PLL lock timeout for Fast POST mode operation. 0h - PLLs locked, Fast POST mode was entered 1h - PLLs lock timeout occurred. Slow speed POST was performed
16	FPOST_PLL_LOCKLOSS	R	X	Indicates if PLL lock was lost during POST 0h - No PLL lock loss. Fast POST was executed 1h - PLL lock was lost. POST was terminated
15	POST_MCU_PBIST_FAIL	R	X	MCU PBIST failed
14-10	RESERVED	R	0h	Reserved
9	POST_MCU_PBIST_TIMEOUT	R	X	MCU PBIST timed out
8	POST_MCU_PBIST_DONE	R	X	MCU PBIST done
7-6	RESERVED	R	0h	Reserved
5	POST_MCU_LBIST_TIMEOUT	R	X	MCU LBIST timed out

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Table 2-179. CTRLMMR_WKUP_POST_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	POST_DMSC_LBIST_TIMEOUT	R	X	DMSC LBIST timed out
3-2	RESERVED	R	0h	Reserved
1	POST_MCU_LBIST_DONE	R	X	MCU LBIST done
0	POST_DMSC_LBIST_DONE	R	X	DMSC LBIST done

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2.90 CTRLMMR_WKUP_FUSE_CRC_STAT Register (Proxy0 Offset = C320h; Proxy1 Offset = E320h) [reset = X]

CTRLMMR_WKUP_FUSE_CRC_STAT is shown in Figure 2-89 and described in Table 2-181.

Return to Summary Table.

Indicates status of fuse chain CRC.

Table 2-180. CTRLMMR_WKUP_FUSE_CRC_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 C320h	4300 E320h

Figure 2-89. CTRLMMR_WKUP_FUSE_CRC_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
CRC_ERR_7	CRC_ERR_6	RESERVED	CRC_ERR_4	CRC_ERR_3	CRC_ERR_2	CRC_ERR_1	RESERVED
R-X	R-X	R-0h	R-X	R-X	R-X	R-X	R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 2-181. CTRLMMR_WKUP_FUSE_CRC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	CRC_ERR_7	R	X	Indicates eFuse CRC error on chain 7
6	CRC_ERR_6	R	X	Indicates eFuse CRC error on chain 6
5	RESERVED	R	0h	Reserved
4	CRC_ERR_4	R	X	Indicates eFuse CRC error on chain 4
3	CRC_ERR_3	R	X	Indicates eFuse CRC error on chain 3
2	CRC_ERR_2	R	X	Indicates eFuse CRC error on chain 2
1	CRC_ERR_1	R	X	Indicates eFuse CRC error on chain 1
0	RESERVED	R	0h	Reserved

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2.91 CTRLMMR_WKUP_LOCK3_KICK0 Register (Proxy0 Offset = D008h; Proxy1 Offset = F008h) [reset = 0h]

CTRLMMR_WKUP_LOCK3_KICK0 is shown in Figure 2-90 and described in Table 2-183.

Return to Summary Table.

Lower 32-bits of Partition3 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_WKUP_LOCK3_KICK1 with its key value before write-protected Partition 3 registers can be written.

Table 2-182. CTRLMMR_WKUP_LOCK3_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 D008h	4300 F008h

Figure 2-90. CTRLMMR_WKUP_LOCK3_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-183. CTRLMMR_WKUP_LOCK3_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition3 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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2.92 CTRLMMR_WKUP_LOCK3_KICK1 Register (Proxy0 Offset = D00Ch; Proxy1 Offset = F00Ch) [reset = 0h]

CTRLMMR_WKUP_LOCK3_KICK1 is shown in Figure 2-91 and described in Table 2-185.

Return to Summary Table.

Upper 32-bits of Partition 3 write lock key. This register must be written with the designated key value after a write to CTRLMMR_WKUP_LOCK3_KICK0 with its key value before write-protected Partition 3 registers can be written.

Table 2-184. CTRLMMR_WKUP_LOCK3_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 D00Ch	4300 F00Ch

Figure 2-91. CTRLMMR_WKUP_LOCK3_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-185. CTRLMMR_WKUP_LOCK3_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition3 registers

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2.93 CTRLMMR_WKUP_P3_CLAIM0 Register (Proxy0 Offset = D100h; Proxy1 Offset = F100h) [reset = 0h]

CTRLMMR_WKUP_P3_CLAIM0 is shown in Figure 2-92 and described in Table 2-187.

Return to Summary Table.

Claim bits for Partition 3 Registers.

Table 2-186. CTRLMMR_WKUP_P3_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 D100h	4300 F100h

Figure 2-92. CTRLMMR_WKUP_P3_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-187. CTRLMMR_WKUP_P3_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (0 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (0 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.94 CTRLMMR_WKUP_P3_CLAIM1 Register (Proxy0 Offset = D104h; Proxy1 Offset = F104h) [reset = 0h]

CTRLMMR_WKUP_P3_CLAIM1 is shown in Figure 2-93 and described in Table 2-189.

Return to Summary Table.

Claim bits for Partition 3 Registers.

Table 2-188. CTRLMMR_WKUP_P3_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 D104h	4300 F104h

Figure 2-93. CTRLMMR_WKUP_P3_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-189. CTRLMMR_WKUP_P3_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (1 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (1 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.95 CTRLMMR_WKUP_P3_CLAIM2 Register (Proxy0 Offset = D108h; Proxy1 Offset = F108h) [reset = 0h]

CTRLMMR_WKUP_P3_CLAIM2 is shown in Figure 2-94 and described in Table 2-191.

Return to Summary Table.

Claim bits for Partition 3 Registers.

Table 2-190. CTRLMMR_WKUP_P3_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 D108h	4300 F108h

Figure 2-94. CTRLMMR_WKUP_P3_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-191. CTRLMMR_WKUP_P3_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (2 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (2 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.96 CTRLMMR_WKUP_P3_CLAIM3 Register (Proxy0 Offset = D10Ch; Proxy1 Offset = F10Ch) [reset = 0h]

CTRLMMR_WKUP_P3_CLAIM3 is shown in Figure 2-95 and described in Table 2-193.

Return to Summary Table.

Claim bits for Partition 3 Registers.

Table 2-192. CTRLMMR_WKUP_P3_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 D10Ch	4300 F10Ch

Figure 2-95. CTRLMMR_WKUP_P3_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-193. CTRLMMR_WKUP_P3_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (3 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (3 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.97 CTRLMMR_WKUP_P3_CLAIM4 Register (Proxy0 Offset = D110h; Proxy1 Offset = F110h) [reset = 0h]

CTRLMMR_WKUP_P3_CLAIM4 is shown in Figure 2-96 and described in Table 2-195.

Return to Summary Table.

Claim bits for Partition 3 Registers.

Table 2-194. CTRLMMR_WKUP_P3_CLAIM4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 D110h	4300 F110h

Figure 2-96. CTRLMMR_WKUP_P3_CLAIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-195. CTRLMMR_WKUP_P3_CLAIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (4 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (4 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.98 CTRLMMR_WKUP_P3_CLAIM5 Register (Proxy0 Offset = D114h; Proxy1 Offset = F114h) [reset = 0h]

CTRLMMR_WKUP_P3_CLAIM5 is shown in Figure 2-97 and described in Table 2-197.

Return to Summary Table.

Claim bits for Partition 3 Registers.

Table 2-196. CTRLMMR_WKUP_P3_CLAIM5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 D114h	4300 F114h

Figure 2-97. CTRLMMR_WKUP_P3_CLAIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-197. CTRLMMR_WKUP_P3_CLAIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (5 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (5 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.99 CTRLMMR_WKUP_P3_CLAIM6 Register (Proxy0 Offset = D118h; Proxy1 Offset = F118h) [reset = 0h]

CTRLMMR_WKUP_P3_CLAIM6 is shown in Figure 2-98 and described in Table 2-199.

Return to Summary Table.

Claim bits for Partition 3 Registers.

Table 2-198. CTRLMMR_WKUP_P3_CLAIM6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4300 D118h	4300 F118h

Figure 2-98. CTRLMMR_WKUP_P3_CLAIM6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-199. CTRLMMR_WKUP_P3_CLAIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (6 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (6 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.100 CTRLMMR_WKUP_POR_CTRL Register (Proxy0 Offset = 18000h; Proxy1 Offset = 1A000h) [reset = 10h]

CTRLMMR_WKUP_POR_CTRL is shown in Figure 2-99 and described in Table 2-201.

Return to Summary Table.

Configures POR module reset behavior.

Table 2-200. CTRLMMR_WKUP_POR_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8000h	4301 A000h

Figure 2-99. CTRLMMR_WKUP_POR_CTRL Register

31	30	29	28	27	26	25	24
RESERVED		OVRD_SET5	OVRD_SET4	OVRD_SET3	OVRD_SET2	OVRD_SET1	OVRD_SET0
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
RESERVED		OVRD5	OVRD4	OVRD3	OVRD2	OVRD1	OVRD0
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
TRIM_SEL	RESERVED		MASK_HHV	RESERVED			
R/W-0h	R-0h		R/W-1h	R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-201. CTRLMMR_WKUP_POR_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29	OVRD_SET5	R/W	0h	Reserved override set
28	OVRD_SET4	R/W	0h	POKLVB override set
27	OVRD_SET3	R/W	0h	POKLVA override set
26	OVRD_SET2	R/W	0h	POKHV override set
25	OVRD_SET1	R/W	0h	BGOK override set
24	OVRD_SET0	R/W	0h	PORHV override set
23-22	RESERVED	R	0h	Reserved
21	OVRD5	R/W	0h	Reserved override enable
20	OVRD4	R/W	0h	POKLVB override enable
19	OVRD3	R/W	0h	POKLVA override enable
18	OVRD2	R/W	0h	POKHV override enable
17	OVRD1	R/W	0h	BGOK override enable
16	OVRD0	R/W	0h	PORHV override enable
15-8	RESERVED	R	0h	Reserved

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Table 2-201. CTRLMMR_WKUP_POR_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	TRIM_SEL	R/W	0h	POR Trim Select 0h - Trim selections for Bandgap and POKs come from HHV defaults 1h - Trim selections for Bandgap and POKs come from CTRLMMR_WKUP_POR_BANDGAP_CTRL and POR_POKxxx_CTRL registers
6-5	RESERVED	R	0h	Reserved
4	MASK_HHV	R/W	1h	Mask HHV/SOC_PORz outputs when applying new trim values
3-0	RESERVED	R	0h	Reserved

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2.101 CTRLMMR_WKUP_POR_STAT Register (Proxy0 Offset = 18004h; Proxy1 Offset = 1A004h) [reset = X]

CTRLMMR_WKUP_POR_STAT is shown in Figure 2-100 and described in Table 2-203.

Return to Summary Table.

Shows POR module status.

Table 2-202. CTRLMMR_WKUP_POR_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8004h	4301 A004h

Figure 2-100. CTRLMMR_WKUP_POR_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							BGOK
R-0h							R-X
7	6	5	4	3	2	1	0
RESERVED			SOC_POR	RESERVED			
R-0h			R-X	R-0h			

LEGEND: R = Read Only; *-n* = value after reset

Table 2-203. CTRLMMR_WKUP_POR_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	BGOK	R	X	Bandgap OK status
7-5	RESERVED	R	0h	Reserved
4	SOC_POR	R	X	POR module status 0h - Module is in functional mode 1h - Module is in reset mode
3-0	RESERVED	R	0h	Reserved

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2.102 CTRLMMR_WKUP_PRG0_CTRL Register (Proxy0 Offset = 18008h; Proxy1 Offset = 1A008h) [reset = 34323432h]

CTRLMMR_WKUP_PRG0_CTRL is shown in Figure 2-101 and described in Table 2-205.

Return to Summary Table.

Configures the WKUP domain PRG0 controller.

Table 2-204. CTRLMMR_WKUP_PRG0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8008h	4301 A008h

Figure 2-101. CTRLMMR_WKUP_PRG0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	
R/W-0h	R-0h	R/W-1h	R/W-1h	R-0h	R/W-1h	R-0h	

23	22	21	20	19	18	17	16
RESERVED		RESERVED	RESERVED	RESERVED		RESERVED	RESERVED
R-0h		R/W-1h	R/W-1h	R-0h		R/W-1h	R-0h

15	14	13	12	11	10	9	8
POK_EN_SEL	RESERVED	POK_VDDR_MCU_OV_EN	POK_VDDSHV_WKUP_GEN_OV_EN	RESERVED	POK_VDD_MCU_OV_EN	RESERVED	
R/W-0h	R-0h	R/W-1h	R/W-1h	R-0h	R/W-1h	R-0h	

7	6	5	4	3	2	1	0
RESERVED		POK_VDDR_MCU_UV_EN	POK_VDDSHV_WKUP_GEN_UV_EN	RESERVED		POK_VDDA_PMIC_IN_EN	RESERVED
R-0h		R/W-1h	R/W-1h	R-0h		R/W-1h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-205. CTRLMMR_WKUP_PRG0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30	RESERVED	R	0h	Reserved
29	RESERVED	R/W	1h	Reserved
28	RESERVED	R/W	1h	Reserved
27	RESERVED	R	0h	Reserved
26	RESERVED	R/W	1h	Reserved
25-22	RESERVED	R	0h	Reserved
21	RESERVED	R/W	1h	Reserved
20	RESERVED	R/W	1h	Reserved
19-18	RESERVED	R	0h	Reserved
17	RESERVED	R/W	1h	Reserved
16	RESERVED	R	0h	Reserved

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Table 2-205. CTRLMMR_WKUP_PRG0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	POK_EN_SEL	R/W	0h	Select POK enable source 0h - POK enables come from hardware tie-offs 1h - POK enables come from CTRLMMR_WKUP_PRG0_CTRL register
14	RESERVED	R	0h	Reserved
13	POK_VDDR_MCU_OV_EN	R/W	1h	Enable VDDAR_MCU overvoltage POK detection. 0h - POK detection disabled 1h - POK detection enabled
12	POK_VDDSHV_WKUP_GEN_OV_EN	R/W	1h	Enable VDDSHV0_MCU overvoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
11	RESERVED	R	0h	Reserved
10	POK_VDD_MCU_OV_EN	R/W	1h	Enable VDD_MCU overvoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
9-6	RESERVED	R	0h	Reserved
5	POK_VDDR_MCU_UV_EN	R/W	1h	Enable VDDAR_MCU undervoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
4	POK_VDDSHV_WKUP_GEN_UV_EN	R/W	1h	Enable VDDSHV0_MCU undervoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
3-2	RESERVED	R	0h	Reserved
1	POK_VDDA_PMIC_IN_EN	R/W	1h	Enable VDDA_PMIC_IN POK detection 0h - POK detection disabled 1h - POK detection enabled
0	RESERVED	R	0h	Reserved

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2.103 CTRLMMR_WKUP_PRG0_STAT Register (Proxy0 Offset = 1800Ch; Proxy1 Offset = 1A00Ch) [reset = X]

CTRLMMR_WKUP_PRG0_STAT is shown in Figure 2-102 and described in Table 2-207.

Return to Summary Table.

Provides WKUP domain PRG0 controller status and status clear control.

Table 2-206. CTRLMMR_WKUP_PRG0_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 800Ch	4301 A00Ch

Figure 2-102. CTRLMMR_WKUP_PRG0_STAT Register

31	30	29	28	27	26	25	24
POK_CLR	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		POK_VDDR_MCU_OV	POK_VDDSHV_WKUP_GEN_OV	RESERVED	POK_VDD_MCU_OV	RESERVED	
R-0h		R-X	R-X	R-0h	R-X	R-0h	

7	6	5	4	3	2	1	0
RESERVED		POK_VDDR_MCU_UV	POK_VDDSHV_WKUP_GEN_UV	RESERVED		POK_VDDA_PMIC_IN	RESERVED
R-0h		R-X	R-X	R-0h		R-X	R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-207. CTRLMMR_WKUP_PRG0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_CLR	R/W	0h	When set, resets pgood sticky bits for VDDA_PMIC_IN, VDDR_MCU, VDDSHV_WKUP_GENERAL, and VDD_MCU_OV voltage POK detection.
30-14	RESERVED	R	0h	Reserved
13	POK_VDDR_MCU_OV	R	X	VDDAR_MCU overvoltage POK 0h - Voltage above threshold 1h - Voltage good
12	POK_VDDSHV_WKUP_GEN_OV	R	X	VDDSHV0_MCU overvoltage POK 0h - Voltage above threshold 1h - Voltage good
11	RESERVED	R	0h	Reserved
10	POK_VDD_MCU_OV	R	X	VDD_MCU overvoltage POK 0h - Voltage above threshold 1h - Voltage good
9-6	RESERVED	R	0h	Reserved

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Table 2-207. CTRLMMR_WKUP_PRG0_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	POK_VDDR_MCU_UV	R	X	VDDAR_MCU undervoltage POK 0h - Voltage below threshold 1h - Voltage good
4	POK_VDDSHV_WKUP_GEN_UV	R	X	VDDSHV0_MCU undervoltage POK 0h - Voltage below threshold 1h - Voltage good
3-2	RESERVED	R	0h	Reserved
1	POK_VDDA_PMIC_IN	R	X	VDDA_PMIC_IN POK 0h - Voltage below threshold 1h - Voltage good
0	RESERVED	R	0h	Reserved

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2.104 CTRLMMR_WKUP_POK_VDDA_PMIC_IN_CTRL Register (Proxy0 Offset = 18010h; Proxy1 Offset = 1A010h) [reset = 80000000h]

CTRLMMR_WKUP_POK_VDDA_PMIC_IN_CTRL is shown in Figure 2-103 and described in Table 2-209.

Return to Summary Table.

Controls operation of the VDDA_PMIC_IN POK module.

Table 2-208. CTRLMMR_WKUP_POK_VDDA_PMIC_IN_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8010h	4301 A010h

Figure 2-103. CTRLMMR_WKUP_POK_VDDA_PMIC_IN_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							OVER_VOLT_DET
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-209. CTRLMMR_WKUP_POK_VDDA_PMIC_IN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-1	RESERVED	R	0h	Reserved
0	OVER_VOLT_DET	R/W	0h	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection

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2.105 CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_UV_CTRL Register (Proxy0 Offset = 18014h; Proxy1 Offset = 1A014h) [reset = X]

CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_UV_CTRL is shown in Figure 2-104 and described in Table 2-211.

Return to Summary Table.

Controls operation of the VDDSHV_WKUP_GENERAL undervoltage POK module.

Table 2-210. CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_UV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8014h	4301 A014h

Figure 2-104. CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-211. CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.106 CTRLMMR_WKUP_POK_VDDR_MCU_UV_CTRL Register (Proxy0 Offset = 18018h; Proxy1 Offset = 1A018h) [reset = X]

CTRLMMR_WKUP_POK_VDDR_MCU_UV_CTRL is shown in Figure 2-105 and described in Table 2-213.

Return to Summary Table.

Controls operation of the VDDR_MCU undervoltage POK module.

Table 2-212. CTRLMMR_WKUP_POK_VDDR_MCU_UV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8018h	4301 A018h

Figure 2-105. CTRLMMR_WKUP_POK_VDDR_MCU_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-213. CTRLMMR_WKUP_POK_VDDR_MCU_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.107 CTRLMMR_WKUP_POK_VDD_MCU_OV_CTRL Register (Proxy0 Offset = 18020h; Proxy1 Offset = 1A020h) [reset = X]

CTRLMMR_WKUP_POK_VDD_MCU_OV_CTRL is shown in Figure 2-106 and described in Table 2-215.

Return to Summary Table.

Controls operation of the VDD_MCU overvoltage POK module.

Table 2-214. CTRLMMR_WKUP_POK_VDD_MCU_OV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8020h	4301 A020h

Figure 2-106. CTRLMMR_WKUP_POK_VDD_MCU_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-215. CTRLMMR_WKUP_POK_VDD_MCU_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.108 CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_OV_CTRL Register (Proxy0 Offset = 18024h; Proxy1 Offset = 1A024h) [reset = X]

CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_OV_CTRL is shown in Figure 2-107 and described in Table 2-217.

Return to Summary Table.

Controls operation of the VDDSHV_WKUP_GENERAL overvoltage POK module.

Table 2-216. CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_OV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8024h	4301 A024h

Figure 2-107. CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-217. CTRLMMR_WKUP_POK_VDDSHV_WKUP_GEN_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.109 CTRLMMR_WKUP_POK_VDDR_MCU_OV_CTRL Register (Proxy0 Offset = 18028h; Proxy1 Offset = 1A028h) [reset = X]

CTRLMMR_WKUP_POK_VDDR_MCU_OV_CTRL is shown in Figure 2-108 and described in Table 2-219.

Return to Summary Table.

Controls operation of the VDDR_MCU overvoltage POK module.

Table 2-218. CTRLMMR_WKUP_POK_VDDR_MCU_OV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8028h	4301 A028h

Figure 2-108. CTRLMMR_WKUP_POK_VDDR_MCU_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-219. CTRLMMR_WKUP_POK_VDDR_MCU_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.110 CTRLMMR_WKUP_PRG1_CTRL Register (Proxy0 Offset = 18058h; Proxy1 Offset = 1A058h) [reset = 1030103h]

CTRLMMR_WKUP_PRG1_CTRL is shown in Figure 2-109 and described in Table 2-221.

Return to Summary Table.

Configures the WKUP domain PRG1 controller.

Table 2-220. CTRLMMR_WKUP_PRG1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8058h	4301 A058h

Figure 2-109. CTRLMMR_WKUP_PRG1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED						RESERVED
R/W-0h	R-0h						R/W-1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED						RESERVED	RESERVED
R-0h						R/W-1h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POK_EN_SEL	RESERVED						POKHV_OV_EN
R/W-0h	R-0h						R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						POKLV_UV_EN	POKHV_UV_EN
R-0h						R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-221. CTRLMMR_WKUP_PRG1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30-25	RESERVED	R	0h	Reserved
24	RESERVED	R/W	1h	Reserved
23-18	RESERVED	R	0h	Reserved
17	RESERVED	R/W	1h	Reserved
16	RESERVED	R/W	1h	Reserved
15	POK_EN_SEL	R/W	0h	Select POK enable source 0h - POK enables come from hardware tie-offs 1h - POK enables come from CTRLMMR_WKUP_PRG1_CTRL register
14-9	RESERVED	R	0h	Reserved
8	POKHV_OV_EN	R/W	1h	Enable 1.8V VDDA_MCU overvoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
7-2	RESERVED	R	0h	Reserved

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Table 2-221. CTRLMMR_WKUP_PRG1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	POKLV_UV_EN	R/W	1h	Enable VDD_MCU undervoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
0	POKHV_UV_EN	R/W	1h	Enable 1.8V VDDA_MCU undervoltage POK detection 0h - POK detection disabled 1h - POK detection enabled

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2.111 CTRLMMR_WKUP_PRG1_STAT Register (Proxy0 Offset = 1805Ch; Proxy1 Offset = 1A05Ch) [reset = X]

CTRLMMR_WKUP_PRG1_STAT is shown in Figure 2-110 and described in Table 2-223.

Return to Summary Table.

Provides WKUP domain PRG1 controller status and status clear control.

Table 2-222. CTRLMMR_WKUP_PRG1_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 805Ch	4301 A05Ch

Figure 2-110. CTRLMMR_WKUP_PRG1_STAT Register

31	30	29	28	27	26	25	24
POK_CLR	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							POKHV_OV
R-0h							R-X

7	6	5	4	3	2	1	0
RESERVED						POKLV_UV	POKHV_UV
R-0h						R-X	R-X

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-223. CTRLMMR_WKUP_PRG1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_CLR	R/W	0h	When set, resets pgood sticky bits for 1.8V VDDA_MCU and VDD_MCU_UV voltage POK detection.
30-9	RESERVED	R	0h	Reserved
8	POKHV_OV	R	X	1.8V VDDA_MCU overvoltage POK 0h - Voltage above threshold 1h - Voltage good
7-2	RESERVED	R	0h	Reserved
1	POKLV_UV	R	X	VDD_MCU under voltage POK 0h - Voltage below threshold 1h - Voltage good
0	POKHV_UV	R	X	1.8V VDDA_MCU undervoltage POK 0h - Voltage below threshold 1h - Voltage good

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2.112 CTRLMMR_WKUP_MAIN_VDOM_CTRL Register (Proxy0 Offset = 18070h; Proxy1 Offset = 1A070h) [reset = 0h]

CTRLMMR_WKUP_MAIN_VDOM_CTRL is shown in Figure 2-111 and described in Table 2-225.

Return to Summary Table.

Provides MAIN voltage domain isolation for deep sleep operation.

Table 2-224. CTRLMMR_WKUP_MAIN_VDOM_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8070h	4301 A070h

Figure 2-111. CTRLMMR_WKUP_MAIN_VDOM_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							MAIN_VD_OFF
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-225. CTRLMMR_WKUP_MAIN_VDOM_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MAIN_VD_OFF	R/W	0h	MAIN deep sleep isolation enable. This bit should be set prior to powering off the MAIN voltage domain to ensure proper signal isolation.

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2.113 CTRLMMR_WKUP_POR_POKHV_UV_CTRL Register (Proxy0 Offset = 18080h; Proxy1 Offset = 1A080h) [reset = X]

CTRLMMR_WKUP_POR_POKHV_UV_CTRL is shown in Figure 2-112 and described in Table 2-227.

Return to Summary Table.

Controls operation of the 1.8V VDDA_POR_WKUP undervoltage POK within the POR.

Table 2-226. CTRLMMR_WKUP_POR_POKHV_UV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8080h	4301 A080h

Figure 2-112. CTRLMMR_WKUP_POR_POKHV_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-227. CTRLMMR_WKUP_POR_POKHV_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.114 CTRLMMR_WKUP_POR_POKLV_UV_CTRL Register (Proxy0 Offset = 18084h; Proxy1 Offset = 1A084h) [reset = X]

CTRLMMR_WKUP_POR_POKLV_UV_CTRL is shown in Figure 2-113 and described in Table 2-229.

Return to Summary Table.

Controls operation of the VDD_MCU undervoltage POK within the POR.

Table 2-228. CTRLMMR_WKUP_POR_POKLV_UV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8084h	4301 A084h

Figure 2-113. CTRLMMR_WKUP_POR_POKLV_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-229. CTRLMMR_WKUP_POR_POKLV_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.115 CTRLMMR_WKUP_POR_POKHV_OV_CTRL Register (Proxy0 Offset = 18088h; Proxy1 Offset = 1A088h) [reset = X]

CTRLMMR_WKUP_POR_POKHV_OV_CTRL is shown in Figure 2-114 and described in Table 2-231.

Return to Summary Table.

Controls operation of the 1.8V VDDA_POR_WKUP overvoltage POK within the POR.

Table 2-230. CTRLMMR_WKUP_POR_POKHV_OV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8088h	4301 A088h

Figure 2-114. CTRLMMR_WKUP_POR_POKHV_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-231. CTRLMMR_WKUP_POR_POKHV_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.116 CTRLMMR_WKUP_POR_BANDGAP_CTRL Register (Proxy0 Offset = 1808Ch; Proxy1 Offset = 1A08Ch) [reset = X]

CTRLMMR_WKUP_POR_BANDGAP_CTRL is shown in Figure 2-115 and described in Table 2-233.

Return to Summary Table.

Controls the operation of the bandgap module within the POR.

Table 2-232. CTRLMMR_WKUP_POR_BANDGAP_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 808Ch	4301 A08Ch

Figure 2-115. CTRLMMR_WKUP_POR_BANDGAP_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED				BGAPI			
R-0h				R/W-X			

15	14	13	12	11	10	9	8
BGAPV							
R/W-X							

7	6	5	4	3	2	1	0
BGAPC							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-233. CTRLMMR_WKUP_POR_BANDGAP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	BGAPI	R/W	X	Bandgap output current trim bits
15-8	BGAPV	R/W	X	Bandgap output voltage magnitude trim bits
7-0	BGAPC	R/W	X	Bandgap slope trim bits. Bit7 is used to calculate the offset

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2.117 CTRLMMR_WKUP_TEMP_DIODE_TRIM Register (Proxy0 Offset = 180A0h; Proxy1 Offset = 1A0A0h) [reset = X]

CTRLMMR_WKUP_TEMP_DIODE_TRIM is shown in Figure 2-116 and described in Table 2-235.

Return to Summary Table.

Trims the silicon junction temperature diode calculation.

Table 2-234. CTRLMMR_WKUP_TEMP_DIODE_TRIM Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 80A0h	4301 A0A0h

Figure 2-116. CTRLMMR_WKUP_TEMP_DIODE_TRIM Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																		TRIM													
R-0h																		R/W-X													

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-235. CTRLMMR_WKUP_TEMP_DIODE_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R	0h	Reserved
13-0	TRIM	R/W	X	Sets the diode non-ideality factor (n), starting from 100th place decimal and going down

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2.118 CTRLMMR_WKUP_IO_VOLTAGE_STAT Register (Proxy0 Offset = 180B0h; Proxy1 Offset = 1A0B0h) [reset = X]

CTRLMMR_WKUP_IO_VOLTAGE_STAT is shown in Figure 2-117 and described in Table 2-237.

Return to Summary Table.

Indicates the I/O voltage of each LVCMOS dual I/O group.

Table 2-236. CTRLMMR_WKUP_IO_VOLTAGE_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 80B0h	4301 A0B0h

Figure 2-117. CTRLMMR_WKUP_IO_VOLTAGE_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
MAIN_RGMII6	MAIN_RGMII5	MAIN_PRG1	MAIN_PRG0	MAIN_MMC2	MAIN_MMC1	RESERVED	MAIN_GEN
R-X	R-X	R-X	R-X	R-X	R-X	R-0h	R-X
7	6	5	4	3	2	1	0
RESERVED					MCU_RGMII	MCU_FLASH	MCU_GEN
R-0h					R-X	R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-237. CTRLMMR_WKUP_IO_VOLTAGE_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	MAIN_RGMII6	R	X	Indicates the voltage for the RGMII6 I/O group 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
14	MAIN_RGMII5	R	X	Indicates the voltage for the RGMII5 I/O group 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
13	MAIN_PRG1	R	X	Indicates the voltage for the PRG1 I/O group 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
12	MAIN_PRG0	R	X	Indicates the voltage for the PRG0 I/O group 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
11	MAIN_MMC2	R	X	Indicates the voltage for the MMC2 I/O group 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
10	MAIN_MMC1	R	X	Indicates the voltage for the MMC1 I/O group 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
9	RESERVED	R	0h	Reserved

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Table 2-237. CTRLMMR_WKUP_IO_VOLTAGE_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MAIN_GEN	R	X	Indicates the voltage for the General I/O group 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
7-3	RESERVED	R	0h	Reserved
2	MCU_RGMII	R	X	Indicates the voltage for the MCU CPSW2G RGMII I/O group 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
1	MCU_FLASH	R	X	Indicates the voltage for the MCU Flash I/O group 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V
0	MCU_GEN	R	X	Indicates the voltage for the MCU General I/O group 0h - I/O group is set for 1.8V 1h - I/O group is set for 3.3V

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2.119 CTRLMMR_WKUP_MAIN_POR_TO_CTRL Register (Proxy0 Offset = 18104h; Proxy1 Offset = 1A104h) [reset = X]

CTRLMMR_WKUP_MAIN_POR_TO_CTRL is shown in Figure 2-118 and described in Table 2-239.

Return to Summary Table.

Indicates the MAIN PORz timeout period.

Table 2-238. CTRLMMR_WKUP_MAIN_POR_TO_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8104h	4301 A104h

Figure 2-118. CTRLMMR_WKUP_MAIN_POR_TO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					TIMEOUT_PER		
R-0h					R/W-X		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-239. CTRLMMR_WKUP_MAIN_POR_TO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	TIMEOUT_PER	R/W	X	MAIN PORz hardware timeout period. During normal operation, the assertion of a MAIN Domain PORz generates a reset request interrupt to the DMSC. The DMSC then performs steps to properly isolate the MAIN Domain before the actual reset is performed. A hardware timeout mechanism is provided to ensure that the PORz gets propogated to the MAIN Domain in the event that a error prevents the DMSC from completing the reset isolation. 0h - Immediate 1h - 100 microsec 2h - 200 microsec 3h - 300 microsec 4h - 400 microsec 5h - 500 microsec

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2.120 CTRLMMR_WKUP_MAIN_PRG_CTRL Register (Proxy0 Offset = 18108h; Proxy1 Offset = 1A108h) [reset = 53535353h]

CTRLMMR_WKUP_MAIN_PRG_CTRL is shown in Figure 2-119 and described in Table 2-241.

Return to Summary Table.

Configures the MAIN domain PRG controller.

Table 2-240. CTRLMMR_WKUP_MAIN_PRG_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8108h	4301 A108h

Figure 2-119. CTRLMMR_WKUP_MAIN_PRG_CTRL Register

31	30	29	28	27	26	25	24
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED		RESERVED	RESERVED
R/W-0h	R/W-1h	R-0h	R/W-1h	R-0h		R/W-1h	R/W-1h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED		RESERVED	RESERVED
R-0h	R/W-1h	R-0h	R/W-1h	R-0h		R/W-1h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
POK_EN_SEL	POK_VDDR_CORE_OV_EN	RESERVED	POK_VMON_EXT_OV_EN	RESERVED		POK_VDD_CPU_OV_EN	POK_VDD_CORE_OV_EN
R/W-0h	R/W-1h	R-0h	R/W-1h	R-0h		R/W-1h	R/W-1h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	POK_VDDR_CORE_UV_EN	RESERVED	POK_VMON_EXT_UV_EN	RESERVED		POK_VDD_CPU_UV_EN	POK_VDD_CORE_UV_EN
R-0h	R/W-1h	R-0h	R/W-1h	R-0h		R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-241. CTRLMMR_WKUP_MAIN_PRG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R/W	0h	Reserved
30	RESERVED	R/W	1h	Reserved
29	RESERVED	R	0h	Reserved
28	RESERVED	R/W	1h	Reserved
27-26	RESERVED	R	0h	Reserved
25	RESERVED	R/W	1h	Reserved
24	RESERVED	R/W	1h	Reserved
23	RESERVED	R	0h	Reserved
22	RESERVED	R/W	1h	Reserved
21	RESERVED	R	0h	Reserved
20	RESERVED	R/W	1h	Reserved
19-18	RESERVED	R	0h	Reserved
17	RESERVED	R/W	1h	Reserved
16	RESERVED	R/W	1h	Reserved

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Table 2-241. CTRLMMR_WKUP_MAIN_PRG_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	POK_EN_SEL	R/W	0h	Select POK enable source 0h - POK enables come from hardware tie-offs 1h - POK enables come from CTRLMMR_WKUP_MAIN_PRG_CTRL register
14	POK_VDDR_CORE_OV_EN	R/W	1h	Enable VDDAR_CORE overvoltage POK detection. 0h - POK detection disabled 1h - POK detection enabled
13	RESERVED	R	0h	Reserved
12	POK_VMON_EXT_OV_EN	R/W	1h	Enable VMON_EXT overvoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
11-10	RESERVED	R	0h	Reserved
9	POK_VDD_CPU_OV_EN	R/W	1h	Enable VDD_CPU overvoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
8	POK_VDD_CORE_OV_EN	R/W	1h	Enable VDD_CORE overvoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
7	RESERVED	R	0h	Reserved
6	POK_VDDR_CORE_UV_EN	R/W	1h	Enable VDDAR_CORE undervoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
5	RESERVED	R	0h	Reserved
4	POK_VMON_EXT_UV_EN	R/W	1h	Enable VMON_EXT undervoltage POK detection 0h - POK detection disabled 1h - POK detection enabled
3-2	RESERVED	R	0h	Reserved
1	POK_VDD_CPU_UV_EN	R/W	1h	Enable VDD_CPU undervoltage POK detection. 0h - POK detection disabled 1h - POK detection enabled
0	POK_VDD_CORE_UV_EN	R/W	1h	Enable VDD_CORE undervoltage POK detection 0h - POK detection disabled 1h - POK detection enabled

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2.121 CTRLMMR_WKUP_MAIN_PRG_STAT Register (Proxy0 Offset = 1810Ch; Proxy1 Offset = 1A10Ch) [reset = X]

CTRLMMR_WKUP_MAIN_PRG_STAT is shown in Figure 2-120 and described in Table 2-243.

Return to Summary Table.

Provides MAIN domain PRG controller status.

Table 2-242. CTRLMMR_WKUP_MAIN_PRG_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 810Ch	4301 A10Ch

Figure 2-120. CTRLMMR_WKUP_MAIN_PRG_STAT Register

31	30	29	28	27	26	25	24
POK_CLR	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED	POK_VDDR_CORE_OV	RESERVED	POK_VMON_EXT_OV	RESERVED		POK_VDD_CPU_OV	POK_VDD_CORE_OV
R-0h	R-X	R-0h	R-X	R-0h		R-X	R-X

7	6	5	4	3	2	1	0
RESERVED	POK_VDDR_CORE_UV	RESERVED	POK_VMON_EXT_UV	RESERVED		POK_VDD_CPU_UV	POK_VDD_CORE_UV
R-0h	R-X	R-0h	R-X	R-0h		R-X	R-X

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-243. CTRLMMR_WKUP_MAIN_PRG_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	POK_CLR	R/W	0h	When set, resets pgood sticky bits for VDD_CORE, VDD_CPU, VMON_EXT, and CDDR_CORE voltage POK detection.
30-15	RESERVED	R	0h	Reserved
14	POK_VDDR_CORE_OV	R	X	VDDAR_CORE overvoltage POK 0h - Voltage abovethreshold 1h - Voltage good
13	RESERVED	R	0h	Reserved
12	POK_VMON_EXT_OV	R	X	VMON_EXT overvoltage POK 0h - Voltage above threshold 1h - Voltage good
11-10	RESERVED	R	0h	Reserved
9	POK_VDD_CPU_OV	R	X	VDD_CPU overvoltage POK 0h - Voltage above threshold 1h - Voltage good
8	POK_VDD_CORE_OV	R	X	VDD_CORE overvoltage POK 0h - Voltage above threshold 1h - Voltage good
7	RESERVED	R	0h	Reserved

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Table 2-243. CTRLMMR_WKUP_MAIN_PRG_STAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	POK_VDDR_CORE_UV	R	X	VDDAR_CORE undervoltage POK 0h - Voltage below threshold 1h - Voltage good
5	RESERVED	R	0h	Reserved
4	POK_VMON_EXT_UV	R	X	VMON_EXT undervoltage POK 0h - Voltage below threshold 1h - Voltage good
3-2	RESERVED	R	0h	Reserved
1	POK_VDD_CPU_UV	R	X	VDD_CPU undervoltage POK 0h - Voltage below threshold 1h - Voltage good
0	POK_VDD_CORE_UV	R	X	VDD_CORE undervoltage POK 0h - Voltage below threshold 1h - Voltage good

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2.122 CTRLMMR_WKUP_POK_VDD_CORE_UV_CTRL Register (Proxy0 Offset = 18110h; Proxy1 Offset = 1A110h) [reset = X]

CTRLMMR_WKUP_POK_VDD_CORE_UV_CTRL is shown in Figure 2-121 and described in Table 2-245.

Return to Summary Table.

Controls operation of the VDD_CORE undervoltage POK module.

Table 2-244. CTRLMMR_WKUP_POK_VDD_CORE_UV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8110h	4301 A110h

Figure 2-121. CTRLMMR_WKUP_POK_VDD_CORE_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-245. CTRLMMR_WKUP_POK_VDD_CORE_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.123 CTRLMMR_WKUP_POK_VDD_CPU_UV_CTRL Register (Proxy0 Offset = 18114h; Proxy1 Offset = 1A114h) [reset = X]

CTRLMMR_WKUP_POK_VDD_CPU_UV_CTRL is shown in Figure 2-122 and described in Table 2-247.

Return to Summary Table.

Controls operation of the VDD_CPU undervoltage POK module.

Table 2-246. CTRLMMR_WKUP_POK_VDD_CPU_UV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8114h	4301 A114h

Figure 2-122. CTRLMMR_WKUP_POK_VDD_CPU_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-247. CTRLMMR_WKUP_POK_VDD_CPU_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.124 CTRLMMR_WKUP_POK_VMON_EXT_UV_CTRL Register (Proxy0 Offset = 18118h; Proxy1 Offset = 1A118h) [reset = X]

CTRLMMR_WKUP_POK_VMON_EXT_UV_CTRL is shown in Figure 2-123 and described in Table 2-249.

Return to Summary Table.

Controls operation of the VMON_EXTC undervoltage POK module.

Table 2-248. CTRLMMR_WKUP_POK_VMON_EXT_UV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8118h	4301 A118h

Figure 2-123. CTRLMMR_WKUP_POK_VMON_EXT_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-249. CTRLMMR_WKUP_POK_VMON_EXT_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.125 CTRLMMR_WKUP_POK_VDDR_CORE_UV_CTRL Register (Proxy0 Offset = 1811Ch; Proxy1 Offset = 1A11Ch) [reset = X]

CTRLMMR_WKUP_POK_VDDR_CORE_UV_CTRL is shown in Figure 2-124 and described in Table 2-251.

Return to Summary Table.

Controls operation of the VDDR_CORE undervoltage POK module.

Table 2-250. CTRLMMR_WKUP_POK_VDDR_CORE_UV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 811Ch	4301 A11Ch

Figure 2-124. CTRLMMR_WKUP_POK_VDDR_CORE_UV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-251. CTRLMMR_WKUP_POK_VDDR_CORE_UV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.126 CTRLMMR_WKUP_POK_VDD_CORE_OV_CTRL Register (Proxy0 Offset = 18120h; Proxy1 Offset = 1A120h) [reset = X]

CTRLMMR_WKUP_POK_VDD_CORE_OV_CTRL is shown in Figure 2-125 and described in Table 2-253.

Return to Summary Table.

Controls operation of the VDD_CORE overvoltage POK module.

Table 2-252. CTRLMMR_WKUP_POK_VDD_CORE_OV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8120h	4301 A120h

Figure 2-125. CTRLMMR_WKUP_POK_VDD_CORE_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-253. CTRLMMR_WKUP_POK_VDD_CORE_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.127 CTRLMMR_WKUP_POK_VDD_CPU_OV_CTRL Register (Proxy0 Offset = 18124h; Proxy1 Offset = 1A124h) [reset = X]

CTRLMMR_WKUP_POK_VDD_CPU_OV_CTRL is shown in Figure 2-126 and described in Table 2-255.

Return to Summary Table.

Controls operation of the VDD_CPU overvoltage POK module.

Table 2-254. CTRLMMR_WKUP_POK_VDD_CPU_OV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8124h	4301 A124h

Figure 2-126. CTRLMMR_WKUP_POK_VDD_CPU_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-255. CTRLMMR_WKUP_POK_VDD_CPU_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.128 CTRLMMR_WKUP_POK_VMON_EXT_OV_CTRL Register (Proxy0 Offset = 18128h; Proxy1 Offset = 1A128h) [reset = X]

CTRLMMR_WKUP_POK_VMON_EXT_OV_CTRL is shown in Figure 2-127 and described in Table 2-257.

Return to Summary Table.

Controls operation of the VMON_EXT overvoltage POK module.

Table 2-256. CTRLMMR_WKUP_POK_VMON_EXT_OV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8128h	4301 A128h

Figure 2-127. CTRLMMR_WKUP_POK_VMON_EXT_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-257. CTRLMMR_WKUP_POK_VMON_EXT_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.129 CTRLMMR_WKUP_POK_VDDR_CORE_OV_CTRL Register (Proxy0 Offset = 1812Ch; Proxy1 Offset = 1A12Ch) [reset = X]

CTRLMMR_WKUP_POK_VDDR_CORE_OV_CTRL is shown in Figure 2-128 and described in Table 2-259.

Return to Summary Table.

Controls operation of the VDDR_CORE overvoltage POK module.

Table 2-258. CTRLMMR_WKUP_POK_VDDR_CORE_OV_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 812Ch	4301 A12Ch

Figure 2-128. CTRLMMR_WKUP_POK_VDDR_CORE_OV_CTRL Register

31	30	29	28	27	26	25	24
HYST_EN	RESERVED						
R/W-1h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OVER_VOLT_DET	POK_TRIM						
R/W-X	R/W-X						

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-259. CTRLMMR_WKUP_POK_VDDR_CORE_OV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	HYST_EN	R/W	1h	Enable POK hysteresis
30-8	RESERVED	R	0h	Reserved
7	OVER_VOLT_DET	R/W	X	Over / under voltage detection mode 0h - Under voltage detection 1h - Over voltage detection
6-0	POK_TRIM	R/W	X	POK trim bits. These bits are used to trim the comparator threshold voltage.

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2.130 CTRLMMR_WKUP_DEEPSLEEP_CTRL Register (Proxy0 Offset = 18160h; Proxy1 Offset = 1A160h) [reset = 0h]

CTRLMMR_WKUP_DEEPSLEEP_CTRL is shown in Figure 2-129 and described in Table 2-261.

Return to Summary Table.

Used to control IO deepsleep operation.

Table 2-260. CTRLMMR_WKUP_DEEPSLEEP_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8160h	4301 A160h

Figure 2-129. CTRLMMR_WKUP_DEEPSLEEP_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							FORCE_DS_MAIN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							FORCE_DS_WKUP
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-261. CTRLMMR_WKUP_DEEPSLEEP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	FORCE_DS_MAIN	R/W	0h	Force all MAIN IOs into deepsleep mode when set
7-1	RESERVED	R	0h	Reserved
0	FORCE_DS_WKUP	R/W	0h	Force all WKUP IOs into deepsleep mode when set

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2.131 CTRLMMR_WKUP_POR_RST_CTRL Register (Proxy0 Offset = 18170h; Proxy1 Offset = 1A170h) [reset = F0000h]

CTRLMMR_WKUP_POR_RST_CTRL is shown in Figure 2-130 and described in Table 2-263.

Return to Summary Table.

Controls MAIN domain power-on reset behavior.

Table 2-262. CTRLMMR_WKUP_POR_RST_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8170h	4301 A170h

Figure 2-130. CTRLMMR_WKUP_POR_RST_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							MAIN_PORZ_DAISYCHAIN_EN
R-0h							R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				SW_MAIN_POR			
R-0h				R/W-Fh			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED			MAIN_PORZ_DS_STRETCH	RESERVED			
R-0h			R/W-0h	R-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							POR_RST_ISO_DONE_Z
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-263. CTRLMMR_WKUP_POR_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	MAIN_PORZ_DAISYCHAIN_EN	R/W	0h	MAIN PORz daisy-chain event enable. Determines if MAIN PORz reset events affect daisy-chain wakeup 0h - DeepSleep MAIN PORz event is not part of daisy-chain 1h - DeepSleep MAIN PORz event is combined w/ other daisy chain events.
23-20	RESERVED	R	0h	Reserved
19-16	SW_MAIN_POR	R/W	Fh	Main Domain software power-on reset. When set to 6h, a power-on is issued to the MAIN voltage domain. (Bits will reset to Fh on reset of the Main Domain)
15-13	RESERVED	R	0h	Reserved
12	MAIN_PORZ_DS_STRETCH	R/W	0h	DeepSleep mode MAIN PORz stretch. 0h - No stretching 1h - Stretch the Main PORz event captured during DeepSleep mode
11-1	RESERVED	R	0h	Reserved

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Table 2-263. CTRLMMR_WKUP_POR_RST_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	POR_RST_ISO_DONE_Z	R/W	0h	Reset isolation completion (active low). This bit should be cleared only after reset isolation of the MAIN domain is complete. 0h - POR reset propagates to MAIN domain 1h - POR reset blocked from MAIN domain

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2.132 CTRLMMR_WKUP_MAIN_WARM_RST_CTRL Register (Proxy0 Offset = 18174h; Proxy1 Offset = 1A174h) [reset = F0000h]

CTRLMMR_WKUP_MAIN_WARM_RST_CTRL is shown in Figure 2-131 and described in Table 2-265.

Return to Summary Table.

Controls warm reset propagation to the MAIN domain. This allows the DMSC to ensure that the MCU domain is properly isolated before the MAIN domain is reset.

Table 2-264. CTRLMMR_WKUP_MAIN_WARM_RST_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8174h	4301 A174h

Figure 2-131. CTRLMMR_WKUP_MAIN_WARM_RST_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED				SW_WARMRST			
R-0h				R/W-Fh			

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							SOC_WARMRST_ISO_DONE_Z
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-265. CTRLMMR_WKUP_MAIN_WARM_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	SW_WARMRST	R/W	Fh	Main Domain software warm reset. When set to 6h, a warm reset is issued to the MAIN voltage domain. (Bits will reset to Fh on reset of the Main Domain)
15-1	RESERVED	R	0h	Reserved
0	SOC_WARMRST_ISO_DONE_Z	R/W	0h	Reset isolation completion (active low). This bit should be cleared only after reset isolation of the MAIN domain is complete. 0h - Warm reset propagates to MAIN domain 1h - Warm reset blocked from MAIN domain

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2.133 CTRLMMR_WKUP_RST_STAT Register (Proxy0 Offset = 18178h; Proxy1 Offset = 1A178h) [reset = X]

CTRLMMR_WKUP_RST_STAT is shown in Figure 2-132 and described in Table 2-267.

Return to Summary Table.

Shows the reset status.

Table 2-266. CTRLMMR_WKUP_RST_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8178h	4301 A178h

Figure 2-132. CTRLMMR_WKUP_RST_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							MCU_RST_DONE
R-0h							R-X
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							MAIN_RST_DONE
R-0h							R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-267. CTRLMMR_WKUP_RST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MCU_RST_DONE	R	X	Indicates MCU domain reset status. 0h - MCU domain is in reset 1h - MCU domain reset is complete
15-1	RESERVED	R	0h	Reserved
0	MAIN_RST_DONE	R	X	Indicates MAIN domain Warm reset status. 0h - MAIN domain is in Warm reset 1h - MAIN domain Warm reset is complete

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2.134 CTRLMMR_WKUP_MCU_WARM_RST_CTRL Register (Proxy0 Offset = 1817Ch; Proxy1 Offset = 1A17Ch) [reset = F0000h]

CTRLMMR_WKUP_MCU_WARM_RST_CTRL is shown in Figure 2-133 and described in Table 2-269.

Return to Summary Table.

Controls warm reset propagation to the MCU domain. This allows the DMSC to ensure that the WKUP domain is properly isolated before the MCU domain is reset.

Table 2-268. CTRLMMR_WKUP_MCU_WARM_RST_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 817Ch	4301 A17Ch

Figure 2-133. CTRLMMR_WKUP_MCU_WARM_RST_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED				SW_WARMRST			
R-0h				R/W-Fh			

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-269. CTRLMMR_WKUP_MCU_WARM_RST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	SW_WARMRST	R/W	Fh	Chip software warm reset. When set to 6h, a warm reset is issued to the device (all voltage domains). (Bits will reset to Fh on reset completion.)
15-0	RESERVED	R	0h	Reserved

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2.135 CTRLMMR_WKUP_VDD_CPU_GLDTC_CTRL Register (Proxy0 Offset = 18180h; Proxy1 Offset = 1A180h) [reset = X]

CTRLMMR_WKUP_VDD_CPU_GLDTC_CTRL is shown in Figure 2-134 and described in Table 2-271.

Return to Summary Table.

Controls the voltage glitch detector circuit monitoring the VDD_CPU voltage domain.

Table 2-270. CTRLMMR_WKUP_VDD_CPU_GLDTC_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8180h	4301 A180h

Figure 2-134. CTRLMMR_WKUP_VDD_CPU_GLDTC_CTRL Register

31	30	29	28	27	26	25	24
PWDB	RSTB	RESERVED					
R/W-0h	R/W-0h	R-0h					

23	22	21	20	19	18	17	16
RESERVED					LP_FILTER_SEL		
R-0h					R/W-X		

15	14	13	12	11	10	9	8
RESERVED		THRESH_HI_SEL					
R-0h		R/W-X					

7	6	5	4	3	2	1	0
RESERVED		THRESH_LO_SEL					
R-0h		R/W-X					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-271. CTRLMMR_WKUP_VDD_CPU_GLDTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PWDB	R/W	0h	Power down - active low. 0h - Disable all functions 1h - Enable glitch detectors
30	RSTB	R/W	0h	Reset - active low. To ensure proper operation, rstb must not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. 0h - Reset glitch detector flags 1h - Glitch detection flags are enabled
29-19	RESERVED	R	0h	Reserved
18-16	LP_FILTER_SEL	R/W	X	Selects the glitch detect low-pass filter bandwidth 0h - 150 kHz 1h - 125 kHz 2h - 100 kHz 3h - 80 kHz 4h - 60 kHz 5h - 45 kHz 6h - 30 kHz 7h - 15 kHz

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Table 2-271. CTRLMMR_WKUP_VDD_CPU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	THRESH_HI_SEL	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage 0h - 93.5% of VDD 1h - 94.0% of VDD 2h - 94.5% of VDD 3h - 95.0% of VDD 4h - 95.5% of VDD 5h - 96.0% of VDD 6h - 96.5% of VDD 7h - 97.0% of VDD 8h - 97.5% of VDD 9h - 98.0% of VDD Ah - 98.5% of VDD Bh - 99.0% of VDD Ch - 99.5% of VDD Dh - 100.0% of VDD Eh - 100.5% of VDD Fh - 101.0% of VDD 10h - 101.5% of VDD 11h - 102.0% of VDD 12h - 102.5% of VDD 13h - 103.0% of VDD 14h - 103.5% of VDD 15h - 104.0% of VDD 16h - 104.5% of VDD 17h - 105.0% of VDD 18h - 105.5% of VDD 19h - 106.0% of VDD 1Ah - 106.5% of VDD 1Bh - 107.0% of VDD 1Ch - 107.5% of VDD 1Dh - 108.0% of VDD 1Eh - 108.5% of VDD 1Fh - 109.0% of VDD

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Table 2-271. CTRLMMR_WKUP_VDD_CPU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 109.5% of VDD 21h - 110.0% of VDD 22h - 111.0% of VDD 23h - 112.0% of VDD 24h - 113.0% of VDD 25h - 114.0% of VDD 26h - 115.0% of VDD 27h - 116.0% of VDD 28h - 117.0% of VDD 29h - 118.0% of VDD 2Ah - 119.0% of VDD 2Bh - 120.0% of VDD 2Ch - 121.0% of VDD 2Dh - 122.0% of VDD 2Eh - 123.0% of VDD 2Fh - 124.0% of VDD 30h - 125.0% of VDD 31h - 126.0% of VDD 32h - 127.0% of VDD 33h - 128.0% of VDD 34h - 129.0% of VDD 35h - 130.0% of VDD 36h - 131.0% of VDD 37h - 132.0% of VDD 38h - 133.0% of VDD 39h - 134.0% of VDD 3Ah - 135.0% of VDD 3Bh - 136.0% of VDD 3Ch - 137.0% of VDD 3Dh - 138.0% of VDD 3Eh - 139.0% of VDD 3Fh - 140.0% of VDD
7-6	RESERVED	R	0h	Reserved

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Table 2-271. CTRLMMR_WKUP_VDD_CPU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	THRESH_LO_SEL	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage 0h - 106.5% of VDD 1h - 106.0% of VDD 2h - 105.5% of VDD 3h - 105.0% of VDD 4h - 104.5% of VDD 5h - 104.0% of VDD 6h - 103.5% of VDD 7h - 103.0% of VDD 8h - 102.5% of VDD 9h - 102.0% of VDD Ah - 101.5% of VDD Bh - 101.0% of VDD Ch - 100.5% of VDD Dh - 100.0% of VDD Eh - 99.5% of VDD Fh - 99.0% of VDD 10h - 98.5% of VDD 11h - 98.0% of VDD 12h - 97.5% of VDD 13h - 97.0% of VDD 14h - 96.5% of VDD 15h - 96.0% of VDD 16h - 95.5% of VDD 17h - 95.0% of VDD 18h - 94.5% of VDD 19h - 94.0% of VDD 1Ah - 93.5% of VDD 1Bh - 93.0% of VDD 1Ch - 92.5% of VDD 1Dh - 92.0% of VDD 1Eh - 91.5% of VDD 1Fh - 91.0% of VDD

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Table 2-271. CTRLMMR_WKUP_VDD_CPU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 90.5% of VDD 21h - 90.0% of VDD 22h - 89.0% of VDD 23h - 88.0% of VDD 24h - 87.0% of VDD 25h - 86.0% of VDD 26h - 85.0% of VDD 27h - 84.0% of VDD 28h - 83.0% of VDD 29h - 82.0% of VDD 2Ah - 81.0% of VDD 2Bh - 80.0% of VDD 2Ch - 79.0% of VDD 2Dh - 78.0% of VDD 2Eh - 77.0% of VDD 2Fh - 76.0% of VDD 30h - 75.0% of VDD 31h - 74.0% of VDD 32h - 73.0% of VDD 33h - 72.0% of VDD 34h - 71.0% of VDD 35h - 70.0% of VDD 36h - 69.0% of VDD 37h - 68.0% of VDD 38h - 67.0% of VDD 39h - 66.0% of VDD 3Ah - 65.0% of VDD 3Bh - 64.0% of VDD 3Ch - 63.0% of VDD 3Dh - 62.0% of VDD 3Eh - 61.0% of VDD 3Fh - 60.0% of VDD

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2.136 CTRLMMR_WKUP_VDD_CORE_GLDTC_CTRL Register (Proxy0 Offset = 18190h; Proxy1 Offset = 1A190h) [reset = X]

CTRLMMR_WKUP_VDD_CORE_GLDTC_CTRL is shown in Figure 2-135 and described in Table 2-273.

Return to Summary Table.

Controls the voltage glitch detector circuit monitoring the VDD_CORE voltage domain.

Table 2-272. CTRLMMR_WKUP_VDD_CORE_GLDTC_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8190h	4301 A190h

Figure 2-135. CTRLMMR_WKUP_VDD_CORE_GLDTC_CTRL Register

31	30	29	28	27	26	25	24
PWDB	RSTB	RESERVED					
R/W-0h	R/W-0h	R-0h					

23	22	21	20	19	18	17	16
RESERVED					LP_FILTER_SEL		
R-0h					R/W-X		

15	14	13	12	11	10	9	8
RESERVED		THRESH_HI_SEL					
R-0h		R/W-X					

7	6	5	4	3	2	1	0
RESERVED		THRESH_LO_SEL					
R-0h		R/W-X					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-273. CTRLMMR_WKUP_VDD_CORE_GLDTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PWDB	R/W	0h	Power down - active low. 0h - Disable all functions 1h - Enable glitch detectors
30	RSTB	R/W	0h	Reset - active low. To ensure proper operation, rstb must not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. 0h - Reset glitch detector flags 1h - Glitch detection flags are enabled
29-19	RESERVED	R	0h	Reserved
18-16	LP_FILTER_SEL	R/W	X	Selects the glitch detect low-pass filter bandwidth 0h - 150 kHz 1h - 125 kHz 2h - 100 kHz 3h - 80 kHz 4h - 60 kHz 5h - 45 kHz 6h - 30 kHz 7h - 15 kHz

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Table 2-273. CTRLMMR_WKUP_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	THRESH_HI_SEL	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage 0h - 93.5% of VDD 1h - 94.0% of VDD 2h - 94.5% of VDD 3h - 95.0% of VDD 4h - 95.5% of VDD 5h - 96.0% of VDD 6h - 96.5% of VDD 7h - 97.0% of VDD 8h - 97.5% of VDD 9h - 98.0% of VDD Ah - 98.5% of VDD Bh - 99.0% of VDD Ch - 99.5% of VDD Dh - 100.0% of VDD Eh - 100.5% of VDD Fh - 101.0% of VDD 10h - 101.5% of VDD 11h - 102.0% of VDD 12h - 102.5% of VDD 13h - 103.0% of VDD 14h - 103.5% of VDD 15h - 104.0% of VDD 16h - 104.5% of VDD 17h - 105.0% of VDD 18h - 105.5% of VDD 19h - 106.0% of VDD 1Ah - 106.5% of VDD 1Bh - 107.0% of VDD 1Ch - 107.5% of VDD 1Dh - 108.0% of VDD 1Eh - 108.5% of VDD 1Fh - 109.0% of VDD

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Table 2-273. CTRLMMR_WKUP_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 109.5% of VDD 21h - 110.0% of VDD 22h - 111.0% of VDD 23h - 112.0% of VDD 24h - 113.0% of VDD 25h - 114.0% of VDD 26h - 115.0% of VDD 27h - 116.0% of VDD 28h - 117.0% of VDD 29h - 118.0% of VDD 2Ah - 119.0% of VDD 2Bh - 120.0% of VDD 2Ch - 121.0% of VDD 2Dh - 122.0% of VDD 2Eh - 123.0% of VDD 2Fh - 124.0% of VDD 30h - 125.0% of VDD 31h - 126.0% of VDD 32h - 127.0% of VDD 33h - 128.0% of VDD 34h - 129.0% of VDD 35h - 130.0% of VDD 36h - 131.0% of VDD 37h - 132.0% of VDD 38h - 133.0% of VDD 39h - 134.0% of VDD 3Ah - 135.0% of VDD 3Bh - 136.0% of VDD 3Ch - 137.0% of VDD 3Dh - 138.0% of VDD 3Eh - 139.0% of VDD 3Fh - 140.0% of VDD
7-6	RESERVED	R	0h	Reserved

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Table 2-273. CTRLMMR_WKUP_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	THRESH_LO_SEL	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage 0h - 106.5% of VDD 1h - 106.0% of VDD 2h - 105.5% of VDD 3h - 105.0% of VDD 4h - 104.5% of VDD 5h - 104.0% of VDD 6h - 103.5% of VDD 7h - 103.0% of VDD 8h - 102.5% of VDD 9h - 102.0% of VDD Ah - 101.5% of VDD Bh - 101.0% of VDD Ch - 100.5% of VDD Dh - 100.0% of VDD Eh - 99.5% of VDD Fh - 99.0% of VDD 10h - 98.5% of VDD 11h - 98.0% of VDD 12h - 97.5% of VDD 13h - 97.0% of VDD 14h - 96.5% of VDD 15h - 96.0% of VDD 16h - 95.5% of VDD 17h - 95.0% of VDD 18h - 94.5% of VDD 19h - 94.0% of VDD 1Ah - 93.5% of VDD 1Bh - 93.0% of VDD 1Ch - 92.5% of VDD 1Dh - 92.0% of VDD 1Eh - 91.5% of VDD 1Fh - 91.0% of VDD

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Table 2-273. CTRLMMR_WKUP_VDD_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 90.5% of VDD 21h - 90.0% of VDD 22h - 89.0% of VDD 23h - 88.0% of VDD 24h - 87.0% of VDD 25h - 86.0% of VDD 26h - 85.0% of VDD 27h - 84.0% of VDD 28h - 83.0% of VDD 29h - 82.0% of VDD 2Ah - 81.0% of VDD 2Bh - 80.0% of VDD 2Ch - 79.0% of VDD 2Dh - 78.0% of VDD 2Eh - 77.0% of VDD 2Fh - 76.0% of VDD 30h - 75.0% of VDD 31h - 74.0% of VDD 32h - 73.0% of VDD 33h - 72.0% of VDD 34h - 71.0% of VDD 35h - 70.0% of VDD 36h - 69.0% of VDD 37h - 68.0% of VDD 38h - 67.0% of VDD 39h - 66.0% of VDD 3Ah - 65.0% of VDD 3Bh - 64.0% of VDD 3Ch - 63.0% of VDD 3Dh - 62.0% of VDD 3Eh - 61.0% of VDD 3Fh - 60.0% of VDD

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2.137 CTRLMMR_WKUP_VDDR_CPU_GLDTC_CTRL Register (Proxy0 Offset = 18194h; Proxy1 Offset = 1A194h) [reset = X]

CTRLMMR_WKUP_VDDR_CPU_GLDTC_CTRL is shown in Figure 2-136 and described in Table 2-275.

Return to Summary Table.

Controls the voltage glitch detector circuit monitoring the VDDR_CORE voltage domain.

Table 2-274. CTRLMMR_WKUP_VDDR_CPU_GLDTC_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8194h	4301 A194h

Figure 2-136. CTRLMMR_WKUP_VDDR_CPU_GLDTC_CTRL Register

31	30	29	28	27	26	25	24
PWDB	RSTB	RESERVED					
R/W-0h	R/W-0h	R-0h					

23	22	21	20	19	18	17	16
RESERVED					LP_FILTER_SEL		
R-0h					R/W-X		

15	14	13	12	11	10	9	8
RESERVED		THRESH_HI_SEL					
R-0h		R/W-X					

7	6	5	4	3	2	1	0
RESERVED		THRESH_LO_SEL					
R-0h		R/W-X					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-275. CTRLMMR_WKUP_VDDR_CPU_GLDTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PWDB	R/W	0h	Power down - active low. 0h - Disable all functions 1h - Enable glitch detectors
30	RSTB	R/W	0h	Reset - active low. To ensure proper operation, rstb must not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. 0h - Reset glitch detector flags 1h - Glitch detection flags are enabled
29-19	RESERVED	R	0h	Reserved
18-16	LP_FILTER_SEL	R/W	X	Selects the glitch detect low-pass filter bandwidth 0h - 150 kHz 1h - 125 kHz 2h - 100 kHz 3h - 80 kHz 4h - 60 kHz 5h - 45 kHz 6h - 30 kHz 7h - 15 kHz

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Table 2-275. CTRLMMR_WKUP_VDDR_CPU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	THRESH_HI_SEL	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage 0h - 93.5% of VDD 1h - 94.0% of VDD 2h - 94.5% of VDD 3h - 95.0% of VDD 4h - 95.5% of VDD 5h - 96.0% of VDD 6h - 96.5% of VDD 7h - 97.0% of VDD 8h - 97.5% of VDD 9h - 98.0% of VDD Ah - 98.5% of VDD Bh - 99.0% of VDD Ch - 99.5% of VDD Dh - 100.0% of VDD Eh - 100.5% of VDD Fh - 101.0% of VDD 10h - 101.5% of VDD 11h - 102.0% of VDD 12h - 102.5% of VDD 13h - 103.0% of VDD 14h - 103.5% of VDD 15h - 104.0% of VDD 16h - 104.5% of VDD 17h - 105.0% of VDD 18h - 105.5% of VDD 19h - 106.0% of VDD 1Ah - 106.5% of VDD 1Bh - 107.0% of VDD 1Ch - 107.5% of VDD 1Dh - 108.0% of VDD 1Eh - 108.5% of VDD 1Fh - 109.0% of VDD

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Table 2-275. CTRLMMR_WKUP_VDDR_CPU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 109.5% of VDD 21h - 110.0% of VDD 22h - 111.0% of VDD 23h - 112.0% of VDD 24h - 113.0% of VDD 25h - 114.0% of VDD 26h - 115.0% of VDD 27h - 116.0% of VDD 28h - 117.0% of VDD 29h - 118.0% of VDD 2Ah - 119.0% of VDD 2Bh - 120.0% of VDD 2Ch - 121.0% of VDD 2Dh - 122.0% of VDD 2Eh - 123.0% of VDD 2Fh - 124.0% of VDD 30h - 125.0% of VDD 31h - 126.0% of VDD 32h - 127.0% of VDD 33h - 128.0% of VDD 34h - 129.0% of VDD 35h - 130.0% of VDD 36h - 131.0% of VDD 37h - 132.0% of VDD 38h - 133.0% of VDD 39h - 134.0% of VDD 3Ah - 135.0% of VDD 3Bh - 136.0% of VDD 3Ch - 137.0% of VDD 3Dh - 138.0% of VDD 3Eh - 139.0% of VDD 3Fh - 140.0% of VDD
7-6	RESERVED	R	0h	Reserved

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Table 2-275. CTRLMMR_WKUP_VDDR_CPU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	THRESH_LO_SEL	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage 0h - 106.5% of VDD 1h - 106.0% of VDD 2h - 105.5% of VDD 3h - 105.0% of VDD 4h - 104.5% of VDD 5h - 104.0% of VDD 6h - 103.5% of VDD 7h - 103.0% of VDD 8h - 102.5% of VDD 9h - 102.0% of VDD Ah - 101.5% of VDD Bh - 101.0% of VDD Ch - 100.5% of VDD Dh - 100.0% of VDD Eh - 99.5% of VDD Fh - 99.0% of VDD 10h - 98.5% of VDD 11h - 98.0% of VDD 12h - 97.5% of VDD 13h - 97.0% of VDD 14h - 96.5% of VDD 15h - 96.0% of VDD 16h - 95.5% of VDD 17h - 95.0% of VDD 18h - 94.5% of VDD 19h - 94.0% of VDD 1Ah - 93.5% of VDD 1Bh - 93.0% of VDD 1Ch - 92.5% of VDD 1Dh - 92.0% of VDD 1Eh - 91.5% of VDD 1Fh - 91.0% of VDD

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Table 2-275. CTRLMMR_WKUP_VDDR_CPU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 90.5% of VDD 21h - 90.0% of VDD 22h - 89.0% of VDD 23h - 88.0% of VDD 24h - 87.0% of VDD 25h - 86.0% of VDD 26h - 85.0% of VDD 27h - 84.0% of VDD 28h - 83.0% of VDD 29h - 82.0% of VDD 2Ah - 81.0% of VDD 2Bh - 80.0% of VDD 2Ch - 79.0% of VDD 2Dh - 78.0% of VDD 2Eh - 77.0% of VDD 2Fh - 76.0% of VDD 30h - 75.0% of VDD 31h - 74.0% of VDD 32h - 73.0% of VDD 33h - 72.0% of VDD 34h - 71.0% of VDD 35h - 70.0% of VDD 36h - 69.0% of VDD 37h - 68.0% of VDD 38h - 67.0% of VDD 39h - 66.0% of VDD 3Ah - 65.0% of VDD 3Bh - 64.0% of VDD 3Ch - 63.0% of VDD 3Dh - 62.0% of VDD 3Eh - 61.0% of VDD 3Fh - 60.0% of VDD

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2.138 CTRLMMR_WKUP_VDDR_CORE_GLDTC_CTRL Register (Proxy0 Offset = 18198h; Proxy1 Offset = 1A198h) [reset = X]

CTRLMMR_WKUP_VDDR_CORE_GLDTC_CTRL is shown in Figure 2-137 and described in Table 2-277.

Return to Summary Table.

Controls the voltage glitch detector circuit monitoring the VDDR_CPU voltage domain.

Table 2-276. CTRLMMR_WKUP_VDDR_CORE_GLDTC_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 8198h	4301 A198h

Figure 2-137. CTRLMMR_WKUP_VDDR_CORE_GLDTC_CTRL Register

31	30	29	28	27	26	25	24
PWDB	RSTB	RESERVED					
R/W-0h	R/W-0h	R-0h					

23	22	21	20	19	18	17	16
RESERVED					LP_FILTER_SEL		
R-0h					R/W-X		

15	14	13	12	11	10	9	8
RESERVED		THRESH_HI_SEL					
R-0h		R/W-X					

7	6	5	4	3	2	1	0
RESERVED		THRESH_LO_SEL					
R-0h		R/W-X					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-277. CTRLMMR_WKUP_VDDR_CORE_GLDTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PWDB	R/W	0h	Power down - active low. 0h - Disable all functions 1h - Enable glitch detectors
30	RSTB	R/W	0h	Reset - active low. To ensure proper operation, rstb must not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. 0h - Reset glitch detector flags 1h - Glitch detection flags are enabled
29-19	RESERVED	R	0h	Reserved
18-16	LP_FILTER_SEL	R/W	X	Selects the glitch detect low-pass filter bandwidth 0h - 150 kHz 1h - 125 kHz 2h - 100 kHz 3h - 80 kHz 4h - 60 kHz 5h - 45 kHz 6h - 30 kHz 7h - 15 kHz

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Table 2-277. CTRLMMR_WKUP_VDDR_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	THRESH_HI_SEL	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage 0h - 93.5% of VDD 1h - 94.0% of VDD 2h - 94.5% of VDD 3h - 95.0% of VDD 4h - 95.5% of VDD 5h - 96.0% of VDD 6h - 96.5% of VDD 7h - 97.0% of VDD 8h - 97.5% of VDD 9h - 98.0% of VDD Ah - 98.5% of VDD Bh - 99.0% of VDD Ch - 99.5% of VDD Dh - 100.0% of VDD Eh - 100.5% of VDD Fh - 101.0% of VDD 10h - 101.5% of VDD 11h - 102.0% of VDD 12h - 102.5% of VDD 13h - 103.0% of VDD 14h - 103.5% of VDD 15h - 104.0% of VDD 16h - 104.5% of VDD 17h - 105.0% of VDD 18h - 105.5% of VDD 19h - 106.0% of VDD 1Ah - 106.5% of VDD 1Bh - 107.0% of VDD 1Ch - 107.5% of VDD 1Dh - 108.0% of VDD 1Eh - 108.5% of VDD 1Fh - 109.0% of VDD

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Table 2-277. CTRLMMR_WKUP_VDDR_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 109.5% of VDD 21h - 110.0% of VDD 22h - 111.0% of VDD 23h - 112.0% of VDD 24h - 113.0% of VDD 25h - 114.0% of VDD 26h - 115.0% of VDD 27h - 116.0% of VDD 28h - 117.0% of VDD 29h - 118.0% of VDD 2Ah - 119.0% of VDD 2Bh - 120.0% of VDD 2Ch - 121.0% of VDD 2Dh - 122.0% of VDD 2Eh - 123.0% of VDD 2Fh - 124.0% of VDD 30h - 125.0% of VDD 31h - 126.0% of VDD 32h - 127.0% of VDD 33h - 128.0% of VDD 34h - 129.0% of VDD 35h - 130.0% of VDD 36h - 131.0% of VDD 37h - 132.0% of VDD 38h - 133.0% of VDD 39h - 134.0% of VDD 3Ah - 135.0% of VDD 3Bh - 136.0% of VDD 3Ch - 137.0% of VDD 3Dh - 138.0% of VDD 3Eh - 139.0% of VDD 3Fh - 140.0% of VDD
7-6	RESERVED	R	0h	Reserved

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Table 2-277. CTRLMMR_WKUP_VDDR_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	THRESH_LO_SEL	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage 0h - 106.5% of VDD 1h - 106.0% of VDD 2h - 105.5% of VDD 3h - 105.0% of VDD 4h - 104.5% of VDD 5h - 104.0% of VDD 6h - 103.5% of VDD 7h - 103.0% of VDD 8h - 102.5% of VDD 9h - 102.0% of VDD Ah - 101.5% of VDD Bh - 101.0% of VDD Ch - 100.5% of VDD Dh - 100.0% of VDD Eh - 99.5% of VDD Fh - 99.0% of VDD 10h - 98.5% of VDD 11h - 98.0% of VDD 12h - 97.5% of VDD 13h - 97.0% of VDD 14h - 96.5% of VDD 15h - 96.0% of VDD 16h - 95.5% of VDD 17h - 95.0% of VDD 18h - 94.5% of VDD 19h - 94.0% of VDD 1Ah - 93.5% of VDD 1Bh - 93.0% of VDD 1Ch - 92.5% of VDD 1Dh - 92.0% of VDD 1Eh - 91.5% of VDD 1Fh - 91.0% of VDD

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Table 2-277. CTRLMMR_WKUP_VDDR_CORE_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 90.5% of VDD 21h - 90.0% of VDD 22h - 89.0% of VDD 23h - 88.0% of VDD 24h - 87.0% of VDD 25h - 86.0% of VDD 26h - 85.0% of VDD 27h - 84.0% of VDD 28h - 83.0% of VDD 29h - 82.0% of VDD 2Ah - 81.0% of VDD 2Bh - 80.0% of VDD 2Ch - 79.0% of VDD 2Dh - 78.0% of VDD 2Eh - 77.0% of VDD 2Fh - 76.0% of VDD 30h - 75.0% of VDD 31h - 74.0% of VDD 32h - 73.0% of VDD 33h - 72.0% of VDD 34h - 71.0% of VDD 35h - 70.0% of VDD 36h - 69.0% of VDD 37h - 68.0% of VDD 38h - 67.0% of VDD 39h - 66.0% of VDD 3Ah - 65.0% of VDD 3Bh - 64.0% of VDD 3Ch - 63.0% of VDD 3Dh - 62.0% of VDD 3Eh - 61.0% of VDD 3Fh - 60.0% of VDD

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2.139 CTRLMMR_WKUP_VDD_CPU_GLDTC_STAT Register (Proxy0 Offset = 181A0h; Proxy1 Offset = 1A1A0h) [reset = X]

CTRLMMR_WKUP_VDD_CPU_GLDTC_STAT is shown in Figure 2-138 and described in Table 2-279.

Return to Summary Table.

Shows the status of the voltage glitch detector circuit monitoring the VDD_CPU voltage domain.

Table 2-278. CTRLMMR_WKUP_VDD_CPU_GLDTC_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 81A0h	4301 A1A0h

Figure 2-138. CTRLMMR_WKUP_VDD_CPU_GLDTC_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							THRESH_HI_FLAG
R-0h							R-X
7	6	5	4	3	2	1	0
RESERVED							THRESH_LOW_FLAG
R-0h							R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-279. CTRLMMR_WKUP_VDD_CPU_GLDTC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	THRESH_HI_FLAG	R	X	High voltage flag. This flag is cleared by clearing the VDD_CPU_GLDTC_CTRL_rstb bit. 0h - No high voltage detected 1h - Voltage above the high voltage threshold was detected.
7-1	RESERVED	R	0h	Reserved
0	THRESH_LOW_FLAG	R	X	Low voltage flag. This flag is cleared by clearing the VDD_CPU_GLDTC_CTRL_rstb bit. 0h - No low voltage detected 1h - Voltage below the low voltage threshold was detected.

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2.140 CTRLMMR_WKUP_VDD_CORE_GLDTC_STAT Register (Proxy0 Offset = 181B0h; Proxy1 Offset = 1A1B0h) [reset = X]

CTRLMMR_WKUP_VDD_CORE_GLDTC_STAT is shown in Figure 2-139 and described in Table 2-281.

Return to Summary Table.

Shows the status of the voltage glitch detector circuit monitoring the VDD_CORE voltage domain.

Table 2-280. CTRLMMR_WKUP_VDD_CORE_GLDTC_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 81B0h	4301 A1B0h

Figure 2-139. CTRLMMR_WKUP_VDD_CORE_GLDTC_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							THRESH_HI_FLAG
R-0h							R-X
7	6	5	4	3	2	1	0
RESERVED							THRESH_LOW_FLAG
R-0h							R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-281. CTRLMMR_WKUP_VDD_CORE_GLDTC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	THRESH_HI_FLAG	R	X	High voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. 0h - No high voltage detected 1h - Voltage above the high voltage threshold was detected.
7-1	RESERVED	R	0h	Reserved
0	THRESH_LOW_FLAG	R	X	Low voltage flag. This flag is cleared by clearing the VDD_CORE_GLDTC_CTRL_rstb bit. 0h - No low voltage detected 1h - Voltage below the low voltage threshold was detected.

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2.141 CTRLMMR_WKUP_VDDR_CPU_GLDTC_STAT Register (Proxy0 Offset = 181B4h; Proxy1 Offset = 1A1B4h) [reset = X]

CTRLMMR_WKUP_VDDR_CPU_GLDTC_STAT is shown in Figure 2-140 and described in Table 2-283.

Return to Summary Table.

Shows the status of the voltage glitch detector circuit monitoring the VDDR_CPU voltage domain.

Table 2-282. CTRLMMR_WKUP_VDDR_CPU_GLDTC_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 81B4h	4301 A1B4h

Figure 2-140. CTRLMMR_WKUP_VDDR_CPU_GLDTC_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							THRESH_HI_FLAG
R-0h							R-X
7	6	5	4	3	2	1	0
RESERVED							THRESH_LOW_FLAG
R-0h							R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-283. CTRLMMR_WKUP_VDDR_CPU_GLDTC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	THRESH_HI_FLAG	R	X	High voltage flag. This flag is cleared by clearing the VDDR_CPU_GLDTC_CTRL_rstb bit. 0h - No high voltage detected 1h - Voltage above the high voltage threshold was detected.
7-1	RESERVED	R	0h	Reserved
0	THRESH_LOW_FLAG	R	X	Low voltage flag. This flag is cleared by clearing the VDDR_CPU_GLDTC_CTRL_rstb bit. 0h - No low voltage detected 1h - Voltage below the low voltage threshold was detected.

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2.142 CTRLMMR_WKUP_VDDR_CORE_GLDTC_STAT Register (Proxy0 Offset = 181B8h; Proxy1 Offset = 1A1B8h) [reset = X]

CTRLMMR_WKUP_VDDR_CORE_GLDTC_STAT is shown in Figure 2-141 and described in Table 2-285.

Return to Summary Table.

Shows the status of the voltage glitch detector circuit monitoring the VDDR_CORE voltage domain.

Table 2-284. CTRLMMR_WKUP_VDDR_CORE_GLDTC_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 81B8h	4301 A1B8h

Figure 2-141. CTRLMMR_WKUP_VDDR_CORE_GLDTC_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							THRESH_HI_FLAG
R-0h							R-X
7	6	5	4	3	2	1	0
RESERVED							THRESH_LOW_FLAG
R-0h							R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-285. CTRLMMR_WKUP_VDDR_CORE_GLDTC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	THRESH_HI_FLAG	R	X	High voltage flag. This flag is cleared by clearing the VDDR_CORE_GLDTC_CTRL_rstb bit. 0h - No high voltage detected 1h - Voltage above the high voltage threshold was detected.
7-1	RESERVED	R	0h	Reserved
0	THRESH_LOW_FLAG	R	X	Low voltage flag. This flag is cleared by clearing the VDDR_CORE_GLDTC_CTRL_rstb bit. 0h - No low voltage detected 1h - Voltage below the low voltage threshold was detected.

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2.143 CTRLMMR_WKUP_VDD_MCU_GLDTC_CTRL Register (Proxy0 Offset = 181C0h; Proxy1 Offset = 1A1C0h) [reset = X]

CTRLMMR_WKUP_VDD_MCU_GLDTC_CTRL is shown in Figure 2-142 and described in Table 2-287.

Return to Summary Table.

Controls the voltage glitch detector circuit monitoring the VDD_MCU voltage domain.

Table 2-286. CTRLMMR_WKUP_VDD_MCU_GLDTC_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 81C0h	4301 A1C0h

Figure 2-142. CTRLMMR_WKUP_VDD_MCU_GLDTC_CTRL Register

31	30	29	28	27	26	25	24
PWDB	RSTB	RESERVED					
R/W-0h	R/W-0h	R-0h					

23	22	21	20	19	18	17	16
RESERVED					LP_FILTER_SEL		
R-0h					R/W-X		

15	14	13	12	11	10	9	8
RESERVED		THRESH_HI_SEL					
R-0h		R/W-X					

7	6	5	4	3	2	1	0
RESERVED		THRESH_LO_SEL					
R-0h		R/W-X					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-287. CTRLMMR_WKUP_VDD_MCU_GLDTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PWDB	R/W	0h	Power down - active low. 0h - Disable all functions 1h - Enable glitch detectors
30	RSTB	R/W	0h	Reset - active low. To ensure proper operation, rstb must not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. 0h - Reset glitch detector flags 1h - Glitch detection flags are enabled
29-19	RESERVED	R	0h	Reserved
18-16	LP_FILTER_SEL	R/W	X	Selects the glitch detect low-pass filter bandwidth 0h - 150 kHz 1h - 125 kHz 2h - 100 kHz 3h - 80 kHz 4h - 60 kHz 5h - 45 kHz 6h - 30 kHz 7h - 15 kHz

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Table 2-287. CTRLMMR_WKUP_VDD_MCU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	THRESH_HI_SEL	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage 0h - 93.5% of VDD 1h - 94.0% of VDD 2h - 94.5% of VDD 3h - 95.0% of VDD 4h - 95.5% of VDD 5h - 96.0% of VDD 6h - 96.5% of VDD 7h - 97.0% of VDD 8h - 97.5% of VDD 9h - 98.0% of VDD Ah - 98.5% of VDD Bh - 99.0% of VDD Ch - 99.5% of VDD Dh - 100.0% of VDD Eh - 100.5% of VDD Fh - 101.0% of VDD 10h - 101.5% of VDD 11h - 102.0% of VDD 12h - 102.5% of VDD 13h - 103.0% of VDD 14h - 103.5% of VDD 15h - 104.0% of VDD 16h - 104.5% of VDD 17h - 105.0% of VDD 18h - 105.5% of VDD 19h - 106.0% of VDD 1Ah - 106.5% of VDD 1Bh - 107.0% of VDD 1Ch - 107.5% of VDD 1Dh - 108.0% of VDD 1Eh - 108.5% of VDD 1Fh - 109.0% of VDD

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Table 2-287. CTRLMMR_WKUP_VDD_MCU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 109.5% of VDD 21h - 110.0% of VDD 22h - 111.0% of VDD 23h - 112.0% of VDD 24h - 113.0% of VDD 25h - 114.0% of VDD 26h - 115.0% of VDD 27h - 116.0% of VDD 28h - 117.0% of VDD 29h - 118.0% of VDD 2Ah - 119.0% of VDD 2Bh - 120.0% of VDD 2Ch - 121.0% of VDD 2Dh - 122.0% of VDD 2Eh - 123.0% of VDD 2Fh - 124.0% of VDD 30h - 125.0% of VDD 31h - 126.0% of VDD 32h - 127.0% of VDD 33h - 128.0% of VDD 34h - 129.0% of VDD 35h - 130.0% of VDD 36h - 131.0% of VDD 37h - 132.0% of VDD 38h - 133.0% of VDD 39h - 134.0% of VDD 3Ah - 135.0% of VDD 3Bh - 136.0% of VDD 3Ch - 137.0% of VDD 3Dh - 138.0% of VDD 3Eh - 139.0% of VDD 3Fh - 140.0% of VDD
7-6	RESERVED	R	0h	Reserved

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Table 2-287. CTRLMMR_WKUP_VDD_MCU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	THRESH_LO_SEL	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage 0h - 106.5% of VDD 1h - 106.0% of VDD 2h - 105.5% of VDD 3h - 105.0% of VDD 4h - 104.5% of VDD 5h - 104.0% of VDD 6h - 103.5% of VDD 7h - 103.0% of VDD 8h - 102.5% of VDD 9h - 102.0% of VDD Ah - 101.5% of VDD Bh - 101.0% of VDD Ch - 100.5% of VDD Dh - 100.0% of VDD Eh - 99.5% of VDD Fh - 99.0% of VDD 10h - 98.5% of VDD 11h - 98.0% of VDD 12h - 97.5% of VDD 13h - 97.0% of VDD 14h - 96.5% of VDD 15h - 96.0% of VDD 16h - 95.5% of VDD 17h - 95.0% of VDD 18h - 94.5% of VDD 19h - 94.0% of VDD 1Ah - 93.5% of VDD 1Bh - 93.0% of VDD 1Ch - 92.5% of VDD 1Dh - 92.0% of VDD 1Eh - 91.5% of VDD 1Fh - 91.0% of VDD

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Table 2-287. CTRLMMR_WKUP_VDD_MCU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 90.5% of VDD 21h - 90.0% of VDD 22h - 89.0% of VDD 23h - 88.0% of VDD 24h - 87.0% of VDD 25h - 86.0% of VDD 26h - 85.0% of VDD 27h - 84.0% of VDD 28h - 83.0% of VDD 29h - 82.0% of VDD 2Ah - 81.0% of VDD 2Bh - 80.0% of VDD 2Ch - 79.0% of VDD 2Dh - 78.0% of VDD 2Eh - 77.0% of VDD 2Fh - 76.0% of VDD 30h - 75.0% of VDD 31h - 74.0% of VDD 32h - 73.0% of VDD 33h - 72.0% of VDD 34h - 71.0% of VDD 35h - 70.0% of VDD 36h - 69.0% of VDD 37h - 68.0% of VDD 38h - 67.0% of VDD 39h - 66.0% of VDD 3Ah - 65.0% of VDD 3Bh - 64.0% of VDD 3Ch - 63.0% of VDD 3Dh - 62.0% of VDD 3Eh - 61.0% of VDD 3Fh - 60.0% of VDD

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2.144 CTRLMMR_WKUP_VDDR_MCU_GLDTC_CTRL Register (Proxy0 Offset = 181C4h; Proxy1 Offset = 1A1C4h) [reset = X]

CTRLMMR_WKUP_VDDR_MCU_GLDTC_CTRL is shown in Figure 2-143 and described in Table 2-289.

Return to Summary Table.

Controls the voltage glitch detector circuit monitoring the VDDR_MCU voltage domain.

Table 2-288. CTRLMMR_WKUP_VDDR_MCU_GLDTC_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 81C4h	4301 A1C4h

Figure 2-143. CTRLMMR_WKUP_VDDR_MCU_GLDTC_CTRL Register

31	30	29	28	27	26	25	24
PWDB	RSTB	RESERVED					
R/W-0h	R/W-0h	R-0h					

23	22	21	20	19	18	17	16
RESERVED					LP_FILTER_SEL		
R-0h					R/W-X		

15	14	13	12	11	10	9	8
RESERVED		THRESH_HI_SEL					
R-0h		R/W-X					

7	6	5	4	3	2	1	0
RESERVED		THRESH_LO_SEL					
R-0h		R/W-X					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-289. CTRLMMR_WKUP_VDDR_MCU_GLDTC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PWDB	R/W	0h	Power down - active low. 0h - Disable all functions 1h - Enable glitch detectors
30	RSTB	R/W	0h	Reset - active low. To ensure proper operation, rstb must not be de-asserted for at least 100 ns after power-up (pwdb de-asserted). Additionally, rstb must be toggled low at least 200 ns after any change in threshold or low-pass filter settings to prevent abnormal trigger events. 0h - Reset glitch detector flags 1h - Glitch detection flags are enabled
29-19	RESERVED	R	0h	Reserved
18-16	LP_FILTER_SEL	R/W	X	Selects the glitch detect low-pass filter bandwidth 0h - 150 kHz 1h - 125 kHz 2h - 100 kHz 3h - 80 kHz 4h - 60 kHz 5h - 45 kHz 6h - 30 kHz 7h - 15 kHz

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Table 2-289. CTRLMMR_WKUP_VDDR_MCU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0h	Reserved
13-8	THRESH_HI_SEL	R/W	X	Selects the high voltage glitch threshold as a percentage of the monitored voltage 0h - 93.5% of VDD 1h - 94.0% of VDD 2h - 94.5% of VDD 3h - 95.0% of VDD 4h - 95.5% of VDD 5h - 96.0% of VDD 6h - 96.5% of VDD 7h - 97.0% of VDD 8h - 97.5% of VDD 9h - 98.0% of VDD Ah - 98.5% of VDD Bh - 99.0% of VDD Ch - 99.5% of VDD Dh - 100.0% of VDD Eh - 100.5% of VDD Fh - 101.0% of VDD 10h - 101.5% of VDD 11h - 102.0% of VDD 12h - 102.5% of VDD 13h - 103.0% of VDD 14h - 103.5% of VDD 15h - 104.0% of VDD 16h - 104.5% of VDD 17h - 105.0% of VDD 18h - 105.5% of VDD 19h - 106.0% of VDD 1Ah - 106.5% of VDD 1Bh - 107.0% of VDD 1Ch - 107.5% of VDD 1Dh - 108.0% of VDD 1Eh - 108.5% of VDD 1Fh - 109.0% of VDD

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Table 2-289. CTRLMMR_WKUP_VDDR_MCU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 109.5% of VDD 21h - 110.0% of VDD 22h - 111.0% of VDD 23h - 112.0% of VDD 24h - 113.0% of VDD 25h - 114.0% of VDD 26h - 115.0% of VDD 27h - 116.0% of VDD 28h - 117.0% of VDD 29h - 118.0% of VDD 2Ah - 119.0% of VDD 2Bh - 120.0% of VDD 2Ch - 121.0% of VDD 2Dh - 122.0% of VDD 2Eh - 123.0% of VDD 2Fh - 124.0% of VDD 30h - 125.0% of VDD 31h - 126.0% of VDD 32h - 127.0% of VDD 33h - 128.0% of VDD 34h - 129.0% of VDD 35h - 130.0% of VDD 36h - 131.0% of VDD 37h - 132.0% of VDD 38h - 133.0% of VDD 39h - 134.0% of VDD 3Ah - 135.0% of VDD 3Bh - 136.0% of VDD 3Ch - 137.0% of VDD 3Dh - 138.0% of VDD 3Eh - 139.0% of VDD 3Fh - 140.0% of VDD
7-6	RESERVED	R	0h	Reserved

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Table 2-289. CTRLMMR_WKUP_VDDR_MCU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	THRESH_LO_SEL	R/W	X	Selects the low voltage glitch threshold as a percentage of the monitored voltage 0h - 106.5% of VDD 1h - 106.0% of VDD 2h - 105.5% of VDD 3h - 105.0% of VDD 4h - 104.5% of VDD 5h - 104.0% of VDD 6h - 103.5% of VDD 7h - 103.0% of VDD 8h - 102.5% of VDD 9h - 102.0% of VDD Ah - 101.5% of VDD Bh - 101.0% of VDD Ch - 100.5% of VDD Dh - 100.0% of VDD Eh - 99.5% of VDD Fh - 99.0% of VDD 10h - 98.5% of VDD 11h - 98.0% of VDD 12h - 97.5% of VDD 13h - 97.0% of VDD 14h - 96.5% of VDD 15h - 96.0% of VDD 16h - 95.5% of VDD 17h - 95.0% of VDD 18h - 94.5% of VDD 19h - 94.0% of VDD 1Ah - 93.5% of VDD 1Bh - 93.0% of VDD 1Ch - 92.5% of VDD 1Dh - 92.0% of VDD 1Eh - 91.5% of VDD 1Fh - 91.0% of VDD

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Table 2-289. CTRLMMR_WKUP_VDDR_MCU_GLDTC_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				20h - 90.5% of VDD 21h - 90.0% of VDD 22h - 89.0% of VDD 23h - 88.0% of VDD 24h - 87.0% of VDD 25h - 86.0% of VDD 26h - 85.0% of VDD 27h - 84.0% of VDD 28h - 83.0% of VDD 29h - 82.0% of VDD 2Ah - 81.0% of VDD 2Bh - 80.0% of VDD 2Ch - 79.0% of VDD 2Dh - 78.0% of VDD 2Eh - 77.0% of VDD 2Fh - 76.0% of VDD 30h - 75.0% of VDD 31h - 74.0% of VDD 32h - 73.0% of VDD 33h - 72.0% of VDD 34h - 71.0% of VDD 35h - 70.0% of VDD 36h - 69.0% of VDD 37h - 68.0% of VDD 38h - 67.0% of VDD 39h - 66.0% of VDD 3Ah - 65.0% of VDD 3Bh - 64.0% of VDD 3Ch - 63.0% of VDD 3Dh - 62.0% of VDD 3Eh - 61.0% of VDD 3Fh - 60.0% of VDD

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2.145 CTRLMMR_WKUP_VDD_MCU_GLDTC_STAT Register (Proxy0 Offset = 181D0h; Proxy1 Offset = 1A1D0h) [reset = X]

CTRLMMR_WKUP_VDD_MCU_GLDTC_STAT is shown in Figure 2-144 and described in Table 2-291.

Return to Summary Table.

Shows the status of the voltage glitch detector circuit monitoring the VDD_MCU voltage domain.

Table 2-290. CTRLMMR_WKUP_VDD_MCU_GLDTC_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 81D0h	4301 A1D0h

Figure 2-144. CTRLMMR_WKUP_VDD_MCU_GLDTC_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							THRESH_HI_FLAG
R-0h							R-X
7	6	5	4	3	2	1	0
RESERVED							THRESH_LOW_FLAG
R-0h							R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-291. CTRLMMR_WKUP_VDD_MCU_GLDTC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	THRESH_HI_FLAG	R	X	High voltage flag. This flag is cleared by clearing the VDD_MCU_GLDTC_CTRL_rstb bit. 0h - No high voltage detected 1h - Voltage above the high voltage threshold was detected.
7-1	RESERVED	R	0h	Reserved
0	THRESH_LOW_FLAG	R	X	Low voltage flag. This flag is cleared by clearing the VDD_MCU_GLDTC_CTRL_rstb bit. 0h - No low voltage detected 1h - Voltage below the low voltage threshold was detected.

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2.146 CTRLMMR_WKUP_VDDR_MCU_GLDTC_STAT Register (Proxy0 Offset = 181D4h; Proxy1 Offset = 1A1D4h) [reset = X]

CTRLMMR_WKUP_VDDR_MCU_GLDTC_STAT is shown in Figure 2-145 and described in Table 2-293.

Return to Summary Table.

Shows the status of the voltage glitch detector circuit monitoring the VDDR_MCU voltage domain.

Table 2-292. CTRLMMR_WKUP_VDDR_MCU_GLDTC_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 81D4h	4301 A1D4h

Figure 2-145. CTRLMMR_WKUP_VDDR_MCU_GLDTC_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							THRESH_HI_FLAG
R-0h							R-X
7	6	5	4	3	2	1	0
RESERVED							THRESH_LOW_FLAG
R-0h							R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 2-293. CTRLMMR_WKUP_VDDR_MCU_GLDTC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	THRESH_HI_FLAG	R	X	High voltage flag. This flag is cleared by clearing the VDDR_MCU_GLDTC_CTRL_rstb bit. 0h - No high voltage detected 1h - Voltage above the high voltage threshold was detected.
7-1	RESERVED	R	0h	Reserved
0	THRESH_LOW_FLAG	R	X	Low voltage flag. This flag is cleared by clearing the VDDR_MCU_GLDTC_CTRL_rstb bit. 0h - No low voltage detected 1h - Voltage below the low voltage threshold was detected.

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2.147 CTRLMMR_WKUP_LOCK6_KICK0 Register (Proxy0 Offset = 19008h; Proxy1 Offset = 1B008h) [reset = 0h]

CTRLMMR_WKUP_LOCK6_KICK0 is shown in Figure 2-146 and described in Table 2-295.

Return to Summary Table.

Lower 32-bits of Partition6 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_WKUP_LOCK6_KICK1 with its key value before write-protected Partition 6 registers can be written.

Table 2-294. CTRLMMR_WKUP_LOCK6_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 9008h	4301 B008h

Figure 2-146. CTRLMMR_WKUP_LOCK6_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-295. CTRLMMR_WKUP_LOCK6_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition6 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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2.148 CTRLMMR_WKUP_LOCK6_KICK1 Register (Proxy0 Offset = 1900Ch; Proxy1 Offset = 1B00Ch) [reset = 0h]

CTRLMMR_WKUP_LOCK6_KICK1 is shown in Figure 2-147 and described in Table 2-297.

Return to Summary Table.

Upper 32-bits of Partition 6 write lock key. This register must be written with the designated key value after a write to CTRLMMR_WKUP_LOCK6_KICK0 with its key value before write-protected Partition 6 registers can be written.

Table 2-296. CTRLMMR_WKUP_LOCK6_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 900Ch	4301 B00Ch

Figure 2-147. CTRLMMR_WKUP_LOCK6_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-297. CTRLMMR_WKUP_LOCK6_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition6 registers

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2.149 CTRLMMR_WKUP_P6_CLAIM0 Register (Proxy0 Offset = 19100h; Proxy1 Offset = 1B100h) [reset = 0h]

CTRLMMR_WKUP_P6_CLAIM0 is shown in Figure 2-148 and described in Table 2-299.

Return to Summary Table.

Claim bits for Partition 6 Registers.

Table 2-298. CTRLMMR_WKUP_P6_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 9100h	4301 B100h

Figure 2-148. CTRLMMR_WKUP_P6_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-299. CTRLMMR_WKUP_P6_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 10000h + (0 x 80h) + (b x 4h) and register Proxy1 address of: 12000h + (0 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.150 CTRLMMR_WKUP_P6_CLAIM1 Register (Proxy0 Offset = 19104h; Proxy1 Offset = 1B104h) [reset = 0h]

CTRLMMR_WKUP_P6_CLAIM1 is shown in Figure 2-149 and described in Table 2-301.

Return to Summary Table.

Claim bits for Partition 6 Registers.

Table 2-300. CTRLMMR_WKUP_P6_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 9104h	4301 B104h

Figure 2-149. CTRLMMR_WKUP_P6_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-301. CTRLMMR_WKUP_P6_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 10000h + (1 x 80h) + (b x 4h) and register Proxy1 address of: 12000h + (1 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.151 CTRLMMR_WKUP_P6_CLAIM2 Register (Proxy0 Offset = 19108h; Proxy1 Offset = 1B108h) [reset = 0h]

CTRLMMR_WKUP_P6_CLAIM2 is shown in Figure 2-150 and described in Table 2-303.

Return to Summary Table.

Claim bits for Partition 6 Registers.

Table 2-302. CTRLMMR_WKUP_P6_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 9108h	4301 B108h

Figure 2-150. CTRLMMR_WKUP_P6_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-303. CTRLMMR_WKUP_P6_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 10000h + (2 x 80h) + (b x 4h) and register Proxy1 address of: 12000h + (2 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.152 CTRLMMR_WKUP_P6_CLAIM3 Register (Proxy0 Offset = 1910Ch; Proxy1 Offset = 1B10Ch) [reset = 0h]

CTRLMMR_WKUP_P6_CLAIM3 is shown in Figure 2-151 and described in Table 2-305.

Return to Summary Table.

Claim bits for Partition 6 Registers.

Table 2-304. CTRLMMR_WKUP_P6_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 910Ch	4301 B10Ch

Figure 2-151. CTRLMMR_WKUP_P6_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-305. CTRLMMR_WKUP_P6_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 10000h + (3 x 80h) + (b x 4h) and register Proxy1 address of: 12000h + (3 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.153 CTRLMMR_WKUP_PADCONFIG0 Register (Proxy0 Offset = 1C000h; Proxy1 Offset = 1E000h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG0 is shown in Figure 2-152 and described in Table 2-307.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-306. CTRLMMR_WKUP_PADCONFIG0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C000h	4301 E000h

Figure 2-152. CTRLMMR_WKUP_PADCONFIG0 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-307. CTRLMMR_WKUP_PADCONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-307. CTRLMMR_WKUP_PADCONFIG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-307. CTRLMMR_WKUP_PADCONFIG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.154 CTRLMMR_WKUP_PADCONFIG1 Register (Proxy0 Offset = 1C004h; Proxy1 Offset = 1E004h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG1 is shown in Figure 2-153 and described in Table 2-309.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-308. CTRLMMR_WKUP_PADCONFIG1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C004h	4301 E004h

Figure 2-153. CTRLMMR_WKUP_PADCONFIG1 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-309. CTRLMMR_WKUP_PADCONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-309. CTRLMMR_WKUP_PADCONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-309. CTRLMMR_WKUP_PADCONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.155 CTRLMMR_WKUP_PADCONFIG2 Register (Proxy0 Offset = 1C008h; Proxy1 Offset = 1E008h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG2 is shown in Figure 2-154 and described in Table 2-311.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-310. CTRLMMR_WKUP_PADCONFIG2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C008h	4301 E008h

Figure 2-154. CTRLMMR_WKUP_PADCONFIG2 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-311. CTRLMMR_WKUP_PADCONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-311. CTRLMMR_WKUP_PADCONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-311. CTRLMMR_WKUP_PADCONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.156 CTRLMMR_WKUP_PADCONFIG3 Register (Proxy0 Offset = 1C00Ch; Proxy1 Offset = 1E00Ch) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG3 is shown in Figure 2-155 and described in Table 2-313.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-312. CTRLMMR_WKUP_PADCONFIG3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C00Ch	4301 E00Ch

Figure 2-155. CTRLMMR_WKUP_PADCONFIG3 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-313. CTRLMMR_WKUP_PADCONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-313. CTRLMMR_WKUP_PADCONFIG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-313. CTRLMMR_WKUP_PADCONFIG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.157 CTRLMMR_WKUP_PADCONFIG4 Register (Proxy0 Offset = 1C010h; Proxy1 Offset = 1E010h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG4 is shown in Figure 2-156 and described in Table 2-315.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-314. CTRLMMR_WKUP_PADCONFIG4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C010h	4301 E010h

Figure 2-156. CTRLMMR_WKUP_PADCONFIG4 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-315. CTRLMMR_WKUP_PADCONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-315. CTRLMMR_WKUP_PADCONFIG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-315. CTRLMMR_WKUP_PADCONFIG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.158 CTRLMMR_WKUP_PADCONFIG5 Register (Proxy0 Offset = 1C014h; Proxy1 Offset = 1E014h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG5 is shown in Figure 2-157 and described in Table 2-317.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-316. CTRLMMR_WKUP_PADCONFIG5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C014h	4301 E014h

Figure 2-157. CTRLMMR_WKUP_PADCONFIG5 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-317. CTRLMMR_WKUP_PADCONFIG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-317. CTRLMMR_WKUP_PADCONFIG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-317. CTRLMMR_WKUP_PADCONFIG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.159 CTRLMMR_WKUP_PADCONFIG6 Register (Proxy0 Offset = 1C018h; Proxy1 Offset = 1E018h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG6 is shown in Figure 2-158 and described in Table 2-319.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-318. CTRLMMR_WKUP_PADCONFIG6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C018h	4301 E018h

Figure 2-158. CTRLMMR_WKUP_PADCONFIG6 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-319. CTRLMMR_WKUP_PADCONFIG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-319. CTRLMMR_WKUP_PADCONFIG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-319. CTRLMMR_WKUP_PADCONFIG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.160 CTRLMMR_WKUP_PADCONFIG7 Register (Proxy0 Offset = 1C01Ch; Proxy1 Offset = 1E01Ch) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG7 is shown in Figure 2-159 and described in Table 2-321.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-320. CTRLMMR_WKUP_PADCONFIG7 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C01Ch	4301 E01Ch

Figure 2-159. CTRLMMR_WKUP_PADCONFIG7 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-321. CTRLMMR_WKUP_PADCONFIG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-321. CTRLMMR_WKUP_PADCONFIG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-321. CTRLMMR_WKUP_PADCONFIG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.161 CTRLMMR_WKUP_PADCONFIG8 Register (Proxy0 Offset = 1C020h; Proxy1 Offset = 1E020h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG8 is shown in Figure 2-160 and described in Table 2-323.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-322. CTRLMMR_WKUP_PADCONFIG8 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C020h	4301 E020h

Figure 2-160. CTRLMMR_WKUP_PADCONFIG8 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-323. CTRLMMR_WKUP_PADCONFIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-323. CTRLMMR_WKUP_PADCONFIG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-323. CTRLMMR_WKUP_PADCONFIG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.162 CTRLMMR_WKUP_PADCONFIG9 Register (Proxy0 Offset = 1C024h; Proxy1 Offset = 1E024h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG9 is shown in Figure 2-161 and described in Table 2-325.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-324. CTRLMMR_WKUP_PADCONFIG9 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C024h	4301 E024h

Figure 2-161. CTRLMMR_WKUP_PADCONFIG9 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-325. CTRLMMR_WKUP_PADCONFIG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-325. CTRLMMR_WKUP_PADCONFIG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-325. CTRLMMR_WKUP_PADCONFIG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.163 CTRLMMR_WKUP_PADCONFIG10 Register (Proxy0 Offset = 1C028h; Proxy1 Offset = 1E028h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG10 is shown in Figure 2-162 and described in Table 2-327.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-326. CTRLMMR_WKUP_PADCONFIG10 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C028h	4301 E028h

Figure 2-162. CTRLMMR_WKUP_PADCONFIG10 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-327. CTRLMMR_WKUP_PADCONFIG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-327. CTRLMMR_WKUP_PADCONFIG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-327. CTRLMMR_WKUP_PADCONFIG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.164 CTRLMMR_WKUP_PADCONFIG11 Register (Proxy0 Offset = 1C02Ch; Proxy1 Offset = 1E02Ch) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG11 is shown in Figure 2-163 and described in Table 2-329.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-328. CTRLMMR_WKUP_PADCONFIG11 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C02Ch	4301 E02Ch

Figure 2-163. CTRLMMR_WKUP_PADCONFIG11 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-329. CTRLMMR_WKUP_PADCONFIG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-329. CTRLMMR_WKUP_PADCONFIG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-329. CTRLMMR_WKUP_PADCONFIG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.165 CTRLMMR_WKUP_PADCONFIG12 Register (Proxy0 Offset = 1C030h; Proxy1 Offset = 1E030h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG12 is shown in Figure 2-164 and described in Table 2-331.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-330. CTRLMMR_WKUP_PADCONFIG12 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C030h	4301 E030h

Figure 2-164. CTRLMMR_WKUP_PADCONFIG12 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-331. CTRLMMR_WKUP_PADCONFIG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-331. CTRLMMR_WKUP_PADCONFIG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-331. CTRLMMR_WKUP_PADCONFIG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.166 CTRLMMR_WKUP_PADCONFIG13 Register (Proxy0 Offset = 1C034h; Proxy1 Offset = 1E034h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG13 is shown in Figure 2-165 and described in Table 2-333.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-332. CTRLMMR_WKUP_PADCONFIG13 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C034h	4301 E034h

Figure 2-165. CTRLMMR_WKUP_PADCONFIG13 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-333. CTRLMMR_WKUP_PADCONFIG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-333. CTRLMMR_WKUP_PADCONFIG13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-333. CTRLMMR_WKUP_PADCONFIG13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.167 CTRLMMR_WKUP_PADCONFIG14 Register (Proxy0 Offset = 1C038h; Proxy1 Offset = 1E038h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG14 is shown in Figure 2-166 and described in Table 2-335.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-334. CTRLMMR_WKUP_PADCONFIG14 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C038h	4301 E038h

Figure 2-166. CTRLMMR_WKUP_PADCONFIG14 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-335. CTRLMMR_WKUP_PADCONFIG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-335. CTRLMMR_WKUP_PADCONFIG14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-335. CTRLMMR_WKUP_PADCONFIG14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.168 CTRLMMR_WKUP_PADCONFIG15 Register (Proxy0 Offset = 1C03Ch; Proxy1 Offset = 1E03Ch) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG15 is shown in Figure 2-167 and described in Table 2-337.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-336. CTRLMMR_WKUP_PADCONFIG15 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C03Ch	4301 E03Ch

Figure 2-167. CTRLMMR_WKUP_PADCONFIG15 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-337. CTRLMMR_WKUP_PADCONFIG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-337. CTRLMMR_WKUP_PADCONFIG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-337. CTRLMMR_WKUP_PADCONFIG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.169 CTRLMMR_WKUP_PADCONFIG16 Register (Proxy0 Offset = 1C040h; Proxy1 Offset = 1E040h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG16 is shown in Figure 2-168 and described in Table 2-339.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-338. CTRLMMR_WKUP_PADCONFIG16 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C040h	4301 E040h

Figure 2-168. CTRLMMR_WKUP_PADCONFIG16 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-339. CTRLMMR_WKUP_PADCONFIG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-339. CTRLMMR_WKUP_PADCONFIG16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-339. CTRLMMR_WKUP_PADCONFIG16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.170 CTRLMMR_WKUP_PADCONFIG17 Register (Proxy0 Offset = 1C044h; Proxy1 Offset = 1E044h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG17 is shown in Figure 2-169 and described in Table 2-341.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-340. CTRLMMR_WKUP_PADCONFIG17 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C044h	4301 E044h

Figure 2-169. CTRLMMR_WKUP_PADCONFIG17 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-341. CTRLMMR_WKUP_PADCONFIG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-341. CTRLMMR_WKUP_PADCONFIG17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-341. CTRLMMR_WKUP_PADCONFIG17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.171 CTRLMMR_WKUP_PADCONFIG18 Register (Proxy0 Offset = 1C048h; Proxy1 Offset = 1E048h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG18 is shown in Figure 2-170 and described in Table 2-343.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-342. CTRLMMR_WKUP_PADCONFIG18 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C048h	4301 E048h

Figure 2-170. CTRLMMR_WKUP_PADCONFIG18 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-343. CTRLMMR_WKUP_PADCONFIG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-343. CTRLMMR_WKUP_PADCONFIG18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-343. CTRLMMR_WKUP_PADCONFIG18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.172 CTRLMMR_WKUP_PADCONFIG19 Register (Proxy0 Offset = 1C04Ch; Proxy1 Offset = 1E04Ch) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG19 is shown in Figure 2-171 and described in Table 2-345.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-344. CTRLMMR_WKUP_PADCONFIG19 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C04Ch	4301 E04Ch

Figure 2-171. CTRLMMR_WKUP_PADCONFIG19 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-345. CTRLMMR_WKUP_PADCONFIG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-345. CTRLMMR_WKUP_PADCONFIG19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-345. CTRLMMR_WKUP_PADCONFIG19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.173 CTRLMMR_WKUP_PADCONFIG20 Register (Proxy0 Offset = 1C050h; Proxy1 Offset = 1E050h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG20 is shown in Figure 2-172 and described in Table 2-347.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-346. CTRLMMR_WKUP_PADCONFIG20 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C050h	4301 E050h

Figure 2-172. CTRLMMR_WKUP_PADCONFIG20 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-347. CTRLMMR_WKUP_PADCONFIG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-347. CTRLMMR_WKUP_PADCONFIG20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-347. CTRLMMR_WKUP_PADCONFIG20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.174 CTRLMMR_WKUP_PADCONFIG21 Register (Proxy0 Offset = 1C054h; Proxy1 Offset = 1E054h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG21 is shown in Figure 2-173 and described in Table 2-349.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-348. CTRLMMR_WKUP_PADCONFIG21 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C054h	4301 E054h

Figure 2-173. CTRLMMR_WKUP_PADCONFIG21 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-349. CTRLMMR_WKUP_PADCONFIG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-349. CTRLMMR_WKUP_PADCONFIG21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-349. CTRLMMR_WKUP_PADCONFIG21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.175 CTRLMMR_WKUP_PADCONFIG22 Register (Proxy0 Offset = 1C058h; Proxy1 Offset = 1E058h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG22 is shown in Figure 2-174 and described in Table 2-351.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-350. CTRLMMR_WKUP_PADCONFIG22 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C058h	4301 E058h

Figure 2-174. CTRLMMR_WKUP_PADCONFIG22 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-351. CTRLMMR_WKUP_PADCONFIG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-351. CTRLMMR_WKUP_PADCONFIG22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-351. CTRLMMR_WKUP_PADCONFIG22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.176 CTRLMMR_WKUP_PADCONFIG23 Register (Proxy0 Offset = 1C05Ch; Proxy1 Offset = 1E05Ch) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG23 is shown in Figure 2-175 and described in Table 2-353.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-352. CTRLMMR_WKUP_PADCONFIG23 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C05Ch	4301 E05Ch

Figure 2-175. CTRLMMR_WKUP_PADCONFIG23 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-353. CTRLMMR_WKUP_PADCONFIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-353. CTRLMMR_WKUP_PADCONFIG23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-353. CTRLMMR_WKUP_PADCONFIG23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.177 CTRLMMR_WKUP_PADCONFIG24 Register (Proxy0 Offset = 1C060h; Proxy1 Offset = 1E060h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG24 is shown in Figure 2-176 and described in Table 2-355.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-354. CTRLMMR_WKUP_PADCONFIG24 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C060h	4301 E060h

Figure 2-176. CTRLMMR_WKUP_PADCONFIG24 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-355. CTRLMMR_WKUP_PADCONFIG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-355. CTRLMMR_WKUP_PADCONFIG24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-355. CTRLMMR_WKUP_PADCONFIG24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.178 CTRLMMR_WKUP_PADCONFIG25 Register (Proxy0 Offset = 1C064h; Proxy1 Offset = 1E064h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG25 is shown in Figure 2-177 and described in Table 2-357.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-356. CTRLMMR_WKUP_PADCONFIG25 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C064h	4301 E064h

Figure 2-177. CTRLMMR_WKUP_PADCONFIG25 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-357. CTRLMMR_WKUP_PADCONFIG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-357. CTRLMMR_WKUP_PADCONFIG25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-357. CTRLMMR_WKUP_PADCONFIG25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.179 CTRLMMR_WKUP_PADCONFIG26 Register (Proxy0 Offset = 1C068h; Proxy1 Offset = 1E068h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG26 is shown in Figure 2-178 and described in Table 2-359.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-358. CTRLMMR_WKUP_PADCONFIG26 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C068h	4301 E068h

Figure 2-178. CTRLMMR_WKUP_PADCONFIG26 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-359. CTRLMMR_WKUP_PADCONFIG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-359. CTRLMMR_WKUP_PADCONFIG26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-359. CTRLMMR_WKUP_PADCONFIG26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.180 CTRLMMR_WKUP_PADCONFIG27 Register (Proxy0 Offset = 1C06Ch; Proxy1 Offset = 1E06Ch) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG27 is shown in Figure 2-179 and described in Table 2-361.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-360. CTRLMMR_WKUP_PADCONFIG27 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C06Ch	4301 E06Ch

Figure 2-179. CTRLMMR_WKUP_PADCONFIG27 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-361. CTRLMMR_WKUP_PADCONFIG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-361. CTRLMMR_WKUP_PADCONFIG27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-361. CTRLMMR_WKUP_PADCONFIG27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.181 CTRLMMR_WKUP_PADCONFIG28 Register (Proxy0 Offset = 1C070h; Proxy1 Offset = 1E070h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG28 is shown in Figure 2-180 and described in Table 2-363.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-362. CTRLMMR_WKUP_PADCONFIG28 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C070h	4301 E070h

Figure 2-180. CTRLMMR_WKUP_PADCONFIG28 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-363. CTRLMMR_WKUP_PADCONFIG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-363. CTRLMMR_WKUP_PADCONFIG28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-363. CTRLMMR_WKUP_PADCONFIG28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.182 CTRLMMR_WKUP_PADCONFIG29 Register (Proxy0 Offset = 1C074h; Proxy1 Offset = 1E074h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG29 is shown in Figure 2-181 and described in Table 2-365.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-364. CTRLMMR_WKUP_PADCONFIG29 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C074h	4301 E074h

Figure 2-181. CTRLMMR_WKUP_PADCONFIG29 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-365. CTRLMMR_WKUP_PADCONFIG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-365. CTRLMMR_WKUP_PADCONFIG29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-365. CTRLMMR_WKUP_PADCONFIG29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.183 CTRLMMR_WKUP_PADCONFIG30 Register (Proxy0 Offset = 1C078h; Proxy1 Offset = 1E078h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG30 is shown in Figure 2-182 and described in Table 2-367.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-366. CTRLMMR_WKUP_PADCONFIG30 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C078h	4301 E078h

Figure 2-182. CTRLMMR_WKUP_PADCONFIG30 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-367. CTRLMMR_WKUP_PADCONFIG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-367. CTRLMMR_WKUP_PADCONFIG30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-367. CTRLMMR_WKUP_PADCONFIG30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.184 CTRLMMR_WKUP_PADCONFIG31 Register (Proxy0 Offset = 1C07Ch; Proxy1 Offset = 1E07Ch) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG31 is shown in Figure 2-183 and described in Table 2-369.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-368. CTRLMMR_WKUP_PADCONFIG31 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C07Ch	4301 E07Ch

Figure 2-183. CTRLMMR_WKUP_PADCONFIG31 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-369. CTRLMMR_WKUP_PADCONFIG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-369. CTRLMMR_WKUP_PADCONFIG31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-369. CTRLMMR_WKUP_PADCONFIG31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.185 CTRLMMR_WKUP_PADCONFIG32 Register (Proxy0 Offset = 1C080h; Proxy1 Offset = 1E080h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG32 is shown in Figure 2-184 and described in Table 2-371.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-370. CTRLMMR_WKUP_PADCONFIG32 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C080h	4301 E080h

Figure 2-184. CTRLMMR_WKUP_PADCONFIG32 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-371. CTRLMMR_WKUP_PADCONFIG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-371. CTRLMMR_WKUP_PADCONFIG32 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-371. CTRLMMR_WKUP_PADCONFIG32 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.186 CTRLMMR_WKUP_PADCONFIG33 Register (Proxy0 Offset = 1C084h; Proxy1 Offset = 1E084h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG33 is shown in Figure 2-185 and described in Table 2-373.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-372. CTRLMMR_WKUP_PADCONFIG33 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C084h	4301 E084h

Figure 2-185. CTRLMMR_WKUP_PADCONFIG33 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-373. CTRLMMR_WKUP_PADCONFIG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-373. CTRLMMR_WKUP_PADCONFIG33 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-373. CTRLMMR_WKUP_PADCONFIG33 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.187 CTRLMMR_WKUP_PADCONFIG34 Register (Proxy0 Offset = 1C088h; Proxy1 Offset = 1E088h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG34 is shown in Figure 2-186 and described in Table 2-375.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-374. CTRLMMR_WKUP_PADCONFIG34 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C088h	4301 E088h

Figure 2-186. CTRLMMR_WKUP_PADCONFIG34 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-375. CTRLMMR_WKUP_PADCONFIG34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-375. CTRLMMR_WKUP_PADCONFIG34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-375. CTRLMMR_WKUP_PADCONFIG34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.188 CTRLMMR_WKUP_PADCONFIG35 Register (Proxy0 Offset = 1C08Ch; Proxy1 Offset = 1E08Ch) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG35 is shown in Figure 2-187 and described in Table 2-377.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-376. CTRLMMR_WKUP_PADCONFIG35 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C08Ch	4301 E08Ch

Figure 2-187. CTRLMMR_WKUP_PADCONFIG35 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-377. CTRLMMR_WKUP_PADCONFIG35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-377. CTRLMMR_WKUP_PADCONFIG35 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-377. CTRLMMR_WKUP_PADCONFIG35 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.189 CTRLMMR_WKUP_PADCONFIG36 Register (Proxy0 Offset = 1C090h; Proxy1 Offset = 1E090h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG36 is shown in Figure 2-188 and described in Table 2-379.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-378. CTRLMMR_WKUP_PADCONFIG36 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C090h	4301 E090h

Figure 2-188. CTRLMMR_WKUP_PADCONFIG36 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-379. CTRLMMR_WKUP_PADCONFIG36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-379. CTRLMMR_WKUP_PADCONFIG36 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-379. CTRLMMR_WKUP_PADCONFIG36 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.190 CTRLMMR_WKUP_PADCONFIG37 Register (Proxy0 Offset = 1C094h; Proxy1 Offset = 1E094h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG37 is shown in Figure 2-189 and described in Table 2-381.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-380. CTRLMMR_WKUP_PADCONFIG37 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C094h	4301 E094h

Figure 2-189. CTRLMMR_WKUP_PADCONFIG37 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-381. CTRLMMR_WKUP_PADCONFIG37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-381. CTRLMMR_WKUP_PADCONFIG37 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-381. CTRLMMR_WKUP_PADCONFIG37 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.191 CTRLMMR_WKUP_PADCONFIG38 Register (Proxy0 Offset = 1C098h; Proxy1 Offset = 1E098h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG38 is shown in Figure 2-190 and described in Table 2-383.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-382. CTRLMMR_WKUP_PADCONFIG38 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C098h	4301 E098h

Figure 2-190. CTRLMMR_WKUP_PADCONFIG38 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-383. CTRLMMR_WKUP_PADCONFIG38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-383. CTRLMMR_WKUP_PADCONFIG38 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-383. CTRLMMR_WKUP_PADCONFIG38 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.192 CTRLMMR_WKUP_PADCONFIG39 Register (Proxy0 Offset = 1C09Ch; Proxy1 Offset = 1E09Ch) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG39 is shown in Figure 2-191 and described in Table 2-385.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-384. CTRLMMR_WKUP_PADCONFIG39 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C09Ch	4301 E09Ch

Figure 2-191. CTRLMMR_WKUP_PADCONFIG39 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-385. CTRLMMR_WKUP_PADCONFIG39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-385. CTRLMMR_WKUP_PADCONFIG39 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-385. CTRLMMR_WKUP_PADCONFIG39 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.193 CTRLMMR_WKUP_PADCONFIG40 Register (Proxy0 Offset = 1C0A0h; Proxy1 Offset = 1E0A0h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG40 is shown in Figure 2-192 and described in Table 2-387.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-386. CTRLMMR_WKUP_PADCONFIG40 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0A0h	4301 E0A0h

Figure 2-192. CTRLMMR_WKUP_PADCONFIG40 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-387. CTRLMMR_WKUP_PADCONFIG40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-387. CTRLMMR_WKUP_PADCONFIG40 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-387. CTRLMMR_WKUP_PADCONFIG40 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.194 CTRLMMR_WKUP_PADCONFIG41 Register (Proxy0 Offset = 1C0A4h; Proxy1 Offset = 1E0A4h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG41 is shown in Figure 2-193 and described in Table 2-389.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-388. CTRLMMR_WKUP_PADCONFIG41 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0A4h	4301 E0A4h

Figure 2-193. CTRLMMR_WKUP_PADCONFIG41 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-389. CTRLMMR_WKUP_PADCONFIG41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-389. CTRLMMR_WKUP_PADCONFIG41 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-389. CTRLMMR_WKUP_PADCONFIG41 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.195 CTRLMMR_WKUP_PADCONFIG42 Register (Proxy0 Offset = 1C0A8h; Proxy1 Offset = 1E0A8h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG42 is shown in Figure 2-194 and described in Table 2-391.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-390. CTRLMMR_WKUP_PADCONFIG42 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0A8h	4301 E0A8h

Figure 2-194. CTRLMMR_WKUP_PADCONFIG42 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-391. CTRLMMR_WKUP_PADCONFIG42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-391. CTRLMMR_WKUP_PADCONFIG42 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-391. CTRLMMR_WKUP_PADCONFIG42 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.196 CTRLMMR_WKUP_PADCONFIG43 Register (Proxy0 Offset = 1C0ACh; Proxy1 Offset = 1E0ACh) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG43 is shown in Figure 2-195 and described in Table 2-393.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-392. CTRLMMR_WKUP_PADCONFIG43 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0ACh	4301 E0ACh

Figure 2-195. CTRLMMR_WKUP_PADCONFIG43 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-393. CTRLMMR_WKUP_PADCONFIG43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-393. CTRLMMR_WKUP_PADCONFIG43 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-393. CTRLMMR_WKUP_PADCONFIG43 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.197 CTRLMMR_WKUP_PADCONFIG44 Register (Proxy0 Offset = 1C0B0h; Proxy1 Offset = 1E0B0h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG44 is shown in Figure 2-196 and described in Table 2-395.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-394. CTRLMMR_WKUP_PADCONFIG44 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0B0h	4301 E0B0h

Figure 2-196. CTRLMMR_WKUP_PADCONFIG44 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-395. CTRLMMR_WKUP_PADCONFIG44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-395. CTRLMMR_WKUP_PADCONFIG44 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-395. CTRLMMR_WKUP_PADCONFIG44 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.198 CTRLMMR_WKUP_PADCONFIG45 Register (Proxy0 Offset = 1C0B4h; Proxy1 Offset = 1E0B4h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG45 is shown in Figure 2-197 and described in Table 2-397.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-396. CTRLMMR_WKUP_PADCONFIG45 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0B4h	4301 E0B4h

Figure 2-197. CTRLMMR_WKUP_PADCONFIG45 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-397. CTRLMMR_WKUP_PADCONFIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-397. CTRLMMR_WKUP_PADCONFIG45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-397. CTRLMMR_WKUP_PADCONFIG45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.199 CTRLMMR_WKUP_PADCONFIG46 Register (Proxy0 Offset = 1C0B8h; Proxy1 Offset = 1E0B8h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG46 is shown in Figure 2-198 and described in Table 2-399.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-398. CTRLMMR_WKUP_PADCONFIG46 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0B8h	4301 E0B8h

Figure 2-198. CTRLMMR_WKUP_PADCONFIG46 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-399. CTRLMMR_WKUP_PADCONFIG46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-399. CTRLMMR_WKUP_PADCONFIG46 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-399. CTRLMMR_WKUP_PADCONFIG46 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.200 CTRLMMR_WKUP_PADCONFIG47 Register (Proxy0 Offset = 1C0BCh; Proxy1 Offset = 1E0BCh) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG47 is shown in Figure 2-199 and described in Table 2-401.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-400. CTRLMMR_WKUP_PADCONFIG47 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0BCh	4301 E0BCh

Figure 2-199. CTRLMMR_WKUP_PADCONFIG47 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-401. CTRLMMR_WKUP_PADCONFIG47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-401. CTRLMMR_WKUP_PADCONFIG47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-401. CTRLMMR_WKUP_PADCONFIG47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.201 CTRLMMR_WKUP_PADCONFIG48 Register (Proxy0 Offset = 1C0C0h; Proxy1 Offset = 1E0C0h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG48 is shown in Figure 2-200 and described in Table 2-403.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-402. CTRLMMR_WKUP_PADCONFIG48 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0C0h	4301 E0C0h

Figure 2-200. CTRLMMR_WKUP_PADCONFIG48 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-403. CTRLMMR_WKUP_PADCONFIG48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-403. CTRLMMR_WKUP_PADCONFIG48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-403. CTRLMMR_WKUP_PADCONFIG48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.202 CTRLMMR_WKUP_PADCONFIG49 Register (Proxy0 Offset = 1C0C4h; Proxy1 Offset = 1E0C4h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG49 is shown in Figure 2-201 and described in Table 2-405.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-404. CTRLMMR_WKUP_PADCONFIG49 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0C4h	4301 E0C4h

Figure 2-201. CTRLMMR_WKUP_PADCONFIG49 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-405. CTRLMMR_WKUP_PADCONFIG49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-405. CTRLMMR_WKUP_PADCONFIG49 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-405. CTRLMMR_WKUP_PADCONFIG49 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.203 CTRLMMR_WKUP_PADCONFIG50 Register (Proxy0 Offset = 1C0C8h; Proxy1 Offset = 1E0C8h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG50 is shown in Figure 2-202 and described in Table 2-407.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-406. CTRLMMR_WKUP_PADCONFIG50 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0C8h	4301 E0C8h

Figure 2-202. CTRLMMR_WKUP_PADCONFIG50 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-407. CTRLMMR_WKUP_PADCONFIG50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-407. CTRLMMR_WKUP_PADCONFIG50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-407. CTRLMMR_WKUP_PADCONFIG50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.204 CTRLMMR_WKUP_PADCONFIG51 Register (Proxy0 Offset = 1C0CCh; Proxy1 Offset = 1E0CCh) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG51 is shown in Figure 2-203 and described in Table 2-409.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-408. CTRLMMR_WKUP_PADCONFIG51 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0CCh	4301 E0CCh

Figure 2-203. CTRLMMR_WKUP_PADCONFIG51 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-409. CTRLMMR_WKUP_PADCONFIG51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-409. CTRLMMR_WKUP_PADCONFIG51 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-409. CTRLMMR_WKUP_PADCONFIG51 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.205 CTRLMMR_WKUP_PADCONFIG52 Register (Proxy0 Offset = 1C0D0h; Proxy1 Offset = 1E0D0h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG52 is shown in Figure 2-204 and described in Table 2-411.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-410. CTRLMMR_WKUP_PADCONFIG52 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0D0h	4301 E0D0h

Figure 2-204. CTRLMMR_WKUP_PADCONFIG52 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-411. CTRLMMR_WKUP_PADCONFIG52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-411. CTRLMMR_WKUP_PADCONFIG52 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-411. CTRLMMR_WKUP_PADCONFIG52 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.206 CTRLMMR_WKUP_PADCONFIG53 Register (Proxy0 Offset = 1C0D4h; Proxy1 Offset = 1E0D4h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG53 is shown in Figure 2-205 and described in Table 2-413.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-412. CTRLMMR_WKUP_PADCONFIG53 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0D4h	4301 E0D4h

Figure 2-205. CTRLMMR_WKUP_PADCONFIG53 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-413. CTRLMMR_WKUP_PADCONFIG53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-413. CTRLMMR_WKUP_PADCONFIG53 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-413. CTRLMMR_WKUP_PADCONFIG53 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.207 CTRLMMR_WKUP_PADCONFIG54 Register (Proxy0 Offset = 1C0D8h; Proxy1 Offset = 1E0D8h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG54 is shown in Figure 2-206 and described in Table 2-415.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-414. CTRLMMR_WKUP_PADCONFIG54 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0D8h	4301 E0D8h

Figure 2-206. CTRLMMR_WKUP_PADCONFIG54 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-415. CTRLMMR_WKUP_PADCONFIG54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-415. CTRLMMR_WKUP_PADCONFIG54 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-415. CTRLMMR_WKUP_PADCONFIG54 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.208 CTRLMMR_WKUP_PADCONFIG55 Register (Proxy0 Offset = 1C0DCh; Proxy1 Offset = 1E0DCh) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG55 is shown in Figure 2-207 and described in Table 2-417.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-416. CTRLMMR_WKUP_PADCONFIG55 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0DCh	4301 E0DCh

Figure 2-207. CTRLMMR_WKUP_PADCONFIG55 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-417. CTRLMMR_WKUP_PADCONFIG55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-417. CTRLMMR_WKUP_PADCONFIG55 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-417. CTRLMMR_WKUP_PADCONFIG55 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.209 CTRLMMR_WKUP_PADCONFIG56 Register (Proxy0 Offset = 1C0E0h; Proxy1 Offset = 1E0E0h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG56 is shown in Figure 2-208 and described in Table 2-419.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-418. CTRLMMR_WKUP_PADCONFIG56 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0E0h	4301 E0E0h

Figure 2-208. CTRLMMR_WKUP_PADCONFIG56 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-419. CTRLMMR_WKUP_PADCONFIG56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-419. CTRLMMR_WKUP_PADCONFIG56 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-419. CTRLMMR_WKUP_PADCONFIG56 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.210 CTRLMMR_WKUP_PADCONFIG57 Register (Proxy0 Offset = 1C0E4h; Proxy1 Offset = 1E0E4h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG57 is shown in Figure 2-209 and described in Table 2-421.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-420. CTRLMMR_WKUP_PADCONFIG57 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0E4h	4301 E0E4h

Figure 2-209. CTRLMMR_WKUP_PADCONFIG57 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-421. CTRLMMR_WKUP_PADCONFIG57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-421. CTRLMMR_WKUP_PADCONFIG57 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-421. CTRLMMR_WKUP_PADCONFIG57 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.211 CTRLMMR_WKUP_PADCONFIG58 Register (Proxy0 Offset = 1C0E8h; Proxy1 Offset = 1E0E8h) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG58 is shown in Figure 2-210 and described in Table 2-423.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-422. CTRLMMR_WKUP_PADCONFIG58 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0E8h	4301 E0E8h

Figure 2-210. CTRLMMR_WKUP_PADCONFIG58 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-423. CTRLMMR_WKUP_PADCONFIG58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-423. CTRLMMR_WKUP_PADCONFIG58 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-423. CTRLMMR_WKUP_PADCONFIG58 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.212 CTRLMMR_WKUP_PADCONFIG59 Register (Proxy0 Offset = 1C0ECh; Proxy1 Offset = 1E0ECh) [reset = 8254007h]

CTRLMMR_WKUP_PADCONFIG59 is shown in Figure 2-211 and described in Table 2-425.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-424. CTRLMMR_WKUP_PADCONFIG59 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0ECh	4301 E0ECh

Figure 2-211. CTRLMMR_WKUP_PADCONFIG59 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-425. CTRLMMR_WKUP_PADCONFIG59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-425. CTRLMMR_WKUP_PADCONFIG59 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-425. CTRLMMR_WKUP_PADCONFIG59 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.213 CTRLMMR_WKUP_PADCONFIG60 Register (Proxy0 Offset = 1C0F0h; Proxy1 Offset = 1E0F0h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG60 is shown in Figure 2-212 and described in Table 2-427.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-426. CTRLMMR_WKUP_PADCONFIG60 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0F0h	4301 E0F0h

Figure 2-212. CTRLMMR_WKUP_PADCONFIG60 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-427. CTRLMMR_WKUP_PADCONFIG60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-427. CTRLMMR_WKUP_PADCONFIG60 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-427. CTRLMMR_WKUP_PADCONFIG60 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.214 CTRLMMR_WKUP_PADCONFIG61 Register (Proxy0 Offset = 1C0F4h; Proxy1 Offset = 1E0F4h) [reset = 8214007h]

CTRLMMR_WKUP_PADCONFIG61 is shown in Figure 2-213 and described in Table 2-429.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-428. CTRLMMR_WKUP_PADCONFIG61 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0F4h	4301 E0F4h

Figure 2-213. CTRLMMR_WKUP_PADCONFIG61 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-429. CTRLMMR_WKUP_PADCONFIG61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-429. CTRLMMR_WKUP_PADCONFIG61 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-429. CTRLMMR_WKUP_PADCONFIG61 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.215 CTRLMMR_WKUP_PADCONFIG62 Register (Proxy0 Offset = 1C0F8h; Proxy1 Offset = 1E0F8h) [reset = 44000h]

CTRLMMR_WKUP_PADCONFIG62 is shown in Figure 2-214 and described in Table 2-431.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-430. CTRLMMR_WKUP_PADCONFIG62 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0F8h	4301 E0F8h

Figure 2-214. CTRLMMR_WKUP_PADCONFIG62 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	RESERVED		DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R-0h	

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-431. CTRLMMR_WKUP_PADCONFIG62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28-27	RESERVED	R	0h	Reserved
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active

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Table 2-431. CTRLMMR_WKUP_PADCONFIG62 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17-16	RESERVED	R	0h	Reserved
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.216 CTRLMMR_WKUP_PADCONFIG63 Register (Proxy0 Offset = 1C0FCh; Proxy1 Offset = 1E0FCh) [reset = 44000h]

CTRLMMR_WKUP_PADCONFIG63 is shown in Figure 2-215 and described in Table 2-433.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-432. CTRLMMR_WKUP_PADCONFIG63 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C0FCh	4301 E0FCh

Figure 2-215. CTRLMMR_WKUP_PADCONFIG63 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	RESERVED		DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R-0h	

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-433. CTRLMMR_WKUP_PADCONFIG63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28-27	RESERVED	R	0h	Reserved
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active

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Table 2-433. CTRLMMR_WKUP_PADCONFIG63 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17-16	RESERVED	R	0h	Reserved
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.217 CTRLMMR_WKUP_PADCONFIG64 Register (Proxy0 Offset = 1C100h; Proxy1 Offset = 1E100h) [reset = 44000h]

CTRLMMR_WKUP_PADCONFIG64 is shown in Figure 2-216 and described in Table 2-435.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-434. CTRLMMR_WKUP_PADCONFIG64 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C100h	4301 E100h

Figure 2-216. CTRLMMR_WKUP_PADCONFIG64 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	RESERVED		DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R-0h	

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-435. CTRLMMR_WKUP_PADCONFIG64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28-27	RESERVED	R	0h	Reserved
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active

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Table 2-435. CTRLMMR_WKUP_PADCONFIG64 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17-16	RESERVED	R	0h	Reserved
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.218 CTRLMMR_WKUP_PADCONFIG65 Register (Proxy0 Offset = 1C104h; Proxy1 Offset = 1E104h) [reset = 44000h]

CTRLMMR_WKUP_PADCONFIG65 is shown in Figure 2-217 and described in Table 2-437.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-436. CTRLMMR_WKUP_PADCONFIG65 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C104h	4301 E104h

Figure 2-217. CTRLMMR_WKUP_PADCONFIG65 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	RESERVED		DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R-0h	

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-437. CTRLMMR_WKUP_PADCONFIG65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28-27	RESERVED	R	0h	Reserved
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active

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Table 2-437. CTRLMMR_WKUP_PADCONFIG65 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17-16	RESERVED	R	0h	Reserved
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.219 CTRLMMR_WKUP_PADCONFIG66 Register (Proxy0 Offset = 1C108h; Proxy1 Offset = 1E108h) [reset = 8014007h]

CTRLMMR_WKUP_PADCONFIG66 is shown in Figure 2-218 and described in Table 2-439.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-438. CTRLMMR_WKUP_PADCONFIG66 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C108h	4301 E108h

Figure 2-218. CTRLMMR_WKUP_PADCONFIG66 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-439. CTRLMMR_WKUP_PADCONFIG66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-439. CTRLMMR_WKUP_PADCONFIG66 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-439. CTRLMMR_WKUP_PADCONFIG66 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.220 CTRLMMR_WKUP_PADCONFIG67 Register (Proxy0 Offset = 1C10Ch; Proxy1 Offset = 1E10Ch) [reset = 8014000h]

CTRLMMR_WKUP_PADCONFIG67 is shown in Figure 2-219 and described in Table 2-441.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-440. CTRLMMR_WKUP_PADCONFIG67 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C10Ch	4301 E10Ch

Figure 2-219. CTRLMMR_WKUP_PADCONFIG67 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-441. CTRLMMR_WKUP_PADCONFIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-441. CTRLMMR_WKUP_PADCONFIG67 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-441. CTRLMMR_WKUP_PADCONFIG67 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.221 CTRLMMR_WKUP_PADCONFIG68 Register (Proxy0 Offset = 1C110h; Proxy1 Offset = 1E110h) [reset = 44000h]

CTRLMMR_WKUP_PADCONFIG68 is shown in Figure 2-220 and described in Table 2-443.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-442. CTRLMMR_WKUP_PADCONFIG68 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C110h	4301 E110h

Figure 2-220. CTRLMMR_WKUP_PADCONFIG68 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-1h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-443. CTRLMMR_WKUP_PADCONFIG68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-443. CTRLMMR_WKUP_PADCONFIG68 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-443. CTRLMMR_WKUP_PADCONFIG68 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.222 CTRLMMR_WKUP_PADCONFIG69 Register (Proxy0 Offset = 1C114h; Proxy1 Offset = 1E114h) [reset = 10264000h]

CTRLMMR_WKUP_PADCONFIG69 is shown in Figure 2-221 and described in Table 2-445.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-444. CTRLMMR_WKUP_PADCONFIG69 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C114h	4301 E114h

Figure 2-221. CTRLMMR_WKUP_PADCONFIG69 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-445. CTRLMMR_WKUP_PADCONFIG69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	1h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-445. CTRLMMR_WKUP_PADCONFIG69 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-445. CTRLMMR_WKUP_PADCONFIG69 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.223 CTRLMMR_WKUP_PADCONFIG70 Register (Proxy0 Offset = 1C118h; Proxy1 Offset = 1E118h) [reset = 8014000h]

CTRLMMR_WKUP_PADCONFIG70 is shown in Figure 2-222 and described in Table 2-447.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-446. CTRLMMR_WKUP_PADCONFIG70 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C118h	4301 E118h

Figure 2-222. CTRLMMR_WKUP_PADCONFIG70 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-447. CTRLMMR_WKUP_PADCONFIG70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-447. CTRLMMR_WKUP_PADCONFIG70 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-447. CTRLMMR_WKUP_PADCONFIG70 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.224 CTRLMMR_WKUP_PADCONFIG71 Register (Proxy0 Offset = 1C11Ch; Proxy1 Offset = 1E11Ch) [reset = 8014000h]

CTRLMMR_WKUP_PADCONFIG71 is shown in Figure 2-223 and described in Table 2-449.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-448. CTRLMMR_WKUP_PADCONFIG71 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C11Ch	4301 E11Ch

Figure 2-223. CTRLMMR_WKUP_PADCONFIG71 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-449. CTRLMMR_WKUP_PADCONFIG71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-449. CTRLMMR_WKUP_PADCONFIG71 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-449. CTRLMMR_WKUP_PADCONFIG71 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.225 CTRLMMR_WKUP_PADCONFIG72 Register (Proxy0 Offset = 1C120h; Proxy1 Offset = 1E120h) [reset = 10264000h]

CTRLMMR_WKUP_PADCONFIG72 is shown in Figure 2-224 and described in Table 2-451.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-450. CTRLMMR_WKUP_PADCONFIG72 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C120h	4301 E120h

Figure 2-224. CTRLMMR_WKUP_PADCONFIG72 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-451. CTRLMMR_WKUP_PADCONFIG72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	1h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-451. CTRLMMR_WKUP_PADCONFIG72 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-451. CTRLMMR_WKUP_PADCONFIG72 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.226 CTRLMMR_WKUP_PADCONFIG73 Register (Proxy0 Offset = 1C124h; Proxy1 Offset = 1E124h) [reset = 244000h]

CTRLMMR_WKUP_PADCONFIG73 is shown in Figure 2-225 and described in Table 2-453.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-452. CTRLMMR_WKUP_PADCONFIG73 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C124h	4301 E124h

Figure 2-225. CTRLMMR_WKUP_PADCONFIG73 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-453. CTRLMMR_WKUP_PADCONFIG73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-453. CTRLMMR_WKUP_PADCONFIG73 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-453. CTRLMMR_WKUP_PADCONFIG73 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.227 CTRLMMR_WKUP_PADCONFIG74 Register (Proxy0 Offset = 1C128h; Proxy1 Offset = 1E128h) [reset = 10264000h]

CTRLMMR_WKUP_PADCONFIG74 is shown in Figure 2-226 and described in Table 2-455.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-454. CTRLMMR_WKUP_PADCONFIG74 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C128h	4301 E128h

Figure 2-226. CTRLMMR_WKUP_PADCONFIG74 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-455. CTRLMMR_WKUP_PADCONFIG74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	1h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-455. CTRLMMR_WKUP_PADCONFIG74 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-455. CTRLMMR_WKUP_PADCONFIG74 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.228 CTRLMMR_WKUP_PADCONFIG75 Register (Proxy0 Offset = 1C12Ch; Proxy1 Offset = 1E12Ch) [reset = 10264000h]

CTRLMMR_WKUP_PADCONFIG75 is shown in Figure 2-227 and described in Table 2-457.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-456. CTRLMMR_WKUP_PADCONFIG75 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C12Ch	4301 E12Ch

Figure 2-227. CTRLMMR_WKUP_PADCONFIG75 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-457. CTRLMMR_WKUP_PADCONFIG75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	1h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-457. CTRLMMR_WKUP_PADCONFIG75 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-457. CTRLMMR_WKUP_PADCONFIG75 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.229 CTRLMMR_WKUP_PADCONFIG76 Register (Proxy0 Offset = 1C130h; Proxy1 Offset = 1E130h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG76 is shown in Figure 2-228 and described in Table 2-459.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-458. CTRLMMR_WKUP_PADCONFIG76 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C130h	4301 E130h

Figure 2-228. CTRLMMR_WKUP_PADCONFIG76 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-459. CTRLMMR_WKUP_PADCONFIG76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC0 (MCU_ADC0_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.230 CTRLMMR_WKUP_PADCONFIG77 Register (Proxy0 Offset = 1C134h; Proxy1 Offset = 1E134h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG77 is shown in Figure 2-229 and described in Table 2-461.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-460. CTRLMMR_WKUP_PADCONFIG77 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C134h	4301 E134h

Figure 2-229. CTRLMMR_WKUP_PADCONFIG77 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-461. CTRLMMR_WKUP_PADCONFIG77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC0 (MCU_ADC0_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.231 CTRLMMR_WKUP_PADCONFIG78 Register (Proxy0 Offset = 1C138h; Proxy1 Offset = 1E138h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG78 is shown in Figure 2-230 and described in Table 2-463.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-462. CTRLMMR_WKUP_PADCONFIG78 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C138h	4301 E138h

Figure 2-230. CTRLMMR_WKUP_PADCONFIG78 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-463. CTRLMMR_WKUP_PADCONFIG78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC0 (MCU_ADC0_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.232 CTRLMMR_WKUP_PADCONFIG79 Register (Proxy0 Offset = 1C13Ch; Proxy1 Offset = 1E13Ch) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG79 is shown in Figure 2-231 and described in Table 2-465.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-464. CTRLMMR_WKUP_PADCONFIG79 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C13Ch	4301 E13Ch

Figure 2-231. CTRLMMR_WKUP_PADCONFIG79 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-465. CTRLMMR_WKUP_PADCONFIG79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC0 (MCU_ADC0_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.233 CTRLMMR_WKUP_PADCONFIG80 Register (Proxy0 Offset = 1C140h; Proxy1 Offset = 1E140h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG80 is shown in Figure 2-232 and described in Table 2-467.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-466. CTRLMMR_WKUP_PADCONFIG80 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C140h	4301 E140h

Figure 2-232. CTRLMMR_WKUP_PADCONFIG80 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-467. CTRLMMR_WKUP_PADCONFIG80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC0 (MCU_ADC0_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.234 CTRLMMR_WKUP_PADCONFIG81 Register (Proxy0 Offset = 1C144h; Proxy1 Offset = 1E144h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG81 is shown in Figure 2-233 and described in Table 2-469.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-468. CTRLMMR_WKUP_PADCONFIG81 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C144h	4301 E144h

Figure 2-233. CTRLMMR_WKUP_PADCONFIG81 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-469. CTRLMMR_WKUP_PADCONFIG81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC0 (MCU_ADC0_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.235 CTRLMMR_WKUP_PADCONFIG82 Register (Proxy0 Offset = 1C148h; Proxy1 Offset = 1E148h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG82 is shown in Figure 2-234 and described in Table 2-471.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-470. CTRLMMR_WKUP_PADCONFIG82 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C148h	4301 E148h

Figure 2-234. CTRLMMR_WKUP_PADCONFIG82 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-471. CTRLMMR_WKUP_PADCONFIG82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC0 (MCU_ADC0_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.236 CTRLMMR_WKUP_PADCONFIG83 Register (Proxy0 Offset = 1C14Ch; Proxy1 Offset = 1E14Ch) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG83 is shown in Figure 2-235 and described in Table 2-473.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-472. CTRLMMR_WKUP_PADCONFIG83 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C14Ch	4301 E14Ch

Figure 2-235. CTRLMMR_WKUP_PADCONFIG83 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-473. CTRLMMR_WKUP_PADCONFIG83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC0 (MCU_ADC0_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.237 CTRLMMR_WKUP_PADCONFIG84 Register (Proxy0 Offset = 1C150h; Proxy1 Offset = 1E150h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG84 is shown in Figure 2-236 and described in Table 2-475.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-474. CTRLMMR_WKUP_PADCONFIG84 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C150h	4301 E150h

Figure 2-236. CTRLMMR_WKUP_PADCONFIG84 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-475. CTRLMMR_WKUP_PADCONFIG84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC1 (MCU_ADC1_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.238 CTRLMMR_WKUP_PADCONFIG85 Register (Proxy0 Offset = 1C154h; Proxy1 Offset = 1E154h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG85 is shown in Figure 2-237 and described in Table 2-477.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-476. CTRLMMR_WKUP_PADCONFIG85 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C154h	4301 E154h

Figure 2-237. CTRLMMR_WKUP_PADCONFIG85 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-477. CTRLMMR_WKUP_PADCONFIG85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC1 (MCU_ADC1_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.239 CTRLMMR_WKUP_PADCONFIG86 Register (Proxy0 Offset = 1C158h; Proxy1 Offset = 1E158h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG86 is shown in Figure 2-238 and described in Table 2-479.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-478. CTRLMMR_WKUP_PADCONFIG86 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C158h	4301 E158h

Figure 2-238. CTRLMMR_WKUP_PADCONFIG86 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-479. CTRLMMR_WKUP_PADCONFIG86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC1 (MCU_ADC1_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.240 CTRLMMR_WKUP_PADCONFIG87 Register (Proxy0 Offset = 1C15Ch; Proxy1 Offset = 1E15Ch) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG87 is shown in Figure 2-239 and described in Table 2-481.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-480. CTRLMMR_WKUP_PADCONFIG87 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C15Ch	4301 E15Ch

Figure 2-239. CTRLMMR_WKUP_PADCONFIG87 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-481. CTRLMMR_WKUP_PADCONFIG87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC1 (MCU_ADC1_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.241 CTRLMMR_WKUP_PADCONFIG88 Register (Proxy0 Offset = 1C160h; Proxy1 Offset = 1E160h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG88 is shown in Figure 2-240 and described in Table 2-483.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-482. CTRLMMR_WKUP_PADCONFIG88 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C160h	4301 E160h

Figure 2-240. CTRLMMR_WKUP_PADCONFIG88 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-483. CTRLMMR_WKUP_PADCONFIG88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC1 (MCU_ADC1_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.242 CTRLMMR_WKUP_PADCONFIG89 Register (Proxy0 Offset = 1C164h; Proxy1 Offset = 1E164h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG89 is shown in Figure 2-241 and described in Table 2-485.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-484. CTRLMMR_WKUP_PADCONFIG89 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C164h	4301 E164h

Figure 2-241. CTRLMMR_WKUP_PADCONFIG89 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-485. CTRLMMR_WKUP_PADCONFIG89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC1 (MCU_ADC1_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.243 CTRLMMR_WKUP_PADCONFIG90 Register (Proxy0 Offset = 1C168h; Proxy1 Offset = 1E168h) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG90 is shown in Figure 2-242 and described in Table 2-487.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-486. CTRLMMR_WKUP_PADCONFIG90 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C168h	4301 E168h

Figure 2-242. CTRLMMR_WKUP_PADCONFIG90 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-487. CTRLMMR_WKUP_PADCONFIG90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC1 (MCU_ADC1_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.244 CTRLMMR_WKUP_PADCONFIG91 Register (Proxy0 Offset = 1C16Ch; Proxy1 Offset = 1E16Ch) [reset = 0h]

CTRLMMR_WKUP_PADCONFIG91 is shown in Figure 2-243 and described in Table 2-489.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-488. CTRLMMR_WKUP_PADCONFIG91 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C16Ch	4301 E16Ch

Figure 2-243. CTRLMMR_WKUP_PADCONFIG91 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED		DEBOUNCE_SEL			RESERVED		
R-0h		R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		RESERVED			
R-0h		R/W-0h		R-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-489. CTRLMMR_WKUP_PADCONFIG91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-14	RESERVED	R	0h	Reserved
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this pin. This allows protection between two different Processor virtual worlds. These bits have no effect if GPI mode is not selected for ADC1 (MCU_ADC1_CTRL_gpi_mode_en=1) 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	RESERVED	R	0h	Reserved

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2.245 CTRLMMR_WKUP_PADCONFIG92 Register (Proxy0 Offset = 1C170h; Proxy1 Offset = 1E170h) [reset = 10264000h]

CTRLMMR_WKUP_PADCONFIG92 is shown in Figure 2-244 and described in Table 2-491.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-490. CTRLMMR_WKUP_PADCONFIG92 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C170h	4301 E170h

Figure 2-244. CTRLMMR_WKUP_PADCONFIG92 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-491. CTRLMMR_WKUP_PADCONFIG92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	1h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-491. CTRLMMR_WKUP_PADCONFIG92 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-491. CTRLMMR_WKUP_PADCONFIG92 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.246 CTRLMMR_WKUP_PADCONFIG93 Register (Proxy0 Offset = 1C174h; Proxy1 Offset = 1E174h) [reset = 8014000h]

CTRLMMR_WKUP_PADCONFIG93 is shown in Figure 2-245 and described in Table 2-493.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 2-492. CTRLMMR_WKUP_PADCONFIG93 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 C174h	4301 E174h

Figure 2-245. CTRLMMR_WKUP_PADCONFIG93 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-493. CTRLMMR_WKUP_PADCONFIG93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for MCU_GENERAL IOs domain. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 2-493. CTRLMMR_WKUP_PADCONFIG93 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output enable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep is active 1h - IO state is forced to OFF mode value when Deep Sleep is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control. Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types). Nominal drive strength is recommended and is the value used for data manual AC timing . Fast or Slow modes can be used where necessary, and should be validated using IBIS simulations to determine the appropriate timing derate from the data manual. 0h - Nominal (recommended) 1h - Fast 2h - Slow 3h - Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved

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Table 2-493. CTRLMMR_WKUP_PADCONFIG93 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	VGPIO_SEL	R/W	0h	Virtual WKUP_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_WKUP_0 instance 1h - Implement GPIO in GPIO_WKUP_1 instance
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 Fh - Mux Mode 15

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2.247 CTRLMMR_WKUP_LOCK7_KICK0 Register (Proxy0 Offset = 1D008h; Proxy1 Offset = 1F008h) [reset = 0h]

CTRLMMR_WKUP_LOCK7_KICK0 is shown in Figure 2-246 and described in Table 2-495.

Return to Summary Table.

Lower 32-bits of Partition7 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_WKUP_LOCK7_KICK1 with its key value before write-protected Partition 7 registers can be written.

Table 2-494. CTRLMMR_WKUP_LOCK7_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 D008h	4301 F008h

Figure 2-246. CTRLMMR_WKUP_LOCK7_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 2-495. CTRLMMR_WKUP_LOCK7_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition7 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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2.248 CTRLMMR_WKUP_LOCK7_KICK1 Register (Proxy0 Offset = 1D00Ch; Proxy1 Offset = 1F00Ch) [reset = 0h]

CTRLMMR_WKUP_LOCK7_KICK1 is shown in Figure 2-247 and described in Table 2-497.

Return to Summary Table.

Upper 32-bits of Partition 7 write lock key. This register must be written with the designated key value after a write to CTRLMMR_WKUP_LOCK7_KICK0 with its key value before write-protected Partition 7 registers can be written.

Table 2-496. CTRLMMR_WKUP_LOCK7_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 D00Ch	4301 F00Ch

Figure 2-247. CTRLMMR_WKUP_LOCK7_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 2-497. CTRLMMR_WKUP_LOCK7_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition7 registers

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2.249 CTRLMMR_WKUP_P7_CLAIM0 Register (Proxy0 Offset = 1D100h; Proxy1 Offset = 1F100h) [reset = 0h]

CTRLMMR_WKUP_P7_CLAIM0 is shown in Figure 2-248 and described in Table 2-499.

Return to Summary Table.

Claim bits for Partition7 Registers.

Table 2-498. CTRLMMR_WKUP_P7_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 D100h	4301 F100h

Figure 2-248. CTRLMMR_WKUP_P7_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-499. CTRLMMR_WKUP_P7_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 1C000h + (0 x 80h) + (b x 4h) and register Proxy1 address of: 1E000h + (0 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.250 CTRLMMR_WKUP_P7_CLAIM1 Register (Proxy0 Offset = 1D104h; Proxy1 Offset = 1F104h) [reset = 0h]

CTRLMMR_WKUP_P7_CLAIM1 is shown in Figure 2-249 and described in Table 2-501.

Return to Summary Table.

Claim bits for Partition7 Registers.

Table 2-500. CTRLMMR_WKUP_P7_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 D104h	4301 F104h

Figure 2-249. CTRLMMR_WKUP_P7_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-501. CTRLMMR_WKUP_P7_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 1C000h + (1 x 80h) + (b x 4h) and register Proxy1 address of: 1E000h + (1 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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2.251 CTRLMMR_WKUP_P7_CLAIM2 Register (Proxy0 Offset = 1D108h; Proxy1 Offset = 1F108h) [reset = 0h]

CTRLMMR_WKUP_P7_CLAIM2 is shown in Figure 2-250 and described in Table 2-503.

Return to Summary Table.

Claim bits for Partition7 Registers.

Table 2-502. CTRLMMR_WKUP_P7_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
WKUP_CTRL_MMR0	4301 D108h	4301 F108h

Figure 2-250. CTRLMMR_WKUP_P7_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 2-503. CTRLMMR_WKUP_P7_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 1C000h + (2 x 80h) + (b x 4h) and register Proxy1 address of: 1E000h + (2 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3 MCU_CTRL_MMR0 Registers

Table 3-2 lists the memory-mapped registers for the MCU_CTRL_MMR0. All register offset addresses not listed in Table 3-2 should be considered as reserved locations and the register contents should not be modified.

Table 3-1. MCU_CTRL_MMR0 Instances

Instance	Base Address
MCU_CTRL_MMR0	40F0 0000h

Table 3-2. MCU_CTRL_MMR0 Registers

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	MCU_CTRL_MMR0 Proxy0 Physical Address	MCU_CTRL_MMR0 Proxy1 Physical Address
0h	2000h	CTRLMMR_MCU_PID	Peripheral Identification Register	40F0 0000h	40F0 2000h
8h	2008h	CTRLMMR_MCU_MMR_CFG1	Configuration register 1	40F0 0008h	40F0 2008h
100h	2100h	CTRLMMR_MCU_IPC_SET0	IPC Generation Register 0	40F0 0100h	40F0 2100h
104h	2104h	CTRLMMR_MCU_IPC_SET1	IPC Generation Register 1	40F0 0104h	40F0 2104h
120h	2120h	CTRLMMR_MCU_IPC_SET8	IPC Generation Register 8	40F0 0120h	40F0 2120h
180h	2180h	CTRLMMR_MCU_IPC_CLR0	IPC Acknowledge Register 0	40F0 0180h	40F0 2180h
184h	2184h	CTRLMMR_MCU_IPC_CLR1	IPC Acknowledge Register 1	40F0 0184h	40F0 2184h
1A0h	21A0h	CTRLMMR_MCU_IPC_CLR8	IPC Acknowledge Register 8	40F0 01A0h	40F0 21A0h
200h	2200h	CTRLMMR_MCU_MAC_ID0	MAC Address Lo register	40F0 0200h	40F0 2200h
204h	2204h	CTRLMMR_MCU_MAC_ID1	MAC Address Hi Register	40F0 0204h	40F0 2204h
1008h	3008h	CTRLMMR_MCU_LOCK0_KICK0	Partition 0 Lock Key 0 Register	40F0 1008h	40F0 3008h
100Ch	300Ch	CTRLMMR_MCU_LOCK0_KICK1	Partition 0 Lock Key 1 Register	40F0 100Ch	40F0 300Ch
1010h	3010h	CTRLMMR_MCU_INTR_RAW_STAT	Interrupt Raw Status Register	40F0 1010h	40F0 3010h
1014h	3014h	CTRLMMR_MCU_INTR_STAT_CLR	Interrupt Status and Clear Register	40F0 1014h	40F0 3014h
1018h	3018h	CTRLMMR_MCU_INTR_EN_SET	Interrupt Enable Set Register	40F0 1018h	40F0 3018h
101Ch	301Ch	CTRLMMR_MCU_INTR_EN_CLR	Interrupt Enable Clear Register	40F0 101Ch	40F0 301Ch
1020h	3020h	CTRLMMR_MCU_EOI	End of Interrupt Register	40F0 1020h	40F0 3020h
1024h	3024h	CTRLMMR_MCU_FAULT_ADDR	Fault Address Register	40F0 1024h	40F0 3024h
1028h	3028h	CTRLMMR_MCU_FAULT_TYPE	Fault Type Register	40F0 1028h	40F0 3028h
102Ch	302Ch	CTRLMMR_MCU_FAULT_ATTR	Fault Attribute Register	40F0 102Ch	40F0 302Ch
1030h	3030h	CTRLMMR_MCU_FAULT_CLR	Fault Clear Register	40F0 1030h	40F0 3030h

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Table 3-2. MCU_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	MCU_CTRL_MMR0 Proxy0 Physical Address	MCU_CTRL_MMR0 Proxy1 Physical Address
1100h	3100h	CTRLMMR_MCU_P0_CLAIM0	Partition 0 Claim Register 0	40F0 1100h	40F0 3100h
1104h	3104h	CTRLMMR_MCU_P0_CLAIM1	Partition 0 Claim Register 1	40F0 1104h	40F0 3104h
1108h	3108h	CTRLMMR_MCU_P0_CLAIM2	Partition 0 Claim Register 2	40F0 1108h	40F0 3108h
110Ch	310Ch	CTRLMMR_MCU_P0_CLAIM3	Partition 0 Claim Register 3	40F0 110Ch	40F0 310Ch
1110h	3110h	CTRLMMR_MCU_P0_CLAIM4	Partition 0 Claim Register 4	40F0 1110h	40F0 3110h
4030h	6030h	CTRLMMR_MCU_MSMC_CFG	MSMC Configuration Register	40F0 4030h	40F0 6030h
4040h	6040h	CTRLMMR_MCU_ENET_CTRL	MCU Ethernet Port1 Control Register	40F0 4040h	40F0 6040h
4060h	6060h	CTRLMMR_MCU_SPI1_CTRL	MCU SPI1 Conectivity Control Register	40F0 4060h	40F0 6060h
4070h	6070h	CTRLMMR_MCU_I3C0_CTRL0	MCU I3C0 Control Register 0	40F0 4070h	40F0 6070h
4074h	6074h	CTRLMMR_MCU_I3C0_CTRL1	MCU I3C0 Control Register 1	40F0 4074h	40F0 6074h
4078h	6078h	CTRLMMR_MCU_I3C1_CTRL0	MCU I3C1 Control Register 0	40F0 4078h	40F0 6078h
407Ch	607Ch	CTRLMMR_MCU_I3C1_CTRL1	MCU I3C1 Control Register 1	40F0 407Ch	40F0 607Ch
4080h	6080h	CTRLMMR_MCU_I2C0_CTRL	MCU I2C0 Control Register	40F0 4080h	40F0 6080h
40A0h	60A0h	CTRLMMR_MCU_FSS_CTRL	Flash Subsystem Control Register	40F0 40A0h	40F0 60A0h
40B0h	60B0h	CTRLMMR_MCU_ADC0_CTRL	MCU_ADC0 Control Register	40F0 40B0h	40F0 60B0h
40B4h	60B4h	CTRLMMR_MCU_ADC1_CTRL	MCU_ADC1 Control Register	40F0 40B4h	40F0 60B4h
4200h	6200h	CTRLMMR_MCU_TIMER0_CTRL	MCU_TIMER0 Control Register	40F0 4200h	40F0 6200h
4204h	6204h	CTRLMMR_MCU_TIMER1_CTRL	MCU_TIMER1 Control Register	40F0 4204h	40F0 6204h
4208h	6208h	CTRLMMR_MCU_TIMER2_CTRL	MCU_TIMER2 Control Register	40F0 4208h	40F0 6208h
420Ch	620Ch	CTRLMMR_MCU_TIMER3_CTRL	MCU_TIMER3 Control Register	40F0 420Ch	40F0 620Ch
4210h	6210h	CTRLMMR_MCU_TIMER4_CTRL	MCU_TIMER4 Control Register	40F0 4210h	40F0 6210h
4214h	6214h	CTRLMMR_MCU_TIMER5_CTRL	MCU_TIMER5 Control Register	40F0 4214h	40F0 6214h
4218h	6218h	CTRLMMR_MCU_TIMER6_CTRL	MCU_TIMER6 Control Register	40F0 4218h	40F0 6218h
421Ch	621Ch	CTRLMMR_MCU_TIMER7_CTRL	MCU_TIMER7 Control Register	40F0 421Ch	40F0 621Ch
4220h	6220h	CTRLMMR_MCU_TIMER8_CTRL	MCU_TIMER8 Control Register	40F0 4220h	40F0 6220h
4224h	6224h	CTRLMMR_MCU_TIMER9_CTRL	MCU_TIMER9 Control Register	40F0 4224h	40F0 6224h

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Table 3-2. MCU_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	MCU_CTRL_MMR0 Proxy0 Physical Address	MCU_CTRL_MMR0 Proxy1 Physical Address
4280h	6280h	CTRLMMR_MCU_TIMERIO0_CTRL	MCU_TIMERIO0 Control Register	40F0 4280h	40F0 6280h
4284h	6284h	CTRLMMR_MCU_TIMERIO1_CTRL	MCU_TIMERIO1 Control Register	40F0 4284h	40F0 6284h
4288h	6288h	CTRLMMR_MCU_TIMERIO2_CTRL	MCU_TIMERIO2 Control Register	40F0 4288h	40F0 6288h
428Ch	628Ch	CTRLMMR_MCU_TIMERIO3_CTRL	MCU_TIMERIO3 Control Register	40F0 428Ch	40F0 628Ch
4290h	6290h	CTRLMMR_MCU_TIMERIO4_CTRL	MCU_TIMERIO4 Control Register	40F0 4290h	40F0 6290h
4294h	6294h	CTRLMMR_MCU_TIMERIO5_CTRL	MCU_TIMERIO5 Control Register	40F0 4294h	40F0 6294h
4298h	6298h	CTRLMMR_MCU_TIMERIO6_CTRL	MCU_TIMERIO6 Control Register	40F0 4298h	40F0 6298h
429Ch	629Ch	CTRLMMR_MCU_TIMERIO7_CTRL	MCU_TIMERIO7 Control Register	40F0 429Ch	40F0 629Ch
42A0h	62A0h	CTRLMMR_MCU_TIMERIO8_CTRL	MCU_TIMERIO8 Control Register	40F0 42A0h	40F0 62A0h
42A4h	62A4h	CTRLMMR_MCU_TIMERIO9_CTRL	MCU_TIMERIO9 Control Register	40F0 42A4h	40F0 62A4h
5008h	7008h	CTRLMMR_MCU_LOCK1_KICK0	Partition 1 Lock Key 0 Register	40F0 5008h	40F0 7008h
500Ch	700Ch	CTRLMMR_MCU_LOCK1_KICK1	Partition 1 Lock Key 1 Register	40F0 500Ch	40F0 700Ch
5100h	7100h	CTRLMMR_MCU_P1_CLAIM0	Partition 1 Claim Register 0	40F0 5100h	40F0 7100h
5104h	7104h	CTRLMMR_MCU_P1_CLAIM1	Partition 1 Claim Register 1	40F0 5104h	40F0 7104h
5108h	7108h	CTRLMMR_MCU_P1_CLAIM2	Partition 1 Claim Register 2	40F0 5108h	40F0 7108h
510Ch	710Ch	CTRLMMR_MCU_P1_CLAIM3	Partition 1 Claim Register 3	40F0 510Ch	40F0 710Ch
5110h	7110h	CTRLMMR_MCU_P1_CLAIM4	Partition 1 Claim Register 4	40F0 5110h	40F0 7110h
5114h	7114h	CTRLMMR_MCU_P1_CLAIM5	Partition 1 Claim Register 5	40F0 5114h	40F0 7114h
8010h	A010h	CTRLMMR_MCU_CLKOUT0_CTRL	MCU_CLKOUT0 Control Register	40F0 8010h	40F0 A010h
8018h	A018h	CTRLMMR_MCU_EFUSE_CLKSEL	MCU eFuse Controller Clock Select Register	40F0 8018h	40F0 A018h
8020h	A020h	CTRLMMR_MCU_MCAN0_CLKSEL	MCU_MCAN Clock Select Register	40F0 8020h	40F0 A020h
8024h	A024h	CTRLMMR_MCU_MCAN1_CLKSEL	MCU_MCAN Clock Select Register	40F0 8024h	40F0 A024h
8030h	A030h	CTRLMMR_MCU_OSPI0_CLKSEL	MCU_OSPI Clock Select Register	40F0 8030h	40F0 A030h
8034h	A034h	CTRLMMR_MCU_OSPI1_CLKSEL	MCU_OSPI Clock Select Register	40F0 8034h	40F0 A034h
8040h	A040h	CTRLMMR_MCU_ADC0_CLKSEL	MCU_ADC Clock Select Register	40F0 8040h	40F0 A040h
8044h	A044h	CTRLMMR_MCU_ADC1_CLKSEL	MCU_ADC Clock Select Register	40F0 8044h	40F0 A044h

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Table 3-2. MCU_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	MCU_CTRL_MMR0 Proxy0 Physical Address	MCU_CTRL_MMR0 Proxy1 Physical Address
8050h	A050h	CTRLMMR_MCU_ENET_CLKSEL	MCU Ethernet Port1 Clock Select Register	40F0 8050h	40F0 A050h
8080h	A080h	CTRLMMR_MCU_R5_CORE0_CLKSEL	MCU R5 Core 0 Clock Select Register	40F0 8080h	40F0 A080h
8100h	A100h	CTRLMMR_MCU_TIMER0_CLKSEL	MCU_TIMER0 Clock Select Register	40F0 8100h	40F0 A100h
8104h	A104h	CTRLMMR_MCU_TIMER1_CLKSEL	MCU_TIMER1 Clock Select Register	40F0 8104h	40F0 A104h
8108h	A108h	CTRLMMR_MCU_TIMER2_CLKSEL	MCU_TIMER2 Clock Select Register	40F0 8108h	40F0 A108h
810Ch	A10Ch	CTRLMMR_MCU_TIMER3_CLKSEL	MCU_TIMER3 Clock Select Register	40F0 810Ch	40F0 A10Ch
8110h	A110h	CTRLMMR_MCU_TIMER4_CLKSEL	MCU_TIMER4 Clock Select Register	40F0 8110h	40F0 A110h
8114h	A114h	CTRLMMR_MCU_TIMER5_CLKSEL	MCU_TIMER5 Clock Select Register	40F0 8114h	40F0 A114h
8118h	A118h	CTRLMMR_MCU_TIMER6_CLKSEL	MCU_TIMER6 Clock Select Register	40F0 8118h	40F0 A118h
811Ch	A11Ch	CTRLMMR_MCU_TIMER7_CLKSEL	MCU_TIMER7 Clock Select Register	40F0 811Ch	40F0 A11Ch
8120h	A120h	CTRLMMR_MCU_TIMER8_CLKSEL	MCU_TIMER8 Clock Select Register	40F0 8120h	40F0 A120h
8124h	A124h	CTRLMMR_MCU_TIMER9_CLKSEL	MCU_TIMER9 Clock Select Register	40F0 8124h	40F0 A124h
8180h	A180h	CTRLMMR_MCU_RTI0_CLKSEL	MCU_RTI[0:0] Clock Select Register	40F0 8180h	40F0 A180h
8184h	A184h	CTRLMMR_MCU_RTI1_CLKSEL	MCU_RTI[0:0] Clock Select Register	40F0 8184h	40F0 A184h
81C0h	A1C0h	CTRLMMR_MCU_USART_CLKSEL	MCU_USART0 Clock Select Register	40F0 81C0h	40F0 A1C0h
9008h	B008h	CTRLMMR_MCU_LOCK2_KICK0	Partition 2 Lock Key 0 Register	40F0 9008h	40F0 B008h
900Ch	B00Ch	CTRLMMR_MCU_LOCK2_KICK1	Partition 2 Lock Key 1 Register	40F0 900Ch	40F0 B00Ch
9100h	B100h	CTRLMMR_MCU_P2_CLAIM0	Partition 2 Claim Register 0	40F0 9100h	40F0 B100h
9104h	B104h	CTRLMMR_MCU_P2_CLAIM1	Partition 2 Claim Register 1	40F0 9104h	40F0 B104h
9108h	B108h	CTRLMMR_MCU_P2_CLAIM2	Partition 2 Claim Register 2	40F0 9108h	40F0 B108h
910Ch	B10Ch	CTRLMMR_MCU_P2_CLAIM3	Partition 2 Claim Register 3	40F0 910Ch	40F0 B10Ch
C000h	E000h	CTRLMMR_MCU_LBIST_CTRL	MCU_Pulsar Logic BIST Control Register	40F0 C000h	40F0 E000h
C004h	E004h	CTRLMMR_MCU_LBIST_PATCOUNT	MCU_Pulsar Logic BIST Pattern Count Register	40F0 C004h	40F0 E004h
C008h	E008h	CTRLMMR_MCU_LBIST_SEED0	MCU_Pulsar Logic BIST Seed0 Register	40F0 C008h	40F0 E008h
C00Ch	E00Ch	CTRLMMR_MCU_LBIST_SEED1	MCU_Pulsar Logic BIST Seed1 Register	40F0 C00Ch	40F0 E00Ch
C010h	E010h	CTRLMMR_MCU_LBIST_SPARE0	MCU_Pulsar Logic BIST Spare0 Register	40F0 C010h	40F0 E010h

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Table 3-2. MCU_CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	MCU_CTRL_MMR0 Proxy0 Physical Address	MCU_CTRL_MMR0 Proxy1 Physical Address
C014h	E014h	CTRLMMR_MCU_LBIST_SPARE1	MCU_Pulsar Logic BIST Spare1 Register	40F0 C014h	40F0 E014h
C018h	E018h	CTRLMMR_MCU_LBIST_STAT	MCU_Pulsar Logic BIST Status Register	40F0 C018h	40F0 E018h
C01Ch	E01Ch	CTRLMMR_MCU_LBIST_MISR	MCU_Pulsar Logic BIST MISR Register	40F0 C01Ch	40F0 E01Ch
C280h	E280h	CTRLMMR_MCU_LBIST_SIG	MCU Pulsar Logic BIST MISR Signature Register	40F0 C280h	40F0 E280h
D008h	F008h	CTRLMMR_MCU_LOCK3_KICK0	Partition 3 Lock Key 0 Register	40F0 D008h	40F0 F008h
D00Ch	F00Ch	CTRLMMR_MCU_LOCK3_KICK1	Partition 3 Lock Key 1 Register	40F0 D00Ch	40F0 F00Ch
D100h	F100h	CTRLMMR_MCU_P3_CLAIM0	Partition 3 Claim Register 0	40F0 D100h	40F0 F100h
D104h	F104h	CTRLMMR_MCU_P3_CLAIM1	Partition 3 Claim Register 1	40F0 D104h	40F0 F104h
D108h	F108h	CTRLMMR_MCU_P3_CLAIM2	Partition 3 Claim Register 2	40F0 D108h	40F0 F108h
D10Ch	F10Ch	CTRLMMR_MCU_P3_CLAIM3	Partition 3 Claim Register 3	40F0 D10Ch	40F0 F10Ch
D110h	F110h	CTRLMMR_MCU_P3_CLAIM4	Partition 3 Claim Register 4	40F0 D110h	40F0 F110h
D114h	F114h	CTRLMMR_MCU_P3_CLAIM5	Partition 3 Claim Register 5	40F0 D114h	40F0 F114h

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3.1 CTRLMMR_MCU_PID Register (Proxy0 Offset = 0h; Proxy1 Offset = 2000h) [reset = 61800000h]

CTRLMMR_MCU_PID is shown in Figure 3-1 and described in Table 3-4.

Return to Summary Table.

Peripheral release details.

Table 3-3. CTRLMMR_MCU_PID Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 0000h	40F0 2000h

Figure 3-1. CTRLMMR_MCU_PID Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R-1h		R-2h		R-180h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
FUNC							
R-180h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
R_RTL					X_MAJOR		
R-0h					R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CUSTOM		Y_MINOR					
R-0h		R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 3-4. CTRLMMR_MCU_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business unit
27-16	FUNC	R	180h	Module functional identifier
15-11	R_RTL	R	0h	RTL revision
10-8	X_MAJOR	R	0h	Major revision
7-6	CUSTOM	R	0h	Custom revision
5-0	Y_MINOR	R	0h	Minor revision

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3.2 CTRLMMR_MCU_MMR_CFG1 Register (Proxy0 Offset = 8h; Proxy1 Offset = 2008h) [reset = 8000001Fh]

CTRLMMR_MCU_MMR_CFG1 is shown in Figure 3-2 and described in Table 3-6.

Return to Summary Table.

Indicates the MMR configuration.

Table 3-5. CTRLMMR_MCU_MMR_CFG1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 0008h	40F0 2008h

Figure 3-2. CTRLMMR_MCU_MMR_CFG1 Register

31	30	29	28	27	26	25	24
PROXY_EN	RESERVED						
R-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
PARTITIONS							
R-1Fh							

LEGEND: R = Read Only; *-n* = value after reset

Table 3-6. CTRLMMR_MCU_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PROXY_EN	R	1h	Proxy addressing enabled
30-8	RESERVED	R	0h	Reserved
7-0	PARTITIONS	R	1Fh	Indicates present partitions

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3.3 CTRLMMR_MCU_IPC_SET0 Register (Proxy0 Offset = 100h; Proxy1 Offset = 2100h) [reset = 0h]

CTRLMMR_MCU_IPC_SET0 is shown in Figure 3-3 and described in Table 3-8.

Return to Summary Table.

Generate interprocessor communication interrupt to MCU R5 core0.

Table 3-7. CTRLMMR_MCU_IPC_SET0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 0100h	40F0 2100h

Figure 3-3. CTRLMMR_MCU_IPC_SET0 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 3-8. CTRLMMR_MCU_IPC_SET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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3.4 CTRLMMR_MCU_IPC_SET1 Register (Proxy0 Offset = 104h; Proxy1 Offset = 2104h) [reset = 0h]

CTRLMMR_MCU_IPC_SET1 is shown in Figure 3-4 and described in Table 3-10.

Return to Summary Table.

Generate interprocessor communication interrupt to MCU R5 core1.

Table 3-9. CTRLMMR_MCU_IPC_SET1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 0104h	40F0 2104h

Figure 3-4. CTRLMMR_MCU_IPC_SET1 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 3-10. CTRLMMR_MCU_IPC_SET1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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3.5 CTRLMMR_MCU_IPC_SET8 Register (Proxy0 Offset = 120h; Proxy1 Offset = 2120h) [reset = 0h]

CTRLMMR_MCU_IPC_SET8 is shown in Figure 3-5 and described in Table 3-12.

Return to Summary Table.

Generate interprocessor communication interrupt to DMSC.

Table 3-11. CTRLMMR_MCU_IPC_SET8 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 0120h	40F0 2120h

Figure 3-5. CTRLMMR_MCU_IPC_SET8 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 3-12. CTRLMMR_MCU_IPC_SET8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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3.6 CTRLMMR_MCU_IPC_CLR0 Register (Proxy0 Offset = 180h; Proxy1 Offset = 2180h) [reset = 0h]

CTRLMMR_MCU_IPC_CLR0 is shown in Figure 3-6 and described in Table 3-14.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to MCU R5 core0.

Table 3-13. CTRLMMR_MCU_IPC_CLR0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 0180h	40F0 2180h

Figure 3-6. CTRLMMR_MCU_IPC_CLR0 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 3-14. CTRLMMR_MCU_IPC_CLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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3.7 CTRLMMR_MCU_IPC_CLR1 Register (Proxy0 Offset = 184h; Proxy1 Offset = 2184h) [reset = 0h]

CTRLMMR_MCU_IPC_CLR1 is shown in Figure 3-7 and described in Table 3-16.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to MCU R5 core1.

Table 3-15. CTRLMMR_MCU_IPC_CLR1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 0184h	40F0 2184h

Figure 3-7. CTRLMMR_MCU_IPC_CLR1 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 3-16. CTRLMMR_MCU_IPC_CLR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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3.8 CTRLMMR_MCU_IPC_CLR8 Register (Proxy0 Offset = 1A0h; Proxy1 Offset = 21A0h) [reset = 0h]

CTRLMMR_MCU_IPC_CLR8 is shown in Figure 3-8 and described in Table 3-18.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to DMSC.

Table 3-17. CTRLMMR_MCU_IPC_CLR8 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 01A0h	40F0 21A0h

Figure 3-8. CTRLMMR_MCU_IPC_CLR8 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 3-18. CTRLMMR_MCU_IPC_CLR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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3.9 CTRLMMR_MCU_MAC_ID0 Register (Proxy0 Offset = 200h; Proxy1 Offset = 2200h) [reset = X]

CTRLMMR_MCU_MAC_ID0 is shown in Figure 3-9 and described in Table 3-20.

Return to Summary Table.

MCU Ethernet MAC address lower 32-bits.

Table 3-19. CTRLMMR_MCU_MAC_ID0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 0200h	40F0 2200h

Figure 3-9. CTRLMMR_MCU_MAC_ID0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MACID_LO																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 3-20. CTRLMMR_MCU_MAC_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MACID_LO	R	X	32 lsbs of MAC address

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3.10 CTRLMMR_MCU_MAC_ID1 Register (Proxy0 Offset = 204h; Proxy1 Offset = 2204h) [reset = X]

CTRLMMR_MCU_MAC_ID1 is shown in Figure 3-10 and described in Table 3-22.

Return to Summary Table.

MCU Ethernet MAC address upper 16-bits.

Table 3-21. CTRLMMR_MCU_MAC_ID1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 0204h	40F0 2204h

Figure 3-10. CTRLMMR_MCU_MAC_ID1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																MACID_HI															
R-0h																R-X															

LEGEND: R = Read Only; *-n* = value after reset

Table 3-22. CTRLMMR_MCU_MAC_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	MACID_HI	R	X	16 msbs of MAC address

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3.11 CTRLMMR_MCU_LOCK0_KICK0 Register (Proxy0 Offset = 1008h; Proxy1 Offset = 3008h) [reset = 0h]

CTRLMMR_MCU_LOCK0_KICK0 is shown in Figure 3-11 and described in Table 3-24.

Return to Summary Table.

Lower 32-bits of Partition0 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_MCU_LOCK0_KICK1 with its key value before write-protected Partition 0 registers can be written.

Table 3-23. CTRLMMR_MCU_LOCK0_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1008h	40F0 3008h

Figure 3-11. CTRLMMR_MCU_LOCK0_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-24. CTRLMMR_MCU_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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3.12 CTRLMMR_MCU_LOCK0_KICK1 Register (Proxy0 Offset = 100Ch; Proxy1 Offset = 300Ch) [reset = 0h]

CTRLMMR_MCU_LOCK0_KICK1 is shown in Figure 3-12 and described in Table 3-26.

Return to Summary Table.

Upper 32-bits of Partition 0 write lock key. This register must be written with the designated key value after a write to CTRLMMR_MCU_LOCK0_KICK0 with its key value before write-protected Partition 0 registers can be written.

Table 3-25. CTRLMMR_MCU_LOCK0_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 100Ch	40F0 300Ch

Figure 3-12. CTRLMMR_MCU_LOCK0_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 3-26. CTRLMMR_MCU_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers

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3.13 CTRLMMR_MCU_INTR_RAW_STAT Register (Proxy0 Offset = 1010h; Proxy1 Offset = 3010h) [reset = 0h]

CTRLMMR_MCU_INTR_RAW_STAT is shown in Figure 3-13 and described in Table 3-28.

Return to Summary Table.

Shows the interupt status (before enabling) and allows setting of the interrupt status (for test).

Table 3-27. CTRLMMR_MCU_INTR_RAW_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1010h	40F0 3010h

Figure 3-13. CTRLMMR_MCU_INTR_RAW_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	LOCK_ERR	ADDR_ERR	PROT_ERR
R-0h				W1TS-0h	W1TS-0h	W1TS-0h	W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 3-28. CTRLMMR_MCU_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PROXY_ERR	W1TS	0h	Proxy violation occurred (attempt to write a Proxy1 claimed register through its Proxy0 address) Write 1 to set the status bit (for test) Writing 0 has no effect.
2	LOCK_ERR	W1TS	0h	Lock violation occurred (attempt to write a write-locked register with partition locked) Write 1 to set the status bit (for test) Writing 0 has no effect.
1	ADDR_ERR	W1TS	0h	Address violation occurred (attempt to read or write an invalid register address) Write 1 to set the status bit (for test) Writing 0 has no effect.
0	PROT_ERR	W1TS	0h	Protection violation occurred (attempt to to read or write a register with insufficient sucurity or privilege access rights) Write 1 to set the status bit (for test) Writing 0 has no effect.

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3.14 CTRLMMR_MCU_INTR_STAT_CLR Register (Proxy0 Offset = 1014h; Proxy1 Offset = 3014h) [reset = 0h]

CTRLMMR_MCU_INTR_STAT_CLR is shown in Figure 3-14 and described in Table 3-30.

Return to Summary Table.

Shows the enabled interrupt status and allows the interrupt to be cleared.

Table 3-29. CTRLMMR_MCU_INTR_STAT_CLR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1014h	40F0 3014h

Figure 3-14. CTRLMMR_MCU_INTR_STAT_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				EN_PROXY_ERR	EN_LOCK_ERR	EN_ADDR_ERR	EN_PROT_ERR
R-0h				W1TC-0h	W1TC-0h	W1TC-0h	W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 3-30. CTRLMMR_MCU_INTR_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	EN_PROXY_ERR	W1TC	0h	Enabled proxy interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
2	EN_LOCK_ERR	W1TC	0h	Enabled lock interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
1	EN_ADDR_ERR	W1TC	0h	Enabled address interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
0	EN_PROT_ERR	W1TC	0h	Enabled protection interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.

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3.15 CTRLMMR_MCU_INTR_EN_SET Register (Proxy0 Offset = 1018h; Proxy1 Offset = 3018h) [reset = 0h]

CTRLMMR_MCU_INTR_EN_SET is shown in Figure 3-15 and described in Table 3-32.

Return to Summary Table.

Allows interrupt enables to be set.

Table 3-31. CTRLMMR_MCU_INTR_EN_SET Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1018h	40F0 3018h

Figure 3-15. CTRLMMR_MCU_INTR_EN_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_SET	LOCK_ERR_EN_SET	ADDR_ERR_EN_SET	PROT_ERR_EN_SET
R-0h				W1TS-0h	W1TS-0h	W1TS-0h	W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 3-32. CTRLMMR_MCU_INTR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PROXY_ERR_EN_SET	W1TS	0h	Proxy interrupt enable Write 1 to enable proxy interrupt events Writing 0 has no effect.
2	LOCK_ERR_EN_SET	W1TS	0h	Lock interrupt enable Write 1 to enable lock interrupt events Writing 0 has no effect.
1	ADDR_ERR_EN_SET	W1TS	0h	Address interrupt enable Write 1 to enable address interrupt events Writing 0 has no effect.
0	PROT_ERR_EN_SET	W1TS	0h	Protection interrupt enable Write 1 to enable protection interrupt events Writing 0 has no effect.

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3.16 CTRLMMR_MCU_INTR_EN_CLR Register (Proxy0 Offset = 101Ch; Proxy1 Offset = 301Ch) [reset = 0h]

CTRLMMR_MCU_INTR_EN_CLR is shown in Figure 3-16 and described in Table 3-34.

Return to Summary Table.

Allows interrupt enables to be cleared.

Table 3-33. CTRLMMR_MCU_INTR_EN_CLR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 101Ch	40F0 301Ch

Figure 3-16. CTRLMMR_MCU_INTR_EN_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	LOCK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
R-0h				W1TC-0h	W1TC-0h	W1TC-0h	W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 3-34. CTRLMMR_MCU_INTR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PROXY_ERR_EN_CLR	W1TC	0h	Proxy interrupt disable Write 1 to disable proxy interrupt events Writing 0 has no effect.
2	LOCK_ERR_EN_CLR	W1TC	0h	Lock interrupt disable Write 1 to disable lock interrupt events Writing 0 has no effect.
1	ADDR_ERR_EN_CLR	W1TC	0h	Address interrupt disable Write 1 to disable address interrupt events Writing 0 has no effect.
0	PROT_ERR_EN_CLR	W1TC	0h	Protection interrupt disable Write 1 to disable protection interrupt events Writing 0 has no effect.

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3.17 CTRLMMR_MCU_EOI Register (Proxy0 Offset = 1020h; Proxy1 Offset = 3020h) [reset = 0h]

CTRLMMR_MCU_EOI is shown in Figure 3-17 and described in Table 3-36.

Return to Summary Table.

CTRLMMR_MCU_EOI Vector value This register should be written with interrupt distribution value required by the device architecture to indicate service completion of the MMR interrupt.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 3-35. CTRLMMR_MCU_EOI Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1020h	40F0 3020h

Figure 3-17. CTRLMMR_MCU_EOI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VECTOR							
R-0h																								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-36. CTRLMMR_MCU_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VECTOR	R/W	0h	CTRLMMR_MCU_EOI vector value

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3.18 CTRLMMR_MCU_FAULT_ADDR Register (Proxy0 Offset = 1024h; Proxy1 Offset = 3024h) [reset = 0h]

CTRLMMR_MCU_FAULT_ADDR is shown in Figure 3-18 and described in Table 3-38.

Return to Summary Table.

Indicates the address of the first transfer that caused a fault to occur.

Table 3-37. CTRLMMR_MCU_FAULT_ADDR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1024h	40F0 3024h

Figure 3-18. CTRLMMR_MCU_FAULT_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 3-38. CTRLMMR_MCU_FAULT_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	Address of the faulted access

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3.19 CTRLMMR_MCU_FAULT_TYPE Register (Proxy0 Offset = 1028h; Proxy1 Offset = 3028h) [reset = 0h]

CTRLMMR_MCU_FAULT_TYPE is shown in Figure 3-19 and described in Table 3-40.

Return to Summary Table.

Indicates the access type of the first transfer that caused a fault to occur.

Table 3-39. CTRLMMR_MCU_FAULT_TYPE Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1028h	40F0 3028h

Figure 3-19. CTRLMMR_MCU_FAULT_TYPE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										TYPE					
R-0h																										R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 3-40. CTRLMMR_MCU_FAULT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	TYPE	R	0h	Type of access which faulted 0h - No fault 1h - User execute access 2h - User write access 4h - User read access 8h - Supervisor execute access 10h - Supervisor write access 20h - Supervisor read access

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3.20 CTRLMMR_MCU_FAULT_ATTR Register (Proxy0 Offset = 102Ch; Proxy1 Offset = 302Ch) [reset = 0h]

CTRLMMR_MCU_FAULT_ATTR is shown in Figure 3-20 and described in Table 3-42.

Return to Summary Table.

Indicates the attributes of the first transfer that caused a fault to occur.

Table 3-41. CTRLMMR_MCU_FAULT_ATTR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 102Ch	40F0 302Ch

Figure 3-20. CTRLMMR_MCU_FAULT_ATTR Register

31	30	29	28	27	26	25	24
XID							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
XID				ROUTEID			
R-0h				R-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ROUTEID							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIVID							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 3-42. CTRLMMR_MCU_FAULT_ATTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	XID	R	0h	Transaction ID
19-8	ROUTEID	R	0h	Route ID
7-0	PRIVID	R	0h	Privilege ID

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3.21 CTRLMMR_MCU_FAULT_CLR Register (Proxy0 Offset = 1030h; Proxy1 Offset = 3030h) [reset = 0h]

CTRLMMR_MCU_FAULT_CLR is shown in Figure 3-21 and described in Table 3-44.

Return to Summary Table.

Allows software to clear the current fault. Clearing the current fault allows the CTRLMMR_MCU_FAULT_ADDR, CTRLMMR_MCU_FAULT_TYPE, and CTRLMMR_MCU_FAULT_ATTR registers to latch the attributes of the next fault that occurs. This does not affect the fault interrupt event itself. The interrupt must be cleared using the appropriate INTR_STATUS_CLR register bits.

Table 3-43. CTRLMMR_MCU_FAULT_CLR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1030h	40F0 3030h

Figure 3-21. CTRLMMR_MCU_FAULT_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLEAR
R-0h							W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 3-44. CTRLMMR_MCU_FAULT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLEAR	W1TC	0h	Fault clear Write 1 to clear the current fault Writing 0 has no effect

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3.22 CTRLMMR_MCU_P0_CLAIM0 Register (Proxy0 Offset = 1100h; Proxy1 Offset = 3100h) [reset = 0h]

CTRLMMR_MCU_P0_CLAIM0 is shown in Figure 3-22 and described in Table 3-46.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 3-45. CTRLMMR_MCU_P0_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1100h	40F0 3100h

Figure 3-22. CTRLMMR_MCU_P0_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-46. CTRLMMR_MCU_P0_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (0 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (0 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.23 CTRLMMR_MCU_P0_CLAIM1 Register (Proxy0 Offset = 1104h; Proxy1 Offset = 3104h) [reset = 0h]

CTRLMMR_MCU_P0_CLAIM1 is shown in Figure 3-23 and described in Table 3-48.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 3-47. CTRLMMR_MCU_P0_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1104h	40F0 3104h

Figure 3-23. CTRLMMR_MCU_P0_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 3-48. CTRLMMR_MCU_P0_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (1 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (1 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.24 CTRLMMR_MCU_P0_CLAIM2 Register (Proxy0 Offset = 1108h; Proxy1 Offset = 3108h) [reset = 0h]

CTRLMMR_MCU_P0_CLAIM2 is shown in Figure 3-24 and described in Table 3-50.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 3-49. CTRLMMR_MCU_P0_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1108h	40F0 3108h

Figure 3-24. CTRLMMR_MCU_P0_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-50. CTRLMMR_MCU_P0_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (2 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (2 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.25 CTRLMMR_MCU_P0_CLAIM3 Register (Proxy0 Offset = 110Ch; Proxy1 Offset = 310Ch) [reset = 0h]

CTRLMMR_MCU_P0_CLAIM3 is shown in Figure 3-25 and described in Table 3-52.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 3-51. CTRLMMR_MCU_P0_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 110Ch	40F0 310Ch

Figure 3-25. CTRLMMR_MCU_P0_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 3-52. CTRLMMR_MCU_P0_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (3 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (3 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.26 CTRLMMR_MCU_P0_CLAIM4 Register (Proxy0 Offset = 1110h; Proxy1 Offset = 3110h) [reset = 0h]

CTRLMMR_MCU_P0_CLAIM4 is shown in Figure 3-26 and described in Table 3-54.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 3-53. CTRLMMR_MCU_P0_CLAIM4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 1110h	40F0 3110h

Figure 3-26. CTRLMMR_MCU_P0_CLAIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 3-54. CTRLMMR_MCU_P0_CLAIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0h + (4 x 80h) + (b x 4h) and register Proxy1 address of: 2000h + (4 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.27 CTRLMMR_MCU_MSMC_CFG Register (Proxy0 Offset = 4030h; Proxy1 Offset = 6030h) [reset = 1h]

CTRLMMR_MCU_MSMC_CFG is shown in Figure 3-27 and described in Table 3-56.

Return to Summary Table.

Used to configure MSMC reset options.

Table 3-55. CTRLMMR_MCU_MSMC_CFG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4030h	40F0 6030h

Figure 3-27. CTRLMMR_MCU_MSMC_CFG Register

31	30	29	28	27	26	25	24
DDR_ASSYM_EMIF_SEL	RESERVED	DDR_INTRLV_GRAN					
R/W-0h	R-0h	R/W-0h					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED		DDR_INTRLV_SIZE					
R-0h		R/W-0h					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			MEM_INIT_DIS	RESERVED			RESERVED
R-0h			R/W-0h	R-0h			R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-56. CTRLMMR_MCU_MSMC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DDR_ASSYM_EMIF_SEL	R/W	0h	In the asymmetric interleave, controls which EMIF controller implements the separated range of the memory window
30	RESERVED	R	0h	Reserved
29-24	DDR_INTRLV_GRAN	R/W	0h	Defines the size of each memory stripe for interleaved memory space
23-22	RESERVED	R	0h	Reserved
21-16	DDR_INTRLV_SIZE	R/W	0h	Defines the memory window size for the interleaved region starting at the bottom of the external memory address range. 00h - 13h - No Interleave region: 14h - 23h - 2^(ddr_intrlv_size) Region size
15-5	RESERVED	R	0h	Reserved
4	MEM_INIT_DIS	R/W	0h	Disables MSMC SRAM initialization (Data, Cache Tags, and Snoop Filters). This is required for proper initial ECC initialization. 0h - Perform memory initialization 1h - Disable memory initialization
3-1	RESERVED	R	0h	Reserved
0	RESERVED	R/W	1h	Reserved. Write 1h for compatibility. Do not write 0h.

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3.28 CTRLMMR_MCU_ENET_CTRL Register (Proxy0 Offset = 4040h; Proxy1 Offset = 6040h) [reset = 1h]

CTRLMMR_MCU_ENET_CTRL is shown in Figure 3-28 and described in Table 3-58.

Return to Summary Table.

Controls MCU Ethernet Port1 operation.

Table 3-57. CTRLMMR_MCU_ENET_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4040h	40F0 6040h

Figure 3-28. CTRLMMR_MCU_ENET_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RGMII_ID_MODE	RESERVED		MODE_SEL	
R-0h			R/W-0h	R-0h		R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-58. CTRLMMR_MCU_ENET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RGMII_ID_MODE	R/W	0h	Port1 RGMII internal transmit delay selection 0h - Internal transmit delay 1h - Reserved
3-2	RESERVED	R	0h	Reserved
1-0	MODE_SEL	R/W	1h	Selects ethernet switch Port1 interface 0h - GMII/MII (not supported) 1h - RMII 2h - RGMII 3h - SGMII (not supported)

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3.29 CTRLMMR_MCU_SPI1_CTRL Register (Proxy0 Offset = 4060h; Proxy1 Offset = 6060h) [reset = 0h]

CTRLMMR_MCU_SPI1_CTRL is shown in Figure 3-29 and described in Table 3-60.

Return to Summary Table.

Controls if MCU_SPI1 is directly connected to SPI3 in the MAIN Domain (default) or if MCU_SPI1 and SPI3 are independently pinned out.

Table 3-59. CTRLMMR_MCU_SPI1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4060h	40F0 6060h

Figure 3-29. CTRLMMR_MCU_SPI1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							SPI1_LINKDIS
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-60. CTRLMMR_MCU_SPI1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	SPI1_LINKDIS	R/W	0h	Disables direct connection of MCU_SPI1 to SPI3 0h - MCU_SPI1 is tied as a slave to SPI3. MCU_SPI1 CLK, DATA1 and CS0 are driven from SPI3, DATA OUT drives SPI3 DATA0 1h - MCU_SPI1 is NOT tied as a slave to SPI3. MCU_SPI1 CLK, DATA0, DATA1 and CS[3:0] are controlled through their respective MCU_SPI1 pins and SPI3 CLK, DATA0, DATA1, and CS[3:0] are controlled through their respective SPI3 pins.

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3.30 CTRLMMR_MCU_I3C0_CTRL0 Register (Proxy0 Offset = 4070h; Proxy1 Offset = 6070h) [reset = 1020000h]

CTRLMMR_MCU_I3C0_CTRL0 is shown in Figure 3-30 and described in Table 3-62.

Return to Summary Table.

Controls MCU I3C0 operation.

Table 3-61. CTRLMMR_MCU_I3C0_CTRL0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4070h	40F0 6070h

Figure 3-30. CTRLMMR_MCU_I3C0_CTRL0 Register

31	30	29	28	27	26	25	24
RESERVED	PID_MFR_ID						
R-0h	R/W-102h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MFR_ID							
R/W-102h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							ROLE
R-0h							R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PID_INSTANCE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-62. CTRLMMR_MCU_I3C0_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-16	PID_MFR_ID	R/W	102h	Manufacturer ID This input corresponds to bits[47:33] of the Provisional ID to identify the manufacturer. Defaults to TI value.
15-9	RESERVED	R	0h	Reserved
8	ROLE	R/W	0h	Master Role 0h - Main master 1h - Secondary master
7-4	RESERVED	R	0h	Reserved
3-0	PID_INSTANCE	R/W	0h	Provisional ID Instance. This input corresponds to bits[15:12] of the Provisional ID. It is intended to provide a way of differentiating several I3C devices if there would be no other way to have each manufactured device have a unique Provisional ID

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3.31 CTRLMMR_MCU_I3C0_CTRL1 Register (Proxy0 Offset = 4074h; Proxy1 Offset = 6074h) [reset = 0h]

CTRLMMR_MCU_I3C0_CTRL1 is shown in Figure 3-31 and described in Table 3-64.

Return to Summary Table.

Controls MCU I3C0 operation.

Table 3-63. CTRLMMR_MCU_I3C0_CTRL1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4074h	40F0 6074h

Figure 3-31. CTRLMMR_MCU_I3C0_CTRL1 Register

31	30	29	28	27	26	25	24
BUS_AVAIL_TIME							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						BUS_IDLE_TIME	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
BUS_IDLE_TIME							
R/W-0h							
7	6	5	4	3	2	1	0
BUS_IDLE_TIME							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-64. CTRLMMR_MCU_I3C0_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BUS_AVAIL_TIME	R/W	0h	Indicates the number of pclk cycles in the Bus Available condition
23-18	RESERVED	R	0h	Reserved
17-0	BUS_IDLE_TIME	R/W	0h	Indicates the number of pclk cycles in the Bus Idle condition

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3.32 CTRLMMR_MCU_I3C1_CTRL0 Register (Proxy0 Offset = 4078h; Proxy1 Offset = 6078h) [reset = 1020000h]

CTRLMMR_MCU_I3C1_CTRL0 is shown in Figure 3-32 and described in Table 3-66.

Return to Summary Table.

Controls MCU I3C1 operation.

Table 3-65. CTRLMMR_MCU_I3C1_CTRL0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4078h	40F0 6078h

Figure 3-32. CTRLMMR_MCU_I3C1_CTRL0 Register

31	30	29	28	27	26	25	24
RESERVED	PID_MFR_ID						
R-0h	R/W-102h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MFR_ID							
R/W-102h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							ROLE
R-0h							R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PID_INSTANCE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-66. CTRLMMR_MCU_I3C1_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-16	PID_MFR_ID	R/W	102h	Manufacturer ID This input corresponds to bits[47:33] of the Provisional ID to identify the manufacturer. Defaults to TI value.
15-9	RESERVED	R	0h	Reserved
8	ROLE	R/W	0h	Master Role 0h - Main master 1h - Secondary master
7-4	RESERVED	R	0h	Reserved
3-0	PID_INSTANCE	R/W	0h	Provisional ID Instance. This input corresponds to bits[15:12] of the Provisional ID. It is intended to provide a way of differentiating several I3C devices if there would be no other way to have each manufactured device have a unique Provisional ID

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3.33 CTRLMMR_MCU_I3C1_CTRL1 Register (Proxy0 Offset = 407Ch; Proxy1 Offset = 607Ch) [reset = 0h]

CTRLMMR_MCU_I3C1_CTRL1 is shown in Figure 3-33 and described in Table 3-68.

Return to Summary Table.

Controls MCU I3C1 operation.

Table 3-67. CTRLMMR_MCU_I3C1_CTRL1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 407Ch	40F0 607Ch

Figure 3-33. CTRLMMR_MCU_I3C1_CTRL1 Register

31	30	29	28	27	26	25	24
BUS_AVAIL_TIME							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						BUS_IDLE_TIME	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
BUS_IDLE_TIME							
R/W-0h							
7	6	5	4	3	2	1	0
BUS_IDLE_TIME							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-68. CTRLMMR_MCU_I3C1_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BUS_AVAIL_TIME	R/W	0h	Indicates the number of pclk cycles in the Bus Available condition
23-18	RESERVED	R	0h	Reserved
17-0	BUS_IDLE_TIME	R/W	0h	Indicates the number of pclk cycles in the Bus Idle condition

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3.34 CTRLMMR_MCU_I2C0_CTRL Register (Proxy0 Offset = 4080h; Proxy1 Offset = 6080h) [reset = 0h]

CTRLMMR_MCU_I2C0_CTRL is shown in Figure 3-34 and described in Table 3-70.

Return to Summary Table.

Controls MCU I2C0 operation.

Table 3-69. CTRLMMR_MCU_I2C0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4080h	40F0 6080h

Figure 3-34. CTRLMMR_MCU_I2C0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							HS_MCS_EN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-70. CTRLMMR_MCU_I2C0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HS_MCS_EN	R/W	0h	HS Mode master current source enable. When set, enables the current-source pull-up on the SCL output. Only one master on the I2C bus should enable SCL current sourcing.

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3.35 CTRLMMR_MCU_FSS_CTRL Register (Proxy0 Offset = 40A0h; Proxy1 Offset = 60A0h) [reset = 0h]

CTRLMMR_MCU_FSS_CTRL is shown in Figure 3-35 and described in Table 3-72.

Return to Summary Table.

Controls Flash boot region size and placement.

Table 3-71. CTRLMMR_MCU_FSS_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 40A0h	40F0 60A0h

Figure 3-35. CTRLMMR_MCU_FSS_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							S1_BOOT_SIZE
R-0h							R/W-0h
23	22	21	20	19	18	17	16
RESERVED		S1_BOOT_SEG					
R-0h		R/W-0h					
15	14	13	12	11	10	9	8
RESERVED							S0_BOOT_SIZE
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		S0_BOOT_SEG					
R-0h		R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-72. CTRLMMR_MCU_FSS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	S1_BOOT_SIZE	R/W	0h	Selects the size of the boot block to be used for the S1 (OSPI1) flash interface 0h - S1 boot size is 64 MB 1h - S1 boot size is 128 MB
23-22	RESERVED	R	0h	Reserved
21-16	S1_BOOT_SEG	R/W	0h	Selects the boot block to be used for the S1 (OSPI1) flash interface. If the s1_boot_size is 128 MB then only bits [4:0] of this field are used. Care must be taken to account for the address translation as to not fall off or wrap the address of the flash. (e.g. if both ECC and authentication are enabled for 64 MB boot, the highest valid block number is is 49, as sector 50 is only .2M Bytes in size.) 6'h00 - Use block 0 6'h01 - Use block 1 : 6'h3F - Use block 63
15-9	RESERVED	R	0h	Reserved
8	S0_BOOT_SIZE	R/W	0h	Selects the size of the boot block to be used for the S0 (OSPI0 or HyperBus) flash interface 0h - S0 boot size is 64 MB 1h - S0 boot size is 128 MB

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Table 3-72. CTRLMMR_MCU_FSS_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	S0_BOOT_SEG	R/W	0h	Selects the boot block to be used for the S0 (OSPI0 or HyperBus) flash interface. If the s0_boot_size is 128 MB then only bits [4:0] of this field are used. Care must be taken to account for the address translation as to not fall off or wrap the address of the flash. (e.g. if both ECC and authentication are enabled for 64 MB boot, the highest valid block number is is 49, as sector 50 is only .2M Bytes in size.) 6'h00 - Use block 0 6'h01 - Use block 1 : 6'h3F - Use block 63

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3.36 CTRLMMR_MCU_ADC0_CTRL Register (Proxy0 Offset = 40B0h; Proxy1 Offset = 60B0h) [reset = 0h]

CTRLMMR_MCU_ADC0_CTRL is shown in Figure 3-36 and described in Table 3-74.

Return to Summary Table.

Controls operation of MCU ADC0.

Table 3-73. CTRLMMR_MCU_ADC0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 40B0h	40F0 60B0h

Figure 3-36. CTRLMMR_MCU_ADC0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							GPI_MODE_EN
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED			TRIG_SEL				
R-0h			R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-74. CTRLMMR_MCU_ADC0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	GPI_MODE_EN	R/W	0h	Enables MCU_ADC0 data pins to be used as general purpose inputs when set. This signal is tied to the en_dig_test input of MCU_ADC0
15-5	RESERVED	R	0h	Reserved

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Table 3-74. CTRLMMR_MCU_ADC0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	TRIG_SEL	R/W	0h	Selects the source of the ADC hardware event trigger 0h - MCU_ADC_EXT_TRIGGER0 pin 1h - MCU_ADC_EXT_TRIGGER1 pin 2h - eHRPWM SOCA event 3h - eHRPWM SOCB event 4h - MCU Timer0 PWM output 5h - MCU Timer1 PWM output 6h - MCU Timer2 PWM output 7h - MCU Timer3 PWM output 8h - Timer0 PWM output 9h - Timer1 PWM output Ah - Timer2 PWM output Bh - Timer3 PWM output Ch - Timer4 PWM output Dh - Timer5 PWM output Eh - Timer6 PWM output Fh - Timer7 PWM output 10h - Timer8 PWM output 11h - Timer9 PWM output 12h - Timer10 PWM output 13h - Timer11 PWM output 14h - ICSS-G0 IEP0 CMP15 event 15h - ICSS-G0 IEP1 CMP15 event 16h - ICSS-G1 IEP0 CMP15 event 17h - ICSS-G1 IEP1 CMP15 event 18h - MCU Timer4 PWM output 19h - MCU Timer5 PWM output 1Ah - MCU Timer6 PWM output 1Bh - MCU Timer7 PWM output 1Ch - MCU Timer8 PWM output 1Dh - MCU Timer9 PWM output 1Eh - Reserved (tied 0h) 1Fh - Reserved (tied 0h)

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3.37 CTRLMMR_MCU_ADC1_CTRL Register (Proxy0 Offset = 40B4h; Proxy1 Offset = 60B4h) [reset = 1h]

CTRLMMR_MCU_ADC1_CTRL is shown in Figure 3-37 and described in Table 3-76.

Return to Summary Table.

Controls operation of MCU ADC1.

Table 3-75. CTRLMMR_MCU_ADC1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 40B4h	40F0 60B4h

Figure 3-37. CTRLMMR_MCU_ADC1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							GPI_MODE_EN
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED			TRIG_SEL				
R-0h			R/W-1h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-76. CTRLMMR_MCU_ADC1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	GPI_MODE_EN	R/W	0h	Enables MCU_ADC1 data pins to be used as general purpose inputs when set. This signal is tied to the en_dig_test input of MCU_ADC1
15-5	RESERVED	R	0h	Reserved

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Table 3-76. CTRLMMR_MCU_ADC1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	TRIG_SEL	R/W	1h	Selects the source of the ADC hardware event trigger 0h - MCU_ADC_EXT_TRIGGER0 pin 1h - MCU_ADC_EXT_TRIGGER1 pin 2h - eHRPWM SOCA event 3h - eHRPWM SOCB event 4h - MCU Timer0 PWM output 5h - MCU Timer1 PWM output 6h - MCU Timer2 PWM output 7h - MCU Timer3 PWM output 8h - Timer0 PWM output 9h - Timer1 PWM output Ah - Timer2 PWM output Bh - Timer3 PWM output Ch - Timer4 PWM output Dh - Timer5 PWM output Eh - Timer6 PWM output Fh - Timer7 PWM output 10h - Timer8 PWM output 11h - Timer9 PWM output 12h - Timer10 PWM output 13h - Timer11 PWM output 14h - ICSS-G0 IEP0 CMP15 event 15h - ICSS-G0 IEP1 CMP15 event 16h - ICSS-G1 IEP0 CMP15 event 17h - ICSS-G1 IEP1 CMP15 event 18h - MCU Timer4 PWM output 19h - MCU Timer5 PWM output 1Ah - MCU Timer6 PWM output 1Bh - MCU Timer7 PWM output 1Ch - MCU Timer8 PWM output 1Dh - MCU Timer9 PWM output 1Eh - Reserved (tied 0h) 1Fh - Reserved (tied 0h)

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3.38 CTRLMMR_MCU_TIMER0_CTRL Register (Proxy0 Offset = 4200h; Proxy1 Offset = 6200h) [reset = 0h]

CTRLMMR_MCU_TIMER0_CTRL is shown in Figure 3-38 and described in Table 3-78.

Return to Summary Table.

Controls MCU Timer0 operation.

Table 3-77. CTRLMMR_MCU_TIMER0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4200h	40F0 6200h

Figure 3-38. CTRLMMR_MCU_TIMER0_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CAP_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-78. CTRLMMR_MCU_TIMER0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CAP_SEL	R/W	0h	Selects the MCU_TIMERIO input pin for capture input signal. This control is only used when TIMER0 is configured for capture operation. 0h - Use MCU_TIMER_IO0 pin 1h - Use MCU_TIMER_IO1 pin 2h - Use MCU_TIMER_IO2 pin 3h - Use MCU_TIMER_IO3 pin 4h - Use MCU_TIMER_IO4 pin 5h - Use MCU_TIMER_IO5 pin 6h - Use MCU_TIMER_IO6 pin 7h - Use MCU_TIMER_IO7 pin 8h - Use MCU_TIMER_IO8 pin 9h - Use MCU_TIMER_IO9 pin

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3.39 CTRLMMR_MCU_TIMER1_CTRL Register (Proxy0 Offset = 4204h; Proxy1 Offset = 6204h) [reset = 0h]

CTRLMMR_MCU_TIMER1_CTRL is shown in Figure 3-39 and described in Table 3-80.

Return to Summary Table.

Controls MCU Timer1 operation.

Table 3-79. CTRLMMR_MCU_TIMER1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4204h	40F0 6204h

Figure 3-39. CTRLMMR_MCU_TIMER1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED				CAP_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-80. CTRLMMR_MCU_TIMER1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	When set, enables cascading of MCU_TIMER1 to MCU_TIMER0
7-4	RESERVED	R	0h	Reserved
3-0	CAP_SEL	R/W	0h	Selects the MCU_TIMERIO input pin for capture input signal. This control is only used when TIMER1 is configured for capture operation. 0h - Use MCU_TIMER_IO0 pin 1h - Use MCU_TIMER_IO1 pin 2h - Use MCU_TIMER_IO2 pin 3h - Use MCU_TIMER_IO3 pin 4h - Use MCU_TIMER_IO4 pin 5h - Use MCU_TIMER_IO5 pin 6h - Use MCU_TIMER_IO6 pin 7h - Use MCU_TIMER_IO7 pin 8h - Use MCU_TIMER_IO8 pin 9h - Use MCU_TIMER_IO9 pin

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3.40 CTRLMMR_MCU_TIMER2_CTRL Register (Proxy0 Offset = 4208h; Proxy1 Offset = 6208h) [reset = 0h]

CTRLMMR_MCU_TIMER2_CTRL is shown in Figure 3-40 and described in Table 3-82.

Return to Summary Table.

Controls MCU Timer2 operation.

Table 3-81. CTRLMMR_MCU_TIMER2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4208h	40F0 6208h

Figure 3-40. CTRLMMR_MCU_TIMER2_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CAP_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-82. CTRLMMR_MCU_TIMER2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CAP_SEL	R/W	0h	Selects the MCU_TIMERIO input pin for capture input signal. This control is only used when TIMER2 is configured for capture operation. 0h - Use MCU_TIMER_IO0 pin 1h - Use MCU_TIMER_IO1 pin 2h - Use MCU_TIMER_IO2 pin 3h - Use MCU_TIMER_IO3 pin 4h - Use MCU_TIMER_IO4 pin 5h - Use MCU_TIMER_IO5 pin 6h - Use MCU_TIMER_IO6 pin 7h - Use MCU_TIMER_IO7 pin 8h - Use MCU_TIMER_IO8 pin 9h - Use MCU_TIMER_IO9 pin

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3.41 CTRLMMR_MCU_TIMER3_CTRL Register (Proxy0 Offset = 420Ch; Proxy1 Offset = 620Ch) [reset = 0h]

CTRLMMR_MCU_TIMER3_CTRL is shown in Figure 3-41 and described in Table 3-84.

Return to Summary Table.

Controls MCU Timer3 operation.

Table 3-83. CTRLMMR_MCU_TIMER3_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 420Ch	40F0 620Ch

Figure 3-41. CTRLMMR_MCU_TIMER3_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED				CAP_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-84. CTRLMMR_MCU_TIMER3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	When set, enables cascading of MCU_TIMER3 to MCU_TIMER2
7-4	RESERVED	R	0h	Reserved
3-0	CAP_SEL	R/W	0h	Selects the MCU_TIMERIO input pin for capture input signal. This control is only used when TIMER3 is configured for capture operation. 0h - Use MCU_TIMER_IO0 pin 1h - Use MCU_TIMER_IO1 pin 2h - Use MCU_TIMER_IO2 pin 3h - Use MCU_TIMER_IO3 pin 4h - Use MCU_TIMER_IO4 pin 5h - Use MCU_TIMER_IO5 pin 6h - Use MCU_TIMER_IO6 pin 7h - Use MCU_TIMER_IO7 pin 8h - Use MCU_TIMER_IO8 pin 9h - Use MCU_TIMER_IO9 pin

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3.42 CTRLMMR_MCU_TIMER4_CTRL Register (Proxy0 Offset = 4210h; Proxy1 Offset = 6210h) [reset = 0h]

CTRLMMR_MCU_TIMER4_CTRL is shown in Figure 3-42 and described in Table 3-86.

Return to Summary Table.

Controls MCU Timer4 operation.

Table 3-85. CTRLMMR_MCU_TIMER4_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4210h	40F0 6210h

Figure 3-42. CTRLMMR_MCU_TIMER4_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CAP_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-86. CTRLMMR_MCU_TIMER4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CAP_SEL	R/W	0h	Selects the MCU_TIMERIO input pin for capture input signal. This control is only used when TIMER4 is configured for capture operation. 0h - Use MCU_TIMER_IO0 pin 1h - Use MCU_TIMER_IO1 pin 2h - Use MCU_TIMER_IO2 pin 3h - Use MCU_TIMER_IO3 pin 4h - Use MCU_TIMER_IO4 pin 5h - Use MCU_TIMER_IO5 pin 6h - Use MCU_TIMER_IO6 pin 7h - Use MCU_TIMER_IO7 pin 8h - Use MCU_TIMER_IO8 pin 9h - Use MCU_TIMER_IO9 pin

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3.43 CTRLMMR_MCU_TIMER5_CTRL Register (Proxy0 Offset = 4214h; Proxy1 Offset = 6214h) [reset = 0h]

CTRLMMR_MCU_TIMER5_CTRL is shown in Figure 3-43 and described in Table 3-88.

Return to Summary Table.

Controls MCU Timer5 operation.

Table 3-87. CTRLMMR_MCU_TIMER5_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4214h	40F0 6214h

Figure 3-43. CTRLMMR_MCU_TIMER5_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED				CAP_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-88. CTRLMMR_MCU_TIMER5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	When set, enables cascading of MCU_TIMER5 to MCU_TIMER4
7-4	RESERVED	R	0h	Reserved
3-0	CAP_SEL	R/W	0h	Selects the MCU_TIMERIO input pin for capture input signal. This control is only used when TIMER5 is configured for capture operation. 0h - Use MCU_TIMER_IO0 pin 1h - Use MCU_TIMER_IO1 pin 2h - Use MCU_TIMER_IO2 pin 3h - Use MCU_TIMER_IO3 pin 4h - Use MCU_TIMER_IO4 pin 5h - Use MCU_TIMER_IO5 pin 6h - Use MCU_TIMER_IO6 pin 7h - Use MCU_TIMER_IO7 pin 8h - Use MCU_TIMER_IO8 pin 9h - Use MCU_TIMER_IO9 pin

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3.44 CTRLMMR_MCU_TIMER6_CTRL Register (Proxy0 Offset = 4218h; Proxy1 Offset = 6218h) [reset = 0h]

CTRLMMR_MCU_TIMER6_CTRL is shown in Figure 3-44 and described in Table 3-90.

Return to Summary Table.

Controls MCU Timer6 operation.

Table 3-89. CTRLMMR_MCU_TIMER6_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4218h	40F0 6218h

Figure 3-44. CTRLMMR_MCU_TIMER6_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CAP_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-90. CTRLMMR_MCU_TIMER6_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CAP_SEL	R/W	0h	Selects the MCU_TIMERIO input pin for capture input signal. This control is only used when TIMER6 is configured for capture operation. 0h - Use MCU_TIMER_IO0 pin 1h - Use MCU_TIMER_IO1 pin 2h - Use MCU_TIMER_IO2 pin 3h - Use MCU_TIMER_IO3 pin 4h - Use MCU_TIMER_IO4 pin 5h - Use MCU_TIMER_IO5 pin 6h - Use MCU_TIMER_IO6 pin 7h - Use MCU_TIMER_IO7 pin 8h - Use MCU_TIMER_IO8 pin 9h - Use MCU_TIMER_IO9 pin

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3.45 CTRLMMR_MCU_TIMER7_CTRL Register (Proxy0 Offset = 421Ch; Proxy1 Offset = 621Ch) [reset = 0h]

CTRLMMR_MCU_TIMER7_CTRL is shown in Figure 3-45 and described in Table 3-92.

Return to Summary Table.

Controls MCU Timer7 operation.

Table 3-91. CTRLMMR_MCU_TIMER7_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 421Ch	40F0 621Ch

Figure 3-45. CTRLMMR_MCU_TIMER7_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED				CAP_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-92. CTRLMMR_MCU_TIMER7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	When set, enables cascading of MCU_TIMER7 to MCU_TIMER6
7-4	RESERVED	R	0h	Reserved
3-0	CAP_SEL	R/W	0h	Selects the MCU_TIMERIO input pin for capture input signal. This control is only used when TIMER7 is configured for capture operation. 0h - Use MCU_TIMER_IO0 pin 1h - Use MCU_TIMER_IO1 pin 2h - Use MCU_TIMER_IO2 pin 3h - Use MCU_TIMER_IO3 pin 4h - Use MCU_TIMER_IO4 pin 5h - Use MCU_TIMER_IO5 pin 6h - Use MCU_TIMER_IO6 pin 7h - Use MCU_TIMER_IO7 pin 8h - Use MCU_TIMER_IO8 pin 9h - Use MCU_TIMER_IO9 pin

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3.46 CTRLMMR_MCU_TIMER8_CTRL Register (Proxy0 Offset = 4220h; Proxy1 Offset = 6220h) [reset = 0h]

CTRLMMR_MCU_TIMER8_CTRL is shown in Figure 3-46 and described in Table 3-94.

Return to Summary Table.

Controls MCU Timer8 operation.

Table 3-93. CTRLMMR_MCU_TIMER8_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4220h	40F0 6220h

Figure 3-46. CTRLMMR_MCU_TIMER8_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CAP_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-94. CTRLMMR_MCU_TIMER8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CAP_SEL	R/W	0h	Selects the MCU_TIMERIO input pin for capture input signal. This control is only used when TIMER8 is configured for capture operation. 0h - Use MCU_TIMER_IO0 pin 1h - Use MCU_TIMER_IO1 pin 2h - Use MCU_TIMER_IO2 pin 3h - Use MCU_TIMER_IO3 pin 4h - Use MCU_TIMER_IO4 pin 5h - Use MCU_TIMER_IO5 pin 6h - Use MCU_TIMER_IO6 pin 7h - Use MCU_TIMER_IO7 pin 8h - Use MCU_TIMER_IO8 pin 9h - Use MCU_TIMER_IO9 pin

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3.47 CTRLMMR_MCU_TIMER9_CTRL Register (Proxy0 Offset = 4224h; Proxy1 Offset = 6224h) [reset = 0h]

CTRLMMR_MCU_TIMER9_CTRL is shown in Figure 3-47 and described in Table 3-96.

Return to Summary Table.

Controls MCU Timer9 operation.

Table 3-95. CTRLMMR_MCU_TIMER9_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4224h	40F0 6224h

Figure 3-47. CTRLMMR_MCU_TIMER9_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED				CAP_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-96. CTRLMMR_MCU_TIMER9_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	When set, enables cascading of MCU_TIMER9 to MCU_TIMER8
7-4	RESERVED	R	0h	Reserved
3-0	CAP_SEL	R/W	0h	Selects the MCU_TIMERIO input pin for capture input signal. This control is only used when TIMER9 is configured for capture operation. 0h - Use MCU_TIMER_IO0 pin 1h - Use MCU_TIMER_IO1 pin 2h - Use MCU_TIMER_IO2 pin 3h - Use MCU_TIMER_IO3 pin 4h - Use MCU_TIMER_IO4 pin 5h - Use MCU_TIMER_IO5 pin 6h - Use MCU_TIMER_IO6 pin 7h - Use MCU_TIMER_IO7 pin 8h - Use MCU_TIMER_IO8 pin 9h - Use MCU_TIMER_IO9 pin

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3.48 CTRLMMR_MCU_TIMERIO0_CTRL Register (Proxy0 Offset = 4280h; Proxy1 Offset = 6280h) [reset = Fh]

CTRLMMR_MCU_TIMERIO0_CTRL is shown in Figure 3-48 and described in Table 3-98.

Return to Summary Table.

Controls MCU TimerIO muxing.

Table 3-97. CTRLMMR_MCU_TIMERIO0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4280h	40F0 6280h

Figure 3-48. CTRLMMR_MCU_TIMERIO0_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-98. CTRLMMR_MCU_TIMERIO0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	OUT_SEL	R/W	Fh	Selects the source of the MCU_TIMERIO0 output 0h - MCU_TIMERIO0 is driven by MCU_TIMER0 output 1h - MCU_TIMERIO0 is driven by MCU_TIMER1 output 2h - MCU_TIMERIO0 is driven by MCU_TIMER2 output 3h - MCU_TIMERIO0 is driven by MCU_TIMER3 output 4h - MCU_TIMERIO0 is driven by MCU_TIMER4 output 5h - MCU_TIMERIO0 is driven by MCU_TIMER5 output 6h - MCU_TIMERIO0 is driven by MCU_TIMER6 output 7h - MCU_TIMERIO0 is driven by MCU_TIMER7 output 8h - MCU_TIMERIO0 is driven by MCU_TIMER8 output 9h - MCU_TIMERIO0 is driven by MCU_TIMER9 output Ah - MCU_TIMERIO0 is driven low Bh - MCU_TIMERIO0 is driven high Ch - MCU_TIMERIO0 is driven low Dh - MCU_TIMERIO0 is driven high Eh - MCU_TIMERIO0 is driven low Fh - MCU_TIMERIO0 is driven high

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3.49 CTRLMMR_MCU_TIMERIO1_CTRL Register (Proxy0 Offset = 4284h; Proxy1 Offset = 6284h) [reset = Fh]

CTRLMMR_MCU_TIMERIO1_CTRL is shown in Figure 3-49 and described in Table 3-100.

Return to Summary Table.

Controls MCU TimerIO muxing.

Table 3-99. CTRLMMR_MCU_TIMERIO1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4284h	40F0 6284h

Figure 3-49. CTRLMMR_MCU_TIMERIO1_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-100. CTRLMMR_MCU_TIMERIO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	OUT_SEL	R/W	Fh	Selects the source of the MCU_TIMERIO1 output 0h - MCU_TIMERIO1 is driven by MCU_TIMER0 output 1h - MCU_TIMERIO1 is driven by MCU_TIMER1 output 2h - MCU_TIMERIO1 is driven by MCU_TIMER2 output 3h - MCU_TIMERIO1 is driven by MCU_TIMER3 output 4h - MCU_TIMERIO1 is driven by MCU_TIMER4 output 5h - MCU_TIMERIO1 is driven by MCU_TIMER5 output 6h - MCU_TIMERIO1 is driven by MCU_TIMER6 output 7h - MCU_TIMERIO1 is driven by MCU_TIMER7 output 8h - MCU_TIMERIO1 is driven by MCU_TIMER8 output 9h - MCU_TIMERIO1 is driven by MCU_TIMER9 output Ah - MCU_TIMERIO1 is driven low Bh - MCU_TIMERIO1 is driven high Ch - MCU_TIMERIO1 is driven low Dh - MCU_TIMERIO1 is driven high Eh - MCU_TIMERIO1 is driven low Fh - MCU_TIMERIO1 is driven high

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3.50 CTRLMMR_MCU_TIMERIO2_CTRL Register (Proxy0 Offset = 4288h; Proxy1 Offset = 6288h) [reset = Fh]

CTRLMMR_MCU_TIMERIO2_CTRL is shown in Figure 3-50 and described in Table 3-102.

Return to Summary Table.

Controls MCU TimerIO muxing.

Table 3-101. CTRLMMR_MCU_TIMERIO2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4288h	40F0 6288h

Figure 3-50. CTRLMMR_MCU_TIMERIO2_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-102. CTRLMMR_MCU_TIMERIO2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	OUT_SEL	R/W	Fh	Selects the source of the MCU_TIMERIO2 output 0h - MCU_TIMERIO2 is driven by MCU_TIMER0 output 1h - MCU_TIMERIO2 is driven by MCU_TIMER1 output 2h - MCU_TIMERIO2 is driven by MCU_TIMER2 output 3h - MCU_TIMERIO2 is driven by MCU_TIMER3 output 4h - MCU_TIMERIO2 is driven by MCU_TIMER4 output 5h - MCU_TIMERIO2 is driven by MCU_TIMER5 output 6h - MCU_TIMERIO2 is driven by MCU_TIMER6 output 7h - MCU_TIMERIO2 is driven by MCU_TIMER7 output 8h - MCU_TIMERIO2 is driven by MCU_TIMER8 output 9h - MCU_TIMERIO2 is driven by MCU_TIMER9 output Ah - MCU_TIMERIO2 is driven low Bh - MCU_TIMERIO2 is driven high Ch - MCU_TIMERIO2 is driven low Dh - MCU_TIMERIO2 is driven high Eh - MCU_TIMERIO2 is driven low Fh - MCU_TIMERIO2 is driven high

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3.51 CTRLMMR_MCU_TIMERIO3_CTRL Register (Proxy0 Offset = 428Ch; Proxy1 Offset = 628Ch) [reset = Fh]

CTRLMMR_MCU_TIMERIO3_CTRL is shown in Figure 3-51 and described in Table 3-104.

Return to Summary Table.

Controls MCU TimerIO muxing.

Table 3-103. CTRLMMR_MCU_TIMERIO3_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 428Ch	40F0 628Ch

Figure 3-51. CTRLMMR_MCU_TIMERIO3_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-104. CTRLMMR_MCU_TIMERIO3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	OUT_SEL	R/W	Fh	Selects the source of the MCU_TIMERIO3 output 0h - MCU_TIMERIO3 is driven by MCU_TIMER0 output 1h - MCU_TIMERIO3 is driven by MCU_TIMER1 output 2h - MCU_TIMERIO3 is driven by MCU_TIMER2 output 3h - MCU_TIMERIO3 is driven by MCU_TIMER3 output 4h - MCU_TIMERIO3 is driven by MCU_TIMER4 output 5h - MCU_TIMERIO3 is driven by MCU_TIMER5 output 6h - MCU_TIMERIO3 is driven by MCU_TIMER6 output 7h - MCU_TIMERIO3 is driven by MCU_TIMER7 output 8h - MCU_TIMERIO3 is driven by MCU_TIMER8 output 9h - MCU_TIMERIO3 is driven by MCU_TIMER9 output Ah - MCU_TIMERIO3 is driven low Bh - MCU_TIMERIO3 is driven high Ch - MCU_TIMERIO3 is driven low Dh - MCU_TIMERIO3 is driven high Eh - MCU_TIMERIO3 is driven low Fh - MCU_TIMERIO3 is driven high

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3.52 CTRLMMR_MCU_TIMERIO4_CTRL Register (Proxy0 Offset = 4290h; Proxy1 Offset = 6290h) [reset = Fh]

CTRLMMR_MCU_TIMERIO4_CTRL is shown in Figure 3-52 and described in Table 3-106.

Return to Summary Table.

Controls MCU TimerIO muxing.

Table 3-105. CTRLMMR_MCU_TIMERIO4_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4290h	40F0 6290h

Figure 3-52. CTRLMMR_MCU_TIMERIO4_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-106. CTRLMMR_MCU_TIMERIO4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	OUT_SEL	R/W	Fh	Selects the source of the MCU_TIMERIO4 output 0h - MCU_TIMERIO4 is driven by MCU_TIMER0 output 1h - MCU_TIMERIO4 is driven by MCU_TIMER1 output 2h - MCU_TIMERIO4 is driven by MCU_TIMER2 output 3h - MCU_TIMERIO4 is driven by MCU_TIMER3 output 4h - MCU_TIMERIO4 is driven by MCU_TIMER4 output 5h - MCU_TIMERIO4 is driven by MCU_TIMER5 output 6h - MCU_TIMERIO4 is driven by MCU_TIMER6 output 7h - MCU_TIMERIO4 is driven by MCU_TIMER7 output 8h - MCU_TIMERIO4 is driven by MCU_TIMER8 output 9h - MCU_TIMERIO4 is driven by MCU_TIMER9 output Ah - MCU_TIMERIO4 is driven low Bh - MCU_TIMERIO4 is driven high Ch - MCU_TIMERIO4 is driven low Dh - MCU_TIMERIO4 is driven high Eh - MCU_TIMERIO4 is driven low Fh - MCU_TIMERIO4 is driven high

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3.53 CTRLMMR_MCU_TIMERIO5_CTRL Register (Proxy0 Offset = 4294h; Proxy1 Offset = 6294h) [reset = Fh]

CTRLMMR_MCU_TIMERIO5_CTRL is shown in Figure 3-53 and described in Table 3-108.

Return to Summary Table.

Controls MCU TimerIO muxing.

Table 3-107. CTRLMMR_MCU_TIMERIO5_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4294h	40F0 6294h

Figure 3-53. CTRLMMR_MCU_TIMERIO5_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-108. CTRLMMR_MCU_TIMERIO5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	OUT_SEL	R/W	Fh	Selects the source of the MCU_TIMERIO5 output 0h - MCU_TIMERIO5 is driven by MCU_TIMER0 output 1h - MCU_TIMERIO5 is driven by MCU_TIMER1 output 2h - MCU_TIMERIO5 is driven by MCU_TIMER2 output 3h - MCU_TIMERIO5 is driven by MCU_TIMER3 output 4h - MCU_TIMERIO5 is driven by MCU_TIMER4 output 5h - MCU_TIMERIO5 is driven by MCU_TIMER5 output 6h - MCU_TIMERIO5 is driven by MCU_TIMER6 output 7h - MCU_TIMERIO5 is driven by MCU_TIMER7 output 8h - MCU_TIMERIO5 is driven by MCU_TIMER8 output 9h - MCU_TIMERIO5 is driven by MCU_TIMER9 output Ah - MCU_TIMERIO5 is driven low Bh - MCU_TIMERIO5 is driven high Ch - MCU_TIMERIO5 is driven low Dh - MCU_TIMERIO5 is driven high Eh - MCU_TIMERIO5 is driven low Fh - MCU_TIMERIO5 is driven high

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3.54 CTRLMMR_MCU_TIMERIO6_CTRL Register (Proxy0 Offset = 4298h; Proxy1 Offset = 6298h) [reset = Fh]

CTRLMMR_MCU_TIMERIO6_CTRL is shown in Figure 3-54 and described in Table 3-110.

Return to Summary Table.

Controls MCU TimerIO muxing.

Table 3-109. CTRLMMR_MCU_TIMERIO6_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 4298h	40F0 6298h

Figure 3-54. CTRLMMR_MCU_TIMERIO6_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-110. CTRLMMR_MCU_TIMERIO6_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	OUT_SEL	R/W	Fh	Selects the source of the MCU_TIMERIO6 output 0h - MCU_TIMERIO6 is driven by MCU_TIMER0 output 1h - MCU_TIMERIO6 is driven by MCU_TIMER1 output 2h - MCU_TIMERIO6 is driven by MCU_TIMER2 output 3h - MCU_TIMERIO6 is driven by MCU_TIMER3 output 4h - MCU_TIMERIO6 is driven by MCU_TIMER4 output 5h - MCU_TIMERIO6 is driven by MCU_TIMER5 output 6h - MCU_TIMERIO6 is driven by MCU_TIMER6 output 7h - MCU_TIMERIO6 is driven by MCU_TIMER7 output 8h - MCU_TIMERIO6 is driven by MCU_TIMER8 output 9h - MCU_TIMERIO6 is driven by MCU_TIMER9 output Ah - MCU_TIMERIO6 is driven low Bh - MCU_TIMERIO6 is driven high Ch - MCU_TIMERIO6 is driven low Dh - MCU_TIMERIO6 is driven high Eh - MCU_TIMERIO6 is driven low Fh - MCU_TIMERIO6 is driven high

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3.55 CTRLMMR_MCU_TIMERIO7_CTRL Register (Proxy0 Offset = 429Ch; Proxy1 Offset = 629Ch) [reset = Fh]

CTRLMMR_MCU_TIMERIO7_CTRL is shown in Figure 3-55 and described in Table 3-112.

Return to Summary Table.

Controls MCU TimerIO muxing.

Table 3-111. CTRLMMR_MCU_TIMERIO7_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 429Ch	40F0 629Ch

Figure 3-55. CTRLMMR_MCU_TIMERIO7_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-112. CTRLMMR_MCU_TIMERIO7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	OUT_SEL	R/W	Fh	Selects the source of the MCU_TIMERIO7 output 0h - MCU_TIMERIO7 is driven by MCU_TIMER0 output 1h - MCU_TIMERIO7 is driven by MCU_TIMER1 output 2h - MCU_TIMERIO7 is driven by MCU_TIMER2 output 3h - MCU_TIMERIO7 is driven by MCU_TIMER3 output 4h - MCU_TIMERIO7 is driven by MCU_TIMER4 output 5h - MCU_TIMERIO7 is driven by MCU_TIMER5 output 6h - MCU_TIMERIO7 is driven by MCU_TIMER6 output 7h - MCU_TIMERIO7 is driven by MCU_TIMER7 output 8h - MCU_TIMERIO7 is driven by MCU_TIMER8 output 9h - MCU_TIMERIO7 is driven by MCU_TIMER9 output Ah - MCU_TIMERIO7 is driven low Bh - MCU_TIMERIO7 is driven high Ch - MCU_TIMERIO7 is driven low Dh - MCU_TIMERIO7 is driven high Eh - MCU_TIMERIO7 is driven low Fh - MCU_TIMERIO7 is driven high

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3.56 CTRLMMR_MCU_TIMERIO8_CTRL Register (Proxy0 Offset = 42A0h; Proxy1 Offset = 62A0h) [reset = Fh]

CTRLMMR_MCU_TIMERIO8_CTRL is shown in Figure 3-56 and described in Table 3-114.

Return to Summary Table.

Controls MCU TimerIO muxing.

Table 3-113. CTRLMMR_MCU_TIMERIO8_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 42A0h	40F0 62A0h

Figure 3-56. CTRLMMR_MCU_TIMERIO8_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-114. CTRLMMR_MCU_TIMERIO8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	OUT_SEL	R/W	Fh	Selects the source of the MCU_TIMERIO8 output 0h - MCU_TIMERIO8 is driven by MCU_TIMER0 output 1h - MCU_TIMERIO8 is driven by MCU_TIMER1 output 2h - MCU_TIMERIO8 is driven by MCU_TIMER2 output 3h - MCU_TIMERIO8 is driven by MCU_TIMER3 output 4h - MCU_TIMERIO8 is driven by MCU_TIMER4 output 5h - MCU_TIMERIO8 is driven by MCU_TIMER5 output 6h - MCU_TIMERIO8 is driven by MCU_TIMER6 output 7h - MCU_TIMERIO8 is driven by MCU_TIMER7 output 8h - MCU_TIMERIO8 is driven by MCU_TIMER8 output 9h - MCU_TIMERIO8 is driven by MCU_TIMER9 output Ah - MCU_TIMERIO8 is driven low Bh - MCU_TIMERIO8 is driven high Ch - MCU_TIMERIO8 is driven low Dh - MCU_TIMERIO8 is driven high Eh - MCU_TIMERIO8 is driven low Fh - MCU_TIMERIO8 is driven high

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3.57 CTRLMMR_MCU_TIMERIO9_CTRL Register (Proxy0 Offset = 42A4h; Proxy1 Offset = 62A4h) [reset = Fh]

CTRLMMR_MCU_TIMERIO9_CTRL is shown in Figure 3-57 and described in Table 3-116.

Return to Summary Table.

Controls MCU TimerIO muxing.

Table 3-115. CTRLMMR_MCU_TIMERIO9_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 42A4h	40F0 62A4h

Figure 3-57. CTRLMMR_MCU_TIMERIO9_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-Fh			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-116. CTRLMMR_MCU_TIMERIO9_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	OUT_SEL	R/W	Fh	Selects the source of the MCU_TIMERIO9 output 0h - MCU_TIMERIO9 is driven by MCU_TIMER0 output 1h - MCU_TIMERIO9 is driven by MCU_TIMER1 output 2h - MCU_TIMERIO9 is driven by MCU_TIMER2 output 3h - MCU_TIMERIO9 is driven by MCU_TIMER3 output 4h - MCU_TIMERIO9 is driven by MCU_TIMER4 output 5h - MCU_TIMERIO9 is driven by MCU_TIMER5 output 6h - MCU_TIMERIO9 is driven by MCU_TIMER6 output 7h - MCU_TIMERIO9 is driven by MCU_TIMER7 output 8h - MCU_TIMERIO9 is driven by MCU_TIMER8 output 9h - MCU_TIMERIO9 is driven by MCU_TIMER9 output Ah - MCU_TIMERIO9 is driven low Bh - MCU_TIMERIO9 is driven high Ch - MCU_TIMERIO9 is driven low Dh - MCU_TIMERIO9 is driven high Eh - MCU_TIMERIO9 is driven low Fh - MCU_TIMERIO9 is driven high

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3.58 CTRLMMR_MCU_LOCK1_KICK0 Register (Proxy0 Offset = 5008h; Proxy1 Offset = 7008h) [reset = 0h]

CTRLMMR_MCU_LOCK1_KICK0 is shown in Figure 3-58 and described in Table 3-118.

Return to Summary Table.

Lower 32-bits of Partition1 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_MCU_LOCK1_KICK1 with its key value before write-protected Partition 1 registers can be written.

Table 3-117. CTRLMMR_MCU_LOCK1_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 5008h	40F0 7008h

Figure 3-58. CTRLMMR_MCU_LOCK1_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-118. CTRLMMR_MCU_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition1 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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3.59 CTRLMMR_MCU_LOCK1_KICK1 Register (Proxy0 Offset = 500Ch; Proxy1 Offset = 700Ch) [reset = 0h]

CTRLMMR_MCU_LOCK1_KICK1 is shown in Figure 3-59 and described in Table 3-120.

Return to Summary Table.

Upper 32-bits of Partition 1 write lock key. This register must be written with the designated key value after a write to CTRLMMR_MCU_LOCK1_KICK0 with its key value before write-protected Partition 1 registers can be written.

Table 3-119. CTRLMMR_MCU_LOCK1_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 500Ch	40F0 700Ch

Figure 3-59. CTRLMMR_MCU_LOCK1_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-120. CTRLMMR_MCU_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition1 registers

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3.60 CTRLMMR_MCU_P1_CLAIM0 Register (Proxy0 Offset = 5100h; Proxy1 Offset = 7100h) [reset = 0h]

CTRLMMR_MCU_P1_CLAIM0 is shown in Figure 3-60 and described in Table 3-122.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 3-121. CTRLMMR_MCU_P1_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 5100h	40F0 7100h

Figure 3-60. CTRLMMR_MCU_P1_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-122. CTRLMMR_MCU_P1_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 4000h + (0 x 80h) + (b x 4h) and register Proxy1 address of: 6000h + (0 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.61 CTRLMMR_MCU_P1_CLAIM1 Register (Proxy0 Offset = 5104h; Proxy1 Offset = 7104h) [reset = 0h]

CTRLMMR_MCU_P1_CLAIM1 is shown in Figure 3-61 and described in Table 3-124.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 3-123. CTRLMMR_MCU_P1_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 5104h	40F0 7104h

Figure 3-61. CTRLMMR_MCU_P1_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-124. CTRLMMR_MCU_P1_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 4000h + (1 x 80h) + (b x 4h) and register Proxy1 address of: 6000h + (1 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.62 CTRLMMR_MCU_P1_CLAIM2 Register (Proxy0 Offset = 5108h; Proxy1 Offset = 7108h) [reset = 0h]

CTRLMMR_MCU_P1_CLAIM2 is shown in Figure 3-62 and described in Table 3-126.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 3-125. CTRLMMR_MCU_P1_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 5108h	40F0 7108h

Figure 3-62. CTRLMMR_MCU_P1_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-126. CTRLMMR_MCU_P1_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 4000h + (2 x 80h) + (b x 4h) and register Proxy1 address of: 6000h + (2 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.63 CTRLMMR_MCU_P1_CLAIM3 Register (Proxy0 Offset = 510Ch; Proxy1 Offset = 710Ch) [reset = 0h]

CTRLMMR_MCU_P1_CLAIM3 is shown in Figure 3-63 and described in Table 3-128.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 3-127. CTRLMMR_MCU_P1_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 510Ch	40F0 710Ch

Figure 3-63. CTRLMMR_MCU_P1_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-128. CTRLMMR_MCU_P1_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 4000h + (3 x 80h) + (b x 4h) and register Proxy1 address of: 6000h + (3 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.64 CTRLMMR_MCU_P1_CLAIM4 Register (Proxy0 Offset = 5110h; Proxy1 Offset = 7110h) [reset = 0h]

CTRLMMR_MCU_P1_CLAIM4 is shown in Figure 3-64 and described in Table 3-130.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 3-129. CTRLMMR_MCU_P1_CLAIM4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 5110h	40F0 7110h

Figure 3-64. CTRLMMR_MCU_P1_CLAIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 3-130. CTRLMMR_MCU_P1_CLAIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 4000h + (4 x 80h) + (b x 4h) and register Proxy1 address of: 6000h + (4 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.65 CTRLMMR_MCU_P1_CLAIM5 Register (Proxy0 Offset = 5114h; Proxy1 Offset = 7114h) [reset = 0h]

CTRLMMR_MCU_P1_CLAIM5 is shown in Figure 3-65 and described in Table 3-132.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 3-131. CTRLMMR_MCU_P1_CLAIM5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 5114h	40F0 7114h

Figure 3-65. CTRLMMR_MCU_P1_CLAIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-132. CTRLMMR_MCU_P1_CLAIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 4000h + (5 x 80h) + (b x 4h) and register Proxy1 address of: 6000h + (5 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.66 CTRLMMR_MCU_CLKOUT0_CTRL Register (Proxy0 Offset = 8010h; Proxy1 Offset = A010h) [reset = 0h]

CTRLMMR_MCU_CLKOUT0_CTRL is shown in Figure 3-66 and described in Table 3-134.

Return to Summary Table.

Enables and selects clock source of CPSW MCU_CLKOUT0 pin.

Table 3-133. CTRLMMR_MCU_CLKOUT0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8010h	40F0 A010h

Figure 3-66. CTRLMMR_MCU_CLKOUT0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			CLK_EN	RESERVED			CLK_SEL
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-134. CTRLMMR_MCU_CLKOUT0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	CLK_EN	R/W	0h	When set, enables MCU_CLKOUT0 output
3-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects MCU_CLKOUT0 clock source 0h - RGMII_MHZ_50_CLK (50 MHz) 1h - RGMII_MHZ_50_CLK / 2 (25 MHz)

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3.67 CTRLMMR_MCU_EFUSE_CLKSEL Register (Proxy0 Offset = 8018h; Proxy1 Offset = A018h) [reset = 0h]

CTRLMMR_MCU_EFUSE_CLKSEL is shown in Figure 3-67 and described in Table 3-136.

Return to Summary Table.

Selects the functional clock source for the MCU domain eFuse Controller.

Table 3-135. CTRLMMR_MCU_EFUSE_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8018h	40F0 A018h

Figure 3-67. CTRLMMR_MCU_EFUSE_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-136. CTRLMMR_MCU_EFUSE_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source 0h - EFUSE_CLK (WKUP_HFOSC0_CLKOUT or CLK_12M_RC) 1h - MCU_SYSCLK0 / 8

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3.68 CTRLMMR_MCU_MCAN0_CLKSEL Register (Proxy0 Offset = 8020h; Proxy1 Offset = A020h) [reset = 0h]

CTRLMMR_MCU_MCAN0_CLKSEL is shown in Figure 3-68 and described in Table 3-138.

Return to Summary Table.

Controls the functional clock source for MCU_MCAN0.

Table 3-137. CTRLMMR_MCU_MCAN0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8020h	40F0 A020h

Figure 3-68. CTRLMMR_MCU_MCAN0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-138. CTRLMMR_MCU_MCAN0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MCU_MCAN MCAN_CLK selection 0h - MCU_PLL2_HSDIV3_CLKOUT 1h - MCU_EXT_REFCLK0 2h - MCU_PLL1_HSDIV2_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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3.69 CTRLMMR_MCU_MCAN1_CLKSEL Register (Proxy0 Offset = 8024h; Proxy1 Offset = A024h) [reset = 0h]

CTRLMMR_MCU_MCAN1_CLKSEL is shown in Figure 3-69 and described in Table 3-140.

Return to Summary Table.

Controls the functional clock source for MCU_MCAN1.

Table 3-139. CTRLMMR_MCU_MCAN1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8024h	40F0 A024h

Figure 3-69. CTRLMMR_MCU_MCAN1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-140. CTRLMMR_MCU_MCAN1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MCU_MCAN MCAN_CLK selection 0h - MCU_PLL2_HSDIV3_CLKOUT 1h - MCU_EXT_REFCLK0 2h - MCU_PLL1_HSDIV2_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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3.70 CTRLMMR_MCU_OSPI0_CLKSEL Register (Proxy0 Offset = 8030h; Proxy1 Offset = A030h) [reset = 0h]

CTRLMMR_MCU_OSPI0_CLKSEL is shown in Figure 3-70 and described in Table 3-142.

Return to Summary Table.

Controls the OSPI loopback clock source.

Table 3-141. CTRLMMR_MCU_OSPI0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8030h	40F0 A030h

Figure 3-70. CTRLMMR_MCU_OSPI0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			LOOPCLK_SEL	RESERVED			CLK_SEL
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-142. CTRLMMR_MCU_OSPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	LOOPCLK_SEL	R/W	0h	OBSPI0 Loopback clock source 0h - OSPI_DQS external pin (external) 1h - OSPI_LBCLKO output (internal)
3-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	OSPI0 reference clock selection 0h - MCU_PLL1_HSDIV4_CLKOUT 1h - MCU_PLL2_HSDIV4_CLKOUT

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3.71 CTRLMMR_MCU_OSPI1_CLKSEL Register (Proxy0 Offset = 8034h; Proxy1 Offset = A034h) [reset = 0h]

CTRLMMR_MCU_OSPI1_CLKSEL is shown in Figure 3-71 and described in Table 3-144.

Return to Summary Table.

Controls the OSPI loopback clock source.

Table 3-143. CTRLMMR_MCU_OSPI1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8034h	40F0 A034h

Figure 3-71. CTRLMMR_MCU_OSPI1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			LOOPCLK_SEL	RESERVED			CLK_SEL
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-144. CTRLMMR_MCU_OSPI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	LOOPCLK_SEL	R/W	0h	OBSPI1 Loopback clock source 0h - OSPI_DQS external pin (external) 1h - OSPI_LBCLKO output (internal)
3-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	OSPI1 reference clock selection 0h - MCU_PLL1_HSDIV4_CLKOUT 1h - MCU_PLL2_HSDIV4_CLKOUT

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3.72 CTRLMMR_MCU_ADC0_CLKSEL Register (Proxy0 Offset = 8040h; Proxy1 Offset = A040h) [reset = 0h]

CTRLMMR_MCU_ADC0_CLKSEL is shown in Figure 3-72 and described in Table 3-146.

Return to Summary Table.

Controls the functional clock source for the MCU_ADC0.

Table 3-145. CTRLMMR_MCU_ADC0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8040h	40F0 A040h

Figure 3-72. CTRLMMR_MCU_ADC0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-146. CTRLMMR_MCU_ADC0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	Selects the sampling clock source for ADC0 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_PLL1_HSDIV1_CLKOUT1 2h - MCU_PLL0_HSDIV1_CLKOUT1 3h - MCU_EXT_REFCLK0

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3.73 CTRLMMR_MCU_ADC1_CLKSEL Register (Proxy0 Offset = 8044h; Proxy1 Offset = A044h) [reset = 0h]

CTRLMMR_MCU_ADC1_CLKSEL is shown in Figure 3-73 and described in Table 3-148.

Return to Summary Table.

Controls the functional clock source for the MCU_ADC1.

Table 3-147. CTRLMMR_MCU_ADC1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8044h	40F0 A044h

Figure 3-73. CTRLMMR_MCU_ADC1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-148. CTRLMMR_MCU_ADC1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	Selects the sampling clock source for ADC1 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_PLL1_HSDIV1_CLKOUT1 2h - MCU_PLL0_HSDIV1_CLKOUT1 3h - MCU_EXT_REFCLK0

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3.74 CTRLMMR_MCU_ENET_CLKSEL Register (Proxy0 Offset = 8050h; Proxy1 Offset = A050h) [reset = F00h]

CTRLMMR_MCU_ENET_CLKSEL is shown in Figure 3-74 and described in Table 3-150.

Return to Summary Table.

Controls selectable clock sources for the MCU Ethernet Port1.

Table 3-149. CTRLMMR_MCU_ENET_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8050h	40F0 A050h

Figure 3-74. CTRLMMR_MCU_ENET_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				CPTS_CLKSEL			
R-0h				R/W-Fh			
7	6	5	4	3	2	1	0
RESERVED							RMII_CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-150. CTRLMMR_MCU_ENET_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	CPTS_CLKSEL	R/W	Fh	Selects the clock source for the CPSW2x Ethernet switch Common Platform Time Stamp module 0h - MAIN_PLL3_HSDIV1_CLKOUT 1h - MAIN_PLL0_HSDIV6_CLKOUT 2h - MCU_CPTS_REF_CLK (pin) 3h - CPTS_RFT_CLK (pin) 4h - MCU_EXT_REFCLK0 (pin) 5h - EXT_REFCLK1 (pin) 6h - SERDES0_IP2_LN0_TXMCLK 7h - SERDES0_IP2_LN1_TXMCLK 8h - SERDES1_IP2_LN0_TXMCLK 9h - SERDES1_IP2_LN1_TXMCLK Ah - SERDES2_IP2_LN0_TXMCLK Bh - SERDES2_IP2_LN1_TXMCLK Ch - SERDES3_IP2_LN0_TXMCLK Dh - SERDES3_IP2_LN1_TXMCLK Eh - MCU_PLL2_HSDIV1_CLKOUT Fh - MCU_PLL2_HSDIV1_CLKOUT
7-1	RESERVED	R	0h	Reserved

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Table 3-150. CTRLMMR_MCU_ENET_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RMII_CLK_SEL	R/W	0h	Selects the rmii clock (rmii_mhz_50_clk) source. This defaults to the internal 50 MHz clock source for proper clockstop operation 0h - MCU_PLL2_HSDIV0_CLKOUT / 5 1h - MCU_RMII_REFCLK (pin)

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3.75 CTRLMMR_MCU_R5_CORE0_CLKSEL Register (Proxy0 Offset = 8080h; Proxy1 Offset = A080h) [reset = 0h]

CTRLMMR_MCU_R5_CORE0_CLKSEL is shown in Figure 3-75 and described in Table 3-152.

Return to Summary Table.

MCU Core 0 functional clock selection control.

Table 3-151. CTRLMMR_MCU_R5_CORE0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8080h	40F0 A080h

Figure 3-75. CTRLMMR_MCU_R5_CORE0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-152. CTRLMMR_MCU_R5_CORE0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the Core 0 functional clock and mcu/interface clock ratio 0h - Use MCU_SYSCLK0. MCU/interface is 3:1 clock ratio 1h - Use MCU_SYSCLK0/3. MCU/interface is 1:1 clock ratio

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3.76 CTRLMMR_MCU_TIMER0_CLKSEL Register (Proxy0 Offset = 8100h; Proxy1 Offset = A100h) [reset = 0h]

CTRLMMR_MCU_TIMER0_CLKSEL is shown in Figure 3-76 and described in Table 3-154.

Return to Summary Table.

MCU Timer0 functional clock selection control.

Table 3-153. CTRLMMR_MCU_TIMER0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8100h	40F0 A100h

Figure 3-76. CTRLMMR_MCU_TIMER0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-154. CTRLMMR_MCU_TIMER0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 4 2h - CLK_12M_RC 3h - MCU_PLL2_HSDIV2_CLKOUT 4h - MCU_EXT_REFCLK0 5h - LPXOSC_CLKOUT 6h - CPSW_GENF0 7h - CLK_32K

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3.77 CTRLMMR_MCU_TIMER1_CLKSEL Register (Proxy0 Offset = 8104h; Proxy1 Offset = A104h) [reset = 0h]

CTRLMMR_MCU_TIMER1_CLKSEL is shown in Figure 3-77 and described in Table 3-156.

Return to Summary Table.

MCU Timer1 functional clock selection control.

Table 3-155. CTRLMMR_MCU_TIMER1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8104h	40F0 A104h

Figure 3-77. CTRLMMR_MCU_TIMER1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-156. CTRLMMR_MCU_TIMER1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 4 2h - CLK_12M_RC 3h - MCU_PLL2_HSDIV2_CLKOUT 4h - MCU_EXT_REFCLK0 5h - LPXOSC_CLKOUT 6h - CPSW_GENF0 7h - CLK_32K

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3.78 CTRLMMR_MCU_TIMER2_CLKSEL Register (Proxy0 Offset = 8108h; Proxy1 Offset = A108h) [reset = 0h]

CTRLMMR_MCU_TIMER2_CLKSEL is shown in Figure 3-78 and described in Table 3-158.

Return to Summary Table.

MCU Timer2 functional clock selection control.

Table 3-157. CTRLMMR_MCU_TIMER2_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8108h	40F0 A108h

Figure 3-78. CTRLMMR_MCU_TIMER2_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-158. CTRLMMR_MCU_TIMER2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 4 2h - CLK_12M_RC 3h - MCU_PLL2_HSDIV2_CLKOUT 4h - MCU_EXT_REFCLK0 5h - LPXOSC_CLKOUT 6h - CPSW_GENF0 7h - CLK_32K

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3.79 CTRLMMR_MCU_TIMER3_CLKSEL Register (Proxy0 Offset = 810Ch; Proxy1 Offset = A10Ch) [reset = 0h]

CTRLMMR_MCU_TIMER3_CLKSEL is shown in Figure 3-79 and described in Table 3-160.

Return to Summary Table.

MCU Timer3 functional clock selection control.

Table 3-159. CTRLMMR_MCU_TIMER3_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 810Ch	40F0 A10Ch

Figure 3-79. CTRLMMR_MCU_TIMER3_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-160. CTRLMMR_MCU_TIMER3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 4 2h - CLK_12M_RC 3h - MCU_PLL2_HSDIV2_CLKOUT 4h - MCU_EXT_REFCLK0 5h - LPXOSC_CLKOUT 6h - CPSW_GENF0 7h - CLK_32K

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3.80 CTRLMMR_MCU_TIMER4_CLKSEL Register (Proxy0 Offset = 8110h; Proxy1 Offset = A110h) [reset = 0h]

CTRLMMR_MCU_TIMER4_CLKSEL is shown in Figure 3-80 and described in Table 3-162.

Return to Summary Table.

MCU Timer4 functional clock selection control.

Table 3-161. CTRLMMR_MCU_TIMER4_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8110h	40F0 A110h

Figure 3-80. CTRLMMR_MCU_TIMER4_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-162. CTRLMMR_MCU_TIMER4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 4 2h - CLK_12M_RC 3h - MCU_PLL2_HSDIV2_CLKOUT 4h - MCU_EXT_REFCLK0 5h - LPXOSC_CLKOUT 6h - CPSW_GENF0 7h - CLK_32K

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3.81 CTRLMMR_MCU_TIMER5_CLKSEL Register (Proxy0 Offset = 8114h; Proxy1 Offset = A114h) [reset = 0h]

CTRLMMR_MCU_TIMER5_CLKSEL is shown in Figure 3-81 and described in Table 3-164.

Return to Summary Table.

MCU Timer5 functional clock selection control.

Table 3-163. CTRLMMR_MCU_TIMER5_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8114h	40F0 A114h

Figure 3-81. CTRLMMR_MCU_TIMER5_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-164. CTRLMMR_MCU_TIMER5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 4 2h - CLK_12M_RC 3h - MCU_PLL2_HSDIV2_CLKOUT 4h - MCU_EXT_REFCLK0 5h - LPXOSC_CLKOUT 6h - CPSW_GENF0 7h - CLK_32K

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3.82 CTRLMMR_MCU_TIMER6_CLKSEL Register (Proxy0 Offset = 8118h; Proxy1 Offset = A118h) [reset = 0h]

CTRLMMR_MCU_TIMER6_CLKSEL is shown in Figure 3-82 and described in Table 3-166.

Return to Summary Table.

MCU Timer6 functional clock selection control.

Table 3-165. CTRLMMR_MCU_TIMER6_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8118h	40F0 A118h

Figure 3-82. CTRLMMR_MCU_TIMER6_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-166. CTRLMMR_MCU_TIMER6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 4 2h - CLK_12M_RC 3h - MCU_PLL2_HSDIV2_CLKOUT 4h - MCU_EXT_REFCLK0 5h - LPXOSC_CLKOUT 6h - CPSW_GENF0 7h - CLK_32K

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3.83 CTRLMMR_MCU_TIMER7_CLKSEL Register (Proxy0 Offset = 811Ch; Proxy1 Offset = A11Ch) [reset = 0h]

CTRLMMR_MCU_TIMER7_CLKSEL is shown in Figure 3-83 and described in Table 3-168.

Return to Summary Table.

MCU Timer7 functional clock selection control.

Table 3-167. CTRLMMR_MCU_TIMER7_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 811Ch	40F0 A11Ch

Figure 3-83. CTRLMMR_MCU_TIMER7_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-168. CTRLMMR_MCU_TIMER7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 4 2h - CLK_12M_RC 3h - MCU_PLL2_HSDIV2_CLKOUT 4h - MCU_EXT_REFCLK0 5h - LPXOSC_CLKOUT 6h - CPSW_GENF0 7h - CLK_32K

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3.84 CTRLMMR_MCU_TIMER8_CLKSEL Register (Proxy0 Offset = 8120h; Proxy1 Offset = A120h) [reset = 0h]

CTRLMMR_MCU_TIMER8_CLKSEL is shown in Figure 3-84 and described in Table 3-170.

Return to Summary Table.

MCU Timer8 functional clock selection control.

Table 3-169. CTRLMMR_MCU_TIMER8_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8120h	40F0 A120h

Figure 3-84. CTRLMMR_MCU_TIMER8_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-170. CTRLMMR_MCU_TIMER8_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 4 2h - CLK_12M_RC 3h - MCU_PLL2_HSDIV2_CLKOUT 4h - MCU_EXT_REFCLK0 5h - LPXOSC_CLKOUT 6h - CPSW_GENF0 7h - CLK_32K

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3.85 CTRLMMR_MCU_TIMER9_CLKSEL Register (Proxy0 Offset = 8124h; Proxy1 Offset = A124h) [reset = 0h]

CTRLMMR_MCU_TIMER9_CLKSEL is shown in Figure 3-85 and described in Table 3-172.

Return to Summary Table.

MCU Timer9 functional clock selection control.

Table 3-171. CTRLMMR_MCU_TIMER9_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8124h	40F0 A124h

Figure 3-85. CTRLMMR_MCU_TIMER9_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-172. CTRLMMR_MCU_TIMER9_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - MCU_SYSCLK0 / 4 2h - CLK_12M_RC 3h - MCU_PLL2_HSDIV2_CLKOUT 4h - MCU_EXT_REFCLK0 5h - LPXOSC_CLKOUT 6h - CPSW_GENF0 7h - CLK_32K

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3.86 CTRLMMR_MCU_RTI0_CLKSEL Register (Proxy0 Offset = 8180h; Proxy1 Offset = A180h) [reset = 0h]

CTRLMMR_MCU_RTI0_CLKSEL is shown in Figure 3-86 and described in Table 3-174.

Return to Summary Table.

MCU RTI0 functional clock selection control.

Table 3-173. CTRLMMR_MCU_RTI0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8180h	40F0 A180h

Figure 3-86. CTRLMMR_MCU_RTI0_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-174. CTRLMMR_MCU_RTI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks further writes to CTRLMMR_MCU_RTI0_CLKSEL until the next module reset
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	RTI functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K

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3.87 CTRLMMR_MCU_RTI1_CLKSEL Register (Proxy0 Offset = 8184h; Proxy1 Offset = A184h) [reset = 0h]

CTRLMMR_MCU_RTI1_CLKSEL is shown in Figure 3-87 and described in Table 3-176.

Return to Summary Table.

MCU RTI1 functional clock selection control.

Table 3-175. CTRLMMR_MCU_RTI1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 8184h	40F0 A184h

Figure 3-87. CTRLMMR_MCU_RTI1_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-176. CTRLMMR_MCU_RTI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks further writes to CTRLMMR_MCU_RTI1_CLKSEL until the next module reset
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	RTI functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K

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3.88 CTRLMMR_MCU_USART_CLKSEL Register (Proxy0 Offset = 81C0h; Proxy1 Offset = A1C0h) [reset = 0h]

CTRLMMR_MCU_USART_CLKSEL is shown in Figure 3-88 and described in Table 3-178.

Return to Summary Table.

Controls the functional clock source for MCU_USART0.

Table 3-177. CTRLMMR_MCU_USART_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 81C0h	40F0 A1C0h

Figure 3-88. CTRLMMR_MCU_USART_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-178. CTRLMMR_MCU_USART_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	MCU_USART0 FCLK selection 0h - MCU_PLL1_HSDIV3_CLKOUT 1h - MAIN_PLL1_HSDIV5_CLKOUT

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3.89 CTRLMMR_MCU_LOCK2_KICK0 Register (Proxy0 Offset = 9008h; Proxy1 Offset = B008h) [reset = 0h]

CTRLMMR_MCU_LOCK2_KICK0 is shown in Figure 3-89 and described in Table 3-180.

Return to Summary Table.

Lower 32-bits of Partition2 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_MCU_LOCK2_KICK1 with its key value before write-protected Partition 2 registers can be written.

Table 3-179. CTRLMMR_MCU_LOCK2_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 9008h	40F0 B008h

Figure 3-89. CTRLMMR_MCU_LOCK2_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-180. CTRLMMR_MCU_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition2 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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3.90 CTRLMMR_MCU_LOCK2_KICK1 Register (Proxy0 Offset = 900Ch; Proxy1 Offset = B00Ch) [reset = 0h]

CTRLMMR_MCU_LOCK2_KICK1 is shown in Figure 3-90 and described in Table 3-182.

Return to Summary Table.

Upper 32-bits of Partition 2 write lock key. This register must be written with the designated key value after a write to CTRLMMR_MCU_LOCK2_KICK0 with its key value before write-protected Partition 2 registers can be written.

Table 3-181. CTRLMMR_MCU_LOCK2_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 900Ch	40F0 B00Ch

Figure 3-90. CTRLMMR_MCU_LOCK2_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-182. CTRLMMR_MCU_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition2 registers

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3.91 CTRLMMR_MCU_P2_CLAIM0 Register (Proxy0 Offset = 9100h; Proxy1 Offset = B100h) [reset = 0h]

CTRLMMR_MCU_P2_CLAIM0 is shown in Figure 3-91 and described in Table 3-184.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 3-183. CTRLMMR_MCU_P2_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 9100h	40F0 B100h

Figure 3-91. CTRLMMR_MCU_P2_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-184. CTRLMMR_MCU_P2_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 8000h + (0 x 80h) + (b x 4h) and register Proxy1 address of: A000h + (0 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.92 CTRLMMR_MCU_P2_CLAIM1 Register (Proxy0 Offset = 9104h; Proxy1 Offset = B104h) [reset = 0h]

CTRLMMR_MCU_P2_CLAIM1 is shown in Figure 3-92 and described in Table 3-186.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 3-185. CTRLMMR_MCU_P2_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 9104h	40F0 B104h

Figure 3-92. CTRLMMR_MCU_P2_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-186. CTRLMMR_MCU_P2_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 8000h + (1 x 80h) + (b x 4h) and register Proxy1 address of: A000h + (1 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.93 CTRLMMR_MCU_P2_CLAIM2 Register (Proxy0 Offset = 9108h; Proxy1 Offset = B108h) [reset = 0h]

CTRLMMR_MCU_P2_CLAIM2 is shown in Figure 3-93 and described in Table 3-188.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 3-187. CTRLMMR_MCU_P2_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 9108h	40F0 B108h

Figure 3-93. CTRLMMR_MCU_P2_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-188. CTRLMMR_MCU_P2_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 8000h + (2 x 80h) + (b x 4h) and register Proxy1 address of: A000h + (2 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.94 CTRLMMR_MCU_P2_CLAIM3 Register (Proxy0 Offset = 910Ch; Proxy1 Offset = B10Ch) [reset = 0h]

CTRLMMR_MCU_P2_CLAIM3 is shown in Figure 3-94 and described in Table 3-190.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 3-189. CTRLMMR_MCU_P2_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 910Ch	40F0 B10Ch

Figure 3-94. CTRLMMR_MCU_P2_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-190. CTRLMMR_MCU_P2_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 8000h + (3 x 80h) + (b x 4h) and register Proxy1 address of: A000h + (3 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.95 CTRLMMR_MCU_LBIST_CTRL Register (Proxy0 Offset = C000h; Proxy1 Offset = E000h) [reset = X]

CTRLMMR_MCU_LBIST_CTRL is shown in Figure 3-95 and described in Table 3-192.

Return to Summary Table.

Configures and enables LBIST operation.

Table 3-191. CTRLMMR_MCU_LBIST_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 C000h	40F0 E000h

Figure 3-95. CTRLMMR_MCU_LBIST_CTRL Register

31	30	29	28	27	26	25	24
BIST_RESET	RESERVED			BIST_RUN			
R/W-X	R-0h			R/W-X			

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RUNBIST_MODE				RESERVED		DC_DEF	
R/W-X				R-0h		R/W-X	

7	6	5	4	3	2	1	0
LOAD_DIV	RESERVED		DIVIDE_RATIO				
R/W-X	R-0h		R/W-X				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-192. CTRLMMR_MCU_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_RESET	R/W	X	Reset LBIST macro
30-28	RESERVED	R	0h	Reserved
27-24	BIST_RUN	R/W	X	Starts LBIST if all bits are 1
23-16	RESERVED	R	0h	Reserved
15-12	RUNBIST_MODE	R/W	X	Runbist mode enable if all bits are 1
11-10	RESERVED	R	0h	Reserved
9-8	DC_DEF	R/W	X	Clock delay after scan_enable switching
7	LOAD_DIV	R/W	X	Loads LBIST clock divide ratio on transition from 0 to 1
6-5	RESERVED	R	0h	Reserved
4-0	DIVIDE_RATIO	R/W	X	LBIST clock divide ratio

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3.96 CTRLMMR_MCU_LBIST_PATCOUNT Register (Proxy0 Offset = C004h; Proxy1 Offset = E004h) [reset = X]

CTRLMMR_MCU_LBIST_PATCOUNT is shown in Figure 3-96 and described in Table 3-194.

Return to Summary Table.

Specifies the number of LBIST patterns to run.

Table 3-193. CTRLMMR_MCU_LBIST_PATCOUNT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 C004h	40F0 E004h

Figure 3-96. CTRLMMR_MCU_LBIST_PATCOUNT Register

31	30	29	28	27	26	25	24
RESERVED		STATIC_PC_DEF					
R-0h		R/W-X					
23	22	21	20	19	18	17	16
STATIC_PC_DEF							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				SET_PC_DEF			
R-0h				R/W-X			
7	6	5	4	3	2	1	0
RESET_PC_DEF				SCAN_PC_DEF			
R/W-X				R/W-X			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-194. CTRLMMR_MCU_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	STATIC_PC_DEF	R/W	X	Number of stuck-at patterns to run
15-12	RESERVED	R	0h	Reserved
11-8	SET_PC_DEF	R/W	X	Number of set patterns to run
7-4	RESET_PC_DEF	R/W	X	Number of reset patterns to run
3-0	SCAN_PC_DEF	R/W	X	Number of chain test patterns to run

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3.97 CTRLMMR_MCU_LBIST_SEED0 Register (Proxy0 Offset = C008h; Proxy1 Offset = E008h) [reset = X]

CTRLMMR_MCU_LBIST_SEED0 is shown in Figure 3-97 and described in Table 3-196.

Return to Summary Table.

Specifies the 32 LSBs of the PRPG seed.

Table 3-195. CTRLMMR_MCU_LBIST_SEED0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 C008h	40F0 E008h

Figure 3-97. CTRLMMR_MCU_LBIST_SEED0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRPG_DEF																															
R/W-X																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-196. CTRLMMR_MCU_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRPG_DEF	R/W	X	Initial seed for PRPG (bits 31:0)

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3.98 CTRLMMR_MCU_LBIST_SEED1 Register (Proxy0 Offset = C00Ch; Proxy1 Offset = E00Ch) [reset = X]

CTRLMMR_MCU_LBIST_SEED1 is shown in Figure 3-98 and described in Table 3-198.

Return to Summary Table.

Specifies the 21 MSBs of the PRPG seed.

Table 3-197. CTRLMMR_MCU_LBIST_SEED1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 C00Ch	40F0 E00Ch

Figure 3-98. CTRLMMR_MCU_LBIST_SEED1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRPG_DEF																				
R-0h											R/W-X																				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-198. CTRLMMR_MCU_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	PRPG_DEF	R/W	X	Initial seed for PRPG (bits 52:32)

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3.99 CTRLMMR_MCU_LBIST_SPARE0 Register (Proxy0 Offset = C010h; Proxy1 Offset = E010h) [reset = 0h]

CTRLMMR_MCU_LBIST_SPARE0 is shown in Figure 3-99 and described in Table 3-200.

Return to Summary Table.

Spare LBIST control bits.

Table 3-199. CTRLMMR_MCU_LBIST_SPARE0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 C010h	40F0 E010h

Figure 3-99. CTRLMMR_MCU_LBIST_SPARE0 Register

31	30	29	28	27	26	25	24
SPARE0							
R/W-0h							
23	22	21	20	19	18	17	16
SPARE0							
R/W-0h							
15	14	13	12	11	10	9	8
SPARE0							
R/W-0h							
7	6	5	4	3	2	1	0
SPARE0						PBIST_SELFTEST_EN	LBIST_SELFTEST_EN
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 3-200. CTRLMMR_MCU_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	SPARE0	R/W	0h	LBIST spare bits
1	PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control
0	LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control

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3.100 CTRLMMR_MCU_LBIST_SPARE1 Register (Proxy0 Offset = C014h; Proxy1 Offset = E014h) [reset = 0h]

CTRLMMR_MCU_LBIST_SPARE1 is shown in Figure 3-100 and described in Table 3-202.

Return to Summary Table.

Spare LBIST control bits.

Table 3-201. CTRLMMR_MCU_LBIST_SPARE1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 C014h	40F0 E014h

Figure 3-100. CTRLMMR_MCU_LBIST_SPARE1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 3-202. CTRLMMR_MCU_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE1	R/W	0h	LBIST spare bits

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3.101 CTRLMMR_MCU_LBIST_STAT Register (Proxy0 Offset = C018h; Proxy1 Offset = E018h) [reset = X]

CTRLMMR_MCU_LBIST_STAT is shown in Figure 3-101 and described in Table 3-204.

Return to Summary Table.

Indicates LBIST status and provides MISR selection control.

Table 3-203. CTRLMMR_MCU_LBIST_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 C018h	40F0 E018h

Figure 3-101. CTRLMMR_MCU_LBIST_STAT Register

31	30	29	28	27	26	25	24
BIST_DONE	RESERVED						
R-X	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
BIST_RUNNING	RESERVED					OUT_MUX_CTL	
R-X	R-0h					R/W-0h	

7	6	5	4	3	2	1	0
MISR_MUX_CTL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-204. CTRLMMR_MCU_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_DONE	R	X	LBIST is done
30-16	RESERVED	R	0h	Reserved
15	BIST_RUNNING	R	X	LBIST is running
14-10	RESERVED	R	0h	Reserved
9-8	OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 0h - LBIST IP CTRLMMR_MCU_PID value 1h - LBIST CTRL ID value 2h or 3h - MISR value
7-0	MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR.

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3.102 CTRLMMR_MCU_LBIST_MISR Register (Proxy0 Offset = C01Ch; Proxy1 Offset = E01Ch) [reset = X]

CTRLMMR_MCU_LBIST_MISR is shown in Figure 3-102 and described in Table 3-206.

Return to Summary Table.

Contains LBIST MISR output value.

Table 3-205. CTRLMMR_MCU_LBIST_MISR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 C01Ch	40F0 E01Ch

Figure 3-102. CTRLMMR_MCU_LBIST_MISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_RESULT																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 3-206. CTRLMMR_MCU_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl

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3.103 CTRLMMR_MCU_LBIST_SIG Register (Proxy0 Offset = C280h; Proxy1 Offset = E280h) [reset = X]

CTRLMMR_MCU_LBIST_SIG is shown in Figure 3-103 and described in Table 3-208.

Return to Summary Table.

Contains expected MISR output value.

Table 3-207. CTRLMMR_MCU_LBIST_SIG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 C280h	40F0 E280h

Figure 3-103. CTRLMMR_MCU_LBIST_SIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_SIG																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 3-208. CTRLMMR_MCU_LBIST_SIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_SIG	R	X	MISR signature

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3.104 CTRLMMR_MCU_LOCK3_KICK0 Register (Proxy0 Offset = D008h; Proxy1 Offset = F008h) [reset = 0h]

CTRLMMR_MCU_LOCK3_KICK0 is shown in Figure 3-104 and described in Table 3-210.

Return to Summary Table.

Lower 32-bits of Partition3 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_MCU_LOCK3_KICK1 with its key value before write-protected Partition 3 registers can be written.

Table 3-209. CTRLMMR_MCU_LOCK3_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 D008h	40F0 F008h

Figure 3-104. CTRLMMR_MCU_LOCK3_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
KEY							
R/W-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
KEY							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 3-210. CTRLMMR_MCU_LOCK3_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition3 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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3.105 CTRLMMR_MCU_LOCK3_KICK1 Register (Proxy0 Offset = D00Ch; Proxy1 Offset = F00Ch) [reset = 0h]

CTRLMMR_MCU_LOCK3_KICK1 is shown in Figure 3-105 and described in Table 3-212.

Return to Summary Table.

Upper 32-bits of Partition 3 write lock key. This register must be written with the designated key value after a write to CTRLMMR_MCU_LOCK3_KICK0 with its key value before write-protected Partition 3 registers can be written.

Table 3-211. CTRLMMR_MCU_LOCK3_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 D00Ch	40F0 F00Ch

Figure 3-105. CTRLMMR_MCU_LOCK3_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-212. CTRLMMR_MCU_LOCK3_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition3 registers

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3.106 CTRLMMR_MCU_P3_CLAIM0 Register (Proxy0 Offset = D100h; Proxy1 Offset = F100h) [reset = 0h]

CTRLMMR_MCU_P3_CLAIM0 is shown in Figure 3-106 and described in Table 3-214.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 3-213. CTRLMMR_MCU_P3_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 D100h	40F0 F100h

Figure 3-106. CTRLMMR_MCU_P3_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-214. CTRLMMR_MCU_P3_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (0 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (0 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.107 CTRLMMR_MCU_P3_CLAIM1 Register (Proxy0 Offset = D104h; Proxy1 Offset = F104h) [reset = 0h]

CTRLMMR_MCU_P3_CLAIM1 is shown in Figure 3-107 and described in Table 3-216.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 3-215. CTRLMMR_MCU_P3_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 D104h	40F0 F104h

Figure 3-107. CTRLMMR_MCU_P3_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-216. CTRLMMR_MCU_P3_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (1 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (1 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.108 CTRLMMR_MCU_P3_CLAIM2 Register (Proxy0 Offset = D108h; Proxy1 Offset = F108h) [reset = 0h]

CTRLMMR_MCU_P3_CLAIM2 is shown in Figure 3-108 and described in Table 3-218.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 3-217. CTRLMMR_MCU_P3_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 D108h	40F0 F108h

Figure 3-108. CTRLMMR_MCU_P3_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-218. CTRLMMR_MCU_P3_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (2 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (2 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.109 CTRLMMR_MCU_P3_CLAIM3 Register (Proxy0 Offset = D10Ch; Proxy1 Offset = F10Ch) [reset = 0h]

CTRLMMR_MCU_P3_CLAIM3 is shown in Figure 3-109 and described in Table 3-220.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 3-219. CTRLMMR_MCU_P3_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 D10Ch	40F0 F10Ch

Figure 3-109. CTRLMMR_MCU_P3_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-220. CTRLMMR_MCU_P3_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (3 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (3 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.110 CTRLMMR_MCU_P3_CLAIM4 Register (Proxy0 Offset = D110h; Proxy1 Offset = F110h) [reset = 0h]

CTRLMMR_MCU_P3_CLAIM4 is shown in Figure 3-110 and described in Table 3-222.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 3-221. CTRLMMR_MCU_P3_CLAIM4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 D110h	40F0 F110h

Figure 3-110. CTRLMMR_MCU_P3_CLAIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-222. CTRLMMR_MCU_P3_CLAIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (4 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (4 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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3.111 CTRLMMR_MCU_P3_CLAIM5 Register (Proxy0 Offset = D114h; Proxy1 Offset = F114h) [reset = 0h]

CTRLMMR_MCU_P3_CLAIM5 is shown in Figure 3-111 and described in Table 3-224.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 3-223. CTRLMMR_MCU_P3_CLAIM5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
MCU_CTRL_MMR0	40F0 D114h	40F0 F114h

Figure 3-111. CTRLMMR_MCU_P3_CLAIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 3-224. CTRLMMR_MCU_P3_CLAIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: C000h + (5 x 80h) + (b x 4h) and register Proxy1 address of: E000h + (5 x 80h) + (b x 4h) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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4 MCU_SEC_MMR0_CFG0 Registers

Table 4-2 lists the memory-mapped registers for the MCU_SEC_MMR0_CFG0. All register offset addresses not listed in Table 4-2 should be considered as reserved locations and the register contents should not be modified.

Table 4-1. MCU_SEC_MMR0_CFG0 Instances

Instance	Base Address
MCU_SEC_MMR0_CFG0	45A5 0000h

Table 4-2. MCU_SEC_MMR0_CFG0 Registers

Offset	Acronym	Register Name	MCU_SEC_MMR0_CFG0 Physical Address
20h	CTRLMMR_MCUSEC_CLSTR0_DEF	Cluster0 Definition Register	45A5 0020h
40h	CTRLMMR_MCUSEC_CLSTR0_CFG	Cluster0 Configuration Register	45A5 0040h
100h	CTRLMMR_MCUSEC_CLSTR0_CORE0_CFG	Cluster0 Core0 Configuration Register	45A5 0100h
110h	CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_LO	Cluster0 Core0 Boot Vector Lo Register	45A5 0110h
114h	CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_HI	Cluster0 Core0 Boot Vector Hi Register	45A5 0114h
120h	CTRLMMR_MCUSEC_CLSTR0_CORE0_PMCTRL	Cluster0 Core0 Power Management Control	45A5 0120h
130h	CTRLMMR_MCUSEC_CLSTR0_CORE0_PMSTAT	Cluster0 Core0 Power Management Status Register	45A5 0130h
180h	CTRLMMR_MCUSEC_CLSTR0_CORE1_CFG	Cluster0 Core1 Configuration Register 0	45A5 0180h
190h	CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_LO	Cluster0 Core1 Boot Vector Lo Register	45A5 0190h
194h	CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_HI	Cluster0 Core1 Boot Vector Hi Register	45A5 0194h
1A0h	CTRLMMR_MCUSEC_CLSTR0_CORE1_PMCTRL	Cluster0 Core1 Power Management Control	45A5 01A0h
1B0h	CTRLMMR_MCUSEC_CLSTR0_CORE1_PMSTAT	Cluster0 Core1 Power Management Status Register	45A5 01B0h

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4.1 CTRLMMR_MCUSEC_CLSTR0_DEF Register (Offset = 20h) [reset = 2FF10h]

CTRLMMR_MCUSEC_CLSTR0_DEF is shown in Figure 4-1 and described in Table 4-4.

Return to Summary Table.

Defines the type of the processor cluster.

Table 4-3. CTRLMMR_MCUSEC_CLSTR0_DEF Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 0020h

Figure 4-1. CTRLMMR_MCUSEC_CLSTR0_DEF Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED					CORE_NUM		
R-0h					R-2h		
15	14	13	12	11	10	9	8
DSP_CORE_TYPE							
R-FFh							
7	6	5	4	3	2	1	0
ARM_CORE_TYPE							
R-10h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-4. CTRLMMR_MCUSEC_CLSTR0_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	CORE_NUM	R	2h	Number of cores in cluster 0h - Single Core 1h - Dual Core 2h - Quad Core
15-8	DSP_CORE_TYPE	R	FFh	DSP core type configuration. Not shown values are reserved. 0h - C7x 1h - C6x FFh - Not DSP
7-0	ARM_CORE_TYPE	R	10h	ARM core type configuration. Not shown values are reserved. 0h - A53 1h - A57 10h - R5 FFh - Not ARM

Table 4-5. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_DEF

MCU_SEC_MMR0_CFG0 Registers

- CTRLMMR_MCUSEC_CLSTR0_DEF Register (Offset = 20h) [reset = 2FF10h]: [0]
- MCU_SEC_MMR0_CFG0 Registers: [0]

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4.2 CTRLMMR_MCUSEC_CLSTR0_CFG Register (Offset = 40h) [reset = X]

CTRLMMR_MCUSEC_CLSTR0_CFG is shown in Figure 4-2 and described in Table 4-7.

Return to Summary Table.

Configures cluster level characteristics.

Table 4-6. CTRLMMR_MCUSEC_CLSTR0_CFG Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 0040h

Figure 4-2. CTRLMMR_MCUSEC_CLSTR0_CFG Register

31	30	29	28	27	26	25	24
CLSTR_CFG_RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
CLSTR_CFG_RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
CLSTR_CFG_RSVD							
R/W-0h							
7	6	5	4	3	2	1	0
CLSTR_CFG_RSVD				LOCKSTEP_EN	DBG_NO_CLKSTOP	TEINIT	LOCKSTEP
R/W-0h				R-X	R/W-0h	R/W-0h	R/W-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-7. CTRLMMR_MCUSEC_CLSTR0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	CLSTR_CFG_RSVD	R/W	0h	Reserved for future use. Write '0' to ensure compatibility with future devices.
3	LOCKSTEP_EN	R	X	Lockstep enable. Indicates if R5 lockstep operation is supported on the device
2	DBG_NO_CLKSTOP	R/W	0h	CPU clockstop behavior 0h - CPU clocks stopped and nCLOCKSTOPPED asserted in standby mode 1h - CPU clocks not stopped in standby mode
1	TEINIT	R/W	0h	Exception handling state at reset: 0h - ARM mode 1h - Thumb mode
0	LOCKSTEP	R/W	X	When set, Core0 and Core1 operate in lockstep mode. Can only be changed if lockstep operation is supported as indicated by CLSTR0_CFG_lockstep_en = 1. If CLSTR0_CFG_lockstep_en = 0, lockstep is not supported, this bit will be read only with a value of 0.

Table 4-8. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CFG

MCU_SEC_MMR0_CFG0 Registers

- MCU_SEC_MMR0_CFG0 Registers: [0]
- CTRLMMR_MCUSEC_CLSTR0_CFG Register (Offset = 40h) [reset = X]: [0]

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4.3 CTRLMMR_MCUSEC_CLSTR0_CORE0_CFG Register (Offset = 100h) [reset = 880h]

CTRLMMR_MCUSEC_CLSTR0_CORE0_CFG is shown in Figure 4-3 and described in Table 4-10.

Return to Summary Table.

Configures the TCM and interrupt operation of R5 Core0.

Table 4-9. CTRLMMR_MCUSEC_CLSTR0_CORE0_CFG Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 0100h

Figure 4-3. CTRLMMR_MCUSEC_CLSTR0_CORE0_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
NMFI_EN	RESERVED			TCM_RSTBASE	RESERVED		
R/W-0h	R-0h			R/W-1h	R-0h		
7	6	5	4	3	2	1	0
BTCM_EN	RESERVED			ATCM_EN	RESERVED		
R/W-1h	R-0h			R/W-0h	R-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-10. CTRLMMR_MCUSEC_CLSTR0_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NMFI_EN	R/W	0h	Enable Core0 Non-Maskable Fast Interrupts
14-12	RESERVED	R	0h	Reserved
11	TCM_RSTBASE	R/W	1h	Core0 A/BTCM Reset Base Address Indicator 0h - BTCM located at address 0x0 1h - ATCM located at address 0x0
10-8	RESERVED	R	0h	Reserved
7	BTCM_EN	R/W	1h	Enable Core0 BTCM RAM at reset
6-4	RESERVED	R	0h	Reserved
3	ATCM_EN	R/W	0h	Enable Core0 ATCM RAM at reset
2-0	RESERVED	R	0h	Reserved

Table 4-11. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE0_CFG

MCU_SEC_MMR0_CFG0 Registers

- CTRLMMR_MCUSEC_CLSTR0_CORE0_CFG Register (Offset = 100h) [reset = 880h]: [0]
- MCU_SEC_MMR0_CFG0 Registers: [0]

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4.4 CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_LO Register (Offset = 110h) [reset = 41100000h]

CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_LO is shown in Figure 4-4 and described in Table 4-13.

Return to Summary Table.

Contains the lower 32 bits of the boot vector location for R5 Core0. Bits 6:0 are not used and are always 0.

Table 4-12. CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT _LO Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 0110h

Figure 4-4. CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VECT_ADDR																									RESERVED						
R/W-822000h																									R-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-13. CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	VECT_ADDR	R/W	822000h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0.
6-0	RESERVED	R	0h	Reserved

Table 4-14. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_LO

MCU_SEC_MMR0_CFG0 Registers

- MCU_SEC_MMR0_CFG0 Registers: [0]
- CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_LO Register (Offset = 110h) [reset = 41100000h]: [0]

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4.5 CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_HI Register (Offset = 114h) [reset = 0h]

CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_HI is shown in Figure 4-5 and described in Table 4-16.

Return to Summary Table.

Contains the lower 16 bits of the boot vector location for R5 Core0.

Table 4-15. CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_HI Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 0114h

Figure 4-5. CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VECT_ADDR															
R-0h																R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-16. CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32].

Table 4-17. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_HI

MCU_SEC_MMR0_CFG0 Registers

- MCU_SEC_MMR0_CFG0 Registers: [0]
- CTRLMMR_MCUSEC_CLSTR0_CORE0_BOOTVECT_HI Register (Offset = 114h) [reset = 0h]: [0]

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4.6 CTRLMMR_MCUSEC_CLSTR0_CORE0_PMCTRL Register (Offset = 120h) [reset = 0h]

CTRLMMR_MCUSEC_CLSTR0_CORE0_PMCTRL is shown in Figure 4-6 and described in Table 4-19.

Return to Summary Table.

Configures Cluster Core0 power state.

Table 4-18. CTRLMMR_MCUSEC_CLSTR0_CORE0_PMCTRL Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 0120h

Figure 4-6. CTRLMMR_MCUSEC_CLSTR0_CORE0_PMCTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CORE_HALT
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-19. CTRLMMR_MCUSEC_CLSTR0_CORE0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CORE_HALT	R/W	0h	Halt Core0. When 0, indicates that Core0 is in the Halt state.

Table 4-20. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE0_PMCTRL

MCU_SEC_MMR0_CFG0 Registers
- MCU_SEC_MMR0_CFG0 Registers: [0]
- CTRLMMR_MCUSEC_CLSTR0_CORE0_PMCTRL Register (Offset = 120h) [reset = 0h]: [0]

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4.7 CTRLMMR_MCUSEC_CLSTR0_CORE0_PMSTAT Register (Offset = 130h) [reset = X]

CTRLMMR_MCUSEC_CLSTR0_CORE0_PMSTAT is shown in Figure 4-7 and described in Table 4-22.

Return to Summary Table.

Shows Cluster Core0 power status.

Table 4-21. CTRLMMR_MCUSEC_CLSTR0_CORE0_PMSTAT Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 0130h

Figure 4-7. CTRLMMR_MCUSEC_CLSTR0_CORE0_PMSTAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CLK_GATE	RESERVED	WFE	WFI
R-0h				R-X	R-0h	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 4-22. CTRLMMR_MCUSEC_CLSTR0_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CLK_GATE	R	X	Core0 Clocked stopped due to WFI or WFE state
2	RESERVED	R	0h	Reserved
1	WFE	R	X	Core0 WFE When 0, indicates that Core0 is in the WFE state
0	WFI	R	X	Core0 WFI When 0, indicates that Core0 is in the WFI state

Table 4-23. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE0_PMSTAT

MCU_SEC_MMR0_CFG0 Registers

- MCU_SEC_MMR0_CFG0 Registers: [0]
- CTRLMMR_MCUSEC_CLSTR0_CORE0_PMSTAT Register (Offset = 130h) [reset = X]: [0]

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4.8 CTRLMMR_MCUSEC_CLSTR0_CORE1_CFG Register (Offset = 180h) [reset = 880h]

CTRLMMR_MCUSEC_CLSTR0_CORE1_CFG is shown in Figure 4-8 and described in Table 4-25.

Return to Summary Table.

Configures the TCM and interrupt operation of R5 Core1.

Table 4-24. CTRLMMR_MCUSEC_CLSTR0_CORE1_CFG Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 0180h

Figure 4-8. CTRLMMR_MCUSEC_CLSTR0_CORE1_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
NMFI_EN	RESERVED			TCM_RSTBASE	RESERVED		
R/W-0h	R-0h			R/W-1h	R-0h		
7	6	5	4	3	2	1	0
BTCM_EN	RESERVED			ATCM_EN	RESERVED		
R/W-1h	R-0h			R/W-0h	R-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-25. CTRLMMR_MCUSEC_CLSTR0_CORE1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NMFI_EN	R/W	0h	Enable Core1 Non-Maskable Fast Interrupts
14-12	RESERVED	R	0h	Reserved
11	TCM_RSTBASE	R/W	1h	Core1 A/BTCM Reset Base Address Indicator 0h - BTCM located at address 0x0 1h - ATCM located at address 0x0
10-8	RESERVED	R	0h	Reserved
7	BTCM_EN	R/W	1h	Enable Core1 BTCM RAM at reset
6-4	RESERVED	R	0h	Reserved
3	ATCM_EN	R/W	0h	Enable Core1 ATCM RAM at reset
2-0	RESERVED	R	0h	Reserved

Table 4-26. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE1_CFG

MCU_SEC_MMR0_CFG0 Registers
- MCU_SEC_MMR0_CFG0 Registers: [0]
- CTRLMMR_MCUSEC_CLSTR0_CORE1_CFG Register (Offset = 180h) [reset = 880h]: [0]

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4.9 CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_LO Register (Offset = 190h) [reset = 41100000h]

CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_LO is shown in Figure 4-9 and described in Table 4-28.

Return to Summary Table.

Contains the lower 32 bits of the boot vector location for R5 Core1. Bits 6:0 are not used and are always 0.

Table 4-27. CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT _LO Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 0190h

Figure 4-9. CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VECT_ADDR																									RESERVED						
R/W-822000h																									R-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-28. CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	VECT_ADDR	R/W	822000h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0.
6-0	RESERVED	R	0h	Reserved

Table 4-29. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_LO

MCU_SEC_MMR0_CFG0 Registers

- CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_LO Register (Offset = 190h) [reset = 41100000h]: [0]
- MCU_SEC_MMR0_CFG0 Registers: [0]

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4.10 CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_HI Register (Offset = 194h) [reset = 0h]

CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_HI is shown in Figure 4-10 and described in Table 4-31.

Return to Summary Table.

Contains the lower 16 bits of the boot vector location for R5 Core1.

Table 4-30. CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_HI Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 0194h

Figure 4-10. CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VECT_ADDR															
R-0h																R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-31. CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32].

Table 4-32. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_HI

MCU_SEC_MMR0_CFG0 Registers

- CTRLMMR_MCUSEC_CLSTR0_CORE1_BOOTVECT_HI Register (Offset = 194h) [reset = 0h]: [0]
- MCU_SEC_MMR0_CFG0 Registers: [0]

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4.11 CTRLMMR_MCUSEC_CLSTR0_CORE1_PMCTRL Register (Offset = 1A0h) [reset = 0h]

CTRLMMR_MCUSEC_CLSTR0_CORE1_PMCTRL is shown in Figure 4-11 and described in Table 4-34.

Return to Summary Table.

Configures Cluster Core1 power state.

Table 4-33. CTRLMMR_MCUSEC_CLSTR0_CORE1_PMCTRL Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 01A0h

Figure 4-11. CTRLMMR_MCUSEC_CLSTR0_CORE1_PMCTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CORE_HALT
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-34. CTRLMMR_MCUSEC_CLSTR0_CORE1_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CORE_HALT	R/W	0h	Halt Core1. When 0, indicates that Core1 is in the Halt state.

Table 4-35. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE1_PMCTRL

MCU_SEC_MMR0_CFG0 Registers

- CTRLMMR_MCUSEC_CLSTR0_CORE1_PMCTRL Register (Offset = 1A0h) [reset = 0h]: [0]
- MCU_SEC_MMR0_CFG0 Registers: [0]

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4.12 CTRLMMR_MCUSEC_CLSTR0_CORE1_PMSTAT Register (Offset = 1B0h) [reset = X]

CTRLMMR_MCUSEC_CLSTR0_CORE1_PMSTAT is shown in Figure 4-12 and described in Table 4-37.

Return to Summary Table.

Shows Cluster Core1 power status.

Table 4-36. CTRLMMR_MCUSEC_CLSTR0_CORE1_PMSTAT Instances

Instance	Physical Address
MCU_SEC_MMR0_CFG0	45A5 01B0h

Figure 4-12. CTRLMMR_MCUSEC_CLSTR0_CORE1_PMSTAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CLK_GATE	RESERVED	WFE	WFI
R-0h				R-X	R-0h	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 4-37. CTRLMMR_MCUSEC_CLSTR0_CORE1_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CLK_GATE	R	X	Core1 Clocked stopped due to WFI or WFE state
2	RESERVED	R	0h	Reserved
1	WFE	R	X	Core1 WFE When 0, indicates that Core1 is in the WFE state
0	WFI	R	X	Core1 WFI When 0, indicates that Core1 is in the WFI state

Table 4-38. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE1_PMSTAT

MCU_SEC_MMR0_CFG0 Registers
- CTRLMMR_MCUSEC_CLSTR0_CORE1_PMSTAT Register (Offset = 1B0h) [reset = X]: [0]
- MCU_SEC_MMR0_CFG0 Registers: [0]

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5 MCU_SEC_MMR0_DBG_CTRL Registers

Table 5-2 lists the memory-mapped registers for the MCU_SEC_MMR0_DBG_CTRL. All register offset addresses not listed in Table 5-2 should be considered as reserved locations and the register contents should not be modified.

Table 5-1. MCU_SEC_MMR0_DBG_CTRL Instances

Instance	Base Address
MCU_SEC_MMR0_DBG_CTRL	4595 0000h

Table 5-2. MCU_SEC_MMR0_DBG_CTRL Registers

Offset	Acronym	Register Name	MCU_SEC_MMR0_DBG_CTRL Physical Address
0h	CTRLMMR_MCUSEC_CLSTR0_CORE0_DBG_CFG	Cluster0 Core0 Debug Configuration Register	4595 0000h
40h	CTRLMMR_MCUSEC_CLSTR0_CORE1_DBG_CFG	Cluster0 Core1 Debug Configuration Register	4595 0040h

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5.1 CTRLMMR_MCUSEC_CLSTR0_CORE0_DBG_CFG Register (Offset = 0h) [reset = AA00h]

CTRLMMR_MCUSEC_CLSTR0_CORE0_DBG_CFG is shown in Figure 5-1 and described in Table 5-4.

Return to Summary Table.

Configures debug operation for Cluster Core0.

Table 5-3. CTRLMMR_MCUSEC_CLSTR0_CORE0_DBG_CFG Instances

Instance	Physical Address
MCU_SEC_MMR0_DBG_CTRL	4595 0000h

Figure 5-1. CTRLMMR_MCUSEC_CLSTR0_CORE0_DBG_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
DBGEN				NIDEN			
R/W-Ah				R/W-Ah			
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 5-4. CTRLMMR_MCUSEC_CLSTR0_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	DBGEN	R/W	Ah	Core0 Invasive debug enable. This is a fault tolerant bitfield that must be set Ah to enable Ah - Enabled others - Disabled
11-8	NIDEN	R/W	Ah	Core0 Non-invasive debug enable. This is a fault tolerant bitfield that must be set Ah to enable Ah - Enabled others - Disabled
7-0	RESERVED	R	0h	Reserved

Table 5-5. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE0_DBG_CFG

MCU_SEC_MMR0_DBG_CTRL Registers

- CTRLMMR_MCUSEC_CLSTR0_CORE0_DBG_CFG Register (Offset = 0h) [reset = AA00h]: [0]
- MCU_SEC_MMR0_DBG_CTRL Registers: [0]

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5.2 CTRLMMR_MCUSEC_CLSTR0_CORE1_DBG_CFG Register (Offset = 40h) [reset = AA00h]

CTRLMMR_MCUSEC_CLSTR0_CORE1_DBG_CFG is shown in Figure 5-2 and described in Table 5-7.

Return to Summary Table.

Configures debug operation for Cluster Core1.

Table 5-6. CTRLMMR_MCUSEC_CLSTR0_CORE1_DBG_CFG Instances

Instance	Physical Address
MCU_SEC_MMR0_DBG_CTRL	4595 0040h

Figure 5-2. CTRLMMR_MCUSEC_CLSTR0_CORE1_DBG_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
DBGEN				NIDEN			
R/W-Ah				R/W-Ah			
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 5-7. CTRLMMR_MCUSEC_CLSTR0_CORE1_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	DBGEN	R/W	Ah	Core1 Invasive debug enable. This is a fault tolerant bitfield that must be set Ah to enable Ah - Enabled others - Disabled
11-8	NIDEN	R/W	Ah	Core1 Non-invasive debug enable. This is a fault tolerant bitfield that must be set Ah to enable Ah - Enabled others - Disabled
7-0	RESERVED	R	0h	Reserved

Table 5-8. Register Call Summary for CTRLMMR_MCUSEC_CLSTR0_CORE1_DBG_CFG

MCU_SEC_MMR0_DBG_CTRL Registers

- CTRLMMR_MCUSEC_CLSTR0_CORE1_DBG_CFG Register (Offset = 40h) [reset = AA00h]: [0]
- MCU_SEC_MMR0_DBG_CTRL Registers: [0]

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6 CTRL_MMR0 Registers

Table 6-2 lists the memory-mapped registers for the CTRL_MMR0. All register offset addresses not listed in Table 6-2 should be considered as reserved locations and the register contents should not be modified.

Table 6-1. CTRL_MMR0 Instances

Instance	Base Address
CTRL_MMR0	0010 0000h

Table 6-2. CTRL_MMR0 Registers

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
0h	2000h	CTRLMMR_PID	Peripheral Identification Register	0010 0000h	0010 2000h
8h	2008h	CTRLMMR_MMR_CFG1	Configuration register 1	0010 0008h	0010 2008h
30h	2030h	CTRLMMR_MAIN_DEVSTAT	MAIN Domain Device Status Register	0010 0030h	0010 2030h
34h	2034h	CTRLMMR_MAIN_BOOTCFG	MAIN Domain Boot Configuration Register	0010 0034h	0010 2034h
40h	2040h	CTRLMMR_MAIN_FEATURE_STAT 0	MAIN Domain Feature Status Register 0	0010 0040h	0010 2040h
44h	2044h	CTRLMMR_MAIN_FEATURE_STAT 1	MAIN Domain Feature Status Register 1	0010 0044h	0010 2044h
100h	2100h	CTRLMMR_IPC_SET0	IPC Generation Register 0	0100 0100h	0100 2100h
118h	2118h	CTRLMMR_IPC_SET6	IPC Generation Register 6	0010 0118h	0010 2118h
11Ch	211Ch	CTRLMMR_IPC_SET7	IPC Generation Register 7	0010 011Ch	0010 211Ch
120h	2120h	CTRLMMR_IPC_SET8	IPC Generation Register 8	0010 0120h	0010 2120h
124h	2124h	CTRLMMR_IPC_SET9	IPC Generation Register 9	0010 0124h	0010 2124h
140h	2140h	CTRLMMR_IPC_SET16	IPC Generation Register 16	0010 0140h	0010 2140h
144h	2144h	CTRLMMR_IPC_SET17	IPC Generation Register 17	0010 0144h	0010 2144h
148h	2148h	CTRLMMR_IPC_SET18	IPC Generation Register 18	0010 0148h	0010 2148h
14Ch	214Ch	CTRLMMR_IPC_SET19	IPC Generation Register 19	0010 014Ch	0010 214Ch
150h	2150h	CTRLMMR_IPC_SET20	IPC Generation Register 20	0010 0150h	0010 2150h
154h	2154h	CTRLMMR_IPC_SET21	IPC Generation Register 21	0010 0154h	0010 2154h
158h	2158h	CTRLMMR_IPC_SET22	IPC Generation Register 22	0010 0158h	0010 2158h
15Ch	215Ch	CTRLMMR_IPC_SET23	IPC Generation Register 23	0010 015Ch	0010 215Ch
180h	2180h	CTRLMMR_IPC_CLR0	IPC Acknowledge Register0	0010 0180h	0010 2180h
198h	2198h	CTRLMMR_IPC_CLR6	IPC Acknowledge Register6	0010 0198h	0010 2198h
19Ch	219Ch	CTRLMMR_IPC_CLR7	IPC Acknowledge Register7	0010 019Ch	0010 219Ch

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
1A0h	21A0h	CTRLMMR_IPC_CLR8	IPC Acknowledge Register8	0010 01A0h	0010 21A0h
1A4h	21A4h	CTRLMMR_IPC_CLR9	IPC Acknowledge Register9	0010 01A4h	0010 21A4h
1C0h	21C0h	CTRLMMR_IPC_CLR16	IPC Acknowledge Register 16	0010 01C0h	0010 21C0h
1C4h	21C4h	CTRLMMR_IPC_CLR17	IPC Acknowledge Register 17	0010 01C4h	0010 21C4h
1C8h	21C8h	CTRLMMR_IPC_CLR18	IPC Acknowledge Register 18	0010 01C8h	0010 21C8h
1CCh	21CCh	CTRLMMR_IPC_CLR19	IPC Acknowledge Register 19	0010 01CCh	0010 21CCh
1D0h	21D0h	CTRLMMR_IPC_CLR20	IPC Acknowledge Register 20	0010 01D0h	0010 21D0h
1D4h	21D4h	CTRLMMR_IPC_CLR21	IPC Acknowledge Register 21	0010 01D4h	0010 21D4h
1D8h	21D8h	CTRLMMR_IPC_CLR22	IPC Acknowledge Register 22	0010 01D8h	0010 21D8h
1DCh	21DCh	CTRLMMR_IPC_CLR23	IPC Acknowledge Register 23	0010 01DCh	0010 21DCh
210h	2210h	CTRLMMR_PCI_DEVICE_ID	PCI Device ID Register	0010 0210h	0010 2210h
220h	2220h	CTRLMMR_USB_DEVICE_ID	USB Device ID Register	0010 0220h	0010 2220h
1008h	3008h	CTRLMMR_LOCK0_KICK0	Partition 0 Lock Key 0 Register	0010 1008h	0010 3008h
100Ch	300Ch	CTRLMMR_LOCK0_KICK1	Partition 0 Lock Key 1 Register	0010 100Ch	0010 300Ch
1010h	3010h	CTRLMMR_INTR_RAW_STAT	Interrupt Raw Status Register	0010 1010h	0010 3010h
1014h	3014h	CTRLMMR_INTR_STAT_CLR	Interrupt Status and Clear Register	0010 1014h	0010 3014h
1018h	3018h	CTRLMMR_INTR_EN_SET	Interrupt Enable Set Register	0010 1018h	0010 3018h
101Ch	301Ch	CTRLMMR_INTR_EN_CLR	Interrupt Enable Clear Register	0010 101Ch	0010 301Ch
1020h	3020h	CTRLMMR_EOI	End of Interrupt Register	0010 1020h	0010 3020h
1024h	3024h	CTRLMMR_FAULT_ADDR	Fault Address Register	0010 1024h	0010 3024h
1028h	3028h	CTRLMMR_FAULT_TYPE	Fault Type Register	0010 1028h	0010 3028h
102Ch	302Ch	CTRLMMR_FAULT_ATTR	Fault Attribute Register	0010 102Ch	0010 302Ch
1030h	3030h	CTRLMMR_FAULT_CLR	Fault Clear Register	0010 1030h	0010 3030h
1100h	3100h	CTRLMMR_P0_CLAIM0	Partition 0 Claim Register 0	0010 1100h	0010 3100h
1104h	3104h	CTRLMMR_P0_CLAIM1	Partition 0 Claim Register 1	0010 1104h	0010 3104h
1108h	3108h	CTRLMMR_P0_CLAIM2	Partition 0 Claim Register 2	0010 1108h	0010 3108h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
110Ch	310Ch	CTRLMMR_P0_CLAIM3	Partition 0 Claim Register 3	0010 110Ch	0010 310Ch
1110h	3110h	CTRLMMR_P0_CLAIM4	Partition 0 Claim Register 4	0010 1110h	0010 3110h
1114h	3114h	CTRLMMR_P0_CLAIM5	Partition 0 Claim Register 5	0010 1114h	0010 3114h
1118h	3118h	CTRLMMR_P0_CLAIM6	Partition 0 Claim Register 6	0010 1118h	0010 3118h
4000h	6000h	CTRLMMR_USB0_CTRL	USB0 Control Register	0010 4000h	0010 6000h
4010h	6010h	CTRLMMR_USB1_CTRL	USB1 Control Register	0010 4010h	0010 6010h
4044h	6044h	CTRLMMR_ENET1_CTRL	Ethernet1 Control Register	0010 4044h	0010 6044h
4048h	6048h	CTRLMMR_ENET2_CTRL	Ethernet2 Control Register	0010 4048h	0010 6048h
404Ch	604Ch	CTRLMMR_ENET3_CTRL	Ethernet3 Control Register	0010 404Ch	0010 604Ch
4050h	6050h	CTRLMMR_ENET4_CTRL	Ethernet4 Control Register	0010 4050h	0010 6050h
4054h	6054h	CTRLMMR_ENET5_CTRL	Ethernet5 Control Register	0010 4054h	0010 6054h
4058h	6058h	CTRLMMR_ENET6_CTRL	Ethernet6 Control Register	0010 4058h	0010 6058h
405Ch	605Ch	CTRLMMR_ENET7_CTRL	Ethernet7 Control Register	0010 405Ch	0010 605Ch
4060h	6060h	CTRLMMR_ENET8_CTRL	Ethernet8 Control Register	0010 4060h	0010 6060h
4070h	6070h	CTRLMMR_PCIE0_CTRL	PCEI0 Control Register	0010 4070h	0010 6070h
4074h	6074h	CTRLMMR_PCIE1_CTRL	PCEI1 Control Register	0010 4074h	0010 6074h
4078h	6078h	CTRLMMR_PCIE2_CTRL	PCEI2 Control Register	0010 4078h	0010 6078h
407Ch	607Ch	CTRLMMR_PCIE3_CTRL	PCEI3 Control Register	0010 407Ch	0010 607Ch
4080h	6080h	CTRLMMR_SERDES0_LN0_CTRL	SERDES0 Lane0 Control Register	0010 4080h	0010 6080h
4084h	6084h	CTRLMMR_SERDES0_LN1_CTRL	SERDES0 Lane1 Control Register	0010 4084h	0010 6084h
4090h	6090h	CTRLMMR_SERDES1_LN0_CTRL	SERDES1 Lane0 Control Register	0010 4090h	0010 6090h
4094h	6094h	CTRLMMR_SERDES1_LN1_CTRL	SERDES1 Lane1 Control Register	0010 4094h	0010 6094h
40A0h	60A0h	CTRLMMR_SERDES2_LN0_CTRL	SERDES2 Lane0 Control Register	0010 40A0h	0010 60A0h
40A4h	60A4h	CTRLMMR_SERDES2_LN1_CTRL	SERDES2 Lane1 Control Register	0010 40A4h	0010 60A4h
40B0h	60B0h	CTRLMMR_SERDES3_LN0_CTRL	SERDES3 Lane0 Control Register	0010 40B0h	0010 60B0h
40B4h	60B4h	CTRLMMR_SERDES3_LN1_CTRL	SERDES3 Lane1 Control Register	0010 40B4h	0010 60B4h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
40C0h	60C0h	CTRLMMR_SERDES4_LN0_CTRL	SERDES4 Lane0 Control Register	0010 40C0h	0010 60C0h
40C4h	60C4h	CTRLMMR_SERDES4_LN1_CTRL	SERDES4 Lane1 Control Register	0010 40C4h	0010 60C4h
40C8h	60C8h	CTRLMMR_SERDES4_LN2_CTRL	SERDES4 Lane2 Control Register	0010 40C8h	0010 60C8h
40CCh	60CCh	CTRLMMR_SERDES4_LN3_CTRL	SERDES4 Lane3 Control Register	0010 40CCh	0010 60CCh
40E0h	60E0h	CTRLMMR_SERDES0_CTRL	SERDES0 Control Register	0010 40E0h	0010 60E0h
40E4h	60E4h	CTRLMMR_SERDES1_CTRL	SERDES1 Control Register	0010 40E4h	0010 60E4h
40E8h	60E8h	CTRLMMR_SERDES2_CTRL	SERDES2 Control Register	0010 40E8h	0010 60E8h
40ECh	60ECh	CTRLMMR_SERDES3_CTRL	SERDES3 Control Register	0010 40ECh	0010 60ECh
40F0h	60F0h	CTRLMMR_SERDES4_CTRL	SERDES4 Control Register	0010 40F0h	0010 60F0h
4100h	6100h	CTRLMMR_ICSSG0_CTRL0	ICSS_G0 Control Register 0	0010 4100h	0010 6100h
4104h	6104h	CTRLMMR_ICSSG0_CTRL1	ICSS_G0 Control Register 1	0010 4104h	0010 6104h
4110h	6110h	CTRLMMR_ICSSG1_CTRL0	ICSS_G1 Control Register 0	0010 4110h	0010 6110h
4114h	6114h	CTRLMMR_ICSSG1_CTRL1	ICSS_G1 Control Register 1	0010 4114h	0010 6114h
4140h	6140h	CTRLMMR_EPWM0_CTRL	PWM0 Control Register	0010 4140h	0010 6140h
4144h	6144h	CTRLMMR_EPWM1_CTRL	PWM1 Control Register	0010 4144h	0010 6144h
4148h	6148h	CTRLMMR_EPWM2_CTRL	PWM2 Control Register	0010 4148h	0010 6148h
414Ch	614Ch	CTRLMMR_EPWM3_CTRL	PWM3 Control Register	0010 414Ch	0010 614Ch
4150h	6150h	CTRLMMR_EPWM4_CTRL	PWM4 Control Register	0010 4150h	0010 6150h
4154h	6154h	CTRLMMR_EPWM5_CTRL	PWM5 Control Register	0010 4154h	0010 6154h
4160h	6160h	CTRLMMR_SOCA_SEL	PWM SOCA Select Register	0010 4160h	0010 6160h
4164h	6164h	CTRLMMR_SOCB_SEL	PWM SOCB Select Register	0010 4164h	0010 6164h
41A0h	61A0h	CTRLMMR_EQEP_STAT	EQEP Status Register	0010 41A0h	0010 61A0h
41B4h	61B4h	CTRLMMR_SDIO1_CTRL	SDIO1 Control Register	0010 41B4h	0010 61B4h
41B8h	61B8h	CTRLMMR_SDIO2_CTRL	SDIO2 Control Register	0010 41B8h	0010 61B8h
41C0h	61C0h	CTRLMMR_MLB_SIG_IO_CTRL	MLB SIG LVDS IO Control Register	0010 41C0h	0010 61C0h
41C4h	61C4h	CTRLMMR_MLB_DAT_IO_CTRL	MLB DATA LVDS IO Control Register	0010 41C4h	0010 61C4h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
41C8h	61C8h	CTRLMMR_MLB_CLK_IO_CTRL	MLB CLK LVDS IO Control Register	0010 41C8h	0010 61C8h
41D0h	61D0h	CTRLMMR_MLB_GPIO_CTRL	MLB GPIO Control Register	0010 41D0h	0010 61D0h
4200h	6200h	CTRLMMR_TIMER0_CTRL	TIMER0 Control Register	0010 4200h	0010 6200h
4204h	6204h	CTRLMMR_TIMER1_CTRL	TIMER1 Control Register	0010 4204h	0010 6204h
4208h	6208h	CTRLMMR_TIMER2_CTRL	TIMER2 Control Register	0010 4208h	0010 6208h
420Ch	620Ch	CTRLMMR_TIMER3_CTRL	TIMER3 Control Register	0010 420Ch	0010 620Ch
4210h	6210h	CTRLMMR_TIMER4_CTRL	TIMER4 Control Register	0010 4210h	0010 6210h
4214h	6214h	CTRLMMR_TIMER5_CTRL	TIMER5 Control Register	0010 4214h	0010 6214h
4218h	6218h	CTRLMMR_TIMER6_CTRL	TIMER6 Control Register	0010 4218h	0010 6218h
421Ch	621Ch	CTRLMMR_TIMER7_CTRL	TIMER7 Control Register	0010 421Ch	0010 621Ch
4220h	6220h	CTRLMMR_TIMER8_CTRL	TIMER8 Control Register	0010 4220h	0010 6220h
4224h	6224h	CTRLMMR_TIMER9_CTRL	TIMER9 Control Register	0010 4224h	0010 6224h
4228h	6228h	CTRLMMR_TIMER10_CTRL	TIMER10 Control Register	0010 4228h	0010 6228h
422Ch	622Ch	CTRLMMR_TIMER11_CTRL	TIMER11 Control Register	0010 422Ch	0010 622Ch
4230h	6230h	CTRLMMR_TIMER12_CTRL	TIMER12 Control Register	0010 4230h	0010 6230h
4234h	6234h	CTRLMMR_TIMER13_CTRL	TIMER13 Control Register	0010 4234h	0010 6234h
4238h	6238h	CTRLMMR_TIMER14_CTRL	TIMER14 Control Register	0010 4238h	0010 6238h
423Ch	623Ch	CTRLMMR_TIMER15_CTRL	TIMER15 Control Register	0010 423Ch	0010 623Ch
4240h	6240h	CTRLMMR_TIMER16_CTRL	TIMER16 Control Register	0010 4240h	0010 6240h
4244h	6244h	CTRLMMR_TIMER17_CTRL	TIMER17 Control Register	0010 4244h	0010 6244h
4248h	6248h	CTRLMMR_TIMER18_CTRL	TIMER18 Control Register	0010 4248h	0010 6248h
424Ch	624Ch	CTRLMMR_TIMER19_CTRL	TIMER19 Control Register	0010 424Ch	0010 624Ch
4280h	6280h	CTRLMMR_TIMERIO0_CTRL	TIMERIO0 Control Register	0010 4280h	0010 6280h
4284h	6284h	CTRLMMR_TIMERIO1_CTRL	TIMERIO1 Control Register	0010 4284h	0010 6284h
4288h	6288h	CTRLMMR_TIMERIO2_CTRL	TIMERIO2 Control Register	0010 4288h	0010 6288h
428Ch	628Ch	CTRLMMR_TIMERIO3_CTRL	TIMERIO3 Control Register	0010 428Ch	0010 628Ch

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
4290h	6290h	CTRLMMR_TIMERIO4_CTRL	TIMERIO4 Control Register	0010 4290h	0010 6290h
4294h	6294h	CTRLMMR_TIMERIO5_CTRL	TIMERIO5 Control Register	0010 4294h	0010 6294h
4298h	6298h	CTRLMMR_TIMERIO6_CTRL	TIMERIO6 Control Register	0010 4298h	0010 6298h
429Ch	629Ch	CTRLMMR_TIMERIO7_CTRL	TIMERIO7 Control Register	0010 429Ch	0010 629Ch
42C0h	62C0h	CTRLMMR_I3C0_CTRL0	I3C0 Control Register 0	0010 42C0h	0010 62C0h
42C4h	62C4h	CTRLMMR_I3C0_CTRL1	I3C0 Control Register 1	0010 42C4h	0010 62C4h
42C8h	62C8h	CTRLMMR_I3C1_CTRL0	I3C1 Control Register 0	0010 42C8h	0010 62C8h
42CCh	62CCh	CTRLMMR_I3C1_CTRL1	I3C1 Control Register 1	0010 42CCh	0010 62CCh
42E0h	62E0h	CTRLMMR_I2C0_CTRL	I2C0 Control Register	0010 42E0h	0010 62E0h
42E4h	62E4h	CTRLMMR_I2C1_CTRL	I2C1 Control Register	0010 42E4h	0010 62E4h
4300h	6300h	CTRLMMR_DPHY_TX0_CTRL	Video Transmit MIPI DPHY0 Lane0 Control Register	0010 4300h	0010 6300h
43F0h	63F0h	CTRLMMR_CSI_RX_LOOPBACK	CSI-RX Loopback Control Register	0010 43F0h	0010 63F0h
4500h	6500h	CTRLMMR_GPU_GP_IN_REQ	GPU GPIO In Request Register	0010 4500h	0010 6500h
4504h	6504h	CTRLMMR_GPU_GP_IN_ACK	GPU GPIO In Acknowledge Register	0010 4504h	0010 6504h
4508h	6508h	CTRLMMR_GPU_GP_OUT_REQ	GPU GPIO Out Request Register	0010 4508h	0010 6508h
450Ch	650Ch	CTRLMMR_GPU_GP_OUT_ACK	GPU GPIO Out Acknowledge Register	0010 450Ch	0010 650Ch
4548h	6548h	CTRLMMR_UFS_PHY_CAL_CTRL2	UFS PHY Calibration Control Register 2	0010 4548h	0010 6548h
5008h	7008h	CTRLMMR_LOCK1_KICK0	Partition 1 Lock Key 0 Register	0010 5008h	0010 7008h
500Ch	700Ch	CTRLMMR_LOCK1_KICK1	Partition 1 Lock Key 1 Register	0010 500Ch	0010 700Ch
5100h	7100h	CTRLMMR_P1_CLAIM0	Partition 1 Claim Register 0	0010 5100h	0010 7100h
5104h	7104h	CTRLMMR_P1_CLAIM1	Partition 1 Claim Register 1	0010 5104h	0010 7104h
5108h	7108h	CTRLMMR_P1_CLAIM2	Partition 1 Claim Register 2	0010 5108h	0010 7108h
510Ch	710Ch	CTRLMMR_P1_CLAIM3	Partition 1 Claim Register 3	0010 510Ch	0010 710Ch
5110h	7110h	CTRLMMR_P1_CLAIM4	Partition 1 Claim Register 4	0010 5110h	0010 7110h
5114h	7114h	CTRLMMR_P1_CLAIM5	Partition 1 Claim Register 5	0010 5114h	0010 7114h
5118h	7118h	CTRLMMR_P1_CLAIM6	Partition 1 Claim Register 6	0010 5118h	0010 7118h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
511Ch	711Ch	CTRLMMR_P1_CLAIM7	Partition 1 Claim Register 7	0010 511Ch	0010 711Ch
5120h	7120h	CTRLMMR_P1_CLAIM8	Partition 1 Claim Register 8	0010 5120h	0010 7120h
5124h	7124h	CTRLMMR_P1_CLAIM9	Partition 1 Claim Register 9	0010 5124h	0010 7124h
5128h	7128h	CTRLMMR_P1_CLAIM10	Partition 1 Claim Register 10	0010 5128h	0010 7128h
512Ch	712Ch	CTRLMMR_P1_CLAIM11	Partition 1 Claim Register 11	0010 512Ch	0010 712Ch
5130h	7130h	CTRLMMR_P1_CLAIM12	Partition 1 Claim Register 12	0010 5130h	0010 7130h
5134h	7134h	CTRLMMR_P1_CLAIM13	Partition 1 Claim Register 13	0010 5134h	0010 7134h
5138h	7138h	CTRLMMR_P1_CLAIM14	Partition 1 Claim Register 14	0010 5138h	0010 7138h
513Ch	713Ch	CTRLMMR_P1_CLAIM15	Partition 1 Claim Register 15	0010 513Ch	0010 713Ch
5140h	7140h	CTRLMMR_P1_CLAIM16	Partition 1 Claim Register 16	0010 5140h	0010 7140h
5144h	7144h	CTRLMMR_P1_CLAIM17	Partition 1 Claim Register 17	0010 5144h	0010 7144h
5148h	7148h	CTRLMMR_P1_CLAIM18	Partition 1 Claim Register 18	0010 5148h	0010 7148h
514Ch	714Ch	CTRLMMR_P1_CLAIM19	Partition 1 Claim Register 19	0010 514Ch	0010 714Ch
5150h	7150h	CTRLMMR_P1_CLAIM20	Partition 1 Claim Register 20	0010 5150h	0010 7150h
8000h	A000h	CTRLMMR_OBSCLK0_CTRL	Observe Clock 0 Output Control Register	0010 8000h	0010 A000h
8004h	A004h	CTRLMMR_OBSCLK1_CTRL	Observe Clock 1 Select Register	0010 8004h	0010 A004h
8010h	A010h	CTRLMMR_CLKOUT_CTRL	CLKOUT Control Register	0010 8010h	0010 A010h
8030h	A030h	CTRLMMR_GTC_CLKSEL	GTC Clock Select Register	0010 8030h	0010 A030h
803Ch	A03Ch	CTRLMMR_EFUSE_CLKSEL	Main eFuse Controller Clock Select Register	0010 803Ch	0010 A03Ch
8040h	A040h	CTRLMMR_ICSSG0_CLKSEL	ICSS_G0 Clock Select Register	0010 8040h	0010 A040h
8044h	A044h	CTRLMMR_ICSSG1_CLKSEL	ICSS_G1 Clock Select Register	0010 8044h	0010 A044h
8070h	A070h	CTRLMMR_PCIE_REFCLK0_CLKSEL	PCIE Reference Clock 0 Select Register	0010 8070h	0010 A070h
8074h	A074h	CTRLMMR_PCIE_REFCLK1_CLKSEL	PCIE Reference Clock 1 Select Register	0010 8074h	0010 A074h
8078h	A078h	CTRLMMR_PCIE_REFCLK2_CLKSEL	PCIE Reference Clock 2 Select Register	0010 8078h	0010 A078h
807Ch	A07Ch	CTRLMMR_PCIE_REFCLK3_CLKSEL	PCIE Reference Clock 3 Select Register	0010 807Ch	0010 A07Ch
8080h	A080h	CTRLMMR_PCIE0_CLKSEL	PCIE0 Clock Select Register	0010 8080h	0010 A080h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
8084h	A084h	CTRLMMR_PCIE1_CLKSEL	PCIE1 Clock Select Register	0010 8084h	0010 A084h
8088h	A088h	CTRLMMR_PCIE2_CLKSEL	PCIE2 Clock Select Register	0010 8088h	0010 A088h
808Ch	A08Ch	CTRLMMR_PCIE3_CLKSEL	PCIE3 Clock Select Register	0010 808Ch	0010 A08Ch
8090h	A090h	CTRLMMR_CPSW_CLKSEL	CPSW Clock Select Register	0010 8090h	0010 A090h
8098h	A098h	CTRLMMR_NAVSS_CLKSEL	Navigator Subsystem Clock Select Register	0010 8098h	0010 A098h
80B0h	A0B0h	CTRLMMR_EMMC0_CLKSEL	eMMC0 Clock Select Register	0010 80B0h	0010 A0B0h
80B4h	A0B4h	CTRLMMR_EMMC1_CLKSEL	eMMC1 Clock Select Register	0010 80B4h	0010 A0B4h
80B8h	A0B8h	CTRLMMR_EMMC2_CLKSEL	eMMC2 Clock Select Register	0010 80B8h	0010 A0B8h
80C0h	A0C0h	CTRLMMR_UFS0_CLKSEL	UFS0 Clock Select Register	0010 80C0h	0010 A0C0h
80D0h	A0D0h	CTRLMMR_GPMC_CLKSEL	GPMC Clock Select Register	0010 80D0h	0010 A0D0h
80E0h	A0E0h	CTRLMMR_USB0_CLKSEL	USB0 Clock Select Register	0010 80E0h	0010 A0E0h
80E4h	A0E4h	CTRLMMR_USB1_CLKSEL	USB1 Clock Select Register	0010 80E4h	0010 A0E4h
8100h	A100h	CTRLMMR_TIMER0_CLKSEL	Timer0 Clock Select Register	0010 8100h	0010 A100h
8104h	A104h	CTRLMMR_TIMER1_CLKSEL	Timer1 Clock Select Register	0010 8104h	0010 A104h
8108h	A108h	CTRLMMR_TIMER2_CLKSEL	Timer2 Clock Select Register	0010 8108h	0010 A108h
810Ch	A10Ch	CTRLMMR_TIMER3_CLKSEL	Timer3 Clock Select Register	0010 810Ch	0010 A10Ch
8110h	A110h	CTRLMMR_TIMER4_CLKSEL	Timer4 Clock Select Register	0010 8110h	0010 A110h
8114h	A114h	CTRLMMR_TIMER5_CLKSEL	Timer5 Clock Select Register	0010 8114h	0010 A114h
8118h	A118h	CTRLMMR_TIMER6_CLKSEL	Timer6 Clock Select Register	0010 8118h	0010 A118h
811Ch	A11Ch	CTRLMMR_TIMER7_CLKSEL	Timer7 Clock Select Register	0010 811Ch	0010 A11Ch
8120h	A120h	CTRLMMR_TIMER8_CLKSEL	Timer8 Clock Select Register	0010 8120h	0010 A120h
8124h	A124h	CTRLMMR_TIMER9_CLKSEL	Timer9 Clock Select Register	0010 8124h	0010 A124h
8128h	A128h	CTRLMMR_TIMER10_CLKSEL	Timer10 Clock Select Register	0010 8128h	0010 A128h
812Ch	A12Ch	CTRLMMR_TIMER11_CLKSEL	Timer11 Clock Select Register	0010 812Ch	0010 A12Ch
8130h	A130h	CTRLMMR_TIMER12_CLKSEL	Timer12 Clock Select Register	0010 8130h	0010 A130h
8134h	A134h	CTRLMMR_TIMER13_CLKSEL	Timer13 Clock Select Register	0010 8134h	0010 A134h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
8138h	A138h	CTRLMMR_TIMER14_CLKSEL	Timer14 Clock Select Register	0010 8138h	0010 A138h
813Ch	A13Ch	CTRLMMR_TIMER15_CLKSEL	Timer15 Clock Select Register	0010 813Ch	0010 A13Ch
8140h	A140h	CTRLMMR_TIMER16_CLKSEL	Timer16 Clock Select Register	0010 8140h	0010 A140h
8144h	A144h	CTRLMMR_TIMER17_CLKSEL	Timer17 Clock Select Register	0010 8144h	0010 A144h
8148h	A148h	CTRLMMR_TIMER18_CLKSEL	Timer18 Clock Select Register	0010 8148h	0010 A148h
814Ch	A14Ch	CTRLMMR_TIMER19_CLKSEL	Timer19 Clock Select Register	0010 814Ch	0010 A14Ch
8190h	A190h	CTRLMMR_SPI0_CLKSEL	SPI0 Clock Select Register	0010 8190h	0010 A190h
8194h	A194h	CTRLMMR_SPI1_CLKSEL	SPI1 Clock Select Register	0010 8194h	0010 A194h
8198h	A198h	CTRLMMR_SPI2_CLKSEL	SPI2 Clock Select Register	0010 8198h	0010 A198h
819Ch	A19Ch	CTRLMMR_SPI3_CLKSEL	SPI3 Clock Select Register	0010 819Ch	0010 A19Ch
81A4h	A1A4h	CTRLMMR_SPI5_CLKSEL	SPI5 Clock Select Register	0010 81A4h	0010 A1A4h
81A8h	A1A8h	CTRLMMR_SPI6_CLKSEL	SPI6 Clock Select Register	0010 81A8h	0010 A1A8h
81ACh	A1ACh	CTRLMMR_SPI7_CLKSEL	SPI7 Clock Select Register	0010 81ACh	0010 A1ACh
81C0h	A1C0h	CTRLMMR_USART0_CLK_CTRL	USART0 Functional Clock Control	0010 81C0h	0010 A1C0h
81C4h	A1C4h	CTRLMMR_USART1_CLK_CTRL	USART1 Functional Clock Control	0010 81C4h	0010 A1C4h
81C8h	A1C8h	CTRLMMR_USART2_CLK_CTRL	USART2 Functional Clock Control	0010 81C8h	0010 A1C8h
81CCh	A1CCh	CTRLMMR_USART3_CLK_CTRL	USART3 Functional Clock Control	0010 81CCh	0010 A1CCh
81D0h	A1D0h	CTRLMMR_USART4_CLK_CTRL	USART4 Functional Clock Control	0010 81D0h	0010 A1D0h
81D4h	A1D4h	CTRLMMR_USART5_CLK_CTRL	USART5 Functional Clock Control	0010 81D4h	0010 A1D4h
81D8h	A1D8h	CTRLMMR_USART6_CLK_CTRL	USART6 Functional Clock Control	0010 81D8h	0010 A1D8h
81DCh	A1DCh	CTRLMMR_USART7_CLK_CTRL	USART7 Functional Clock Control	0010 81DCh	0010 A1DCh
81E0h	A1E0h	CTRLMMR_USART8_CLK_CTRL	USART8 Functional Clock Control	0010 81E0h	0010 A1E0h
81E4h	A1E4h	CTRLMMR_USART9_CLK_CTRL	USART9 Functional Clock Control	0010 81E4h	0010 A1E4h
8200h	A200h	CTRLMMR_MCASP0_CLKSEL	McASP0 Clock Select Register	0010 8200h	0010 A200h
8204h	A204h	CTRLMMR_MCASP1_CLKSEL	McASP1 Clock Select Register	0010 8204h	0010 A204h
8208h	A208h	CTRLMMR_MCASP2_CLKSEL	McASP2 Clock Select Register	0010 8208h	0010 A208h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
820Ch	A20Ch	CTRLMMR_MCASP3_CLKSEL	McASP3 Clock Select Register	0010 820Ch	0010 A20Ch
8210h	A210h	CTRLMMR_MCASP4_CLKSEL	McASP4 Clock Select Register	0010 8210h	0010 A210h
8214h	A214h	CTRLMMR_MCASP5_CLKSEL	McASP5 Clock Select Register	0010 8214h	0010 A214h
8218h	A218h	CTRLMMR_MCASP6_CLKSEL	McASP6 Clock Select Register	0010 8218h	0010 A218h
821Ch	A21Ch	CTRLMMR_MCASP7_CLKSEL	McASP7 Clock Select Register	0010 821Ch	0010 A21Ch
8220h	A220h	CTRLMMR_MCASP8_CLKSEL	McASP8 Clock Select Register	0010 8220h	0010 A220h
8224h	A224h	CTRLMMR_MCASP9_CLKSEL	McASP9 Clock Select Register	0010 8224h	0010 A224h
8228h	A228h	CTRLMMR_MCASP10_CLKSEL	McASP10 Clock Select Register	0010 8228h	0010 A228h
822Ch	A22Ch	CTRLMMR_MCASP11_CLKSEL	McASP11 Clock Select Register	0010 822Ch	0010 A22Ch
8240h	A240h	CTRLMMR_MCASP0_AHCLKSEL	McASP0 AHClock Select Register	0010 8240h	0010 A240h
8244h	A244h	CTRLMMR_MCASP1_AHCLKSEL	McASP1 AHClock Select Register	0010 8244h	0010 A244h
8248h	A248h	CTRLMMR_MCASP2_AHCLKSEL	McASP2 AHClock Select Register	0010 8248h	0010 A248h
824Ch	A24Ch	CTRLMMR_MCASP3_AHCLKSEL	McASP3 AHClock Select Register	0010 824Ch	0010 A24Ch
8250h	A250h	CTRLMMR_MCASP4_AHCLKSEL	McASP4 AHClock Select Register	0010 8250h	0010 A250h
8254h	A254h	CTRLMMR_MCASP5_AHCLKSEL	McASP5 AHClock Select Register	0010 8254h	0010 A254h
8258h	A258h	CTRLMMR_MCASP6_AHCLKSEL	McASP6 AHClock Select Register	0010 8258h	0010 A258h
825Ch	A25Ch	CTRLMMR_MCASP7_AHCLKSEL	McASP7 AHClock Select Register	0010 825Ch	0010 A25Ch
8260h	A260h	CTRLMMR_MCASP8_AHCLKSEL	McASP8 AHClock Select Register	0010 8260h	0010 A260h
8264h	A264h	CTRLMMR_MCASP9_AHCLKSEL	McASP9 AHClock Select Register	0010 8264h	0010 A264h
8268h	A268h	CTRLMMR_MCASP10_AHCLKSEL	McASP10 AHClock Select Register	0010 8268h	0010 A268h
826Ch	A26Ch	CTRLMMR_MCASP11_AHCLKSEL	McASP11 AHClock Select Register	0010 826Ch	0010 A26Ch
8280h	A280h	CTRLMMR_ASRC_RXSYNC0_SEL	ASRC Receive Frame Sync Select Register	0010 8280h	0010 A280h
8284h	A284h	CTRLMMR_ASRC_RXSYNC1_SEL	ASRC Receive Frame Sync Select Register	0010 8284h	0010 A284h
8288h	A288h	CTRLMMR_ASRC_RXSYNC2_SEL	ASRC Receive Frame Sync Select Register	0010 8288h	0010 A288h
828Ch	A28Ch	CTRLMMR_ASRC_RXSYNC3_SEL	ASRC Receive Frame Sync Select Register	0010 828Ch	0010 A28Ch
8290h	A290h	CTRLMMR_ASRC_TXSYNC0_SEL	ASRC Transmit Frame Sync Select Register	0010 8290h	0010 A290h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
8294h	A294h	CTRLMMR_ASRC_TXSYNC1_SEL	ASRC Transmit Frame Sync Select Register	0010 8294h	0010 A294h
8298h	A298h	CTRLMMR_ASRC_TXSYNC2_SEL	ASRC Transmit Frame Sync Select Register	0010 8298h	0010 A298h
829Ch	A29Ch	CTRLMMR_ASRC_TXSYNC3_SEL	ASRC Transmit Frame Sync Select Register	0010 829Ch	0010 A29Ch
82A0h	A2A0h	CTRLMMR_ATL_BWS0_SEL	ATL BWS0 Select Register	0010 82A0h	0010 A2A0h
82A4h	A2A4h	CTRLMMR_ATL_BWS1_SEL	ATL BWS1 Select Register	0010 82A4h	0010 A2A4h
82A8h	A2A8h	CTRLMMR_ATL_BWS2_SEL	ATL BWS2 Select Register	0010 82A8h	0010 A2A8h
82ACh	A2ACh	CTRLMMR_ATL_BWS3_SEL	ATL BWS3 Select Register	0010 82ACh	0010 A2ACh
82B0h	A2B0h	CTRLMMR_ATL_AWS0_SEL	ATL AWS Select Register	0010 82B0h	0010 A2B0h
82B4h	A2B4h	CTRLMMR_ATL_AWS1_SEL	ATL AWS Select Register	0010 82B4h	0010 A2B4h
82B8h	A2B8h	CTRLMMR_ATL_AWS2_SEL	ATL AWS Select Register	0010 82B8h	0010 A2B8h
82BCh	A2BCh	CTRLMMR_ATL_AWS3_SEL	ATL AWS Select Register	0010 82BCh	0010 A2BCh
82C0h	A2C0h	CTRLMMR_ATL_CLKSEL	ATL Clock Select Register	0010 82C0h	0010 A2C0h
82E0h	A2E0h	CTRLMMR_AUDIO_REFCLK0_CTRL	Audio External Reference Clock Control Register	0010 82E0h	0010 A2E0h
82E4h	A2E4h	CTRLMMR_AUDIO_REFCLK1_CTRL	Audio External Reference Clock Control Register	0010 82E4h	0010 A2E4h
82E8h	A2E8h	CTRLMMR_AUDIO_REFCLK2_CTRL	Audio External Reference Clock Control Register	0010 82E8h	0010 A2E8h
82ECh	A2ECh	CTRLMMR_AUDIO_REFCLK3_CTRL	Audio External Reference Clock Control Register	0010 82ECh	0010 A2ECh
8300h	A300h	CTRLMMR_DPI0_CLK_CTRL	DPI0 Clock Control Register	0010 8300h	0010 A300h
8304h	A304h	CTRLMMR_DPI1_CLK_CTRL	DPI1 Clock Control Register	0010 8304h	0010 A304h
8310h	A310h	CTRLMMR_DPHY0_CLKSEL	DSI0 PHY Clock Select Register	0010 8310h	0010 A310h
8324h	A324h	CTRLMMR_DSS_DISPC0_CLKSEL1	DSS Display Controller0 Clock Select1 Register	0010 8324h	0010 A324h
8328h	A328h	CTRLMMR_DSS_DISPC0_CLKSEL2	DSS Display Controller0 Clock Select2 Register	0010 8328h	0010 A328h
832Ch	A32Ch	CTRLMMR_DSS_DISPC0_CLKSEL3	DSS Display Controller0 Clock Select3 Register	0010 832Ch	0010 A32Ch
8340h	A340h	CTRLMMR_EDP_PHY0_CLKSEL	EDP Phy0 Clock Select Register	0010 8340h	0010 A340h
8350h	A350h	CTRLMMR_EDP0_CLK_CTRL	EDP0 Clock Control Register	0010 8350h	0010 A350h
8380h	A380h	CTRLMMR_WWD0_CLKSEL	WWD0 Clock Select Register	0010 8380h	0010 A380h
8384h	A384h	CTRLMMR_WWD1_CLKSEL	WWD1 Clock Select Register	0010 8384h	0010 A384h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
83BCh	A3BCh	CTRLMMR_WWD15_CLKSEL	WWD15 Clock Select Register	0010 83BCh	0010 A3BCh
83C0h	A3C0h	CTRLMMR_WWD16_CLKSEL	WWD16 Clock Select Register	0010 83C0h	0010 A3C0h
83E0h	A3E0h	CTRLMMR_WWD24_CLKSEL	WWD24 Clock Select Register	0010 83E0h	0010 A3E0h
83E4h	A3E4h	CTRLMMR_WWD25_CLKSEL	WWD25 Clock Select Register	0010 83E4h	0010 A3E4h
83F0h	A3F0h	CTRLMMR_WWD28_CLKSEL	WWD28 Clock Select Register	0010 83F0h	0010 A3F0h
83F4h	A3F4h	CTRLMMR_WWD29_CLKSEL	WWD29 Clock Select Register	0010 83F4h	0010 A3F4h
83F8h	A3F8h	CTRLMMR_WWD30_CLKSEL	WWD30 Clock Select Register	0010 83F8h	0010 A3F8h
83FCh	A3FCh	CTRLMMR_WWD31_CLKSEL	WWD31 Clock Select Register	0010 83FCh	0010 A3FCh
8400h	A400h	CTRLMMR_SERDES0_CLKSEL	SERDES 0 Clock Select Register	0010 8400h	0010 A400h
8404h	A404h	CTRLMMR_SERDES0_CLK1SEL	SERDES 0 Clock1 Select Register	0010 8404h	0010 A404h
8410h	A410h	CTRLMMR_SERDES1_CLKSEL	SERDES 1 Clock Select Register	0010 8410h	0010 A410h
8414h	A414h	CTRLMMR_SERDES1_CLK1SEL	SERDES 1 Clock1 Select Register	0010 8414h	0010 A414h
8420h	A420h	CTRLMMR_SERDES2_CLKSEL	SERDES 2 Clock Select Register	0010 8420h	0010 A420h
8424h	A424h	CTRLMMR_SERDES2_CLK1SEL	SERDES 2 Clock1 Select Register	0010 8424h	0010 A424h
8430h	A430h	CTRLMMR_SERDES3_CLKSEL	SERDES 3 Clock Select Register	0010 8430h	0010 A430h
8434h	A434h	CTRLMMR_SERDES3_CLK1SEL	SERDES 3 Clock1 Select Register	0010 8434h	0010 A434h
8480h	A480h	CTRLMMR_MCAN0_CLKSEL	MCAN0 Clock Select Register	0010 8480h	0010 A480h
8484h	A484h	CTRLMMR_MCAN1_CLKSEL	MCAN1 Clock Select Register	0010 8484h	0010 A484h
8488h	A488h	CTRLMMR_MCAN2_CLKSEL	MCAN2 Clock Select Register	0010 8488h	0010 A488h
848Ch	A48Ch	CTRLMMR_MCAN3_CLKSEL	MCAN3 Clock Select Register	0010 848Ch	0010 A48Ch
8490h	A490h	CTRLMMR_MCAN4_CLKSEL	MCAN4 Clock Select Register	0010 8490h	0010 A490h
8494h	A494h	CTRLMMR_MCAN5_CLKSEL	MCAN5 Clock Select Register	0010 8494h	0010 A494h
8498h	A498h	CTRLMMR_MCAN6_CLKSEL	MCAN6 Clock Select Register	0010 8498h	0010 A498h
849Ch	A49Ch	CTRLMMR_MCAN7_CLKSEL	MCAN7 Clock Select Register	0010 849Ch	0010 A49Ch
84A0h	A4A0h	CTRLMMR_MCAN8_CLKSEL	MCAN8 Clock Select Register	0010 84A0h	0010 A4A0h
84A4h	A4A4h	CTRLMMR_MCAN9_CLKSEL	MCAN9 Clock Select Register	0010 84A4h	0010 A4A4h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
84A8h	A4A8h	CTRLMMR_MCAN10_CLKSEL	MCAN10 Clock Select Register	0010 84A8h	0010 A4A8h
84ACh	A4ACh	CTRLMMR_MCAN11_CLKSEL	MCAN11 Clock Select Register	0010 84ACh	0010 A4ACh
84B0h	A4B0h	CTRLMMR_MCAN12_CLKSEL	MCAN12 Clock Select Register	0010 84B0h	0010 A4B0h
84B4h	A4B4h	CTRLMMR_MCAN13_CLKSEL	MCAN13 Clock Select Register	0010 84B4h	0010 A4B4h
9008h	B008h	CTRLMMR_LOCK2_KICK0	Partition 2 Lock Key 0 Register	0010 9008h	0010 B008h
900Ch	B00Ch	CTRLMMR_LOCK2_KICK1	Partition 2 Lock Key 1 Register	0010 900Ch	0010 B00Ch
9100h	B100h	CTRLMMR_P2_CLAIM0	Partition 2 Claim Register 0	0010 9100h	0010 B100h
9104h	B104h	CTRLMMR_P2_CLAIM1	Partition 2 Claim Register 1	0010 9104h	0010 B104h
9108h	B108h	CTRLMMR_P2_CLAIM2	Partition 2 Claim Register 2	0010 9108h	0010 B108h
910Ch	B10Ch	CTRLMMR_P2_CLAIM3	Partition 2 Claim Register 3	0010 910Ch	0010 B10Ch
9110h	B110h	CTRLMMR_P2_CLAIM4	Partition 2 Claim Register 4	0010 9110h	0010 B110h
9114h	B114h	CTRLMMR_P2_CLAIM5	Partition 2 Claim Register 5	0010 9114h	0010 B114h
9118h	B118h	CTRLMMR_P2_CLAIM6	Partition 2 Claim Register 6	0010 9118h	0010 B118h
911Ch	B11Ch	CTRLMMR_P2_CLAIM7	Partition 2 Claim Register 7	0010 911Ch	0010 B11Ch
9120h	B120h	CTRLMMR_P2_CLAIM8	Partition 2 Claim Register 8	0010 9120h	0010 B120h
9124h	B124h	CTRLMMR_P2_CLAIM9	Partition 2 Claim Register 9	0010 9124h	0010 B124h
C000h	E000h	CTRLMMR_MCU0_LBIST_CTRL	SoC_Pulsar Logic BIST Control Register	0010 C000h	0010 E000h
C004h	E004h	CTRLMMR_MCU0_LBIST_PATCOUNT	SoC_Pulsar Logic BIST Pattern Count Register	0010 C004h	0010 E004h
C008h	E008h	CTRLMMR_MCU0_LBIST_SEED0	SoC_Pulsar Logic BIST Seed0 Register	0010 C008h	0010 E008h
C00Ch	E00Ch	CTRLMMR_MCU0_LBIST_SEED1	SoC_Pulsar Logic BIST Seed1 Register	0010 C00Ch	0010 E00Ch
C010h	E010h	CTRLMMR_MCU0_LBIST_SPARE0	SoC_Pulsar Logic BIST Spare0 Register	0010 C010h	0010 E010h
C014h	E014h	CTRLMMR_MCU0_LBIST_SPARE1	SoC_Pulsar Logic BIST Spare1 Register	0010 C014h	0010 E014h
C018h	E018h	CTRLMMR_MCU0_LBIST_STAT	SoC_Pulsar Logic BIST Status Register	0010 C018h	0010 E018h
C01Ch	E01Ch	CTRLMMR_MCU0_LBIST_MISR	SoC_Pulsar Logic BIST MISR Register	0010 C01Ch	0010 E01Ch
C020h	E020h	CTRLMMR_MCU1_LBIST_CTRL	SoC_Pulsar Logic BIST Control Register	0010 C020h	0010 E020h
C024h	E024h	CTRLMMR_MCU1_LBIST_PATCOUNT	SoC_Pulsar Logic BIST Pattern Count Register	0010 C024h	0010 E024h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
C028h	E028h	CTRLMMR_MCU1_LBIST_SEED0	SoC_Pulsar Logic BIST Seed0 Register	0010 C028h	0010 E028h
C02Ch	E02Ch	CTRLMMR_MCU1_LBIST_SEED1	SoC_Pulsar Logic BIST Seed1 Register	0010 C02Ch	0010 E02Ch
C030h	E030h	CTRLMMR_MCU1_LBIST_SPARE0	SoC_Pulsar Logic BIST Spare0 Register	0010 C030h	0010 E030h
C034h	E034h	CTRLMMR_MCU1_LBIST_SPARE1	SoC_Pulsar Logic BIST Spare1 Register	0010 C034h	0010 E034h
C038h	E038h	CTRLMMR_MCU1_LBIST_STAT	SoC_Pulsar Logic BIST Status Register	0010 C038h	0010 E038h
C03Ch	E03Ch	CTRLMMR_MCU1_LBIST_MISR	SoC_Pulsar Logic BIST MISR Register	0010 C03Ch	0010 E03Ch
C040h	E040h	CTRLMMR_DMPAC_LBIST_CTRL	DMPAC Logic BIST Control Register	0010 C040h	0010 E040h
C044h	E044h	CTRLMMR_DMPAC_LBIST_PATCOUNT	DMPAC Logic BIST Pattern Count Register	0010 C044h	0010 E044h
C048h	E048h	CTRLMMR_DMPAC_LBIST_SEED0	DMPAC Logic BIST Seed0 Register	0010 C048h	0010 E048h
C04Ch	E04Ch	CTRLMMR_DMPAC_LBIST_SEED1	DMPAC Logic BIST Seed1 Register	0010 C04Ch	0010 E04Ch
C050h	E050h	CTRLMMR_DMPAC_LBIST_SPARE0	DMPAC Logic BIST Spare0 Register	0010 C050h	0010 E050h
C054h	E054h	CTRLMMR_DMPAC_LBIST_SPARE1	DMPAC Logic BIST Spare1 Register	0010 C054h	0010 E054h
C058h	E058h	CTRLMMR_DMPAC_LBIST_STAT	DMPAC Logic BIST Status Register	0010 C058h	0010 E058h
C05Ch	E05Ch	CTRLMMR_DMPAC_LBIST_MISR	DMPAC Logic BIST MISR Register	0010 C05Ch	0010 E05Ch
C060h	E060h	CTRLMMR_VPAC_LBIST_CTRL	VPAC Logic BIST Control Register	0010 C060h	0010 E060h
C064h	E064h	CTRLMMR_VPAC_LBIST_PATCOUNT	VPAC Logic BIST Pattern Count Register	0010 C064h	0010 E064h
C068h	E068h	CTRLMMR_VPAC_LBIST_SEED0	VPAC Logic BIST Seed0 Register	0010 C068h	0010 E068h
C06Ch	E06Ch	CTRLMMR_VPAC_LBIST_SEED1	VPAC Logic BIST Seed1 Register	0010 C06Ch	0010 E06Ch
C070h	E070h	CTRLMMR_VPAC_LBIST_SPARE0	VPAC Logic BIST Spare0 Register	0010 C070h	0010 E070h
C074h	E074h	CTRLMMR_VPAC_LBIST_SPARE1	VPAC Logic BIST Spare1 Register	0010 C074h	0010 E074h
C078h	E078h	CTRLMMR_VPAC_LBIST_STAT	VPAC Logic BIST Status Register	0010 C078h	0010 E078h
C07Ch	E07Ch	CTRLMMR_VPAC_LBIST_MISR	VPAC Logic BIST MISR Register	0010 C07Ch	0010 E07Ch
C080h	E080h	CTRLMMR_DSP0_LBIST_CTRL	DSP Cluster0 Logic BIST Control Register	0010 C080h	0010 E080h
C084h	E084h	CTRLMMR_DSP0_LBIST_PATCOUNT	DSP Cluster0 Logic BIST Pattern Count Register	0010 C084h	0010 E084h
C088h	E088h	CTRLMMR_DSP0_LBIST_SEED0	DSP Cluster0 Logic BIST Seed0 Register	0010 C088h	0010 E088h
C08Ch	E08Ch	CTRLMMR_DSP0_LBIST_SEED1	DSP Cluster0 Logic BIST Seed1 Register	0010 C08Ch	0010 E08Ch

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
C090h	E090h	CTRLMMR_DSP0_LBIST_SPARE0	DSP Cluster0 Logic BIST Spare0 Register	0010 C090h	0010 E090h
C094h	E094h	CTRLMMR_DSP0_LBIST_SPARE1	DSP Cluster0 Logic BIST Spare1 Register	0010 C094h	0010 E094h
C098h	E098h	CTRLMMR_DSP0_LBIST_STAT	DSP Cluster0 Logic BIST Status Register	0010 C098h	0010 E098h
C09Ch	E09Ch	CTRLMMR_DSP0_LBIST_MISR	DSP Cluster0 Logic BIST MISR Register	0010 C09Ch	0010 E09Ch
C100h	E100h	CTRLMMR_MPU0_LBIST_CTRL	ARM Cluster0 Logic BIST Control Register	0010 C100h	0010 E100h
C104h	E104h	CTRLMMR_MPU0_LBIST_PATCOUNT	ARM Cluster0 Logic BIST Pattern Count Register	0010 C104h	0010 E104h
C108h	E108h	CTRLMMR_MPU0_LBIST_SEED0	ARM Cluster0 Logic BIST Seed0 Register	0010 C108h	0010 E108h
C10Ch	E10Ch	CTRLMMR_MPU0_LBIST_SEED1	ARM Cluster0 Logic BIST Seed1 Register	0010 C10Ch	0010 E10Ch
C110h	E110h	CTRLMMR_MPU0_LBIST_SPARE0	ARM Cluster0 Logic BIST Spare0 Register	0010 C110h	0010 E110h
C114h	E114h	CTRLMMR_MPU0_LBIST_SPARE1	ARM Cluster0 Logic BIST Spare1 Register	0010 C114h	0010 E114h
C118h	E118h	CTRLMMR_MPU0_LBIST_STAT	ARM Cluster0 Logic BIST Status Register	0010 C118h	0010 E118h
C11Ch	E11Ch	CTRLMMR_MPU0_LBIST_MISR	ARM Cluster0 Logic BIST MISR Register	0010 C11Ch	0010 E11Ch
C280h	E280h	CTRLMMR_MCU0_LBIST_SIG	MCU Cluster0 Logic BIST MISR Signature Register	0010 C280h	0010 E280h
C284h	E284h	CTRLMMR_MCU1_LBIST_SIG	MCU Cluster1 Logic BIST MISR Signature Register	0010 C284h	0010 E284h
C288h	E288h	CTRLMMR_DMPAC_LBIST_SIG	DMPAC Logic BIST MISR Signature Register	0010 C288h	0010 E288h
C28Ch	E28Ch	CTRLMMR_VPAC_LBIST_SIG	VPAC] Logic BIST MISR Signature Register	0010 C28Ch	0010 E28Ch
C290h	E290h	CTRLMMR_DSP0_LBIST_SIG	DSP0 Logic BIST MISR Signature Register	0010 C290h	0010 E290h
C2A0h	E2A0h	CTRLMMR_MPU0_LBIST_SIG	ARM Cluster0 Logic BIST MISR Signature Register	0010 C2A0h	0010 E2A0h
C320h	E320h	CTRLMMR_FUSE_CRC_STAT	MAIN eFUse CRC Status Register	0010 C320h	0010 E320h
D008h	F008h	CTRLMMR_LOCK3_KICK0	Partition 3 Lock Key 0 Register	0010 D008h	0010 F008h
D00Ch	F00Ch	CTRLMMR_LOCK3_KICK1	Partition 3 Lock Key 1 Register	0010 D00Ch	0010 F00Ch
D100h	F100h	CTRLMMR_P3_CLAIM0	Partition 3 Claim Register 0	0010 D100h	0010 F100h
D104h	F104h	CTRLMMR_P3_CLAIM1	Partition 3 Claim Register 1	0010 D104h	0010 F104h
D108h	F108h	CTRLMMR_P3_CLAIM2	Partition 3 Claim Register 2	0010 D108h	0010 F108h
D10Ch	F10Ch	CTRLMMR_P3_CLAIM3	Partition 3 Claim Register 3	0010 D10Ch	0010 F10Ch
D110h	F110h	CTRLMMR_P3_CLAIM4	Partition 3 Claim Register 4	0010 D110h	0010 F110h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
D114h	F114h	CTRLMMR_P3_CLAIM5	Partition 3 Claim Register 5	0010 D114h	0010 F114h
D118h	F118h	CTRLMMR_P3_CLAIM6	Partition 3 Claim Register 6	0010 D118h	0010 F118h
14000h	16000h	CTRLMMR_CHNG_DDR4_FSP_REQ	Change LPDDR4 FSP Request Register	0011 4000h	0011 6000h
14004h	16004h	CTRLMMR_CHNG_DDR4_FSP_ACK	Change LPDDR4 FSP Acknowledge Register	0011 4004h	0011 6004h
14080h	16080h	CTRLMMR_DDR4_FSP_CLKCHNG_REQ	LPDDR4 FSP Clock Change Request Register	0011 4080h	0011 6080h
140C0h	160C0h	CTRLMMR_DDR4_FSP_CLKCHNG_ACK	LPDDR4 FSP Clock Change Acknowledge Register	0011 40C0h	0011 60C0h
15008h	17008h	CTRLMMR_LOCK5_KICK0	Partition 5 Lock Key 0 Register	0011 5008h	0011 7008h
1500Ch	1700Ch	CTRLMMR_LOCK5_KICK1	Partition 5 Lock Key 1 Register	0011 500Ch	0011 700Ch
15100h	17100h	CTRLMMR_P5_CLAIM0	Partition 5 Claim Register 0	0011 5100h	0011 7100h
15104h	17104h	CTRLMMR_P5_CLAIM1	Partition 5 Claim Register 1	0011 5104h	0011 7104h
18090h	1A090h	CTRLMMR_ACSPCIE0_CTRL	ACSPCIE 0 Control Register	0011 8090h	0011 A090h
18094h	1A094h	CTRLMMR_ACSPCIE1_CTRL	ACSPCIE 1 Control Register	0011 8094h	0011 A094h
19008h	1B008h	CTRLMMR_LOCK6_KICK0	Partition 6 Lock Key 0 Register	0011 9008h	0011 B008h
1900Ch	1B00Ch	CTRLMMR_LOCK6_KICK1	Partition 6 Lock Key 1 Register	0011 900Ch	0011 B00Ch
19100h	1B100h	CTRLMMR_P6_CLAIM0	Partition 6 Claim Register 0	0011 9100h	0011 B100h
19104h	1B104h	CTRLMMR_P6_CLAIM1	Partition 6 Claim Register 1	0011 9104h	0011 B104h
1C000h	1E000h	CTRLMMR_PADCONFIG0	PAD Configuration Register 0	0011 C000h	0011 E000h
1C004h	1E004h	CTRLMMR_PADCONFIG1	PAD Configuration Register 1	0011 C004h	0011 E004h
1C008h	1E008h	CTRLMMR_PADCONFIG2	PAD Configuration Register 2	0011 C008h	0011 E008h
1C00Ch	1E00Ch	CTRLMMR_PADCONFIG3	PAD Configuration Register 3	0011 C00Ch	0011 E00Ch
1C010h	1E010h	CTRLMMR_PADCONFIG4	PAD Configuration Register 4	0011 C010h	0011 E010h
1C014h	1E014h	CTRLMMR_PADCONFIG5	PAD Configuration Register 5	0011 C014h	0011 E014h
1C018h	1E018h	CTRLMMR_PADCONFIG6	PAD Configuration Register 6	0011 C018h	0011 E018h
1C01Ch	1E01Ch	CTRLMMR_PADCONFIG7	PAD Configuration Register 7	0011 C01Ch	0011 E01Ch
1C020h	1E020h	CTRLMMR_PADCONFIG8	PAD Configuration Register 8	0011 C020h	0011 E020h
1C024h	1E024h	CTRLMMR_PADCONFIG9	PAD Configuration Register 9	0011 C024h	0011 E024h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
1C028h	1E028h	CTRLMMR_PADCONFIG10	PAD Configuration Register 10	0011 C028h	0011 E028h
1C02Ch	1E02Ch	CTRLMMR_PADCONFIG11	PAD Configuration Register 11	0011 C02Ch	0011 E02Ch
1C030h	1E030h	CTRLMMR_PADCONFIG12	PAD Configuration Register 12	0011 C030h	0011 E030h
1C034h	1E034h	CTRLMMR_PADCONFIG13	PAD Configuration Register 13	0011 C034h	0011 E034h
1C038h	1E038h	CTRLMMR_PADCONFIG14	PAD Configuration Register 14	0011 C038h	0011 E038h
1C03Ch	1E03Ch	CTRLMMR_PADCONFIG15	PAD Configuration Register 15	0011 C03Ch	0011 E03Ch
1C040h	1E040h	CTRLMMR_PADCONFIG16	PAD Configuration Register 16	0011 C040h	0011 E040h
1C044h	1E044h	CTRLMMR_PADCONFIG17	PAD Configuration Register 17	0011 C044h	0011 E044h
1C048h	1E048h	CTRLMMR_PADCONFIG18	PAD Configuration Register 18	0011 C048h	0011 E048h
1C04Ch	1E04Ch	CTRLMMR_PADCONFIG19	PAD Configuration Register 19	0011 C04Ch	0011 E04Ch
1C050h	1E050h	CTRLMMR_PADCONFIG20	PAD Configuration Register 20	0011 C050h	0011 E050h
1C054h	1E054h	CTRLMMR_PADCONFIG21	PAD Configuration Register 21	0011 C054h	0011 E054h
1C058h	1E058h	CTRLMMR_PADCONFIG22	PAD Configuration Register 22	0011 C058h	0011 E058h
1C05Ch	1E05Ch	CTRLMMR_PADCONFIG23	PAD Configuration Register 23	0011 C05Ch	0011 E05Ch
1C060h	1E060h	CTRLMMR_PADCONFIG24	PAD Configuration Register 24	0011 C060h	0011 E060h
1C064h	1E064h	CTRLMMR_PADCONFIG25	PAD Configuration Register 25	0011 C064h	0011 E064h
1C068h	1E068h	CTRLMMR_PADCONFIG26	PAD Configuration Register 26	0011 C068h	0011 E068h
1C06Ch	1E06Ch	CTRLMMR_PADCONFIG27	PAD Configuration Register 27	0011 C06Ch	0011 E06Ch
1C070h	1E070h	CTRLMMR_PADCONFIG28	PAD Configuration Register 28	0011 C070h	0011 E070h
1C074h	1E074h	CTRLMMR_PADCONFIG29	PAD Configuration Register 29	0011 C074h	0011 E074h
1C078h	1E078h	CTRLMMR_PADCONFIG30	PAD Configuration Register 30	0011 C078h	0011 E078h
1C07Ch	1E07Ch	CTRLMMR_PADCONFIG31	PAD Configuration Register 31	0011 C07Ch	0011 E07Ch
1C080h	1E080h	CTRLMMR_PADCONFIG32	PAD Configuration Register 32	0011 C080h	0011 E080h
1C084h	1E084h	CTRLMMR_PADCONFIG33	PAD Configuration Register 33	0011 C084h	0011 E084h
1C088h	1E088h	CTRLMMR_PADCONFIG34	PAD Configuration Register 34	0011 C088h	0011 E088h
1C08Ch	1E08Ch	CTRLMMR_PADCONFIG35	PAD Configuration Register 35	0011 C08Ch	0011 E08Ch

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
1C090h	1E090h	CTRLMMR_PADCONFIG36	PAD Configuration Register 36	0011 C090h	0011 E090h
1C094h	1E094h	CTRLMMR_PADCONFIG37	PAD Configuration Register 37	0011 C094h	0011 E094h
1C098h	1E098h	CTRLMMR_PADCONFIG38	PAD Configuration Register 38	0011 C098h	0011 E098h
1C09Ch	1E09Ch	CTRLMMR_PADCONFIG39	PAD Configuration Register 39	0011 C09Ch	0011 E09Ch
1C0A0h	1E0A0h	CTRLMMR_PADCONFIG40	PAD Configuration Register 40	0011 C0A0h	0011 E0A0h
1C0A4h	1E0A4h	CTRLMMR_PADCONFIG41	PAD Configuration Register 41	0011 C0A4h	0011 E0A4h
1C0A8h	1E0A8h	CTRLMMR_PADCONFIG42	PAD Configuration Register 42	0011 C0A8h	0011 E0A8h
1C0ACh	1E0ACh	CTRLMMR_PADCONFIG43	PAD Configuration Register 43	0011 C0ACh	0011 E0ACh
1C0B0h	1E0B0h	CTRLMMR_PADCONFIG44	PAD Configuration Register 44	0011 C0B0h	0011 E0B0h
1C0B4h	1E0B4h	CTRLMMR_PADCONFIG45	PAD Configuration Register 45	0011 C0B4h	0011 E0B4h
1C0B8h	1E0B8h	CTRLMMR_PADCONFIG46	PAD Configuration Register 46	0011 C0B8h	0011 E0B8h
1C0BCh	1E0BCh	CTRLMMR_PADCONFIG47	PAD Configuration Register 47	0011 C0BCh	0011 E0BCh
1C0C0h	1E0C0h	CTRLMMR_PADCONFIG48	PAD Configuration Register 48	0011 C0C0h	0011 E0C0h
1C0C4h	1E0C4h	CTRLMMR_PADCONFIG49	PAD Configuration Register 49	0011 C0C4h	0011 E0C4h
1C0C8h	1E0C8h	CTRLMMR_PADCONFIG50	PAD Configuration Register 50	0011 C0C8h	0011 E0C8h
1C0CCh	1E0CCh	CTRLMMR_PADCONFIG51	PAD Configuration Register 51	0011 C0CCh	0011 E0CCh
1C0D0h	1E0D0h	CTRLMMR_PADCONFIG52	PAD Configuration Register 52	0011 C0D0h	0011 E0D0h
1C0D4h	1E0D4h	CTRLMMR_PADCONFIG53	PAD Configuration Register 53	0011 C0D4h	0011 E0D4h
1C0D8h	1E0D8h	CTRLMMR_PADCONFIG54	PAD Configuration Register 54	0011 C0D8h	0011 E0D8h
1C0DCh	1E0DCh	CTRLMMR_PADCONFIG55	PAD Configuration Register 55	0011 C0DCh	0011 E0DCh
1C0E0h	1E0E0h	CTRLMMR_PADCONFIG56	PAD Configuration Register 56	0011 C0E0h	0011 E0E0h
1C0E4h	1E0E4h	CTRLMMR_PADCONFIG57	PAD Configuration Register 57	0011 C0E4h	0011 E0E4h
1C0E8h	1E0E8h	CTRLMMR_PADCONFIG58	PAD Configuration Register 58	0011 C0E8h	0011 E0E8h
1C0ECh	1E0ECh	CTRLMMR_PADCONFIG59	PAD Configuration Register 59	0011 C0ECh	0011 E0ECh
1C0F0h	1E0F0h	CTRLMMR_PADCONFIG60	PAD Configuration Register 60	0011 C0F0h	0011 E0F0h
1C0F4h	1E0F4h	CTRLMMR_PADCONFIG61	PAD Configuration Register 61	0011 C0F4h	0011 E0F4h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
1C0F8h	1E0F8h	CTRLMMR_PADCONFIG62	PAD Configuration Register 62	0011 C0F8h	0011 E0F8h
1C0FCh	1E0FCh	CTRLMMR_PADCONFIG63	PAD Configuration Register 63	0011 C0FCh	0011 E0FCh
1C100h	1E100h	CTRLMMR_PADCONFIG64	PAD Configuration Register 64	0011 C100h	0011 E100h
1C104h	1E104h	CTRLMMR_PADCONFIG65	PAD Configuration Register 65	0011 C104h	0011 E104h
1C108h	1E108h	CTRLMMR_PADCONFIG66	PAD Configuration Register 66	0011 C108h	0011 E108h
1C10Ch	1E10Ch	CTRLMMR_PADCONFIG67	PAD Configuration Register 67	0011 C10Ch	0011 E10Ch
1C110h	1E110h	CTRLMMR_PADCONFIG68	PAD Configuration Register 68	0011 C110h	0011 E110h
1C114h	1E114h	CTRLMMR_PADCONFIG69	PAD Configuration Register 69	0011 C114h	0011 E114h
1C118h	1E118h	CTRLMMR_PADCONFIG70	PAD Configuration Register 70	0011 C118h	0011 E118h
1C11Ch	1E11Ch	CTRLMMR_PADCONFIG71	PAD Configuration Register 71	0011 C11Ch	0011 E11Ch
1C120h	1E120h	CTRLMMR_PADCONFIG72	PAD Configuration Register 72	0011 C120h	0011 E120h
1C124h	1E124h	CTRLMMR_PADCONFIG73	PAD Configuration Register 73	0011 C124h	0011 E124h
1C128h	1E128h	CTRLMMR_PADCONFIG74	PAD Configuration Register 74	0011 C128h	0011 E128h
1C12Ch	1E12Ch	CTRLMMR_PADCONFIG75	PAD Configuration Register 75	0011 C12Ch	0011 E12Ch
1C130h	1E130h	CTRLMMR_PADCONFIG76	PAD Configuration Register 76	0011 C130h	0011 E130h
1C134h	1E134h	CTRLMMR_PADCONFIG77	PAD Configuration Register 77	0011 C134h	0011 E134h
1C138h	1E138h	CTRLMMR_PADCONFIG78	PAD Configuration Register 78	0011 C138h	0011 E138h
1C13Ch	1E13Ch	CTRLMMR_PADCONFIG79	PAD Configuration Register 79	0011 C13Ch	0011 E13Ch
1C140h	1E140h	CTRLMMR_PADCONFIG80	PAD Configuration Register 80	0011 C140h	0011 E140h
1C144h	1E144h	CTRLMMR_PADCONFIG81	PAD Configuration Register 81	0011 C144h	0011 E144h
1C148h	1E148h	CTRLMMR_PADCONFIG82	PAD Configuration Register 82	0011 C148h	0011 E148h
1C14Ch	1E14Ch	CTRLMMR_PADCONFIG83	PAD Configuration Register 83	0011 C14Ch	0011 E14Ch
1C150h	1E150h	CTRLMMR_PADCONFIG84	PAD Configuration Register 84	0011 C150h	0011 E150h
1C154h	1E154h	CTRLMMR_PADCONFIG85	PAD Configuration Register 85	0011 C154h	0011 E154h
1C158h	1E158h	CTRLMMR_PADCONFIG86	PAD Configuration Register 86	0011 C158h	0011 E158h
1C15Ch	1E15Ch	CTRLMMR_PADCONFIG87	PAD Configuration Register 87	0011 C15Ch	0011 E15Ch

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
1C160h	1E160h	CTRLMMR_PADCONFIG88	PAD Configuration Register 88	0011 C160h	0011 E160h
1C164h	1E164h	CTRLMMR_PADCONFIG89	PAD Configuration Register 89	0011 C164h	0011 E164h
1C168h	1E168h	CTRLMMR_PADCONFIG90	PAD Configuration Register 90	0011 C168h	0011 E168h
1C16Ch	1E16Ch	CTRLMMR_PADCONFIG91	PAD Configuration Register 91	0011 C16Ch	0011 E16Ch
1C170h	1E170h	CTRLMMR_PADCONFIG92	PAD Configuration Register 92	0011 C170h	0011 E170h
1C174h	1E174h	CTRLMMR_PADCONFIG93	PAD Configuration Register 93	0011 C174h	0011 E174h
1C178h	1E178h	CTRLMMR_PADCONFIG94	PAD Configuration Register 94	0011 C178h	0011 E178h
1C17Ch	1E17Ch	CTRLMMR_PADCONFIG95	PAD Configuration Register 95	0011 C17Ch	0011 E17Ch
1C180h	1E180h	CTRLMMR_PADCONFIG96	PAD Configuration Register 96	0011 C180h	0011 E180h
1C184h	1E184h	CTRLMMR_PADCONFIG97	PAD Configuration Register 97	0011 C184h	0011 E184h
1C188h	1E188h	CTRLMMR_PADCONFIG98	PAD Configuration Register 98	0011 C188h	0011 E188h
1C18Ch	1E18Ch	CTRLMMR_PADCONFIG99	PAD Configuration Register 99	0011 C18Ch	0011 E18Ch
1C190h	1E190h	CTRLMMR_PADCONFIG100	PAD Configuration Register 100	0011 C190h	0011 E190h
1C194h	1E194h	CTRLMMR_PADCONFIG101	PAD Configuration Register 101	0011 C194h	0011 E194h
1C198h	1E198h	CTRLMMR_PADCONFIG102	PAD Configuration Register 102	0011 C198h	0011 E198h
1C19Ch	1E19Ch	CTRLMMR_PADCONFIG103	PAD Configuration Register 103	0011 C19Ch	0011 E19Ch
1C1A0h	1E1A0h	CTRLMMR_PADCONFIG104	PAD Configuration Register 104	0011 C1A0h	0011 E1A0h
1C1A4h	1E1A4h	CTRLMMR_PADCONFIG105	PAD Configuration Register 105	0011 C1A4h	0011 E1A4h
1C1A8h	1E1A8h	CTRLMMR_PADCONFIG106	PAD Configuration Register 106	0011 C1A8h	0011 E1A8h
1C1ACh	1E1ACh	CTRLMMR_PADCONFIG107	PAD Configuration Register 107	0011 C1ACh	0011 E1ACh
1C1B0h	1E1B0h	CTRLMMR_PADCONFIG108	PAD Configuration Register 108	0011 C1B0h	0011 E1B0h
1C1B4h	1E1B4h	CTRLMMR_PADCONFIG109	PAD Configuration Register 109	0011 C1B4h	0011 E1B4h
1C1B8h	1E1B8h	CTRLMMR_PADCONFIG110	PAD Configuration Register 110	0011 C1B8h	0011 E1B8h
1C1BCh	1E1BCh	CTRLMMR_PADCONFIG111	PAD Configuration Register 111	0011 C1BCh	0011 E1BCh
1C1C0h	1E1C0h	CTRLMMR_PADCONFIG112	PAD Configuration Register 112	0011 C1C0h	0011 E1C0h
1C1C4h	1E1C4h	CTRLMMR_PADCONFIG113	PAD Configuration Register 113	0011 C1C4h	0011 E1C4h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
1C1C8h	1E1C8h	CTRLMMR_PADCONFIG114	PAD Configuration Register 114	0011 C1C8h	0011 E1C8h
1C1CCh	1E1CCh	CTRLMMR_PADCONFIG115	PAD Configuration Register 115	0011 C1CCh	0011 E1CCh
1C1D0h	1E1D0h	CTRLMMR_PADCONFIG116	PAD Configuration Register 116	0011 C1D0h	0011 E1D0h
1C1D4h	1E1D4h	CTRLMMR_PADCONFIG117	PAD Configuration Register 117	0011 C1D4h	0011 E1D4h
1C1D8h	1E1D8h	CTRLMMR_PADCONFIG118	PAD Configuration Register 118	0011 C1D8h	0011 E1D8h
1C1DCh	1E1DCh	CTRLMMR_PADCONFIG119	PAD Configuration Register 119	0011 C1DCh	0011 E1DCh
1C1E0h	1E1E0h	CTRLMMR_PADCONFIG120	PAD Configuration Register 120	0011 C1E0h	0011 E1E0h
1C1E4h	1E1E4h	CTRLMMR_PADCONFIG121	PAD Configuration Register 121	0011 C1E4h	0011 E1E4h
1C1E8h	1E1E8h	CTRLMMR_PADCONFIG122	PAD Configuration Register 122	0011 C1E8h	0011 E1E8h
1C1ECh	1E1ECh	CTRLMMR_PADCONFIG123	PAD Configuration Register 123	0011 C1ECh	0011 E1ECh
1C1F0h	1E1F0h	CTRLMMR_PADCONFIG124	PAD Configuration Register 124	0011 C1F0h	0011 E1F0h
1C1F4h	1E1F4h	CTRLMMR_PADCONFIG125	PAD Configuration Register 125	0011 C1F4h	0011 E1F4h
1C1F8h	1E1F8h	CTRLMMR_PADCONFIG126	PAD Configuration Register 126	0011 C1F8h	0011 E1F8h
1C1FCh	1E1FCh	CTRLMMR_PADCONFIG127	PAD Configuration Register 127	0011 C1FCh	0011 E1FCh
1C200h	1E200h	CTRLMMR_PADCONFIG128	PAD Configuration Register 128	0011 C200h	0011 E200h
1C204h	1E204h	CTRLMMR_PADCONFIG129	PAD Configuration Register 129	0011 C204h	0011 E204h
1C208h	1E208h	CTRLMMR_PADCONFIG130	PAD Configuration Register 130	0011 C208h	0011 E208h
1C20Ch	1E20Ch	CTRLMMR_PADCONFIG131	PAD Configuration Register 131	0011 C20Ch	0011 E20Ch
1C210h	1E210h	CTRLMMR_PADCONFIG132	PAD Configuration Register 132	0011 C210h	0011 E210h
1C214h	1E214h	CTRLMMR_PADCONFIG133	PAD Configuration Register 133	0011 C214h	0011 E214h
1C218h	1E218h	CTRLMMR_PADCONFIG134	PAD Configuration Register 134	0011 C218h	0011 E218h
1C21Ch	1E21Ch	CTRLMMR_PADCONFIG135	PAD Configuration Register 135	0011 C21Ch	0011 E21Ch
1C220h	1E220h	CTRLMMR_PADCONFIG136	PAD Configuration Register 136	0011 C220h	0011 E220h
1C224h	1E224h	CTRLMMR_PADCONFIG137	PAD Configuration Register 137	0011 C224h	0011 E224h
1C228h	1E228h	CTRLMMR_PADCONFIG138	PAD Configuration Register 138	0011 C228h	0011 E228h
1C22Ch	1E22Ch	CTRLMMR_PADCONFIG139	PAD Configuration Register 139	0011 C22Ch	0011 E22Ch

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
1C230h	1E230h	CTRLMMR_PADCONFIG140	PAD Configuration Register 140	0011 C230h	0011 E230h
1C234h	1E234h	CTRLMMR_PADCONFIG141	PAD Configuration Register 141	0011 C234h	0011 E234h
1C238h	1E238h	CTRLMMR_PADCONFIG142	PAD Configuration Register 142	0011 C238h	0011 E238h
1C23Ch	1E23Ch	CTRLMMR_PADCONFIG143	PAD Configuration Register 143	0011 C23Ch	0011 E23Ch
1C240h	1E240h	CTRLMMR_PADCONFIG144	PAD Configuration Register 144	0011 C240h	0011 E240h
1C244h	1E244h	CTRLMMR_PADCONFIG145	PAD Configuration Register 145	0011 C244h	0011 E244h
1C248h	1E248h	CTRLMMR_PADCONFIG146	PAD Configuration Register 146	0011 C248h	0011 E248h
1C24Ch	1E24Ch	CTRLMMR_PADCONFIG147	PAD Configuration Register 147	0011 C24Ch	0011 E24Ch
1C250h	1E250h	CTRLMMR_PADCONFIG148	PAD Configuration Register 148	0011 C250h	0011 E250h
1C254h	1E254h	CTRLMMR_PADCONFIG149	PAD Configuration Register 149	0011 C254h	0011 E254h
1C258h	1E258h	CTRLMMR_PADCONFIG150	PAD Configuration Register 150	0011 C258h	0011 E258h
1C25Ch	1E25Ch	CTRLMMR_PADCONFIG151	PAD Configuration Register 151	0011 C25Ch	0011 E25Ch
1C260h	1E260h	CTRLMMR_PADCONFIG152	PAD Configuration Register 152	0011 C260h	0011 E260h
1C264h	1E264h	CTRLMMR_PADCONFIG153	PAD Configuration Register 153	0011 C264h	0011 E264h
1C268h	1E268h	CTRLMMR_PADCONFIG154	PAD Configuration Register 154	0011 C268h	0011 E268h
1C26Ch	1E26Ch	CTRLMMR_PADCONFIG155	PAD Configuration Register 155	0011 C26Ch	0011 E26Ch
1C270h	1E270h	CTRLMMR_PADCONFIG156	PAD Configuration Register 156	0011 C270h	0011 E270h
1C274h	1E274h	CTRLMMR_PADCONFIG157	PAD Configuration Register 157	0011 C274h	0011 E274h
1C278h	1E278h	CTRLMMR_PADCONFIG158	PAD Configuration Register 158	0011 C278h	0011 E278h
1C27Ch	1E27Ch	CTRLMMR_PADCONFIG159	PAD Configuration Register 159	0011 C27Ch	0011 E27Ch
1C280h	1E280h	CTRLMMR_PADCONFIG160	PAD Configuration Register 160	0011 C280h	0011 E280h
1C284h	1E284h	CTRLMMR_PADCONFIG161	PAD Configuration Register 161	0011 C284h	0011 E284h
1C288h	1E288h	CTRLMMR_PADCONFIG162	PAD Configuration Register 162	0011 C288h	0011 E288h
1C28Ch	1E28Ch	CTRLMMR_PADCONFIG163	PAD Configuration Register 163	0011 C28Ch	0011 E28Ch
1C290h	1E290h	CTRLMMR_PADCONFIG164	PAD Configuration Register 164	0011 C290h	0011 E290h
1C294h	1E294h	CTRLMMR_PADCONFIG165	PAD Configuration Register 165	0011 C294h	0011 E294h

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Table 6-2. CTRL_MMR0 Registers (continued)

Proxy0 Offset	Proxy1 Offset	Acronym	Register Name	CTRL_MMR0 Proxy0 Physical Address	CTRL_MMR0 Proxy1 Physical Address
1C298h	1E298h	CTRLMMR_PADCONFIG166	PAD Configuration Register 166	0011 C298h	0011 E298h
1C29Ch	1E29Ch	CTRLMMR_PADCONFIG167	PAD Configuration Register 167	0011 C29Ch	0011 E29Ch
1C2A0h	1E2A0h	CTRLMMR_PADCONFIG168	PAD Configuration Register 168	0011 C2A0h	0011 E2A0h
1C2A4h	1E2A4h	CTRLMMR_PADCONFIG169	PAD Configuration Register 169	0011 C2A4h	0011 E2A4h
1C2A8h	1E2A8h	CTRLMMR_PADCONFIG170	PAD Configuration Register 170	0011 C2A8h	0011 E2A8h
1C2ACh	1E2ACh	CTRLMMR_PADCONFIG171	PAD Configuration Register 171	0011 C2ACh	0011 E2ACh
1C2B0h	1E2B0h	CTRLMMR_PADCONFIG172	PAD Configuration Register 172	0011 C2B0h	0011 E2B0h
1D008h	1F008h	CTRLMMR_LOCK7_KICK0	Partition 7 Lock Key 0 Register	0011 D008h	0011 F008h
1D00Ch	1F00Ch	CTRLMMR_LOCK7_KICK1	Partition 7 Lock Key 1 Register	0011 D00Ch	0011 F00Ch
1D100h	1F100h	CTRLMMR_P7_CLAIM0	Partition 7 Claim Register 0	0011 D100h	0011 F100h
1D104h	1F104h	CTRLMMR_P7_CLAIM1	Partition 7 Claim Register 1	0011 D104h	0011 F104h
1D108h	1F108h	CTRLMMR_P7_CLAIM2	Partition 7 Claim Register 2	0011 D108h	0011 F108h
1D10Ch	1F10Ch	CTRLMMR_P7_CLAIM3	Partition 7 Claim Register 3	0011 D10Ch	0011 F10Ch
1D110h	1F110h	CTRLMMR_P7_CLAIM4	Partition 7 Claim Register 4	0011 D110h	0011 F110h
1D114h	1F114h	CTRLMMR_P7_CLAIM5	Partition 7 Claim Register 5	0011 D114h	0011 F114h

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6.1 CTRLMMR_PID Register (Proxy0 Offset = 0h; Proxy1 Offset = 2000h) [reset = 61800000h]

CTRLMMR_PID is shown in Figure 6-1 and described in Table 6-4.

Return to Summary Table.

Peripheral release details.

Table 6-3. CTRLMMR_PID Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0000h	0010 2000h

Figure 6-1. CTRLMMR_PID Register

31	30	29	28	27	26	25	24
SCHEME		BU		FUNC			
R-1h		R-2h		R-180h			
23	22	21	20	19	18	17	16
FUNC							
R-180h							
15	14	13	12	11	10	9	8
R_RTL					X_MAJOR		
R-0h					R-0h		
7	6	5	4	3	2	1	0
CUSTOM		Y_MINOR					
R-0h		R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 6-4. CTRLMMR_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	Business unit
27-16	FUNC	R	180h	Module functional identifier
15-11	R_RTL	R	0h	RTL revision
10-8	X_MAJOR	R	0h	Major revision
7-6	CUSTOM	R	0h	Custom revision
5-0	Y_MINOR	R	0h	Minor revision

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6.2 CTRLMMR_MMR_CFG1 Register (Proxy0 Offset = 8h; Proxy1 Offset = 2008h) [reset = 8000009Fh]

CTRLMMR_MMR_CFG1 is shown in Figure 6-2 and described in Table 6-6.

Return to Summary Table.

Indicates the MMR configuration.

Table 6-5. CTRLMMR_MMR_CFG1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0008h	0010 2008h

Figure 6-2. CTRLMMR_MMR_CFG1 Register

31	30	29	28	27	26	25	24
PROXY_EN	RESERVED						
R-1h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
PARTITIONS							
R-9Fh							

LEGEND: R = Read Only; *-n* = value after reset

Table 6-6. CTRLMMR_MMR_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PROXY_EN	R	1h	Proxy addressing enabled
30-8	RESERVED	R	0h	Reserved
7-0	PARTITIONS	R	9Fh	Indicates present partitions

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6.3 CTRLMMR_MAIN_DEVSTAT Register (Proxy0 Offset = 30h; Proxy1 Offset = 2030h) [reset = X]

CTRLMMR_MAIN_DEVSTAT is shown in Figure 6-3 and described in Table 6-8.

Return to Summary Table.

Indicates SoC bootstrap selection. The default value of this register is determined by the SoC bootstrap pins when the por_boot_cfg_srst_n input is de-asserted. Note that this register will not be valid when returning from Deepsleep powerdown modes as the bootstrap pins are not relatched in this scenario.

Table 6-7. CTRLMMR_MAIN_DEVSTAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0030h	0010 2030h

Figure 6-3. CTRLMMR_MAIN_DEVSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BOOTMODE							
R-0h																								R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-8. CTRLMMR_MAIN_DEVSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	BOOTMODE	R/W	X	Specifies the device Primary and Backup boot media.

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6.4 CTRLMMR_MAIN_BOOTCFG Register (Proxy0 Offset = 34h; Proxy1 Offset = 2034h) [reset = X]

CTRLMMR_MAIN_BOOTCFG is shown in Figure 6-4 and described in Table 6-10.

Return to Summary Table.

Indicates SoC bootstrap selection latched at power-on reset by PORz. The default value of this register is determined by the SoC bootstrap pins when the MMR por_boot_cfg_srst_n input is de-asserted and will remain until the SOC bootstrap pins are re-latched on a subsequent MMR por_boot_cfg_srst_n rising edge. Note that this register will not be valid when returning from Deepsleep powerdown modes as the bootstrap pins are not relatched in this scenario.

Table 6-9. CTRLMMR_MAIN_BOOTCFG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0034h	0010 2034h

Figure 6-4. CTRLMMR_MAIN_BOOTCFG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								BOOTMODE							
R-0h																								R-X							

LEGEND: R = Read Only; *-n* = value after reset

Table 6-10. CTRLMMR_MAIN_BOOTCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	BOOTMODE	R	X	Specifies the device Primary and Backup boot media.

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6.5 CTRLMMR_MAIN_FEATURE_STAT0 Register (Proxy0 Offset = 40h; Proxy1 Offset = 2040h) [reset = X]

CTRLMMR_MAIN_FEATURE_STAT0 is shown in Figure 6-5 and described in Table 6-12.

Return to Summary Table.

Indicates enable status of MAIN domain IP features.

Table 6-11. CTRLMMR_MAIN_FEATURE_STAT0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0040h	0010 2040h

Figure 6-5. CTRLMMR_MAIN_FEATURE_STAT0 Register

31	30	29	28	27	26	25	24
RESERVED							UFS_AES_DIS
R-0h							R-X
23	22	21	20	19	18	17	16
RESERVED			EDP0_CRYPTO_DIS	RESERVED	CRYPTO_PKA_DIS	CRYPTO_ENCR_DIS	CRYPTO_SHA_DIS
R-0h			R-X	R-0h	R-X	R-X	R-X
15	14	13	12	11	10	9	8
RESERVED						DMPAC_SDE_DIS	DMPAC_DOF_DIS
R-0h						R-X	R-X
7	6	5	4	3	2	1	0
RESERVED						RESERVED	RESERVED
R-0h						R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 6-12. CTRLMMR_MAIN_FEATURE_STAT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	UFS_AES_DIS	R	X	AES disabled on UFS
23-21	RESERVED	R	0h	Reserved
20	EDP0_CRYPTO_DIS	R	X	HDCP Cryptography disabled on eDP0
19	RESERVED	R	0h	Reserved
18	CRYPTO_PKA_DIS	R	X	SA2_UL Crypto Module PKA disabled
17	CRYPTO_ENCR_DIS	R	X	SA2_UL Crypto Module AES/3DES/DBRG disabled
16	CRYPTO_SHA_DIS	R	X	SA2_UL Crypto Module SHA/MD5 disabled
15-10	RESERVED	R	0h	Reserved
9	DMPAC_SDE_DIS	R	X	DMPAC Stereo Disparity Engine disabled
8	DMPAC_DOF_DIS	R	X	DMPAC Dense Optical Flow disabled
7-2	RESERVED	R	0h	Reserved
1	RESERVED	R	X	Reserved
0	RESERVED	R	X	Reserved

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6.6 CTRLMMR_MAIN_FEATURE_STAT1 Register (Proxy0 Offset = 44h; Proxy1 Offset = 2044h) [reset = X]

CTRLMMR_MAIN_FEATURE_STAT1 is shown in Figure 6-6 and described in Table 6-14.

Return to Summary Table.

Indicates enable status of MAIN domain IP features.

Table 6-13. CTRLMMR_MAIN_FEATURE_STAT1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0044h	0010 2044h

Figure 6-6. CTRLMMR_MAIN_FEATURE_STAT1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							MCAN_FD_EN
R-0h							R-X
15	14	13	12	11	10	9	8
GPU_ASTC_EN	RESERVED			DEC_VP8_EN	DEC_VP6_EN	DEC_RV_EN	DEC_SOREN_EN
R-X	R-0h			R-X	R-X	R-X	R-X
7	6	5	4	3	2	1	0
DEC_AVS_EN	DEC_MPEG4_EN	DEC_MPEG2_EN	DEC_MPEG1_EN	DEC_WMV9_EN	DEC_VC1_EN	DEC_HEVC_EN	DEC_H264_EN
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 6-14. CTRLMMR_MAIN_FEATURE_STAT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MCAN_FD_EN	R	X	FD mode is supported on MAIN MCAN interfaces when set
15	GPU_ASTC_EN	R	X	GPU Adaptive Scalable Texture Compression is supported when set
14-12	RESERVED	R	0h	Reserved
11	DEC_VP8_EN	R	X	VP8 Video decode is enabled when set
10	DEC_VP6_EN	R	X	VP6 Video decode is enabled when set
9	DEC_RV_EN	R	X	RealVideo Video decode is enabled when set
8	DEC_SOREN_EN	R	X	Sorenson Video decode is enabled when set
7	DEC_AVS_EN	R	X	AVS Video decode is enabled when set
6	DEC_MPEG4_EN	R	X	MPEG4 Video decode is enabled when set
5	DEC_MPEG2_EN	R	X	MPEG2 Video decode is enabled when set
4	DEC_MPEG1_EN	R	X	MPEG1 Video decode is enabled when set
3	DEC_WMV9_EN	R	X	WMV9 Video decode is enabled when set
2	DEC_VC1_EN	R	X	VC-1 (SMPTE 421M) Video decode is enabled when set
1	DEC_HEVC_EN	R	X	HEVC (H.265) Video decode is enabled when set

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Table 6-14. CTRLMMR_MAIN_FEATURE_STAT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DEC_H264_EN	R	X	H.264 Video decode is enabled when set

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6.7 CTRLMMR_IPC_SET0 Register (Proxy0 Offset = 100h; Proxy1 Offset = 2100h) [reset = 0h]

CTRLMMR_IPC_SET0 is shown in Figure 6-7 and described in Table 6-16.

Return to Summary Table.

Generate interprocessor communication interrupt to C71x core0.

Table 6-15. CTRLMMR_IPC_SET0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0100 0100h	0100 2100h

Figure 6-7. CTRLMMR_IPC_SET0 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-16. CTRLMMR_IPC_SET0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.8 CTRLMMR_IPC_SET6 Register (Proxy0 Offset = 118h; Proxy1 Offset = 2118h) [reset = 0h]

CTRLMMR_IPC_SET6 is shown in Figure 6-8 and described in Table 6-18.

Return to Summary Table.

Generate interprocessor communication interrupt to C66 core0.

Table 6-17. CTRLMMR_IPC_SET6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0118h	0010 2118h

Figure 6-8. CTRLMMR_IPC_SET6 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-18. CTRLMMR_IPC_SET6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.9 CTRLMMR_IPC_SET7 Register (Proxy0 Offset = 11Ch; Proxy1 Offset = 211Ch) [reset = 0h]

CTRLMMR_IPC_SET7 is shown in Figure 6-9 and described in Table 6-20.

Return to Summary Table.

Generate interprocessor communication interrupt to C66 core1.

Table 6-19. CTRLMMR_IPC_SET7 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 011Ch	0010 211Ch

Figure 6-9. CTRLMMR_IPC_SET7 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-20. CTRLMMR_IPC_SET7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.10 CTRLMMR_IPC_SET8 Register (Proxy0 Offset = 120h; Proxy1 Offset = 2120h) [reset = 0h]

CTRLMMR_IPC_SET8 is shown in Figure 6-10 and described in Table 6-22.

Return to Summary Table.

Generate interprocessor communication interrupt to ARM MPU core0.

Table 6-21. CTRLMMR_IPC_SET8 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0120h	0010 2120h

Figure 6-10. CTRLMMR_IPC_SET8 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-22. CTRLMMR_IPC_SET8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.11 CTRLMMR_IPC_SET9 Register (Proxy0 Offset = 124h; Proxy1 Offset = 2124h) [reset = 0h]

CTRLMMR_IPC_SET9 is shown in Figure 6-11 and described in Table 6-24.

Return to Summary Table.

Generate interprocessor communication interrupt to ARM MPU core1.

Table 6-23. CTRLMMR_IPC_SET9 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0124h	0010 2124h

Figure 6-11. CTRLMMR_IPC_SET9 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-24. CTRLMMR_IPC_SET9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.12 CTRLMMR_IPC_SET16 Register (Proxy0 Offset = 140h; Proxy1 Offset = 2140h) [reset = 0h]

CTRLMMR_IPC_SET16 is shown in Figure 6-12 and described in Table 6-26.

Return to Summary Table.

Generate interprocessor communication interrupt to MAIN R5 core0.

Table 6-25. CTRLMMR_IPC_SET16 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0140h	0010 2140h

Figure 6-12. CTRLMMR_IPC_SET16 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-26. CTRLMMR_IPC_SET16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.13 CTRLMMR_IPC_SET17 Register (Proxy0 Offset = 144h; Proxy1 Offset = 2144h) [reset = 0h]

CTRLMMR_IPC_SET17 is shown in Figure 6-13 and described in Table 6-28.

Return to Summary Table.

Generate interprocessor communication interrupt to MAIN R5 core1.

Table 6-27. CTRLMMR_IPC_SET17 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0144h	0010 2144h

Figure 6-13. CTRLMMR_IPC_SET17 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-28. CTRLMMR_IPC_SET17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.14 CTRLMMR_IPC_SET18 Register (Proxy0 Offset = 148h; Proxy1 Offset = 2148h) [reset = 0h]

CTRLMMR_IPC_SET18 is shown in Figure 6-14 and described in Table 6-30.

Return to Summary Table.

Generate interprocessor communication interrupt to MAIN R5 core2.

Table 6-29. CTRLMMR_IPC_SET18 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0148h	0010 2148h

Figure 6-14. CTRLMMR_IPC_SET18 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-30. CTRLMMR_IPC_SET18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.15 CTRLMMR_IPC_SET19 Register (Proxy0 Offset = 14Ch; Proxy1 Offset = 214Ch) [reset = 0h]

CTRLMMR_IPC_SET19 is shown in Figure 6-15 and described in Table 6-32.

Return to Summary Table.

Generate interprocessor communication interrupt to MAIN R5 core3.

Table 6-31. CTRLMMR_IPC_SET19 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 014Ch	0010 214Ch

Figure 6-15. CTRLMMR_IPC_SET19 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-32. CTRLMMR_IPC_SET19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.16 CTRLMMR_IPC_SET20 Register (Proxy0 Offset = 150h; Proxy1 Offset = 2150h) [reset = 0h]

CTRLMMR_IPC_SET20 is shown in Figure 6-16 and described in Table 6-34.

Return to Summary Table.

Generate interprocessor communication interrupt to ICSSG0 PRU0.

Table 6-33. CTRLMMR_IPC_SET20 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0150h	0010 2150h

Figure 6-16. CTRLMMR_IPC_SET20 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-34. CTRLMMR_IPC_SET20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.17 CTRLMMR_IPC_SET21 Register (Proxy0 Offset = 154h; Proxy1 Offset = 2154h) [reset = 0h]

CTRLMMR_IPC_SET21 is shown in Figure 6-17 and described in Table 6-36.

Return to Summary Table.

Generate interprocessor communication interrupt to ICSSG0 PRU1.

Table 6-35. CTRLMMR_IPC_SET21 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0154h	0010 2154h

Figure 6-17. CTRLMMR_IPC_SET21 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-36. CTRLMMR_IPC_SET21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.18 CTRLMMR_IPC_SET22 Register (Proxy0 Offset = 158h; Proxy1 Offset = 2158h) [reset = 0h]

CTRLMMR_IPC_SET22 is shown in Figure 6-18 and described in Table 6-38.

Return to Summary Table.

Generate interprocessor communication interrupt to ICSSG1 PRU0.

Table 6-37. CTRLMMR_IPC_SET22 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0158h	0010 2158h

Figure 6-18. CTRLMMR_IPC_SET22 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-38. CTRLMMR_IPC_SET22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.19 CTRLMMR_IPC_SET23 Register (Proxy0 Offset = 15Ch; Proxy1 Offset = 215Ch) [reset = 0h]

CTRLMMR_IPC_SET23 is shown in Figure 6-19 and described in Table 6-40.

Return to Summary Table.

Generate interprocessor communication interrupt to ICSSG1 PRU1.

Table 6-39. CTRLMMR_IPC_SET23 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 015Ch	0010 215Ch

Figure 6-19. CTRLMMR_IPC_SET23 Register

31	30	29	28	27	26	25	24
IPC_SRC_SET							
W1TS-0h							
23	22	21	20	19	18	17	16
IPC_SRC_SET							
W1TS-0h							
15	14	13	12	11	10	9	8
IPC_SRC_SET							
W1TS-0h							
7	6	5	4	3	2	1	0
IPC_SRC_SET				RESERVED			IPC_SET
W1TS-0h				R-0h			W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-40. CTRLMMR_IPC_SET23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_SET	W1TS	0h	Read returns current value Write: 0h - No effect 1h - Sets both SRC_SETx and the SRC_CLRx bit in the corresponding IPC_CLR register
3-1	RESERVED	R	0h	Reserved
0	IPC_SET	W1TS	0h	Read returns 0 Write: 0h - No effect 1h - Sets both the IPC_SET and the IPC_CLR bit in the corresponding IPC_CLR register

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6.20 CTRLMMR_IPC_CLR0 Register (Proxy0 Offset = 180h; Proxy1 Offset = 2180h) [reset = 0h]

CTRLMMR_IPC_CLR0 is shown in Figure 6-20 and described in Table 6-42.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to C71x core0.

Table 6-41. CTRLMMR_IPC_CLR0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0180h	0010 2180h

Figure 6-20. CTRLMMR_IPC_CLR0 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-42. CTRLMMR_IPC_CLR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.21 CTRLMMR_IPC_CLR6 Register (Proxy0 Offset = 198h; Proxy1 Offset = 2198h) [reset = 0h]

CTRLMMR_IPC_CLR6 is shown in Figure 6-21 and described in Table 6-44.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to C66 core0.

Table 6-43. CTRLMMR_IPC_CLR6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0198h	0010 2198h

Figure 6-21. CTRLMMR_IPC_CLR6 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-44. CTRLMMR_IPC_CLR6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.22 CTRLMMR_IPC_CLR7 Register (Proxy0 Offset = 19Ch; Proxy1 Offset = 219Ch) [reset = 0h]

CTRLMMR_IPC_CLR7 is shown in Figure 6-22 and described in Table 6-46.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to C66 core1.

Table 6-45. CTRLMMR_IPC_CLR7 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 019Ch	0010 219Ch

Figure 6-22. CTRLMMR_IPC_CLR7 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-46. CTRLMMR_IPC_CLR7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.23 CTRLMMR_IPC_CLR8 Register (Proxy0 Offset = 1A0h; Proxy1 Offset = 21A0h) [reset = 0h]

CTRLMMR_IPC_CLR8 is shown in Figure 6-23 and described in Table 6-48.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to ARM MPU core0.

Table 6-47. CTRLMMR_IPC_CLR8 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 01A0h	0010 21A0h

Figure 6-23. CTRLMMR_IPC_CLR8 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-48. CTRLMMR_IPC_CLR8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.24 CTRLMMR_IPC_CLR9 Register (Proxy0 Offset = 1A4h; Proxy1 Offset = 21A4h) [reset = 0h]

CTRLMMR_IPC_CLR9 is shown in Figure 6-24 and described in Table 6-50.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to ARM MPU core1.

Table 6-49. CTRLMMR_IPC_CLR9 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 01A4h	0010 21A4h

Figure 6-24. CTRLMMR_IPC_CLR9 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-50. CTRLMMR_IPC_CLR9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.25 CTRLMMR_IPC_CLR16 Register (Proxy0 Offset = 1C0h; Proxy1 Offset = 21C0h) [reset = 0h]

CTRLMMR_IPC_CLR16 is shown in Figure 6-25 and described in Table 6-52.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to MAIN R5 core0.

Table 6-51. CTRLMMR_IPC_CLR16 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 01C0h	0010 21C0h

Figure 6-25. CTRLMMR_IPC_CLR16 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-52. CTRLMMR_IPC_CLR16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.26 CTRLMMR_IPC_CLR17 Register (Proxy0 Offset = 1C4h; Proxy1 Offset = 21C4h) [reset = 0h]

CTRLMMR_IPC_CLR17 is shown in Figure 6-26 and described in Table 6-54.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to MAIN R5 core1.

Table 6-53. CTRLMMR_IPC_CLR17 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 01C4h	0010 21C4h

Figure 6-26. CTRLMMR_IPC_CLR17 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-54. CTRLMMR_IPC_CLR17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.27 CTRLMMR_IPC_CLR18 Register (Proxy0 Offset = 1C8h; Proxy1 Offset = 21C8h) [reset = 0h]

CTRLMMR_IPC_CLR18 is shown in Figure 6-27 and described in Table 6-56.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to MAIN R5 core2.

Table 6-55. CTRLMMR_IPC_CLR18 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 01C8h	0010 21C8h

Figure 6-27. CTRLMMR_IPC_CLR18 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-56. CTRLMMR_IPC_CLR18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.28 CTRLMMR_IPC_CLR19 Register (Proxy0 Offset = 1CCh; Proxy1 Offset = 21CCh) [reset = 0h]

CTRLMMR_IPC_CLR19 is shown in Figure 6-28 and described in Table 6-58.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to MAIN R5 core3.

Table 6-57. CTRLMMR_IPC_CLR19 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 01CCh	0010 21CCh

Figure 6-28. CTRLMMR_IPC_CLR19 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-58. CTRLMMR_IPC_CLR19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.29 CTRLMMR_IPC_CLR20 Register (Proxy0 Offset = 1D0h; Proxy1 Offset = 21D0h) [reset = 0h]

CTRLMMR_IPC_CLR20 is shown in Figure 6-29 and described in Table 6-60.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to ICSSG0 PRU0.

Table 6-59. CTRLMMR_IPC_CLR20 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 01D0h	0010 21D0h

Figure 6-29. CTRLMMR_IPC_CLR20 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-60. CTRLMMR_IPC_CLR20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.30 CTRLMMR_IPC_CLR21 Register (Proxy0 Offset = 1D4h; Proxy1 Offset = 21D4h) [reset = 0h]

CTRLMMR_IPC_CLR21 is shown in Figure 6-30 and described in Table 6-62.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to ICSSG0 PRU1.

Table 6-61. CTRLMMR_IPC_CLR21 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 01D4h	0010 21D4h

Figure 6-30. CTRLMMR_IPC_CLR21 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-62. CTRLMMR_IPC_CLR21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.31 CTRLMMR_IPC_CLR22 Register (Proxy0 Offset = 1D8h; Proxy1 Offset = 21D8h) [reset = 0h]

CTRLMMR_IPC_CLR22 is shown in Figure 6-31 and described in Table 6-64.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to ICSSG1 PRU0.

Table 6-63. CTRLMMR_IPC_CLR22 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 01D8h	0010 21D8h

Figure 6-31. CTRLMMR_IPC_CLR22 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-64. CTRLMMR_IPC_CLR22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.32 CTRLMMR_IPC_CLR23 Register (Proxy0 Offset = 1DCh; Proxy1 Offset = 21DCh) [reset = 0h]

CTRLMMR_IPC_CLR23 is shown in Figure 6-32 and described in Table 6-66.

Return to Summary Table.

Acknowledge interprocessor communication interrupt to ICSSG1 PRU1.

Table 6-65. CTRLMMR_IPC_CLR23 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 01DCh	0010 21DCh

Figure 6-32. CTRLMMR_IPC_CLR23 Register

31	30	29	28	27	26	25	24
IPC_SRC_CLR							
W1TC-0h							
23	22	21	20	19	18	17	16
IPC_SRC_CLR							
W1TC-0h							
15	14	13	12	11	10	9	8
IPC_SRC_CLR							
W1TC-0h							
7	6	5	4	3	2	1	0
IPC_SRC_CLR				RESERVED			IPC_CLR
W1TC-0h				R-0h			W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-66. CTRLMMR_IPC_CLR23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	IPC_SRC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both SRC_CLRx and the SRC_SETx bit in the corresponding IPC_GEN register
3-1	RESERVED	R	0h	Reserved
0	IPC_CLR	W1TC	0h	Read returns current value Write: 0h - No effect 1h - Clears both IPC_CLR and the IPC_SET bit in the corresponding IPC_SET register

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6.33 CTRLMMR_PCI_DEVICE_ID Register (Proxy0 Offset = 210h; Proxy1 Offset = 2210h) [reset = B00D104Ch]

CTRLMMR_PCI_DEVICE_ID is shown in Figure 6-33 and described in Table 6-68.

Return to Summary Table.

PCIe device ID and vendor ID register.

Table 6-67. CTRLMMR_PCI_DEVICE_ID Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0210h	0010 2210h

Figure 6-33. CTRLMMR_PCI_DEVICE_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE_ID																VENDOR_ID															
R-B00Dh																R-104Ch															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-68. CTRLMMR_PCI_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DEVICE_ID	R	B00Dh	Product ID
15-0	VENDOR_ID	R	104Ch	TI Vendor ID

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6.34 CTRLMMR_USB_DEVICE_ID Register (Proxy0 Offset = 220h; Proxy1 Offset = 2220h) [reset = 61630451h]

CTRLMMR_USB_DEVICE_ID is shown in Figure 6-34 and described in Table 6-70.

Return to Summary Table.

USB device and vendor ID register.

Table 6-69. CTRLMMR_USB_DEVICE_ID Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 0220h	0010 2220h

Figure 6-34. CTRLMMR_USB_DEVICE_ID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE_ID																VENDOR_ID															
R-6163h																R-451h															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-70. CTRLMMR_USB_DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	DEVICE_ID	R	6163h	Product ID
15-0	VENDOR_ID	R	451h	TI Vendor ID

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6.35 CTRLMMR_LOCK0_KICK0 Register (Proxy0 Offset = 1008h; Proxy1 Offset = 3008h) [reset = 0h]

CTRLMMR_LOCK0_KICK0 is shown in Figure 6-35 and described in Table 6-72.

Return to Summary Table.

Lower 32-bits of Partition0 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_LOCK0_KICK1 with its key value before write-protected Partition 0 registers can be written.

Table 6-71. CTRLMMR_LOCK0_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1008h	0010 3008h

Figure 6-35. CTRLMMR_LOCK0_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-72. CTRLMMR_LOCK0_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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6.36 CTRLMMR_LOCK0_KICK1 Register (Proxy0 Offset = 100Ch; Proxy1 Offset = 300Ch) [reset = 0h]

CTRLMMR_LOCK0_KICK1 is shown in Figure 6-36 and described in Table 6-74.

Return to Summary Table.

Upper 32-bits of Partition 0 write lock key. This register must be written with the designated key value after a write to CTRLMMR_LOCK0_KICK0 with its key value before write-protected Partition 0 registers can be written.

Table 6-73. CTRLMMR_LOCK0_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 100Ch	0010 300Ch

Figure 6-36. CTRLMMR_LOCK0_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-74. CTRLMMR_LOCK0_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers

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6.37 CTRLMMR_INTR_RAW_STAT Register (Proxy0 Offset = 1010h; Proxy1 Offset = 3010h) [reset = 0h]

CTRLMMR_INTR_RAW_STAT is shown in Figure 6-37 and described in Table 6-76.

Return to Summary Table.

Shows the interrupt status (before enabling) and allows setting of the interrupt status (for test).

Table 6-75. CTRLMMR_INTR_RAW_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1010h	0010 3010h

Figure 6-37. CTRLMMR_INTR_RAW_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR	LOCK_ERR	ADDR_ERR	PROT_ERR
R-0h				W1TS-0h	W1TS-0h	W1TS-0h	W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-76. CTRLMMR_INTR_RAW_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PROXY_ERR	W1TS	0h	Proxy violation occurred (attempt to write a Proxy1 claimed register through its Proxy0 address) Write 1 to set the status bit (for test) Writing 0 has no effect.
2	LOCK_ERR	W1TS	0h	Lock violation occurred (attempt to write a write-locked register with partition locked) Write 1 to set the status bit (for test) Writing 0 has no effect.
1	ADDR_ERR	W1TS	0h	Address violation occurred (attempt to read or write an invalid register address) Write 1 to set the status bit (for test) Writing 0 has no effect.
0	PROT_ERR	W1TS	0h	Protection violation occurred (attempt to read or write a register with insufficient security or privilege access rights) Write 1 to set the status bit (for test) Writing 0 has no effect.

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6.38 CTRLMMR_INTR_STAT_CLR Register (Proxy0 Offset = 1014h; Proxy1 Offset = 3014h) [reset = 0h]

CTRLMMR_INTR_STAT_CLR is shown in Figure 6-38 and described in Table 6-78.

Return to Summary Table.

Shows the enabled interrupt status and allows the interrupt to be cleared.

Table 6-77. CTRLMMR_INTR_STAT_CLR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1014h	0010 3014h

Figure 6-38. CTRLMMR_INTR_STAT_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				EN_PROXY_ERR	EN_LOCK_ERR	EN_ADDR_ERR	EN_PROT_ERR
R-0h				W1TC-0h	W1TC-0h	W1TC-0h	W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-78. CTRLMMR_INTR_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	EN_PROXY_ERR	W1TC	0h	Enabled proxy interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
2	EN_LOCK_ERR	W1TC	0h	Enabled lock interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
1	EN_ADDR_ERR	W1TC	0h	Enabled address interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.
0	EN_PROT_ERR	W1TC	0h	Enabled protection interrupt event status Write 1 to clear the interrupt event Writing 0 has no effect.

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6.39 CTRLMMR_INTR_EN_SET Register (Proxy0 Offset = 1018h; Proxy1 Offset = 3018h) [reset = 0h]

CTRLMMR_INTR_EN_SET is shown in Figure 6-39 and described in Table 6-80.

Return to Summary Table.

Allows interrupt enables to be set.

Table 6-79. CTRLMMR_INTR_EN_SET Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1018h	0010 3018h

Figure 6-39. CTRLMMR_INTR_EN_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_SET	LOCK_ERR_EN_SET	ADDR_ERR_EN_SET	PROT_ERR_EN_SET
R-0h				W1TS-0h	W1TS-0h	W1TS-0h	W1TS-0h

LEGEND: R = Read Only; W1TS = Write 1 to Set Bit; -*n* = value after reset

Table 6-80. CTRLMMR_INTR_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PROXY_ERR_EN_SET	W1TS	0h	Proxy interrupt enable Write 1 to enable proxy interrupt events Writing 0 has no effect.
2	LOCK_ERR_EN_SET	W1TS	0h	Lock interrupt enable Write 1 to enable lock interrupt events Writing 0 has no effect.
1	ADDR_ERR_EN_SET	W1TS	0h	Address interrupt enable Write 1 to enable address interrupt events Writing 0 has no effect.
0	PROT_ERR_EN_SET	W1TS	0h	Protection interrupt enable Write 1 to enable protection interrupt events Writing 0 has no effect.

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6.40 CTRLMMR_INTR_EN_CLR Register (Proxy0 Offset = 101Ch; Proxy1 Offset = 301Ch) [reset = 0h]

CTRLMMR_INTR_EN_CLR is shown in Figure 6-40 and described in Table 6-82.

Return to Summary Table.

Allows interrupt enables to be cleared.

Table 6-81. CTRLMMR_INTR_EN_CLR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 101Ch	0010 301Ch

Figure 6-40. CTRLMMR_INTR_EN_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PROXY_ERR_EN_CLR	LOCK_ERR_EN_CLR	ADDR_ERR_EN_CLR	PROT_ERR_EN_CLR
R-0h				W1TC-0h	W1TC-0h	W1TC-0h	W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-82. CTRLMMR_INTR_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	PROXY_ERR_EN_CLR	W1TC	0h	Proxy interrupt disable Write 1 to disable proxy interrupt events Writing 0 has no effect.
2	LOCK_ERR_EN_CLR	W1TC	0h	Lock interrupt disable Write 1 to disable lock interrupt events Writing 0 has no effect.
1	ADDR_ERR_EN_CLR	W1TC	0h	Address interrupt disable Write 1 to disable address interrupt events Writing 0 has no effect.
0	PROT_ERR_EN_CLR	W1TC	0h	Protection interrupt disable Write 1 to disable protection interrupt events Writing 0 has no effect.

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6.41 CTRLMMR_EOI Register (Proxy0 Offset = 1020h; Proxy1 Offset = 3020h) [reset = 0h]

CTRLMMR_EOI is shown in Figure 6-41 and described in Table 6-84.

Return to Summary Table.

EOI Vector value. This register should be written with interrupt distribution value required by the device architecture to indicate service completion of the MMR interrupt.

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 6-83. CTRLMMR_EOI Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1020h	0010 3020h

Figure 6-41. CTRLMMR_EOI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								VECTOR							
R-0h																								R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-84. CTRLMMR_EOI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7-0	VECTOR	R/W	0h	CTRLMMR_EOI vector value

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6.42 CTRLMMR_FAULT_ADDR Register (Proxy0 Offset = 1024h; Proxy1 Offset = 3024h) [reset = 0h]

CTRLMMR_FAULT_ADDR is shown in Figure 6-42 and described in Table 6-86.

Return to Summary Table.

Indicates the address of the first transfer that caused a fault to occur.

Table 6-85. CTRLMMR_FAULT_ADDR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1024h	0010 3024h

Figure 6-42. CTRLMMR_FAULT_ADDR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-86. CTRLMMR_FAULT_ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ADDRESS	R	0h	Address of the faulted access

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6.43 CTRLMMR_FAULT_TYPE Register (Proxy0 Offset = 1028h; Proxy1 Offset = 3028h) [reset = 0h]

CTRLMMR_FAULT_TYPE is shown in Figure 6-43 and described in Table 6-88.

Return to Summary Table.

Indicates the access type of the first transfer that caused a fault to occur.

Table 6-87. CTRLMMR_FAULT_TYPE Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1028h	0010 3028h

Figure 6-43. CTRLMMR_FAULT_TYPE Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										TYPE					
R-0h																										R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 6-88. CTRLMMR_FAULT_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved
5-0	TYPE	R	0h	Type of access which faulted 0h - No fault 1h - User execute access 2h - User write access 4h - User read access 8h - Supervisor execute access 10h - Supervisor write access 20h - Supervisor read access

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6.44 CTRLMMR_FAULT_ATTR Register (Proxy0 Offset = 102Ch; Proxy1 Offset = 302Ch) [reset = 0h]

CTRLMMR_FAULT_ATTR is shown in Figure 6-44 and described in Table 6-90.

Return to Summary Table.

Indicates the attributes of the first transfer that caused a fault to occur.

Table 6-89. CTRLMMR_FAULT_ATTR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 102Ch	0010 302Ch

Figure 6-44. CTRLMMR_FAULT_ATTR Register

31	30	29	28	27	26	25	24
XID							
R-0h							
23	22	21	20	19	18	17	16
XID				ROUTEID			
R-0h				R-0h			
15	14	13	12	11	10	9	8
ROUTEID							
R-0h							
7	6	5	4	3	2	1	0
PRIVID							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 6-90. CTRLMMR_FAULT_ATTR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	XID	R	0h	Transaction ID
19-8	ROUTEID	R	0h	Route ID
7-0	PRIVID	R	0h	Privilege ID

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6.45 CTRLMMR_FAULT_CLR Register (Proxy0 Offset = 1030h; Proxy1 Offset = 3030h) [reset = 0h]

CTRLMMR_FAULT_CLR is shown in Figure 6-45 and described in Table 6-92.

Return to Summary Table.

Allows software to clear the current fault Clearing the current fault allows the CTRLMMR_FAULT_ADDR, CTRLMMR_FAULT_TYPE, and CTRLMMR_FAULT_ATTR registers to latch the attributes of the next fault that occurs. This does not affect the fault interrupt event itself. The interrupt must be cleared using the appropriate INTR_STATUS_CLR register bits.

Table 6-91. CTRLMMR_FAULT_CLR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1030h	0010 3030h

Figure 6-45. CTRLMMR_FAULT_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLEAR
R-0h							W1TC-0h

LEGEND: R = Read Only; W1TC = Write 1 to Clear Bit; *-n* = value after reset

Table 6-92. CTRLMMR_FAULT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLEAR	W1TC	0h	Fault clear Write 1 to clear the current fault Writing 0 has no effect

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6.46 CTRLMMR_P0_CLAIM0 Register (Proxy0 Offset = 1100h; Proxy1 Offset = 3100h) [reset = 0h]

CTRLMMR_P0_CLAIM0 is shown in Figure 6-46 and described in Table 6-94.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 6-93. CTRLMMR_P0_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1100h	0010 3100h

Figure 6-46. CTRLMMR_P0_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-94. CTRLMMR_P0_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x0 + (0 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x2000 + (0 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.47 CTRLMMR_P0_CLAIM1 Register (Proxy0 Offset = 1104h; Proxy1 Offset = 3104h) [reset = 0h]

CTRLMMR_P0_CLAIM1 is shown in Figure 6-47 and described in Table 6-96.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 6-95. CTRLMMR_P0_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1104h	0010 3104h

Figure 6-47. CTRLMMR_P0_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-96. CTRLMMR_P0_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x0 + (1 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x2000 + (1 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.48 CTRLMMR_P0_CLAIM2 Register (Proxy0 Offset = 1108h; Proxy1 Offset = 3108h) [reset = 0h]

CTRLMMR_P0_CLAIM2 is shown in Figure 6-48 and described in Table 6-98.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 6-97. CTRLMMR_P0_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1108h	0010 3108h

Figure 6-48. CTRLMMR_P0_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-98. CTRLMMR_P0_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x0 + (2 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x2000 + (2 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.49 CTRLMMR_P0_CLAIM3 Register (Proxy0 Offset = 110Ch; Proxy1 Offset = 310Ch) [reset = 0h]

CTRLMMR_P0_CLAIM3 is shown in Figure 6-49 and described in Table 6-100.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 6-99. CTRLMMR_P0_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 110Ch	0010 310Ch

Figure 6-49. CTRLMMR_P0_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-100. CTRLMMR_P0_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x0 + (3 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x2000 + (3 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.50 CTRLMMR_P0_CLAIM4 Register (Proxy0 Offset = 1110h; Proxy1 Offset = 3110h) [reset = 0h]

CTRLMMR_P0_CLAIM4 is shown in Figure 6-50 and described in Table 6-102.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 6-101. CTRLMMR_P0_CLAIM4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1110h	0010 3110h

Figure 6-50. CTRLMMR_P0_CLAIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-102. CTRLMMR_P0_CLAIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x0 + (4 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x2000 + (4 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.51 CTRLMMR_P0_CLAIM5 Register (Proxy0 Offset = 1114h; Proxy1 Offset = 3114h) [reset = 0h]

CTRLMMR_P0_CLAIM5 is shown in Figure 6-51 and described in Table 6-104.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 6-103. CTRLMMR_P0_CLAIM5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1114h	0010 3114h

Figure 6-51. CTRLMMR_P0_CLAIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-104. CTRLMMR_P0_CLAIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x0 + (5 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x2000 + (5 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.52 CTRLMMR_P0_CLAIM6 Register (Proxy0 Offset = 1118h; Proxy1 Offset = 3118h) [reset = 0h]

CTRLMMR_P0_CLAIM6 is shown in Figure 6-52 and described in Table 6-106.

Return to Summary Table.

Claim bits for Partition 0 Registers.

Table 6-105. CTRLMMR_P0_CLAIM6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 1118h	0010 3118h

Figure 6-52. CTRLMMR_P0_CLAIM6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-106. CTRLMMR_P0_CLAIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x0 + (6 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x2000 + (6 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.53 CTRLMMR_USB0_CTRL Register (Proxy0 Offset = 4000h; Proxy1 Offset = 6000h) [reset = 0h]

CTRLMMR_USB0_CTRL is shown in Figure 6-53 and described in Table 6-108.

Return to Summary Table.

Controls USB0 operation.

Table 6-107. CTRLMMR_USB0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4000h	0010 6000h

Figure 6-53. CTRLMMR_USB0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED				SERDES_SEL	RESERVED		
R-0h				R/W-0h	R-0h		
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-108. CTRLMMR_USB0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27	SERDES_SEL	R/W	0h	Serdes Selection. The USB3 0 interface can be mapped to 2 different SERDES controllers. This bit selects which SERDES drives the USB3 PIPE interface input clock, data and control signals. Programming should align with the CTRLMMR_SERDES0_LN1_CTRL and CTRLMMR_SERDES3_LN0_CTRL lane_func_sel programming. 0h - SERDES0 drives USB3.1 inputs 1h - SERDES3 drives USB3.1 inputs
26-0	RESERVED	R	0h	Reserved

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6.54 CTRLMMR_USB1_CTRL Register (Proxy0 Offset = 4010h; Proxy1 Offset = 6010h) [reset = 0h]

CTRLMMR_USB1_CTRL is shown in Figure 6-54 and described in Table 6-110.

Return to Summary Table.

Controls USB1 operation.

Table 6-109. CTRLMMR_USB1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4010h	0010 6010h

Figure 6-54. CTRLMMR_USB1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED				SERDES_SEL	RESERVED		
R-0h				R/W-0h	R-0h		
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-110. CTRLMMR_USB1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	0h	Reserved
27	SERDES_SEL	R/W	0h	Serdes Selection. The USB3 1 interface can be mapped to 2 different SERDES controllers. This bit selects which SERDES drives the USB3 PIPE interface input clock, data and control signals. Programming should align with the CTRLMMR_SERDES0_LN1_CTRL and CTRLMMR_SERDES3_LN0_CTRL lane_func_sel programming. 0h - SERDES1 drives USB3.1 inputs 1h - SERDES2 drives USB3.1 inputs
26-0	RESERVED	R	0h	Reserved

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6.55 CTRLMMR_ENET1_CTRL Register (Proxy0 Offset = 4044h; Proxy1 Offset = 6044h) [reset = 2h]

CTRLMMR_ENET1_CTRL is shown in Figure 6-55 and described in Table 6-112.

Return to Summary Table.

Controls Ethernet Port1 operation.

Table 6-111. CTRLMMR_ENET1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4044h	0010 6044h

Figure 6-55. CTRLMMR_ENET1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RGMII_ID_MODE	RESERVED	PORT_MODE_SEL		
R-0h			R/W-0h	R-0h	R/W-2h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-112. CTRLMMR_ENET1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RGMII_ID_MODE	R/W	0h	Port1 RGMII internal transmit delay selection 0h - Internal transmit delay 1h - Reserved
3	RESERVED	R	0h	Reserved
2-0	PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port1 interface 0h - GMII/MII (not supported) 1h - RMII 2h - RGMII 3h - SGMII 4h - QSGMII 5h - XFI (not supported) 6h - QSGMII_SUB 7h - Reserved

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6.56 CTRLMMR_ENET2_CTRL Register (Proxy0 Offset = 4048h; Proxy1 Offset = 6048h) [reset = 2h]

CTRLMMR_ENET2_CTRL is shown in Figure 6-56 and described in Table 6-114.

Return to Summary Table.

Controls Ethernet Port2 operation.

Table 6-113. CTRLMMR_ENET2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4048h	0010 6048h

Figure 6-56. CTRLMMR_ENET2_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RGMII_ID_MODE	RESERVED	PORT_MODE_SEL		
R-0h			R/W-0h	R-0h	R/W-2h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-114. CTRLMMR_ENET2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RGMII_ID_MODE	R/W	0h	Port2 RGMII internal transmit delay selection 0h - Internal transmit delay 1h - Reserved
3	RESERVED	R	0h	Reserved
2-0	PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port2 interface 0h - GMII/MII (not supported) 1h - RMII 2h - RGMII 3h - SGMII 4h - QSGMII 5h - XFI (not supported) 6h - QSGMII_SUB 7h - Reserved

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6.57 CTRLMMR_ENET3_CTRL Register (Proxy0 Offset = 404Ch; Proxy1 Offset = 604Ch) [reset = 2h]

CTRLMMR_ENET3_CTRL is shown in Figure 6-57 and described in Table 6-116.

Return to Summary Table.

Controls Ethernet Port3 operation.

Table 6-115. CTRLMMR_ENET3_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 404Ch	0010 604Ch

Figure 6-57. CTRLMMR_ENET3_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RGMII_ID_MODE	RESERVED	PORT_MODE_SEL		
R-0h			R/W-0h	R-0h	R/W-2h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-116. CTRLMMR_ENET3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RGMII_ID_MODE	R/W	0h	Port3 RGMII internal transmit delay selection 0h - Internal transmit delay 1h - Reserved
3	RESERVED	R	0h	Reserved
2-0	PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port3 interface 0h - GMII/MII (not supported) 1h - RMII 2h - RGMII 3h - SGMII 4h - QSGMII 5h - XFI (not supported) 6h - QSGMII_SUB 7h - Reserved

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6.58 CTRLMMR_ENET4_CTRL Register (Proxy0 Offset = 4050h; Proxy1 Offset = 6050h) [reset = 2h]

CTRLMMR_ENET4_CTRL is shown in Figure 6-58 and described in Table 6-118.

Return to Summary Table.

Controls Ethernet Port4 operation.

Table 6-117. CTRLMMR_ENET4_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4050h	0010 6050h

Figure 6-58. CTRLMMR_ENET4_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RGMII_ID_MODE	RESERVED	PORT_MODE_SEL		
R-0h			R/W-0h	R-0h	R/W-2h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-118. CTRLMMR_ENET4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RGMII_ID_MODE	R/W	0h	Port4 RGMII internal transmit delay selection 0h - Internal transmit delay 1h - Reserved
3	RESERVED	R	0h	Reserved
2-0	PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port4 interface 0h - GMII/MII (not supported) 1h - RMII 2h - RGMII 3h - SGMII 4h - QSGMII 5h - XFI (not supported) 6h - QSGMII_SUB 7h - Reserved

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6.59 CTRLMMR_ENET5_CTRL Register (Proxy0 Offset = 4054h; Proxy1 Offset = 6054h) [reset = 2h]

CTRLMMR_ENET5_CTRL is shown in Figure 6-59 and described in Table 6-120.

Return to Summary Table.

Controls Ethernet Port5 operation.

Table 6-119. CTRLMMR_ENET5_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4054h	0010 6054h

Figure 6-59. CTRLMMR_ENET5_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RGMII_ID_MODE	RESERVED	PORT_MODE_SEL		
R-0h			R/W-0h	R-0h	R/W-2h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-120. CTRLMMR_ENET5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RGMII_ID_MODE	R/W	0h	Port5 RGMII internal transmit delay selection 0h - Internal transmit delay 1h - Reserved
3	RESERVED	R	0h	Reserved
2-0	PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port5 interface 0h - GMII/MII (not supported) 1h - RMII 2h - RGMII 3h - SGMII 4h - QSGMII 5h - XFI (not supported) 6h - QSGMII_SUB 7h - Reserved

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6.60 CTRLMMR_ENET6_CTRL Register (Proxy0 Offset = 4058h; Proxy1 Offset = 6058h) [reset = 2h]

CTRLMMR_ENET6_CTRL is shown in Figure 6-60 and described in Table 6-122.

Return to Summary Table.

Controls Ethernet Port6 operation.

Table 6-121. CTRLMMR_ENET6_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4058h	0010 6058h

Figure 6-60. CTRLMMR_ENET6_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RGMII_ID_MODE	RESERVED	PORT_MODE_SEL		
R-0h			R/W-0h	R-0h	R/W-2h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-122. CTRLMMR_ENET6_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RGMII_ID_MODE	R/W	0h	Port6 RGMII internal transmit delay selection 0h - Internal transmit delay 1h - Reserved
3	RESERVED	R	0h	Reserved
2-0	PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port6 interface 0h - GMII/MII (not supported) 1h - RMII 2h - RGMII 3h - SGMII 4h - QSGMII 5h - XFI (not supported) 6h - QSGMII_SUB 7h - Reserved

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6.61 CTRLMMR_ENET7_CTRL Register (Proxy0 Offset = 405Ch; Proxy1 Offset = 605Ch) [reset = 2h]

CTRLMMR_ENET7_CTRL is shown in Figure 6-61 and described in Table 6-124.

Return to Summary Table.

Controls Ethernet Port7 operation.

Table 6-123. CTRLMMR_ENET7_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 405Ch	0010 605Ch

Figure 6-61. CTRLMMR_ENET7_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RGMII_ID_MODE	RESERVED	PORT_MODE_SEL		
R-0h			R/W-0h	R-0h	R/W-2h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-124. CTRLMMR_ENET7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RGMII_ID_MODE	R/W	0h	Port7 RGMII internal transmit delay selection 0h - Internal transmit delay 1h - Reserved
3	RESERVED	R	0h	Reserved
2-0	PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port7 interface 0h - GMII/MII (not supported) 1h - RMII 2h - RGMII 3h - SGMII 4h - QSGMII 5h - XFI (not supported) 6h - QSGMII_SUB 7h - Reserved

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6.62 CTRLMMR_ENET8_CTRL Register (Proxy0 Offset = 4060h; Proxy1 Offset = 6060h) [reset = 2h]

CTRLMMR_ENET8_CTRL is shown in Figure 6-62 and described in Table 6-126.

Return to Summary Table.

Controls Ethernet Port8 operation.

Table 6-125. CTRLMMR_ENET8_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4060h	0010 6060h

Figure 6-62. CTRLMMR_ENET8_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			RGMII_ID_MODE	RESERVED	PORT_MODE_SEL		
R-0h			R/W-0h	R-0h	R/W-2h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-126. CTRLMMR_ENET8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	RGMII_ID_MODE	R/W	0h	Port8 RGMII internal transmit delay selection 0h - Internal transmit delay 1h - Reserved
3	RESERVED	R	0h	Reserved
2-0	PORT_MODE_SEL	R/W	2h	Selects Ethernet switch Port8 interface 0h - GMII/MII (not supported) 1h - RMII 2h - RGMII 3h - SGMII 4h - QSGMII 5h - XFI (not supported) 6h - QSGMII_SUB 7h - Reserved

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6.63 CTRLMMR_PCIE0_CTRL Register (Proxy0 Offset = 4070h; Proxy1 Offset = 6070h) [reset = 103h]

CTRLMMR_PCIE0_CTRL is shown in Figure 6-63 and described in Table 6-128.

Return to Summary Table.

Controls PCIe0 operation.

Table 6-127. CTRLMMR_PCIE0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4070h	0010 6070h

Figure 6-63. CTRLMMR_PCIE0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							LANE_COUNT
R-0h							R/W-1h
7	6	5	4	3	2	1	0
MODE_SEL	RESERVED					GENERATION_SEL	
R/W-0h	R-0h					R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-128. CTRLMMR_PCIE0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	LANE_COUNT	R/W	1h	Configures the PCIe lane count 0h - Select 1-lane operation 1h - Select 2-lane operation
7	MODE_SEL	R/W	0h	Selects the operating mode 0h - Endpoint 1h - Root Complex
6-2	RESERVED	R	0h	Reserved
1-0	GENERATION_SEL	R/W	3h	Configures the PCIe generation support in the PCIe capabilities linked-list 0h - Reserved 1h - Gen2 - Controller advertises Gen1 & Gen2 capability and link operates at either speed 2h - Gen3 - Controller advertises Gen1, Gen2, & Gen3 capability and link operates at any of the three speeds 3h - Gen4 - Controller advertises Gen1, Gen2, Gen3, & Gen4 capability and link operates at any of the four speeds

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6.64 CTRLMMR_PCIE1_CTRL Register (Proxy0 Offset = 4074h; Proxy1 Offset = 6074h) [reset = 103h]

CTRLMMR_PCIE1_CTRL is shown in Figure 6-64 and described in Table 6-130.

Return to Summary Table.

Controls PCIe1 operation.

Table 6-129. CTRLMMR_PCIE1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4074h	0010 6074h

Figure 6-64. CTRLMMR_PCIE1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							LANE_COUNT
R-0h							R/W-1h
7	6	5	4	3	2	1	0
MODE_SEL	RESERVED					GENERATION_SEL	
R/W-0h	R-0h					R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-130. CTRLMMR_PCIE1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	LANE_COUNT	R/W	1h	Configures the PCIe lane count 0h - Select 1-lane operation 1h - Select 2-lane operation
7	MODE_SEL	R/W	0h	Selects the operating mode 0h - Endpoint 1h - Root Complex
6-2	RESERVED	R	0h	Reserved
1-0	GENERATION_SEL	R/W	3h	Configures the PCIe generation support in the PCIe capabilities linked-list 0h - Reserved 1h - Gen2 - Controller advertises Gen1 & Gen2 capability and link operates at either speed 2h - Gen3 - Controller advertises Gen1, Gen2, & Gen3 capability and link operates at any of the three speeds 3h - Gen4 - Controller advertises Gen1, Gen2, Gen3, & Gen4 capability and link operates at any of the four speeds

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6.65 CTRLMMR_PCIE2_CTRL Register (Proxy0 Offset = 4078h; Proxy1 Offset = 6078h) [reset = 103h]

CTRLMMR_PCIE2_CTRL is shown in Figure 6-65 and described in Table 6-132.

Return to Summary Table.

Controls PCIe2 operation.

Table 6-131. CTRLMMR_PCIE2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4078h	0010 6078h

Figure 6-65. CTRLMMR_PCIE2_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							LANE_COUNT
R-0h							R/W-1h
7	6	5	4	3	2	1	0
MODE_SEL	RESERVED					GENERATION_SEL	
R/W-0h	R-0h					R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-132. CTRLMMR_PCIE2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	LANE_COUNT	R/W	1h	Configures the PCIe lane count 0h - Select 1-lane operation 1h - Select 2-lane operation
7	MODE_SEL	R/W	0h	Selects the operating mode 0h - Endpoint 1h - Root Complex
6-2	RESERVED	R	0h	Reserved
1-0	GENERATION_SEL	R/W	3h	Configures the PCIe generation support in the PCIe capabilities linked-list 0h - Reserved 1h - Gen2 - Controller advertises Gen1 & Gen2 capability and link operates at either speed 2h - Gen3 - Controller advertises Gen1, Gen2, & Gen3 capability and link operates at any of the three speeds 3h - Gen4 - Controller advertises Gen1, Gen2, Gen3, & Gen4 capability and link operates at any of the four speeds

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6.66 CTRLMMR_PCIE3_CTRL Register (Proxy0 Offset = 407Ch; Proxy1 Offset = 607Ch) [reset = 103h]

CTRLMMR_PCIE3_CTRL is shown in Figure 6-66 and described in Table 6-134.

Return to Summary Table.

Controls PCIe3 operation.

Table 6-133. CTRLMMR_PCIE3_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 407Ch	0010 607Ch

Figure 6-66. CTRLMMR_PCIE3_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							LANE_COUNT
R-0h							R/W-1h
7	6	5	4	3	2	1	0
MODE_SEL	RESERVED					GENERATION_SEL	
R/W-0h	R-0h					R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-134. CTRLMMR_PCIE3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	LANE_COUNT	R/W	1h	Configures the PCIe lane count 0h - Select 1-lane operation 1h - Select 2-lane operation
7	MODE_SEL	R/W	0h	Selects the operating mode 0h - Endpoint 1h - Root Complex
6-2	RESERVED	R	0h	Reserved
1-0	GENERATION_SEL	R/W	3h	Configures the PCIe generation support in the PCIe capabilities linked-list 0h - Reserved 1h - Gen2 - Controller advertises Gen1 & Gen2 capability and link operates at either speed 2h - Gen3 - Controller advertises Gen1, Gen2, & Gen3 capability and link operates at any of the three speeds 3h - Gen4 - Controller advertises Gen1, Gen2, Gen3, & Gen4 capability and link operates at any of the four speeds

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6.67 CTRLMMR_SERDES0_LN0_CTRL Register (Proxy0 Offset = 4080h; Proxy1 Offset = 6080h) [reset = 0h]

CTRLMMR_SERDES0_LN0_CTRL is shown in Figure 6-67 and described in Table 6-136.

Return to Summary Table.

Controls 2-L SERDES0 lane0 selection.

Table 6-135. CTRLMMR_SERDES0_LN0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4080h	0010 6080h

Figure 6-67. CTRLMMR_SERDES0_LN0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-136. CTRLMMR_SERDES0_LN0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES0 lane0 function 0h - Enet Switch Q/SGMII Lane 1 1h - PCIe0 Lane0 2h - For USB0 lane swap. Select this if USB0 was implemented with Type C connector 3h - Not used

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6.68 CTRLMMR_SERDES0_LN1_CTRL Register (Proxy0 Offset = 4084h; Proxy1 Offset = 6084h) [reset = 0h]

CTRLMMR_SERDES0_LN1_CTRL is shown in Figure 6-68 and described in Table 6-138.

Return to Summary Table.

Controls 2-L SERDES0 lane1 selection.

Table 6-137. CTRLMMR_SERDES0_LN1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4084h	0010 6084h

Figure 6-68. CTRLMMR_SERDES0_LN1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-138. CTRLMMR_SERDES0_LN1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES0 lane1 function 0h - IP1 - Enet Switch Q/SGMII Lane 2 1h - IP2 - PCIe0 Lane1 2h - IP3 - USB0 3h - IP4 - Not Used

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6.69 CTRLMMR_SERDES1_LN0_CTRL Register (Proxy0 Offset = 4090h; Proxy1 Offset = 6090h) [reset = 0h]

CTRLMMR_SERDES1_LN0_CTRL is shown in Figure 6-69 and described in Table 6-140.

Return to Summary Table.

Controls 2-L SERDES1 lane0 selection.

Table 6-139. CTRLMMR_SERDES1_LN0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4090h	0010 6090h

Figure 6-69. CTRLMMR_SERDES1_LN0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-140. CTRLMMR_SERDES1_LN0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES1 lane0 function 0h - Enet Switch Q/SGMII Lane 3 1h - PCIe1 Lane 0 2h - For USB1 lane swap. Select this if USB1 was implemented with Type C connector 3h - ICSS_G1 SGMII Lane 0

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6.70 CTRLMMR_SERDES1_LN1_CTRL Register (Proxy0 Offset = 4094h; Proxy1 Offset = 6094h) [reset = 0h]

CTRLMMR_SERDES1_LN1_CTRL is shown in Figure 6-70 and described in Table 6-142.

Return to Summary Table.

Controls 2-L SERDES1 lane1 selection.

Table 6-141. CTRLMMR_SERDES1_LN1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4094h	0010 6094h

Figure 6-70. CTRLMMR_SERDES1_LN1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-142. CTRLMMR_SERDES1_LN1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES1 lane1 function 0h - Enet Switch Q/SGMII Lane 4 1h - PCIe1 Lane 1 2h - USB1 3h - ICSS_G1 SGMII Lane 1

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6.71 CTRLMMR_SERDES2_LN0_CTRL Register (Proxy0 Offset = 40A0h; Proxy1 Offset = 60A0h) [reset = 0h]

CTRLMMR_SERDES2_LN0_CTRL is shown in Figure 6-71 and described in Table 6-144.

Return to Summary Table.

Controls 2-L SERDES2 lane0 selection.

Table 6-143. CTRLMMR_SERDES2_LN0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40A0h	0010 60A0h

Figure 6-71. CTRLMMR_SERDES2_LN0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-144. CTRLMMR_SERDES2_LN0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES2 lane0 function 0h - Not Used 1h - PCIE2 Lane 0 2h - For USB1 lane swap. Select this if USB1 was implemented with Type C connector 3h - ICSS_G1 SGMII Lane 0

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6.72 CTRLMMR_SERDES2_LN1_CTRL Register (Proxy0 Offset = 40A4h; Proxy1 Offset = 60A4h) [reset = 0h]

CTRLMMR_SERDES2_LN1_CTRL is shown in Figure 6-72 and described in Table 6-146.

Return to Summary Table.

Controls 2-L SERDES2 lane1 selection.

Table 6-145. CTRLMMR_SERDES2_LN1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40A4h	0010 60A4h

Figure 6-72. CTRLMMR_SERDES2_LN1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-146. CTRLMMR_SERDES2_LN1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES2 lane1 function 0h - Not Used 1h - PCIE2 Lane 1 2h - USB1 3h - ICSS_G1 SGMII Lane 1

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6.73 CTRLMMR_SERDES3_LN0_CTRL Register (Proxy0 Offset = 40B0h; Proxy1 Offset = 60B0h) [reset = 0h]

CTRLMMR_SERDES3_LN0_CTRL is shown in Figure 6-73 and described in Table 6-148.

Return to Summary Table.

Controls 2-L SERDES3 lane0 selection.

Table 6-147. CTRLMMR_SERDES3_LN0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40B0h	0010 60B0h

Figure 6-73. CTRLMMR_SERDES3_LN0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-148. CTRLMMR_SERDES3_LN0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES3 lane0 function 0h - Not Used 1h - PCIE3 Lane 0 2h - For USB0 lane swap. Select this if USB0 was implemented with Type C connector 3h - Not Used

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6.74 CTRLMMR_SERDES3_LN1_CTRL Register (Proxy0 Offset = 40B4h; Proxy1 Offset = 60B4h) [reset = 0h]

CTRLMMR_SERDES3_LN1_CTRL is shown in Figure 6-74 and described in Table 6-150.

Return to Summary Table.

Controls 2-L SERDES3 lane1 selection.

Table 6-149. CTRLMMR_SERDES3_LN1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40B4h	0010 60B4h

Figure 6-74. CTRLMMR_SERDES3_LN1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-150. CTRLMMR_SERDES3_LN1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES3 lane1 function 0h - Not Used 1h - PCIE3 Lane 1 2h - USB0 3h - Not Used

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6.75 CTRLMMR_SERDES4_LN0_CTRL Register (Proxy0 Offset = 40C0h; Proxy1 Offset = 60C0h) [reset = 0h]

CTRLMMR_SERDES4_LN0_CTRL is shown in Figure 6-75 and described in Table 6-152.

Return to Summary Table.

Controls 4-L SERDES4 lane0 selection.

Table 6-151. CTRLMMR_SERDES4_LN0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40C0h	0010 60C0h

Figure 6-75. CTRLMMR_SERDES4_LN0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-152. CTRLMMR_SERDES4_LN0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES4 lane0 function 0h - eDP Lane 0 1h - Not Used 2h - Enet Switch Q/SGMII Lane 5 3h - Not Used

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6.76 CTRLMMR_SERDES4_LN1_CTRL Register (Proxy0 Offset = 40C4h; Proxy1 Offset = 60C4h) [reset = 0h]

CTRLMMR_SERDES4_LN1_CTRL is shown in Figure 6-76 and described in Table 6-154.

Return to Summary Table.

Controls 4-L SERDES4 lane1 selection.

Table 6-153. CTRLMMR_SERDES4_LN1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40C4h	0010 60C4h

Figure 6-76. CTRLMMR_SERDES4_LN1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-154. CTRLMMR_SERDES4_LN1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES4 lane1 function 0h - eDP Lane 1 1h - Not Used 2h - Enet Switch Q/SGMII Lane 6 3h - Not Used

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6.77 CTRLMMR_SERDES4_LN2_CTRL Register (Proxy0 Offset = 40C8h; Proxy1 Offset = 60C8h) [reset = 0h]

CTRLMMR_SERDES4_LN2_CTRL is shown in Figure 6-77 and described in Table 6-156.

Return to Summary Table.

Controls 4-L SERDES4 lane2 selection.

Table 6-155. CTRLMMR_SERDES4_LN2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40C8h	0010 60C8h

Figure 6-77. CTRLMMR_SERDES4_LN2_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-156. CTRLMMR_SERDES4_LN2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES4 lane2 function 0h - eDP Lane 2 1h - Not Used 2h - Enet Switch Q/SGMII Lane 7 3h - Not Used

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6.78 CTRLMMR_SERDES4_LN3_CTRL Register (Proxy0 Offset = 40CCh; Proxy1 Offset = 60CCh) [reset = 0h]

CTRLMMR_SERDES4_LN3_CTRL is shown in Figure 6-78 and described in Table 6-158.

Return to Summary Table.

Controls 4-L SERDES4 lane3 selection.

Table 6-157. CTRLMMR_SERDES4_LN3_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40CCh	0010 60CCh

Figure 6-78. CTRLMMR_SERDES4_LN3_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-158. CTRLMMR_SERDES4_LN3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the SERDES4 lane3 function 0h - eDP Lane 3 1h - Not Used 2h - Enet Switch Q/SGMII Lane 8 3h - Not Used

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6.79 CTRLMMR_SERDES0_CTRL Register (Proxy0 Offset = 40E0h; Proxy1 Offset = 60E0h) [reset = 0h]

CTRLMMR_SERDES0_CTRL is shown in Figure 6-79 and described in Table 6-160.

Return to Summary Table.

Controls SERDES0 operation.

Table 6-159. CTRLMMR_SERDES0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40E0h	0010 60E0h

Figure 6-79. CTRLMMR_SERDES0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							RET_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-160. CTRLMMR_SERDES0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	RET_EN	R/W	0h	Retention enable
7-0	RESERVED	R	0h	Reserved

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6.80 CTRLMMR_SERDES1_CTRL Register (Proxy0 Offset = 40E4h; Proxy1 Offset = 60E4h) [reset = 0h]

CTRLMMR_SERDES1_CTRL is shown in Figure 6-80 and described in Table 6-162.

Return to Summary Table.

Controls SERDES1 operation.

Table 6-161. CTRLMMR_SERDES1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40E4h	0010 60E4h

Figure 6-80. CTRLMMR_SERDES1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							RET_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-162. CTRLMMR_SERDES1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	RET_EN	R/W	0h	Retention enable
7-0	RESERVED	R	0h	Reserved

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6.81 CTRLMMR_SERDES2_CTRL Register (Proxy0 Offset = 40E8h; Proxy1 Offset = 60E8h) [reset = 0h]

CTRLMMR_SERDES2_CTRL is shown in Figure 6-81 and described in Table 6-164.

Return to Summary Table.

Controls SERDES2 operation.

Table 6-163. CTRLMMR_SERDES2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40E8h	0010 60E8h

Figure 6-81. CTRLMMR_SERDES2_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							RET_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-164. CTRLMMR_SERDES2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	RET_EN	R/W	0h	Retention enable
7-0	RESERVED	R	0h	Reserved

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6.82 CTRLMMR_SERDES3_CTRL Register (Proxy0 Offset = 40ECh; Proxy1 Offset = 60ECh) [reset = 0h]

CTRLMMR_SERDES3_CTRL is shown in Figure 6-82 and described in Table 6-166.

Return to Summary Table.

Controls SERDES3 operation.

Table 6-165. CTRLMMR_SERDES3_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40ECh	0010 60ECh

Figure 6-82. CTRLMMR_SERDES3_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							RET_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-166. CTRLMMR_SERDES3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	RET_EN	R/W	0h	Retention enable
7-0	RESERVED	R	0h	Reserved

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6.83 CTRLMMR_SERDES4_CTRL Register (Proxy0 Offset = 40F0h; Proxy1 Offset = 60F0h) [reset = 0h]

CTRLMMR_SERDES4_CTRL is shown in Figure 6-83 and described in Table 6-168.

Return to Summary Table.

Controls SERDES4 operation.

Table 6-167. CTRLMMR_SERDES4_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 40F0h	0010 60F0h

Figure 6-83. CTRLMMR_SERDES4_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED			REF_SEL	RESERVED			RET_EN
R-0h			R/W-0h	R-0h			R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-168. CTRLMMR_SERDES4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R	0h	Reserved
12	REF_SEL	R/W	0h	REFCLK output select
11-9	RESERVED	R	0h	Reserved
8	RET_EN	R/W	0h	Retention enable
7-0	RESERVED	R	0h	Reserved

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6.84 CTRLMMR_ICSSG0_CTRL0 Register (Proxy0 Offset = 4100h; Proxy1 Offset = 6100h) [reset = 0h]

CTRLMMR_ICSSG0_CTRL0 is shown in Figure 6-84 and described in Table 6-170.

Return to Summary Table.

Controls ICSS_G0 operation.

Table 6-169. CTRLMMR_ICSSG0_CTRL0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4100h	0010 6100h

Figure 6-84. CTRLMMR_ICSSG0_CTRL0 Register

31	30	29	28	27	26	25	24
RESERVED							RGMII0_ID_MODE
R-0h							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				GPM_BIDI			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
GPM_BIDI							
R/W-0h							
7	6	5	4	3	2	1	0
GPM_BIDI							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-170. CTRLMMR_ICSSG0_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RGMII0_ID_MODE	R/W	0h	Controls the ICSS_G0 RGMII0 port internal transmit delay 0h - Internal transmit delay is enabled 1h - Internal transmit delay is not enabled. TX clock rising edge is aligned with TX data
23-20	RESERVED	R	0h	Reserved
19-0	GPM_BIDI	R/W	0h	Controls operation of the ICSS_G0 PRU0_GPO pins. Each bit n controls the corresponding PRG0_PRU0GPOn I/O 0h - In GPO mode, pin n functions as GPM output only 1h - In GPO mode, pin n functions as GPM output or GPN input. Direction is controlled by the ICSS-G0 _pr1_edio0_data_out_en[n] output.

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6.85 CTRLMMR_ICSSG0_CTRL1 Register (Proxy0 Offset = 4104h; Proxy1 Offset = 6104h) [reset = 0h]

CTRLMMR_ICSSG0_CTRL1 is shown in Figure 6-85 and described in Table 6-172.

Return to Summary Table.

Controls ICSS_G0 operation.

Table 6-171. CTRLMMR_ICSSG0_CTRL1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4104h	0010 6104h

Figure 6-85. CTRLMMR_ICSSG0_CTRL1 Register

31	30	29	28	27	26	25	24
RESERVED							RGMII1_ID_MODE
R-0h							R/W-0h
23	22	21	20	19	18	17	16
RESERVED				GPM_BIDI			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
GPM_BIDI							
R/W-0h							
7	6	5	4	3	2	1	0
GPM_BIDI							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-172. CTRLMMR_ICSSG0_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	RGMII1_ID_MODE	R/W	0h	Controls the ICSS_G0 RGMII1 port internal transmit delay 0h - Internal transmit delay is enabled 1h - Internal transmit delay is not enabled. TX clock rising edge is aligned with TX data
23-20	RESERVED	R	0h	Reserved
19-0	GPM_BIDI	R/W	0h	Controls operation of the ICSS_G0 PRU1_GPO pins. Each bit n controls the corresponding PRG0_PRU1GPOn I/O 0h - In GPO mode, pin n functions as GPM output only 1h - In GPO mode, pin n functions as GPM output or GPN input. Direction is controlled by the ICSS-G0 _pr1_edio1_data_out_en[n] output.

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6.86 CTRLMMR_ICSSG1_CTRL0 Register (Proxy0 Offset = 4110h; Proxy1 Offset = 6110h) [reset = 0h]

CTRLMMR_ICSSG1_CTRL0 is shown in Figure 6-86 and described in Table 6-174.

Return to Summary Table.

Controls ICSS_G1 operation.

Table 6-173. CTRLMMR_ICSSG1_CTRL0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4110h	0010 6110h

Figure 6-86. CTRLMMR_ICSSG1_CTRL0 Register

31	30	29	28	27	26	25	24
RESERVED			SGMII_SERDES_SEL	RESERVED			RGMII0_ID_MODE
R-0h			R/W-0h	R-0h			R/W-0h
23	22	21	20	19	18	17	16
RESERVED				GPM_BIDI			
R-0h				R/W-0h			
15	14	13	12	11	10	9	8
GPM_BIDI							
R/W-0h							
7	6	5	4	3	2	1	0
GPM_BIDI							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-174. CTRLMMR_ICSSG1_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	SGMII_SERDES_SEL	R/W	0h	SGMII0 Serdes Selection. ICSSG1 SGMII Lane 0 interface can be mapped to 2 different SERDES controllers. This bit selects which SERDES drives the SGMII0 input clock, data and control signals. Programming should align with the CTRLMMR_SERDES1_LN0_CTRL and CTRLMMR_SERDES2_LN0_CTRL lane_func_sel programming. 0h - SERDES1 drives SGMII Lane 0 inputs 1h - SERDES2 drives SGMII Lane 0 inputs
27-25	RESERVED	R	0h	Reserved
24	RGMII0_ID_MODE	R/W	0h	Controls the ICSS_G1 RGMII0 port internal transmit delay 0h - Internal transmit delay is enabled 1h - Internal transmit delay is not enabled. TX clock rising edge is aligned with TX data
23-20	RESERVED	R	0h	Reserved
19-0	GPM_BIDI	R/W	0h	Controls operation of the ICSS_G1 PRU0_GPO pins. Each bit n controls the corresponding PRG1_PRU0GPOn I/O 0h - In GPO mode, pin n functions as GPM output only 1h - In GPO mode, pin n functions as GPM output or GPN input. Direction is controlled by the ICSS-G1 _pr1_edio0_data_out_en[n] output.

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6.87 CTRLMMR_ICSSG1_CTRL1 Register (Proxy0 Offset = 4114h; Proxy1 Offset = 6114h) [reset = 0h]

CTRLMMR_ICSSG1_CTRL1 is shown in Figure 6-87 and described in Table 6-176.

Return to Summary Table.

Controls ICSS_G1 operation.

Table 6-175. CTRLMMR_ICSSG1_CTRL1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4114h	0010 6114h

Figure 6-87. CTRLMMR_ICSSG1_CTRL1 Register

31	30	29	28	27	26	25	24
RESERVED			SGMII_SERDES_SEL	RESERVED			RGMII1_ID_MODE
R-0h			R/W-0h	R-0h			R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				GPM_BIDI			
R-0h				R/W-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
GPM_BIDI							
R/W-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GPM_BIDI							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-176. CTRLMMR_ICSSG1_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	0h	Reserved
28	SGMII_SERDES_SEL	R/W	0h	SGMII1 Serdes Selection. ICSSG1 SGMII Lane 1 interface can be mapped to 2 different SERDES controllers. This bit selects which SERDES drives the SGMII1 input clock, data and control signals. Programming should align with the CTRLMMR_SERDES1_LN1_CTRL and CTRLMMR_SERDES2_LN1_CTRL lane_func_sel programming. 0h - SERDES1 drives SGMII Lane 1 inputs 1h - SERDES2 drives SGMII Lane 1 inputs
27-25	RESERVED	R	0h	Reserved
24	RGMII1_ID_MODE	R/W	0h	Controls the ICSS_G1 RGMII1 port internal transmit delay 0h - Internal transmit delay is enabled 1h - Internal transmit delay is not enabled. TX clock rising edge is aligned with TX data
23-20	RESERVED	R	0h	Reserved
19-0	GPM_BIDI	R/W	0h	Controls operation of the ICSS_G1 PRU1_GPO pins. Each bit n controls the corresponding PRG1_PRU1GPOn I/O 0h - In GPO mode, pin n functions as GPM output only 1h - In GPO mode, pin n functions as GPM output or GPN input. Direction is controlled by the ICSS-G1 _pr1_edio1_data_out_en[n] output.

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6.88 CTRLMMR_EPWM0_CTRL Register (Proxy0 Offset = 4140h; Proxy1 Offset = 6140h) [reset = 0h]

CTRLMMR_EPWM0_CTRL is shown in Figure 6-88 and described in Table 6-178.

Return to Summary Table.

Controls eHRPWM0 Operation.

Table 6-177. CTRLMMR_EPWM0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4140h	0010 6140h

Figure 6-88. CTRLMMR_EPWM0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					SYNCIN_SEL		
R-0h					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED			EALLOW	RESERVED			TB_CLKEN
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-178. CTRLMMR_EPWM0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	SYNCIN_SEL	R/W	0h	Selects the source of the PWM0 synchronization input 0h - PWM0_SYNCIN Pin 1h - None 2h - None 3h - None 4h - ICSSG0 Host Interrupt 6 5h - ICSSG1 Host Interrupt 6 6h - None 7h - None
7-5	RESERVED	R	0h	Reserved
4	EALLOW	R/W	0h	Enable write access to ePWM tripzone and HRPWM config registers 0h - Disabled 1h - Enabled
3-1	RESERVED	R	0h	Reserved
0	TB_CLKEN	R/W	0h	Enable eHRPWM timebase clock 0h - Disabled 1h - Enabled

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6.89 CTRLMMR_EPWM1_CTRL Register (Proxy0 Offset = 4144h; Proxy1 Offset = 6144h) [reset = 0h]

CTRLMMR_EPWM1_CTRL is shown in Figure 6-89 and described in Table 6-180.

Return to Summary Table.

Controls eHRPWM1 Operation.

Table 6-179. CTRLMMR_EPWM1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4144h	0010 6144h

Figure 6-89. CTRLMMR_EPWM1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			EALLOW	RESERVED			TB_CLKEN
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-180. CTRLMMR_EPWM1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	EALLOW	R/W	0h	Enable write access to ePWM tripzone and HRPWM config registers 0h - Disabled 1h - Enabled
3-1	RESERVED	R	0h	Reserved
0	TB_CLKEN	R/W	0h	Enable eHRPWM timebase clock 0h - Disabled 1h - Enabled

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6.90 CTRLMMR_EPWM2_CTRL Register (Proxy0 Offset = 4148h; Proxy1 Offset = 6148h) [reset = 0h]

CTRLMMR_EPWM2_CTRL is shown in Figure 6-90 and described in Table 6-182.

Return to Summary Table.

Controls eHRPWM2 Operation.

Table 6-181. CTRLMMR_EPWM2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4148h	0010 6148h

Figure 6-90. CTRLMMR_EPWM2_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			EALLOW	RESERVED			TB_CLKEN
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-182. CTRLMMR_EPWM2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	EALLOW	R/W	0h	Enable write access to ePWM tripzone and HRPWM config registers 0h - Disabled 1h - Enabled
3-1	RESERVED	R	0h	Reserved
0	TB_CLKEN	R/W	0h	Enable eHRPWM timebase clock 0h - Disabled 1h - Enabled

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6.91 CTRLMMR_EPWM3_CTRL Register (Proxy0 Offset = 414Ch; Proxy1 Offset = 614Ch) [reset = 0h]

CTRLMMR_EPWM3_CTRL is shown in Figure 6-91 and described in Table 6-184.

Return to Summary Table.

Controls eHRPWM3 Operation.

Table 6-183. CTRLMMR_EPWM3_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 414Ch	0010 614Ch

Figure 6-91. CTRLMMR_EPWM3_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED					SYNCIN_SEL		
R-0h					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED			EALLOW	RESERVED			TB_CLKEN
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-184. CTRLMMR_EPWM3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	0h	Reserved
10-8	SYNCIN_SEL	R/W	0h	Selects the source of the PWM3 synchronization input 0h - PWM3_SYNCIN Pin 1h - PWM2 syncout signal, daisy chained 2h - None 3h - None 4h - ICSSG0 Host Interrupt 7 5h - ICSSG1 Host Interrupt 7 6h - None 7h - None
7-5	RESERVED	R	0h	Reserved
4	EALLOW	R/W	0h	Enable write access to ePWM tripzone and HRPWM config registers 0h - Disabled 1h - Enabled
3-1	RESERVED	R	0h	Reserved
0	TB_CLKEN	R/W	0h	Enable eHRPWM timebase clock 0h - Disabled 1h - Enabled

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6.92 CTRLMMR_EPWM4_CTRL Register (Proxy0 Offset = 4150h; Proxy1 Offset = 6150h) [reset = 0h]

CTRLMMR_EPWM4_CTRL is shown in Figure 6-92 and described in Table 6-186.

Return to Summary Table.

Controls eHRPWM4 Operation.

Table 6-185. CTRLMMR_EPWM4_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4150h	0010 6150h

Figure 6-92. CTRLMMR_EPWM4_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			EALLOW	RESERVED			TB_CLKEN
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-186. CTRLMMR_EPWM4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	EALLOW	R/W	0h	Enable write access to ePWM tripzone and HRPWM config registers 0h - Disabled 1h - Enabled
3-1	RESERVED	R	0h	Reserved
0	TB_CLKEN	R/W	0h	Enable eHRPWM timebase clock 0h - Disabled 1h - Enabled

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6.93 CTRLMMR_EPWM5_CTRL Register (Proxy0 Offset = 4154h; Proxy1 Offset = 6154h) [reset = 0h]

CTRLMMR_EPWM5_CTRL is shown in Figure 6-93 and described in Table 6-188.

Return to Summary Table.

Controls eHRPWM5 Operation.

Table 6-187. CTRLMMR_EPWM5_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4154h	0010 6154h

Figure 6-93. CTRLMMR_EPWM5_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			EALLOW	RESERVED			TB_CLKEN
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-188. CTRLMMR_EPWM5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	EALLOW	R/W	0h	Enable write access to ePWM tripzone and HRPWM config registers 0h - Disabled 1h - Enabled
3-1	RESERVED	R	0h	Reserved
0	TB_CLKEN	R/W	0h	Enable eHRPWM timebase clock 0h - Disabled 1h - Enabled

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6.94 CTRLMMR_SOCA_SEL Register (Proxy0 Offset = 4160h; Proxy1 Offset = 6160h) [reset = 0h]

CTRLMMR_SOCA_SEL is shown in Figure 6-94 and described in Table 6-190.

Return to Summary Table.

Selects Start of Conversion A output signal source. Each eHRPWM provides a SOCA event that can be used to trigger external ADCs. All eHRPWM SOCA events are ORed together allowing any of the 6 eHRPWMs to generate the event (if enabled within the eHRPWM). This event is then muxed with an ICSSx host interrupt allowing either an ICSSx or eHRPWMs to source the SOCA event pin.

Table 6-189. CTRLMMR_SOCA_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4160h	0010 6160h

Figure 6-94. CTRLMMR_SOCA_SEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						SOCA_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-190. CTRLMMR_SOCA_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	SOCA_SEL	R/W	0h	Selects the SOC A output source 0h - OR of all eHRPWM SOCA outputs 1h - ICSSG0 Host Interrupt 1 2h - ICSSG1 Host Interrupt 1 3h - None

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6.95 CTRLMMR_SOCB_SEL Register (Proxy0 Offset = 4164h; Proxy1 Offset = 6164h) [reset = 0h]

CTRLMMR_SOCB_SEL is shown in Figure 6-95 and described in Table 6-192.

Return to Summary Table.

Selects Start of Conversion B output signal source. Each eHRPWM provides a SOCB event that can be used to trigger external ADCs. All eHRPWM SOCB events are ORed together allowing any of the 6 eHRPWMs to generate the event (if enabled within the eHRPWM). This event is then muxed with an ICSSx host interrupt allowing either an ICSSx or eHRPWMs to source the SOCB event pin.

Table 6-191. CTRLMMR_SOCB_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4164h	0010 6164h

Figure 6-95. CTRLMMR_SOCB_SEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						SOCB_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-192. CTRLMMR_SOCB_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	SOCB_SEL	R/W	0h	Selects the SOC B output source 0h - OR of all eHRPWM SOCB ouputs 1h - ICSSG0 Host Interrupt 2 2h - ICSSG1 Host Interrupt 2 3h - None

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6.96 CTRLMMR_EQEP_STAT Register (Proxy0 Offset = 41A0h; Proxy1 Offset = 61A0h) [reset = X]

CTRLMMR_EQEP_STAT is shown in Figure 6-96 and described in Table 6-194.

Return to Summary Table.

Displays status of EQEP modules.

Table 6-193. CTRLMMR_EQEP_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 41A0h	0010 61A0h

Figure 6-96. CTRLMMR_EQEP_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					PHASE_ERR2	PHASE_ERR1	PHASE_ERR0
R-0h					R-X	R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 6-194. CTRLMMR_EQEP_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2	PHASE_ERR2	R	X	eQEP2 Phase error status 0h - No error 1h - Phase error occurred
1	PHASE_ERR1	R	X	eQEP1 Phase error status 0h - No error 1h - Phase error occurred
0	PHASE_ERR0	R	X	eQEP0 Phase error status 0h - No error 1h - Phase error occurred

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6.97 CTRLMMR_SDIO1_CTRL Register (Proxy0 Offset = 41B4h; Proxy1 Offset = 61B4h) [reset = X]

CTRLMMR_SDIO1_CTRL is shown in Figure 6-97 and described in Table 6-196.

Return to Summary Table.

Controls drive strength of MMC1 SDIO mode pins.

Table 6-195. CTRLMMR_SDIO1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 41B4h	0010 61B4h

Figure 6-97. CTRLMMR_SDIO1_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DRV_STR			
R-0h																												R/W-X			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-196. CTRLMMR_SDIO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	DRV_STR	R/W	X	Selects the SDIO drive strength

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6.98 CTRLMMR_SDIO2_CTRL Register (Proxy0 Offset = 41B8h; Proxy1 Offset = 61B8h) [reset = X]

CTRLMMR_SDIO2_CTRL is shown in Figure 6-98 and described in Table 6-198.

Return to Summary Table.

Controls drive strength of MMC2 SDIO mode pins.

Table 6-197. CTRLMMR_SDIO2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 41B8h	0010 61B8h

Figure 6-98. CTRLMMR_SDIO2_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												DRV_STR			
R-0h																												R/W-X			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-198. CTRLMMR_SDIO2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	DRV_STR	R/W	X	Selects the SDIO drive strength

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6.99 CTRLMMR_MLB_SIG_IO_CTRL Register (Proxy0 Offset = 41C0h; Proxy1 Offset = 61C0h) [reset = X]

CTRLMMR_MLB_SIG_IO_CTRL is shown in Figure 6-99 and described in Table 6-200.

Return to Summary Table.

Controls the characteristics of the MLB SIG IO.

Table 6-199. CTRLMMR_MLB_SIG_IO_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 41C0h	0010 61C0h

Figure 6-99. CTRLMMR_MLB_SIG_IO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED						AUXTRIM	
R-0h						R/W-X	

23	22	21	20	19	18	17	16
RESERVED						TXTRIM	
R-0h						R/W-X	

15	14	13	12	11	10	9	8
RESERVED				TXDRV			
R-0h				R/W-X			

7	6	5	4	3	2	1	0
RESERVED				INT_RTERM_EN	RTERM		
R-0h				R/W-X	R/W-X		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-200. CTRLMMR_MLB_SIG_IO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	AUXTRIM	R/W	X	LVDS aux drive output current ratio trim for VOD offset compenstaion 0h - -8% 1h - 0% 2h - +9% 3h - +20%
23-18	RESERVED	R	0h	Reserved
17-16	TXTRIM	R/W	X	LVDS drive output current ratio trim 0h - -8% 1h - 0% 2h - +9% 3h - +20%
15-12	RESERVED	R	0h	Reserved

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Table 6-200. CTRLMMR_MLB_SIG_IO_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	TXDRV	R/W	X	LVDS drive current. 0h - 0.0 mA 1h - 0.8 mA 2h - 1.6 mA 3h - 2.4 mA 4h - 3.2 mA 5h - 4.0 mA 6h - 4.8 mA 7h - 5.6 mA 8h - 6.4 mA 9h - 7.2 mA Ah - 8.0 mA Bh - 8.8 mA Ch - 9.6 mA Dh - 10.4 mA Eh - 11.2 mA Fh - 12.0 mA
7-4	RESERVED	R	0h	Reserved
3	INT_RTERM_EN	R/W	X	Internal termination resistor control 0h - Disable internal termination resistor 1h - Enable internal termination resistor
2-0	RTERM	R/W	X	Selects the internal termination resistor trim value. This bitfield is valid only if en_int_res is 1. Should be set to the correct value to provide 100 ohms. Typical termination values are: 0h - 77 ohm 1h - 81 ohm 2h - 86 ohm 3h - 91 ohm 4h - 96 ohm 5h - 102 ohm 6h - 110 ohm 7h - 118 ohm

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6.100 CTRLMMR_MLB_DAT_IO_CTRL Register (Proxy0 Offset = 41C4h; Proxy1 Offset = 61C4h) [reset = X]

CTRLMMR_MLB_DAT_IO_CTRL is shown in Figure 6-100 and described in Table 6-202.

Return to Summary Table.

Controls the characteristics of the MLB DATA IO.

Table 6-201. CTRLMMR_MLB_DAT_IO_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 41C4h	0010 61C4h

Figure 6-100. CTRLMMR_MLB_DAT_IO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED						AUXTRIM	
R-0h						R/W-X	

23	22	21	20	19	18	17	16
RESERVED						TXTRIM	
R-0h						R/W-X	

15	14	13	12	11	10	9	8
RESERVED				TXDRV			
R-0h				R/W-X			

7	6	5	4	3	2	1	0
RESERVED				INT_RTERM_EN	RTERM		
R-0h				R/W-X	R/W-X		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-202. CTRLMMR_MLB_DAT_IO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R	0h	Reserved
25-24	AUXTRIM	R/W	X	LVDS aux drive output current ratio trim for VOD offset compenstaion 0h - -8% 1h - 0% 2h - +9% 3h - +20%
23-18	RESERVED	R	0h	Reserved
17-16	TXTRIM	R/W	X	LVDS drive output current ratio trim 0h - -8% 1h - 0% 2h - +9% 3h - +20%
15-12	RESERVED	R	0h	Reserved

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Table 6-202. CTRLMMR_MLB_DAT_IO_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	TXDRV	R/W	X	LVDS drive current. 0h - 0.0 mA 1h - 0.8 mA 2h - 1.6 mA 3h - 2.4 mA 4h - 3.2 mA 5h - 4.0 mA 6h - 4.8 mA 7h - 5.6 mA 8h - 6.4 mA 9h - 7.2 mA Ah - 8.0 mA Bh - 8.8 mA Ch - 9.6 mA Dh - 10.4 mA Eh - 11.2 mA Fh - 12.0 mA
7-4	RESERVED	R	0h	Reserved
3	INT_RTERM_EN	R/W	X	Internal termination resistor control: 0h - Disable internal termination resistor 1h - Enable internal termination resistor
2-0	RTERM	R/W	X	Selects the internal termination resistor trim value. This bitfield is valid only if en_int_res is 1. Should be set to the correct value to provide 100 ohms. Typical termination values are: 0h - 77 ohm 1h - 81 ohm 2h - 86 ohm 3h - 91 ohm 4h - 96 ohm 5h - 102 ohm 6h - 110 ohm 7h - 118 ohm

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6.101 CTRLMMR_MLB_CLK_IO_CTRL Register (Proxy0 Offset = 41C8h; Proxy1 Offset = 61C8h) [reset = X]

CTRLMMR_MLB_CLK_IO_CTRL is shown in Figure 6-101 and described in Table 6-204.

Return to Summary Table.

Controls the characteristics of the MLB CLK IO.

Table 6-203. CTRLMMR_MLB_CLK_IO_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 41C8h	0010 61C8h

Figure 6-101. CTRLMMR_MLB_CLK_IO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED						TXTRIM	
R-0h						R/W-X	

15	14	13	12	11	10	9	8
RESERVED				TXDRV			
R-0h				R/W-X			

7	6	5	4	3	2	1	0
RESERVED				INT_RTERM_EN	RTERM		
R-0h				R/W-X	R/W-X		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-204. CTRLMMR_MLB_CLK_IO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	0h	Reserved
17-16	TXTRIM	R/W	X	LVDS drive output current ratio trim 0h - -8% 1h - 0% 2h - +9% 3h - +20%
15-12	RESERVED	R	0h	Reserved

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Table 6-204. CTRLMMR_MLB_CLK_IO_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	TXDRV	R/W	X	LVDS drive current. 0h - 0.0 mA 1h - 0.8 mA 2h - 1.6 mA 3h - 2.4 mA 4h - 3.2 mA 5h - 4.0 mA 6h - 4.8 mA 7h - 5.6 mA 8h - 6.4 mA 9h - 7.2 mA Ah - 8.0 mA Bh - 8.8 mA Ch - 9.6 mA Dh - 10.4 mA Eh - 11.2 mA Fh - 12.0 mA
7-4	RESERVED	R	0h	Reserved
3	INT_RTERM_EN	R/W	X	Internal termination resistor control: 0h - Disable internal termination resistor 1h - Enable internal termination resistor
2-0	RTERM	R/W	X	Selects the internal termination resistor trim value. This bitfield is valid only if en_int_res is 1. Should be set to the correct value to provide 100 ohms. Typical termination values are: 0h - 77 ohm 1h - 81 ohm 2h - 86 ohm 3h - 91 ohm 4h - 96 ohm 5h - 102 ohm 6h - 110 ohm 7h - 118 ohm

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6.102 CTRLMMR_MLB_GPIO_CTRL Register (Proxy0 Offset = 41D0h; Proxy1 Offset = 61D0h) [reset = 1h]

CTRLMMR_MLB_GPIO_CTRL is shown in Figure 6-102 and described in Table 6-206.

Return to Summary Table.

Controls the MLB GPIO operation.

Table 6-205. CTRLMMR_MLB_GPIO_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 41D0h	0010 61D0h

Figure 6-102. CTRLMMR_MLB_GPIO_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							MLB_MODE_EN
R-0h							R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-206. CTRLMMR_MLB_GPIO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	MLB_MODE_EN	R/W	1h	Controls operation of MLB IOs 0h - MLB IOs are used for GPIO function 1h - MLB IOs are used for MLB function

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6.103 CTRLMMR_TIMER0_CTRL Register (Proxy0 Offset = 4200h; Proxy1 Offset = 6200h) [reset = 0h]

CTRLMMR_TIMER0_CTRL is shown in Figure 6-103 and described in Table 6-208.

Return to Summary Table.

Controls TIMER0 operation.

Table 6-207. CTRLMMR_TIMER0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4200h	0010 6200h

Figure 6-103. CTRLMMR_TIMER0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-208. CTRLMMR_TIMER0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER0 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.104 CTRLMMR_TIMER1_CTRL Register (Proxy0 Offset = 4204h; Proxy1 Offset = 6204h) [reset = 0h]

CTRLMMR_TIMER1_CTRL is shown in Figure 6-104 and described in Table 6-210.

Return to Summary Table.

Controls TIMER1 operation.

Table 6-209. CTRLMMR_TIMER1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4204h	0010 6204h

Figure 6-104. CTRLMMR_TIMER1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-210. CTRLMMR_TIMER1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER1 to TIMER0
7-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER1 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.105 CTRLMMR_TIMER2_CTRL Register (Proxy0 Offset = 4208h; Proxy1 Offset = 6208h) [reset = 0h]

CTRLMMR_TIMER2_CTRL is shown in Figure 6-105 and described in Table 6-212.

Return to Summary Table.

Controls TIMER2 operation.

Table 6-211. CTRLMMR_TIMER2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4208h	0010 6208h

Figure 6-105. CTRLMMR_TIMER2_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-212. CTRLMMR_TIMER2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER2 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.106 CTRLMMR_TIMER3_CTRL Register (Proxy0 Offset = 420Ch; Proxy1 Offset = 620Ch) [reset = 0h]

CTRLMMR_TIMER3_CTRL is shown in Figure 6-106 and described in Table 6-214.

Return to Summary Table.

Controls TIMER3 operation.

Table 6-213. CTRLMMR_TIMER3_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 420Ch	0010 620Ch

Figure 6-106. CTRLMMR_TIMER3_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-214. CTRLMMR_TIMER3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER3 to TIMER2
7-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER3 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.107 CTRLMMR_TIMER4_CTRL Register (Proxy0 Offset = 4210h; Proxy1 Offset = 6210h) [reset = 0h]

CTRLMMR_TIMER4_CTRL is shown in Figure 6-107 and described in Table 6-216.

Return to Summary Table.

Controls TIMER4 operation.

Table 6-215. CTRLMMR_TIMER4_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4210h	0010 6210h

Figure 6-107. CTRLMMR_TIMER4_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-216. CTRLMMR_TIMER4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER4 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.108 CTRLMMR_TIMER5_CTRL Register (Proxy0 Offset = 4214h; Proxy1 Offset = 6214h) [reset = 0h]

CTRLMMR_TIMER5_CTRL is shown in Figure 6-108 and described in Table 6-218.

Return to Summary Table.

Controls TIMER5 operation.

Table 6-217. CTRLMMR_TIMER5_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4214h	0010 6214h

Figure 6-108. CTRLMMR_TIMER5_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-218. CTRLMMR_TIMER5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER5 to TIMER4
7-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER5 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.109 CTRLMMR_TIMER6_CTRL Register (Proxy0 Offset = 4218h; Proxy1 Offset = 6218h) [reset = 0h]

CTRLMMR_TIMER6_CTRL is shown in Figure 6-109 and described in Table 6-220.

Return to Summary Table.

Controls TIMER6 operation.

Table 6-219. CTRLMMR_TIMER6_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4218h	0010 6218h

Figure 6-109. CTRLMMR_TIMER6_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-220. CTRLMMR_TIMER6_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER6 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.110 CTRLMMR_TIMER7_CTRL Register (Proxy0 Offset = 421Ch; Proxy1 Offset = 621Ch) [reset = 0h]

CTRLMMR_TIMER7_CTRL is shown in Figure 6-110 and described in Table 6-222.

Return to Summary Table.

Controls TIMER7 operation.

Table 6-221. CTRLMMR_TIMER7_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 421Ch	0010 621Ch

Figure 6-110. CTRLMMR_TIMER7_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-222. CTRLMMR_TIMER7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER7 to TIMER6
7-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER7 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.111 CTRLMMR_TIMER8_CTRL Register (Proxy0 Offset = 4220h; Proxy1 Offset = 6220h) [reset = 0h]

CTRLMMR_TIMER8_CTRL is shown in Figure 6-111 and described in Table 6-224.

Return to Summary Table.

Controls TIMER8 operation.

Table 6-223. CTRLMMR_TIMER8_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4220h	0010 6220h

Figure 6-111. CTRLMMR_TIMER8_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-224. CTRLMMR_TIMER8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER8 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.112 CTRLMMR_TIMER9_CTRL Register (Proxy0 Offset = 4224h; Proxy1 Offset = 6224h) [reset = 0h]

CTRLMMR_TIMER9_CTRL is shown in Figure 6-112 and described in Table 6-226.

Return to Summary Table.

Controls TIMER9 operation.

Table 6-225. CTRLMMR_TIMER9_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4224h	0010 6224h

Figure 6-112. CTRLMMR_TIMER9_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-226. CTRLMMR_TIMER9_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER9 to TIMER8
7-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER9 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.113 CTRLMMR_TIMER10_CTRL Register (Proxy0 Offset = 4228h; Proxy1 Offset = 6228h) [reset = 0h]

CTRLMMR_TIMER10_CTRL is shown in Figure 6-113 and described in Table 6-228.

Return to Summary Table.

Controls TIMER10 operation.

Table 6-227. CTRLMMR_TIMER10_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4228h	0010 6228h

Figure 6-113. CTRLMMR_TIMER10_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-228. CTRLMMR_TIMER10_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER10 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.114 CTRLMMR_TIMER11_CTRL Register (Proxy0 Offset = 422Ch; Proxy1 Offset = 622Ch) [reset = 0h]

CTRLMMR_TIMER11_CTRL is shown in Figure 6-114 and described in Table 6-230.

Return to Summary Table.

Controls TIMER11 operation.

Table 6-229. CTRLMMR_TIMER11_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 422Ch	0010 622Ch

Figure 6-114. CTRLMMR_TIMER11_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-230. CTRLMMR_TIMER11_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER11 to TIMER10
7-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER11 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.115 CTRLMMR_TIMER12_CTRL Register (Proxy0 Offset = 4230h; Proxy1 Offset = 6230h) [reset = 0h]

CTRLMMR_TIMER12_CTRL is shown in Figure 6-115 and described in Table 6-232.

Return to Summary Table.

Controls TIMER12 operation.

Table 6-231. CTRLMMR_TIMER12_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4230h	0010 6230h

Figure 6-115. CTRLMMR_TIMER12_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-232. CTRLMMR_TIMER12_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER12 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.116 CTRLMMR_TIMER13_CTRL Register (Proxy0 Offset = 4234h; Proxy1 Offset = 6234h) [reset = 0h]

CTRLMMR_TIMER13_CTRL is shown in Figure 6-116 and described in Table 6-234.

Return to Summary Table.

Controls TIMER13 operation.

Table 6-233. CTRLMMR_TIMER13_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4234h	0010 6234h

Figure 6-116. CTRLMMR_TIMER13_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-234. CTRLMMR_TIMER13_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER13 to TIMER12
7-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER13 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.117 CTRLMMR_TIMER14_CTRL Register (Proxy0 Offset = 4238h; Proxy1 Offset = 6238h) [reset = 0h]

CTRLMMR_TIMER14_CTRL is shown in Figure 6-117 and described in Table 6-236.

Return to Summary Table.

Controls TIMER14 operation.

Table 6-235. CTRLMMR_TIMER14_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4238h	0010 6238h

Figure 6-117. CTRLMMR_TIMER14_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-236. CTRLMMR_TIMER14_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER14 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.118 CTRLMMR_TIMER15_CTRL Register (Proxy0 Offset = 423Ch; Proxy1 Offset = 623Ch) [reset = 0h]

CTRLMMR_TIMER15_CTRL is shown in Figure 6-118 and described in Table 6-238.

Return to Summary Table.

Controls TIMER15 operation.

Table 6-237. CTRLMMR_TIMER15_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 423Ch	0010 623Ch

Figure 6-118. CTRLMMR_TIMER15_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-238. CTRLMMR_TIMER15_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER15 to TIMER14
7-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER15 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.119 CTRLMMR_TIMER16_CTRL Register (Proxy0 Offset = 4240h; Proxy1 Offset = 6240h) [reset = 0h]

CTRLMMR_TIMER16_CTRL is shown in Figure 6-119 and described in Table 6-240.

Return to Summary Table.

Controls TIMER16 operation.

Table 6-239. CTRLMMR_TIMER16_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4240h	0010 6240h

Figure 6-119. CTRLMMR_TIMER16_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-240. CTRLMMR_TIMER16_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER16 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.120 CTRLMMR_TIMER17_CTRL Register (Proxy0 Offset = 4244h; Proxy1 Offset = 6244h) [reset = 0h]

CTRLMMR_TIMER17_CTRL is shown in Figure 6-120 and described in Table 6-242.

Return to Summary Table.

Controls TIMER17 operation.

Table 6-241. CTRLMMR_TIMER17_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4244h	0010 6244h

Figure 6-120. CTRLMMR_TIMER17_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-242. CTRLMMR_TIMER17_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER17 to TIMER16
7-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER17 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.121 CTRLMMR_TIMER18_CTRL Register (Proxy0 Offset = 4248h; Proxy1 Offset = 6248h) [reset = 0h]

CTRLMMR_TIMER18_CTRL is shown in Figure 6-121 and described in Table 6-244.

Return to Summary Table.

Controls TIMER18 operation.

Table 6-243. CTRLMMR_TIMER18_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4248h	0010 6248h

Figure 6-121. CTRLMMR_TIMER18_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-244. CTRLMMR_TIMER18_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER18 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.122 CTRLMMR_TIMER19_CTRL Register (Proxy0 Offset = 424Ch; Proxy1 Offset = 624Ch) [reset = 0h]

CTRLMMR_TIMER19_CTRL is shown in Figure 6-122 and described in Table 6-246.

Return to Summary Table.

Controls TIMER19 operation.

Table 6-245. CTRLMMR_TIMER19_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 424Ch	0010 624Ch

Figure 6-122. CTRLMMR_TIMER19_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							CASCADE_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED					CAP_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-246. CTRLMMR_TIMER19_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	CASCADE_EN	R/W	0h	Enables cascading of TIMER19 to TIMER18
7-3	RESERVED	R	0h	Reserved
2-0	CAP_SEL	R/W	0h	Selects the TIMERIO input pin for capture input signal. This control is only used when TIMER19 is configured for capture operation. 0h - Use TIMERIO0 pin 1h - Use TIMERIO1 pin 2h - Use TIMERIO2 pin 3h - Use TIMERIO3 pin 4h - Use TIMERIO4 pin 5h - Use TIMERIO5 pin 6h - Use TIMERIO6 pin 7h - Use TIMERIO7 pin

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6.123 CTRLMMR_TIMERIO0_CTRL Register (Proxy0 Offset = 4280h; Proxy1 Offset = 6280h) [reset = 0h]

CTRLMMR_TIMERIO0_CTRL is shown in Figure 6-123 and described in Table 6-248.

Return to Summary Table.

Controls TIMER_IO0 muxing.

Table 6-247. CTRLMMR_TIMERIO0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4280h	0010 6280h

Figure 6-123. CTRLMMR_TIMERIO0_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-248. CTRLMMR_TIMERIO0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	OUT_SEL	R/W	0h	Selects the source of the TIMER_IO0 output 0h - TIMERIO0 is driven by TIMER0 output 1h - TIMERIO0 is driven by TIMER1 output 2h - TIMERIO0 is driven by TIMER2 output 3h - TIMERIO0 is driven by TIMER3 output 4h - TIMERIO0 is driven by TIMER4 output 5h - TIMERIO0 is driven by TIMER5 output 6h - TIMERIO0 is driven by TIMER6 output 7h - TIMERIO0 is driven by TIMER7 output 8h - TIMERIO0 is driven by TIMER8 output 9h - TIMERIO0 is driven by TIMER9 output Ah - TIMERIO0 is driven by TIMER10 output Bh - TIMERIO0 is driven by TIMER11 output Ch - TIMERIO0 is driven by TIMER12 output Dh - TIMERIO0 is driven by TIMER13 output Eh - TIMERIO0 is driven by TIMER14 output Fh - TIMERIO0 is driven by TIMER15 output 10h - TIMERIO0 is driven by TIMER16 output 11h - TIMERIO0 is driven by TIMER17 output 12h - TIMERIO0 is driven by TIMER18 output 13h - TIMERIO0 is driven by TIMER19 output

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6.124 CTRLMMR_TIMERIO1_CTRL Register (Proxy0 Offset = 4284h; Proxy1 Offset = 6284h) [reset = 0h]

CTRLMMR_TIMERIO1_CTRL is shown in Figure 6-124 and described in Table 6-250.

Return to Summary Table.

Controls TIMER_IO1 muxing.

Table 6-249. CTRLMMR_TIMERIO1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4284h	0010 6284h

Figure 6-124. CTRLMMR_TIMERIO1_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-250. CTRLMMR_TIMERIO1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	OUT_SEL	R/W	0h	Selects the source of the TIMER_IO1 output 0h - TIMERIO1 is driven by TIMER0 output 1h - TIMERIO1 is driven by TIMER1 output 2h - TIMERIO1 is driven by TIMER2 output 3h - TIMERIO1 is driven by TIMER3 output 4h - TIMERIO1 is driven by TIMER4 output 5h - TIMERIO1 is driven by TIMER5 output 6h - TIMERIO1 is driven by TIMER6 output 7h - TIMERIO1 is driven by TIMER7 output 8h - TIMERIO1 is driven by TIMER8 output 9h - TIMERIO1 is driven by TIMER9 output Ah - TIMERIO1 is driven by TIMER10 output Bh - TIMERIO1 is driven by TIMER11 output Ch - TIMERIO1 is driven by TIMER12 output Dh - TIMERIO1 is driven by TIMER13 output Eh - TIMERIO1 is driven by TIMER14 output Fh - TIMERIO1 is driven by TIMER15 output 10h - TIMERIO1 is driven by TIMER16 output 11h - TIMERIO1 is driven by TIMER17 output 12h - TIMERIO1 is driven by TIMER18 output 13h - TIMERIO1 is driven by TIMER19 output

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6.125 CTRLMMR_TIMERIO2_CTRL Register (Proxy0 Offset = 4288h; Proxy1 Offset = 6288h) [reset = 0h]

CTRLMMR_TIMERIO2_CTRL is shown in Figure 6-125 and described in Table 6-252.

Return to Summary Table.

Controls TIMER_IO2 muxing.

Table 6-251. CTRLMMR_TIMERIO2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4288h	0010 6288h

Figure 6-125. CTRLMMR_TIMERIO2_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-252. CTRLMMR_TIMERIO2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	OUT_SEL	R/W	0h	Selects the source of the TIMER_IO2 output 0h - TIMERIO2 is driven by TIMER0 output 1h - TIMERIO2 is driven by TIMER1 output 2h - TIMERIO2 is driven by TIMER2 output 3h - TIMERIO2 is driven by TIMER3 output 4h - TIMERIO2 is driven by TIMER4 output 5h - TIMERIO2 is driven by TIMER5 output 6h - TIMERIO2 is driven by TIMER6 output 7h - TIMERIO2 is driven by TIMER7 output 8h - TIMERIO2 is driven by TIMER8 output 9h - TIMERIO2 is driven by TIMER9 output Ah - TIMERIO2 is driven by TIMER10 output Bh - TIMERIO2 is driven by TIMER11 output Ch - TIMERIO2 is driven by TIMER12 output Dh - TIMERIO2 is driven by TIMER13 output Eh - TIMERIO2 is driven by TIMER14 output Fh - TIMERIO2 is driven by TIMER15 output 10h - TIMERIO2 is driven by TIMER16 output 11h - TIMERIO2 is driven by TIMER17 output 12h - TIMERIO2 is driven by TIMER18 output 13h - TIMERIO2 is driven by TIMER19 output

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6.126 CTRLMMR_TIMERIO3_CTRL Register (Proxy0 Offset = 428Ch; Proxy1 Offset = 628Ch) [reset = 0h]

CTRLMMR_TIMERIO3_CTRL is shown in Figure 6-126 and described in Table 6-254.

Return to Summary Table.

Controls TIMER_IO3 muxing.

Table 6-253. CTRLMMR_TIMERIO3_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 428Ch	0010 628Ch

Figure 6-126. CTRLMMR_TIMERIO3_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-254. CTRLMMR_TIMERIO3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	OUT_SEL	R/W	0h	Selects the source of the TIMER_IO3 output 0h - TIMERIO3 is driven by TIMER0 output 1h - TIMERIO3 is driven by TIMER1 output 2h - TIMERIO3 is driven by TIMER2 output 3h - TIMERIO3 is driven by TIMER3 output 4h - TIMERIO3 is driven by TIMER4 output 5h - TIMERIO3 is driven by TIMER5 output 6h - TIMERIO3 is driven by TIMER6 output 7h - TIMERIO3 is driven by TIMER7 output 8h - TIMERIO3 is driven by TIMER8 output 9h - TIMERIO3 is driven by TIMER9 output Ah - TIMERIO3 is driven by TIMER10 output Bh - TIMERIO3 is driven by TIMER11 output Ch - TIMERIO3 is driven by TIMER12 output Dh - TIMERIO3 is driven by TIMER13 output Eh - TIMERIO3 is driven by TIMER14 output Fh - TIMERIO3 is driven by TIMER15 output 10h - TIMERIO3 is driven by TIMER16 output 11h - TIMERIO3 is driven by TIMER17 output 12h - TIMERIO3 is driven by TIMER18 output 13h - TIMERIO3 is driven by TIMER19 output

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6.127 CTRLMMR_TIMERIO4_CTRL Register (Proxy0 Offset = 4290h; Proxy1 Offset = 6290h) [reset = 0h]

CTRLMMR_TIMERIO4_CTRL is shown in Figure 6-127 and described in Table 6-256.

Return to Summary Table.

Controls TIMER_IO4 muxing.

Table 6-255. CTRLMMR_TIMERIO4_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4290h	0010 6290h

Figure 6-127. CTRLMMR_TIMERIO4_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-256. CTRLMMR_TIMERIO4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	OUT_SEL	R/W	0h	Selects the source of the TIMER_IO4 output 0h - TIMERIO4 is driven by TIMER0 output 1h - TIMERIO4 is driven by TIMER1 output 2h - TIMERIO4 is driven by TIMER2 output 3h - TIMERIO4 is driven by TIMER3 output 4h - TIMERIO4 is driven by TIMER4 output 5h - TIMERIO4 is driven by TIMER5 output 6h - TIMERIO4 is driven by TIMER6 output 7h - TIMERIO4 is driven by TIMER7 output 8h - TIMERIO4 is driven by TIMER8 output 9h - TIMERIO4 is driven by TIMER9 output Ah - TIMERIO4 is driven by TIMER10 output Bh - TIMERIO4 is driven by TIMER11 output Ch - TIMERIO4 is driven by TIMER12 output Dh - TIMERIO4 is driven by TIMER13 output Eh - TIMERIO4 is driven by TIMER14 output Fh - TIMERIO4 is driven by TIMER15 output 10h - TIMERIO4 is driven by TIMER16 output 11h - TIMERIO4 is driven by TIMER17 output 12h - TIMERIO4 is driven by TIMER18 output 13h - TIMERIO4 is driven by TIMER19 output

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6.128 CTRLMMR_TIMERIO5_CTRL Register (Proxy0 Offset = 4294h; Proxy1 Offset = 6294h) [reset = 0h]

CTRLMMR_TIMERIO5_CTRL is shown in Figure 6-128 and described in Table 6-258.

Return to Summary Table.

Controls TIMER_IO5 muxing.

Table 6-257. CTRLMMR_TIMERIO5_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4294h	0010 6294h

Figure 6-128. CTRLMMR_TIMERIO5_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-258. CTRLMMR_TIMERIO5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	OUT_SEL	R/W	0h	Selects the source of the TIMER_IO5 output 0h - TIMERIO5 is driven by TIMER0 output 1h - TIMERIO5 is driven by TIMER1 output 2h - TIMERIO5 is driven by TIMER2 output 3h - TIMERIO5 is driven by TIMER3 output 4h - TIMERIO5 is driven by TIMER4 output 5h - TIMERIO5 is driven by TIMER5 output 6h - TIMERIO5 is driven by TIMER6 output 7h - TIMERIO5 is driven by TIMER7 output 8h - TIMERIO5 is driven by TIMER8 output 9h - TIMERIO5 is driven by TIMER9 output Ah - TIMERIO5 is driven by TIMER10 output Bh - TIMERIO5 is driven by TIMER11 output Ch - TIMERIO5 is driven by TIMER12 output Dh - TIMERIO5 is driven by TIMER13 output Eh - TIMERIO5 is driven by TIMER14 output Fh - TIMERIO5 is driven by TIMER15 output 10h - TIMERIO5 is driven by TIMER16 output 11h - TIMERIO5 is driven by TIMER17 output 12h - TIMERIO5 is driven by TIMER18 output 13h - TIMERIO5 is driven by TIMER19 output

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6.129 CTRLMMR_TIMERIO6_CTRL Register (Proxy0 Offset = 4298h; Proxy1 Offset = 6298h) [reset = 0h]

CTRLMMR_TIMERIO6_CTRL is shown in Figure 6-129 and described in Table 6-260.

Return to Summary Table.

Controls TIMER_IO6 muxing.

Table 6-259. CTRLMMR_TIMERIO6_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4298h	0010 6298h

Figure 6-129. CTRLMMR_TIMERIO6_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-260. CTRLMMR_TIMERIO6_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	OUT_SEL	R/W	0h	Selects the source of the TIMER_IO6 output 0h - TIMERIO6 is driven by TIMER0 output 1h - TIMERIO6 is driven by TIMER1 output 2h - TIMERIO6 is driven by TIMER2 output 3h - TIMERIO6 is driven by TIMER3 output 4h - TIMERIO6 is driven by TIMER4 output 5h - TIMERIO6 is driven by TIMER5 output 6h - TIMERIO6 is driven by TIMER6 output 7h - TIMERIO6 is driven by TIMER7 output 8h - TIMERIO6 is driven by TIMER8 output 9h - TIMERIO6 is driven by TIMER9 output Ah - TIMERIO6 is driven by TIMER10 output Bh - TIMERIO6 is driven by TIMER11 output Ch - TIMERIO6 is driven by TIMER12 output Dh - TIMERIO6 is driven by TIMER13 output Eh - TIMERIO6 is driven by TIMER14 output Fh - TIMERIO6 is driven by TIMER15 output 10h - TIMERIO6 is driven by TIMER16 output 11h - TIMERIO6 is driven by TIMER17 output 12h - TIMERIO6 is driven by TIMER18 output 13h - TIMERIO6 is driven by TIMER19 output

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6.130 CTRLMMR_TIMERIO7_CTRL Register (Proxy0 Offset = 429Ch; Proxy1 Offset = 629Ch) [reset = 0h]

CTRLMMR_TIMERIO7_CTRL is shown in Figure 6-130 and described in Table 6-262.

Return to Summary Table.

Controls TIMER_IO7 muxing.

Table 6-261. CTRLMMR_TIMERIO7_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 429Ch	0010 629Ch

Figure 6-130. CTRLMMR_TIMERIO7_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												OUT_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-262. CTRLMMR_TIMERIO7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	OUT_SEL	R/W	0h	Selects the source of the TIMER_IO7 output 0h - TIMERIO7 is driven by TIMER0 output 1h - TIMERIO7 is driven by TIMER1 output 2h - TIMERIO7 is driven by TIMER2 output 3h - TIMERIO7 is driven by TIMER3 output 4h - TIMERIO7 is driven by TIMER4 output 5h - TIMERIO7 is driven by TIMER5 output 6h - TIMERIO7 is driven by TIMER6 output 7h - TIMERIO7 is driven by TIMER7 output 8h - TIMERIO7 is driven by TIMER8 output 9h - TIMERIO7 is driven by TIMER9 output Ah - TIMERIO7 is driven by TIMER10 output Bh - TIMERIO7 is driven by TIMER11 output Ch - TIMERIO7 is driven by TIMER12 output Dh - TIMERIO7 is driven by TIMER13 output Eh - TIMERIO7 is driven by TIMER14 output Fh - TIMERIO7 is driven by TIMER15 output 10h - TIMERIO7 is driven by TIMER16 output 11h - TIMERIO7 is driven by TIMER17 output 12h - TIMERIO7 is driven by TIMER18 output 13h - TIMERIO7 is driven by TIMER19 output

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6.131 CTRLMMR_I3C0_CTRL0 Register (Proxy0 Offset = 42C0h; Proxy1 Offset = 62C0h) [reset = 1020000h]

CTRLMMR_I3C0_CTRL0 is shown in Figure 6-131 and described in Table 6-264.

Return to Summary Table.

Controls I3C0 operation.

Table 6-263. CTRLMMR_I3C0_CTRL0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 42C0h	0010 62C0h

Figure 6-131. CTRLMMR_I3C0_CTRL0 Register

31	30	29	28	27	26	25	24
RESERVED	PID_MFR_ID						
R-0h	R/W-102h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MFR_ID							
R/W-102h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							ROLE
R-0h							R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PID_INSTANCE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-264. CTRLMMR_I3C0_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-16	PID_MFR_ID	R/W	102h	Manufacturer ID This input corresponds to bits[47:33] of the Provisional ID to identify the manufacturer. Defaults to TI value.
15-9	RESERVED	R	0h	Reserved
8	ROLE	R/W	0h	Master Role 0h - Main master 1h - Secondary master
7-4	RESERVED	R	0h	Reserved
3-0	PID_INSTANCE	R/W	0h	Provisional ID Instance. This input corresponds to bits[15:12] of the Provisional ID. It is intended to provide a way of differentiating several I3C devices if there would be no other way to have each manufactured device have a unique Provisional ID

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6.132 CTRLMMR_I3C0_CTRL1 Register (Proxy0 Offset = 42C4h; Proxy1 Offset = 62C4h) [reset = 0h]

CTRLMMR_I3C0_CTRL1 is shown in Figure 6-132 and described in Table 6-266.

Return to Summary Table.

Controls I3C0 operation.

Table 6-265. CTRLMMR_I3C0_CTRL1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 42C4h	0010 62C4h

Figure 6-132. CTRLMMR_I3C0_CTRL1 Register

31	30	29	28	27	26	25	24
BUS_AVAIL_TIME							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						BUS_IDLE_TIME	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
BUS_IDLE_TIME							
R/W-0h							
7	6	5	4	3	2	1	0
BUS_IDLE_TIME							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-266. CTRLMMR_I3C0_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BUS_AVAIL_TIME	R/W	0h	Indicates the number of sclk cycles in the Bus Available condition
23-18	RESERVED	R	0h	Reserved
17-0	BUS_IDLE_TIME	R/W	0h	Indicates the number of sclk cycles in the Bus Idle condition

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6.133 CTRLMMR_I3C1_CTRL0 Register (Proxy0 Offset = 42C8h; Proxy1 Offset = 62C8h) [reset = 1020000h]

CTRLMMR_I3C1_CTRL0 is shown in Figure 6-133 and described in Table 6-268.

Return to Summary Table.

Controls I3C1 operation.

Table 6-267. CTRLMMR_I3C1_CTRL0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 42C8h	0010 62C8h

Figure 6-133. CTRLMMR_I3C1_CTRL0 Register

31	30	29	28	27	26	25	24
RESERVED	PID_MFR_ID						
R-0h	R/W-102h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PID_MFR_ID							
R/W-102h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							ROLE
R-0h							R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				PID_INSTANCE			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-268. CTRLMMR_I3C1_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-16	PID_MFR_ID	R/W	102h	Manufacturer ID This input corresponds to bits[47:33] of the Provisional ID to identify the manufacturer. Defaults to TI value.
15-9	RESERVED	R	0h	Reserved
8	ROLE	R/W	0h	Master Role 0h - Main master 1h - Secondary master
7-4	RESERVED	R	0h	Reserved
3-0	PID_INSTANCE	R/W	0h	Provisional ID Instance. This input corresponds to bits[15:12] of the Provisional ID. It is intended to provide a way of differentiating several I3C devices if there would be no other way to have each manufactured device have a unique Provisional ID

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6.134 CTRLMMR_I3C1_CTRL1 Register (Proxy0 Offset = 42CCh; Proxy1 Offset = 62CCh) [reset = 0h]

CTRLMMR_I3C1_CTRL1 is shown in Figure 6-134 and described in Table 6-270.

Return to Summary Table.

Controls I3C1 operation.

Table 6-269. CTRLMMR_I3C1_CTRL1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 42CCh	0010 62CCh

Figure 6-134. CTRLMMR_I3C1_CTRL1 Register

31	30	29	28	27	26	25	24
BUS_AVAIL_TIME							
R/W-0h							
23	22	21	20	19	18	17	16
RESERVED						BUS_IDLE_TIME	
R-0h						R/W-0h	
15	14	13	12	11	10	9	8
BUS_IDLE_TIME							
R/W-0h							
7	6	5	4	3	2	1	0
BUS_IDLE_TIME							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-270. CTRLMMR_I3C1_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	BUS_AVAIL_TIME	R/W	0h	Indicates the number of sclk cycles in the Bus Available condition
23-18	RESERVED	R	0h	Reserved
17-0	BUS_IDLE_TIME	R/W	0h	Indicates the number of sclk cycles in the Bus Idle condition

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6.135 CTRLMMR_I2C0_CTRL Register (Proxy0 Offset = 42E0h; Proxy1 Offset = 62E0h) [reset = 0h]

CTRLMMR_I2C0_CTRL is shown in Figure 6-135 and described in Table 6-272.

Return to Summary Table.

Controls I2C0 operation.

Table 6-271. CTRLMMR_I2C0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 42E0h	0010 62E0h

Figure 6-135. CTRLMMR_I2C0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							HS_MCS_EN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-272. CTRLMMR_I2C0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HS_MCS_EN	R/W	0h	HS Mode master current source enable. When set, enables the current-source pull-up on the SCL output. Only one master on the I2C bus should enable SCL current sourcing.

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6.136 CTRLMMR_I2C1_CTRL Register (Proxy0 Offset = 42E4h; Proxy1 Offset = 62E4h) [reset = 0h]

CTRLMMR_I2C1_CTRL is shown in Figure 6-136 and described in Table 6-274.

Return to Summary Table.

Controls I2C1 operation.

Table 6-273. CTRLMMR_I2C1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 42E4h	0010 62E4h

Figure 6-136. CTRLMMR_I2C1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							HS_MCS_EN
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-274. CTRLMMR_I2C1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	HS_MCS_EN	R/W	0h	HS Mode master current source enable. When set, enables the current-source pull-up on the SCL output. Only one master on the I2C bus should enable SCL current sourcing.

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6.137 CTRLMMR_DPHY_TX0_CTRL Register (Proxy0 Offset = 4300h; Proxy1 Offset = 6300h) [reset = 0h]

CTRLMMR_DPHY_TX0_CTRL is shown in Figure 6-137 and described in Table 6-276.

Return to Summary Table.

Controls DPHY_TX0 Lane 0 operation.

Table 6-275. CTRLMMR_DPHY_TX0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4300h	0010 6300h

Figure 6-137. CTRLMMR_DPHY_TX0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							RESERVED
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						LANE_FUNC_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-276. CTRLMMR_DPHY_TX0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7-2	RESERVED	R	0h	Reserved
1-0	LANE_FUNC_SEL	R/W	0h	Selects the source for the 4 lanes of DPHY_TX 0 0h - IP1 (DSI0 PPI0) 1h - IP2 (CSI-TX0)

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6.138 CTRLMMR_CSI_RX_LOOPBACK Register (Proxy0 Offset = 43F0h; Proxy1 Offset = 63F0h) [reset = 0h]

CTRLMMR_CSI_RX_LOOPBACK is shown in Figure 6-138 and described in Table 6-278.

Return to Summary Table.

Controls loopback of CSI-RX inputs to CSI-TX inputs for diagnostics.

Table 6-277. CTRLMMR_CSI_RX_LOOPBACK Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 43F0h	0010 63F0h

Figure 6-138. CTRLMMR_CSI_RX_LOOPBACK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CSITX_LB_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-278. CTRLMMR_CSI_RX_LOOPBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CSITX_LB_SEL	R/W	0h	Selects the CSI-RX loopback source for CSI-TX0 . These are shown as the CSI-TX0 connections below: 0h - CSI-RX0 3h - CSI-RX 1 6h - CSI-RX 2 9h - CSI-RX 3

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6.139 CTRLMMR_GPU_GP_IN_REQ Register (Proxy0 Offset = 4500h; Proxy1 Offset = 6500h) [reset = 0h]

CTRLMMR_GPU_GP_IN_REQ is shown in Figure 6-139 and described in Table 6-280.

Return to Summary Table.

Generates GPIO input event to the GPU.

Table 6-279. CTRLMMR_GPU_GP_IN_REQ Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4500h	0010 6500h

Figure 6-139. CTRLMMR_GPU_GP_IN_REQ Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
REQ	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
DATA							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-280. CTRLMMR_GPU_GP_IN_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	REQ	R/W	0h	Input request. This bit is set to generate a GPIO request to the GPU to read the requestor data input. This bit should be cleared by the requestor after the GPU has acknowledged the request.
14-8	RESERVED	R	0h	Reserved
7-0	DATA	R/W	0h	GPIO requestor data input to the GPU

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6.140 CTRLMMR_GPU_GP_IN_ACK Register (Proxy0 Offset = 4504h; Proxy1 Offset = 6504h) [reset = X]

CTRLMMR_GPU_GP_IN_ACK is shown in Figure 6-140 and described in Table 6-282.

Return to Summary Table.

Acknowledge for GPIO input event from the GPU.

Table 6-281. CTRLMMR_GPU_GP_IN_ACK Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4504h	0010 6504h

Figure 6-140. CTRLMMR_GPU_GP_IN_ACK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ACK	RESERVED						
R-X	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 6-282. CTRLMMR_GPU_GP_IN_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	ACK	R	X	Input acknowledge. The GPU will set this bit to acknowledge a GPIO input request. This will generate a gpu_gpio_ack interrupt which will be cleared when the requestor clears the req bit in the CTRLMMR_GPU_GP_IN_REQ register.
14-0	RESERVED	R	0h	Reserved

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6.141 CTRLMMR_GPU_GP_OUT_REQ Register (Proxy0 Offset = 4508h; Proxy1 Offset = 6508h) [reset = X]

CTRLMMR_GPU_GP_OUT_REQ is shown in Figure 6-141 and described in Table 6-284.

Return to Summary Table.

Generates GPIO output event from the GPU.

Table 6-283. CTRLMMR_GPU_GP_OUT_REQ Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4508h	0010 6508h

Figure 6-141. CTRLMMR_GPU_GP_OUT_REQ Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
REQ	RESERVED						
R-X	R-0h						
7	6	5	4	3	2	1	0
DATA							
R-X							

LEGEND: R = Read Only; *-n* = value after reset

Table 6-284. CTRLMMR_GPU_GP_OUT_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	REQ	R	X	Output request. This bit is set to generate a GPIO request from the GPU to read the requestor data output. This will generat a gpu_gpio_req interrupt which will be cleared when the receiver clears the ack bit in the GPU_GPIO_OUT_ACK register. This bit will be cleared by the GPU after the request has been acknowledged.
14-8	RESERVED	R	0h	Reserved
7-0	DATA	R	X	GPIO requestor data output from the GPU

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6.142 CTRLMMR_GPU_GP_OUT_ACK Register (Proxy0 Offset = 450Ch; Proxy1 Offset = 650Ch) [reset = 0h]

CTRLMMR_GPU_GP_OUT_ACK is shown in Figure 6-142 and described in Table 6-286.

Return to Summary Table.

Acknowledge for GPIO output event to the GPU.

Table 6-285. CTRLMMR_GPU_GP_OUT_ACK Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 450Ch	0010 650Ch

Figure 6-142. CTRLMMR_GPU_GP_OUT_ACK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
ACK	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-286. CTRLMMR_GPU_GP_OUT_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	ACK	R/W	0h	Output acknowledge. The receiver of the gpu_gpio_req interrupt will set this bit to acknowledge the GPIO output request. This bit is cleared when the GPU deasserts its gpio_output_req signal.
14-0	RESERVED	R	0h	Reserved

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6.143 CTRLMMR_UFS_PHY_CAL_CTRL2 Register (Proxy0 Offset = 4548h; Proxy1 Offset = 6548h) [reset = 0h]

CTRLMMR_UFS_PHY_CAL_CTRL2 is shown in Figure 6-143 and described in Table 6-288.

Return to Summary Table.

UFS PHY Calibration Control Register 2.

Table 6-287. CTRLMMR_UFS_PHY_CAL_CTRL2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 4548h	0010 6548h

Figure 6-143. CTRLMMR_UFS_PHY_CAL_CTRL2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
TX1_LDO_LA				TX1_LDO_SA			
R/W-0h				R/W-0h			
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
TX0_LDO_LA				TX0_LDO_SA			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-288. CTRLMMR_UFS_PHY_CAL_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-20	TX1_LDO_LA	R/W	0h	TX1 DP/DN large amplitude trim value. SW needs to add an offset (+4) to the programmed trim value.
19-16	TX1_LDO_SA	R/W	0h	TX1 DP/DN small amplitude trim value. SW needs to add an offset (+4) to the programmed trim value.
15-8	RESERVED	R	0h	Reserved
7-4	TX0_LDO_LA	R/W	0h	TX0 DP/DN large amplitude trim value. SW needs to add an offset (+4) to the programmed trim value.
3-0	TX0_LDO_SA	R/W	0h	TX0 DP/DN small amplitude trim value. SW needs to add an offset (+4) to the programmed trim value.

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6.144 CTRLMMR_LOCK1_KICK0 Register (Proxy0 Offset = 5008h; Proxy1 Offset = 7008h) [reset = 0h]

CTRLMMR_LOCK1_KICK0 is shown in Figure 6-144 and described in Table 6-290.

Return to Summary Table.

Lower 32-bits of Partition1 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_LOCK1_KICK1 with its key value before write-protected Partition 1 registers can be written.

Table 6-289. CTRLMMR_LOCK1_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5008h	0010 7008h

Figure 6-144. CTRLMMR_LOCK1_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-290. CTRLMMR_LOCK1_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition1 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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6.145 CTRLMMR_LOCK1_KICK1 Register (Proxy0 Offset = 500Ch; Proxy1 Offset = 700Ch) [reset = 0h]

CTRLMMR_LOCK1_KICK1 is shown in Figure 6-145 and described in Table 6-292.

Return to Summary Table.

Upper 32-bits of Partition 1 write lock key. This register must be written with the designated key value after a write to CTRLMMR_LOCK1_KICK0 with its key value before write-protected Partition 1 registers can be written.

Table 6-291. CTRLMMR_LOCK1_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 500Ch	0010 700Ch

Figure 6-145. CTRLMMR_LOCK1_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-292. CTRLMMR_LOCK1_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition1 registers

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6.146 CTRLMMR_P1_CLAIM0 Register (Proxy0 Offset = 5100h; Proxy1 Offset = 7100h) [reset = 0h]

CTRLMMR_P1_CLAIM0 is shown in Figure 6-146 and described in Table 6-294.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-293. CTRLMMR_P1_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5100h	0010 7100h

Figure 6-146. CTRLMMR_P1_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-294. CTRLMMR_P1_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (0 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (0 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.147 CTRLMMR_P1_CLAIM1 Register (Proxy0 Offset = 5104h; Proxy1 Offset = 7104h) [reset = 0h]

CTRLMMR_P1_CLAIM1 is shown in Figure 6-147 and described in Table 6-296.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-295. CTRLMMR_P1_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5104h	0010 7104h

Figure 6-147. CTRLMMR_P1_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-296. CTRLMMR_P1_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (1 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (1 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.148 CTRLMMR_P1_CLAIM2 Register (Proxy0 Offset = 5108h; Proxy1 Offset = 7108h) [reset = 0h]

CTRLMMR_P1_CLAIM2 is shown in Figure 6-148 and described in Table 6-298.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-297. CTRLMMR_P1_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5108h	0010 7108h

Figure 6-148. CTRLMMR_P1_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-298. CTRLMMR_P1_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (2 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (2 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.149 CTRLMMR_P1_CLAIM3 Register (Proxy0 Offset = 510Ch; Proxy1 Offset = 710Ch) [reset = 0h]

CTRLMMR_P1_CLAIM3 is shown in Figure 6-149 and described in Table 6-300.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-299. CTRLMMR_P1_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 510Ch	0010 710Ch

Figure 6-149. CTRLMMR_P1_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-300. CTRLMMR_P1_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (3 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (3 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.150 CTRLMMR_P1_CLAIM4 Register (Proxy0 Offset = 5110h; Proxy1 Offset = 7110h) [reset = 0h]

CTRLMMR_P1_CLAIM4 is shown in Figure 6-150 and described in Table 6-302.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-301. CTRLMMR_P1_CLAIM4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5110h	0010 7110h

Figure 6-150. CTRLMMR_P1_CLAIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-302. CTRLMMR_P1_CLAIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (4 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (4 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.151 CTRLMMR_P1_CLAIM5 Register (Proxy0 Offset = 5114h; Proxy1 Offset = 7114h) [reset = 0h]

CTRLMMR_P1_CLAIM5 is shown in Figure 6-151 and described in Table 6-304.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-303. CTRLMMR_P1_CLAIM5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5114h	0010 7114h

Figure 6-151. CTRLMMR_P1_CLAIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-304. CTRLMMR_P1_CLAIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (5 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (5 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.152 CTRLMMR_P1_CLAIM6 Register (Proxy0 Offset = 5118h; Proxy1 Offset = 7118h) [reset = 0h]

CTRLMMR_P1_CLAIM6 is shown in Figure 6-152 and described in Table 6-306.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-305. CTRLMMR_P1_CLAIM6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5118h	0010 7118h

Figure 6-152. CTRLMMR_P1_CLAIM6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-306. CTRLMMR_P1_CLAIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (6 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (6 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.153 CTRLMMR_P1_CLAIM7 Register (Proxy0 Offset = 511Ch; Proxy1 Offset = 711Ch) [reset = 0h]

CTRLMMR_P1_CLAIM7 is shown in Figure 6-153 and described in Table 6-308.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-307. CTRLMMR_P1_CLAIM7 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 511Ch	0010 711Ch

Figure 6-153. CTRLMMR_P1_CLAIM7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-308. CTRLMMR_P1_CLAIM7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (7 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (7 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.154 CTRLMMR_P1_CLAIM8 Register (Proxy0 Offset = 5120h; Proxy1 Offset = 7120h) [reset = 0h]

CTRLMMR_P1_CLAIM8 is shown in Figure 6-154 and described in Table 6-310.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-309. CTRLMMR_P1_CLAIM8 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5120h	0010 7120h

Figure 6-154. CTRLMMR_P1_CLAIM8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-310. CTRLMMR_P1_CLAIM8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (8 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (8 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.155 CTRLMMR_P1_CLAIM9 Register (Proxy0 Offset = 5124h; Proxy1 Offset = 7124h) [reset = 0h]

CTRLMMR_P1_CLAIM9 is shown in Figure 6-155 and described in Table 6-312.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-311. CTRLMMR_P1_CLAIM9 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5124h	0010 7124h

Figure 6-155. CTRLMMR_P1_CLAIM9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-312. CTRLMMR_P1_CLAIM9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (9 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (9 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.156 CTRLMMR_P1_CLAIM10 Register (Proxy0 Offset = 5128h; Proxy1 Offset = 7128h) [reset = 0h]

CTRLMMR_P1_CLAIM10 is shown in Figure 6-156 and described in Table 6-314.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-313. CTRLMMR_P1_CLAIM10 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5128h	0010 7128h

Figure 6-156. CTRLMMR_P1_CLAIM10 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-314. CTRLMMR_P1_CLAIM10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (10 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (10 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.157 CTRLMMR_P1_CLAIM11 Register (Proxy0 Offset = 512Ch; Proxy1 Offset = 712Ch) [reset = 0h]

CTRLMMR_P1_CLAIM11 is shown in Figure 6-157 and described in Table 6-316.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-315. CTRLMMR_P1_CLAIM11 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 512Ch	0010 712Ch

Figure 6-157. CTRLMMR_P1_CLAIM11 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-316. CTRLMMR_P1_CLAIM11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (11 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (11 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.158 CTRLMMR_P1_CLAIM12 Register (Proxy0 Offset = 5130h; Proxy1 Offset = 7130h) [reset = 0h]

CTRLMMR_P1_CLAIM12 is shown in Figure 6-158 and described in Table 6-318.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-317. CTRLMMR_P1_CLAIM12 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5130h	0010 7130h

Figure 6-158. CTRLMMR_P1_CLAIM12 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-318. CTRLMMR_P1_CLAIM12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (12 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (12 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.159 CTRLMMR_P1_CLAIM13 Register (Proxy0 Offset = 5134h; Proxy1 Offset = 7134h) [reset = 0h]

CTRLMMR_P1_CLAIM13 is shown in Figure 6-159 and described in Table 6-320.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-319. CTRLMMR_P1_CLAIM13 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5134h	0010 7134h

Figure 6-159. CTRLMMR_P1_CLAIM13 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-320. CTRLMMR_P1_CLAIM13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (13 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (13 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.160 CTRLMMR_P1_CLAIM14 Register (Proxy0 Offset = 5138h; Proxy1 Offset = 7138h) [reset = 0h]

CTRLMMR_P1_CLAIM14 is shown in Figure 6-160 and described in Table 6-322.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-321. CTRLMMR_P1_CLAIM14 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5138h	0010 7138h

Figure 6-160. CTRLMMR_P1_CLAIM14 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-322. CTRLMMR_P1_CLAIM14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (14 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (14 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.161 CTRLMMR_P1_CLAIM15 Register (Proxy0 Offset = 513Ch; Proxy1 Offset = 713Ch) [reset = 0h]

CTRLMMR_P1_CLAIM15 is shown in Figure 6-161 and described in Table 6-324.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-323. CTRLMMR_P1_CLAIM15 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 513Ch	0010 713Ch

Figure 6-161. CTRLMMR_P1_CLAIM15 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-324. CTRLMMR_P1_CLAIM15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (15 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (15 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.162 CTRLMMR_P1_CLAIM16 Register (Proxy0 Offset = 5140h; Proxy1 Offset = 7140h) [reset = 0h]

CTRLMMR_P1_CLAIM16 is shown in Figure 6-162 and described in Table 6-326.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-325. CTRLMMR_P1_CLAIM16 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5140h	0010 7140h

Figure 6-162. CTRLMMR_P1_CLAIM16 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-326. CTRLMMR_P1_CLAIM16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (16 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (16 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.163 CTRLMMR_P1_CLAIM17 Register (Proxy0 Offset = 5144h; Proxy1 Offset = 7144h) [reset = 0h]

CTRLMMR_P1_CLAIM17 is shown in Figure 6-163 and described in Table 6-328.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-327. CTRLMMR_P1_CLAIM17 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5144h	0010 7144h

Figure 6-163. CTRLMMR_P1_CLAIM17 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-328. CTRLMMR_P1_CLAIM17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (17 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (17 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.164 CTRLMMR_P1_CLAIM18 Register (Proxy0 Offset = 5148h; Proxy1 Offset = 7148h) [reset = 0h]

CTRLMMR_P1_CLAIM18 is shown in Figure 6-164 and described in Table 6-330.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-329. CTRLMMR_P1_CLAIM18 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5148h	0010 7148h

Figure 6-164. CTRLMMR_P1_CLAIM18 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-330. CTRLMMR_P1_CLAIM18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (18 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (18 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.165 CTRLMMR_P1_CLAIM19 Register (Proxy0 Offset = 514Ch; Proxy1 Offset = 714Ch) [reset = 0h]

CTRLMMR_P1_CLAIM19 is shown in Figure 6-165 and described in Table 6-332.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-331. CTRLMMR_P1_CLAIM19 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 514Ch	0010 714Ch

Figure 6-165. CTRLMMR_P1_CLAIM19 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-332. CTRLMMR_P1_CLAIM19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (19 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (19 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.166 CTRLMMR_P1_CLAIM20 Register (Proxy0 Offset = 5150h; Proxy1 Offset = 7150h) [reset = 0h]

CTRLMMR_P1_CLAIM20 is shown in Figure 6-166 and described in Table 6-334.

Return to Summary Table.

Claim bits for Partition1 Registers.

Table 6-333. CTRLMMR_P1_CLAIM20 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 5150h	0010 7150h

Figure 6-166. CTRLMMR_P1_CLAIM20 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-334. CTRLMMR_P1_CLAIM20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x4000 + (20 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x6000 + (20 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.167 CTRLMMR_OBSCLK0_CTRL Register (Proxy0 Offset = 8000h; Proxy1 Offset = A000h) [reset = 1Fh]

CTRLMMR_OBSCLK0_CTRL is shown in Figure 6-167 and described in Table 6-336.

Return to Summary Table.

This register controls which internal clock is made observable on the OBSCLK[2:0] output pins.

Table 6-335. CTRLMMR_OBSCLK0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8000h	0010 A000h

Figure 6-167. CTRLMMR_OBSCLK0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h

15	14	13	12	11	10	9	8
CLK_DIV							
R/W-0h							

7	6	5	4	3	2	1	0
RESERVED			CLK_SEL				
R-0h			R/W-1Fh				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-336. CTRLMMR_OBSCLK0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the OBSCLK0 divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-8	CLK_DIV	R/W	0h	OBSCLK0 output divider Divides the selected clock by clkdiv+1 for output to the OBSCLK[2:0] pins. Supports divide by 1 to 256 (default to 1). To load the new divider value the clk_div_ld bit must be cleared and then set to 1.
7-5	RESERVED	R	0h	Reserved

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Table 6-336. CTRLMMR_OBSCLK0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CLK_SEL	R/W	1Fh	OBSCLK0 clock source selection. Selects the source of the clock to be divided by the OBSCLK0 divider and output on the OBSCLK[2:0] pins. 0h - MAIN_PLL0_HSDIV0_CLKOUT 1h - MAIN_PLL1_HSDIV0_CLKOUT 2h - MAIN_PLL2_HSDIV0_CLKOUT 3h - MAIN_PLL3_HSDIV0_CLKOUT 4h - MAIN_PLL4_HSDIV0_CLKOUT 5h - MAIN_PLL5_HSDIV0_CLKOUT 6h - MAIN_PLL6_HSDIV0_CLKOUT 7h - "0" 8h - "0" 9h - "0" Ah - "0" Bh - "0" Ch - MAIN_PLL12_HSDIV0_CLKOUT Dh - OBSCLK1 OUT Eh - MAIN_PLL14_HSDIV0_CLKOUT Fh - MAIN_PLL15_HSDIV0_CLKOUT 10h - MAIN_PLL16_HSDIV0_CLKOUT 11h - MAIN_PLL17_HSDIV0_CLKOUT 12h - MAIN_PLL18_HSDIV0_CLKOUT 13h - MAIN_PLL19_HSDIV0_CLKOUT 14h - UFS MPHY_TX_REF_SYMBOLCLK 15h - UFS MPHY_M31_VCO_19P2M_CLK 16h - UFS MPHY_M31_VCO_26M_CLK 17h - MAIN_PLL23_HSDIV0_CLKOUT 18h - MAIN_PLL24_HSDIV0_CLKOUT 19h - MAIN_PLL25_HSDIV0_CLKOUT 1Ah - CPTS_GENF3 1Bh - CLK_12M_RC 1Ch - WKUP_LFOSC0_CLKOUT 1Dh - PLLCTRL_OBSCLK 1Eh - HFOSC1_CLKOUT 1Fh - WKUP_HFOSC0_CLKOUT

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6.168 CTRLMMR_OBSCLK1_CTRL Register (Proxy0 Offset = 8004h; Proxy1 Offset = A004h) [reset = 0h]

CTRLMMR_OBSCLK1_CTRL is shown in Figure 6-168 and described in Table 6-338.

Return to Summary Table.

This register controls which internal clock is made observable on the OBSCLK1_OUT internal clock signal.

Table 6-337. CTRLMMR_OBSCLK1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8004h	0010 A004h

Figure 6-168. CTRLMMR_OBSCLK1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-338. CTRLMMR_OBSCLK1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	OBSCLK1_OUT signal output clock source selection 0h - MAIN_PLL7_HSDIV0_CLKOUT / DIV4 1h - MAIN_PLL8_HSDIV0_CLKOUT / DIV8 2h - MAIN_PLL13_HSDIV0_CLKOUT / DIV4 3h - "0"

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6.169 CTRLMMR_CLKOUT_CTRL Register (Proxy0 Offset = 8010h; Proxy1 Offset = A010h) [reset = 0h]

CTRLMMR_CLKOUT_CTRL is shown in Figure 6-169 and described in Table 6-340.

Return to Summary Table.

Enables and selects clock source of CPSW CLKOUT pin.

Table 6-339. CTRLMMR_CLKOUT_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8010h	0010 A010h

Figure 6-169. CTRLMMR_CLKOUT_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			CLK_EN	RESERVED			CLK_SEL
R-0h			R/W-0h	R-0h			R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-340. CTRLMMR_CLKOUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4	CLK_EN	R/W	0h	When set, enables CLKOUT output
3-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects CLKOUT clock source 0h - RGMII_MHZ_50_CLK (50 MHz) 1h - RGMII_MHZ_50_CLK_DIV2 (25 MHz)

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6.170 CTRLMMR_GTC_CLKSEL Register (Proxy0 Offset = 8030h; Proxy1 Offset = A030h) [reset = 0h]

CTRLMMR_GTC_CLKSEL is shown in Figure 6-170 and described in Table 6-342.

Return to Summary Table.

Selects the timebase clock source for the Global Timebase Counter.

Table 6-341. CTRLMMR_GTC_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8030h	0010 A030h

Figure 6-170. CTRLMMR_GTC_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-342. CTRLMMR_GTC_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Selects the GTC timebase clock source 0h - MAIN_PLL3_HSDIV1_CLKOUT 1h - MAIN_PLL0_HSDIV6_CLKOUT 2h - MCU_CPTS_REF_CLK (pin) 3h - CPTS_RFT_CLK (pin) 4h - MCU_EXT_REFCLK0 (pin) 5h - EXT_REFCLK1 (pin) 6h - SERDES0_IP2_LN0_TXMCLK 7h - SERDES0_IP2_LN1_TXMCLK 8h - SERDES1_IP2_LN0_TXMCLK 9h - SERDES1_IP2_LN1_TXMCLK Ah - SERDES2_IP2_LN0_TXMCLK Bh - SERDES2_IP2_LN1_TXMCLK Ch - SERDES3_IP2_LN0_TXMCLK Dh - SERDES3_IP2_LN1_TXMCLK Eh - MCU_PLL2_HSDIV1_CLKOUT Fh - MAIN_SYSCLK0

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6.171 CTRLMMR_EFUSE_CLKSEL Register (Proxy0 Offset = 803Ch; Proxy1 Offset = A03Ch) [reset = 0h]

CTRLMMR_EFUSE_CLKSEL is shown in Figure 6-171 and described in Table 6-344.

Return to Summary Table.

Selects the functional clock source for the MAIN domain eFuse Controller.

Table 6-343. CTRLMMR_EFUSE_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 803Ch	0010 A03Ch

Figure 6-171. CTRLMMR_EFUSE_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-344. CTRLMMR_EFUSE_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CLK_SEL	R/W	0h	Selects the clock source 0h - WKUP_HFOSC0_CLKOUT 1h - MAIN_SYSCLK0 / 4

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6.172 CTRLMMR_ICSSG0_CLKSEL Register (Proxy0 Offset = 8040h; Proxy1 Offset = A040h) [reset = 0h]

CTRLMMR_ICSSG0_CLKSEL is shown in Figure 6-172 and described in Table 6-346.

Return to Summary Table.

Selects the functional clock source for ICSS_G0.

Table 6-345. CTRLMMR_ICSSG0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8040h	0010 A040h

Figure 6-172. CTRLMMR_ICSSG0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED				IEP_CLKSEL			
R-0h				R/W-0h			

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							CORE_CLKSEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-346. CTRLMMR_ICSSG0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	IEP_CLKSEL	R/W	0h	Selects the ICSSG0 IEP clock source 0h - MAIN_PLL3_HSDIV1_CLKOUT 1h - MAIN_PLL0_HSDIV6_CLKOUT 2h - MCU_CPTS_REF_CLK (pin) 3h - CPTS_RFT_CLK (pin) 4h - MCU_EXT_REFCLK0 (pin) 5h - EXT_REFCLK1 (pin) 6h - SERDES0_IP2_LN0_TXMCLK 7h - SERDES0_IP2_LN1_TXMCLK 8h - SERDES1_IP2_LN0_TXMCLK 9h - SERDES1_IP2_LN1_TXMCLK Ah - SERDES2_IP2_LN0_TXMCLK Bh - SERDES2_IP2_LN1_TXMCLK Ch - SERDES3_IP2_LN0_TXMCLK Dh - SERDES3_IP2_LN1_TXMCLK Eh - MCU_PLL2_HSDIV1_CLKOUT Fh - MAIN_SYSCLK0
15-1	RESERVED	R	0h	Reserved

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Table 6-346. CTRLMMR_ICSSG0_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CORE_CLKSEL	R/W	0h	Selects the ICSSG0 functional clock source 0h - MAIN_PLL2_HSDIV0_CLKOUT 1h - MAIN_PLL3_HSDIV1_CLKOUT

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6.173 CTRLMMR_ICSSG1_CLKSEL Register (Proxy0 Offset = 8044h; Proxy1 Offset = A044h) [reset = 0h]

CTRLMMR_ICSSG1_CLKSEL is shown in Figure 6-173 and described in Table 6-348.

Return to Summary Table.

Selects the functional clock source for ICSS_G1.

Table 6-347. CTRLMMR_ICSSG1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8044h	0010 A044h

Figure 6-173. CTRLMMR_ICSSG1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED				IEP_CLKSEL			
R-0h				R/W-0h			

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							CORE_CLKSEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-348. CTRLMMR_ICSSG1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	0h	Reserved
19-16	IEP_CLKSEL	R/W	0h	Selects the ICSSG1 IEP clock source 0h - MAIN_PLL3_HSDIV1_CLKOUT 1h - MAIN_PLL0_HSDIV6_CLKOUT 2h - MCU_CPTS_REF_CLK (pin) 3h - CPTS_RFT_CLK (pin) 4h - MCU_EXT_REFCLK0 (pin) 5h - EXT_REFCLK1 (pin) 6h - SERDES0_IP2_LN0_TXMCLK 7h - SERDES0_IP2_LN1_TXMCLK 8h - SERDES1_IP2_LN0_TXMCLK 9h - SERDES1_IP2_LN1_TXMCLK Ah - SERDES2_IP2_LN0_TXMCLK Bh - SERDES2_IP2_LN1_TXMCLK Ch - SERDES3_IP2_LN0_TXMCLK Dh - SERDES3_IP2_LN1_TXMCLK Eh - MCU_PLL2_HSDIV1_CLKOUT Fh - MAIN_SYSCLK0
15-1	RESERVED	R	0h	Reserved

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Table 6-348. CTRLMMR_ICSSG1_CLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CORE_CLKSEL	R/W	0h	Selects the ICSSG1 functional clock source 0h - MAIN_PLL2_HSDIV0_CLKOUT 1h - MAIN_PLL3_HSDIV1_CLKOUT

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6.174 CTRLMMR_PCIE_REFCLK0_CLKSEL Register (Proxy0 Offset = 8070h; Proxy1 Offset = A070h) [reset = 0h]

CTRLMMR_PCIE_REFCLK0_CLKSEL is shown in Figure 6-174 and described in Table 6-350.

Return to Summary Table.

Selects the ACSPCIE clock source for the PCIE_REFCLK0 P/N output pins PCIE_REFCLK[1:0] P/N are driven by ACSPCIE0 PAD[1:0] and PCIE_REFCLK[3:2] P/N are driven by ACSPCIE1 PAD[1:0].

Table 6-349. CTRLMMR_PCIE_REFCLK0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8070h	0010 A070h

Figure 6-174. CTRLMMR_PCIE_REFCLK0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							OUT_CLK_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						OUT_CLKSEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-350. CTRLMMR_PCIE_REFCLK0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUT_CLK_EN	R/W	0h	Enables the output of the ACSPCIE buffer to drive the PCIE0 REFCLK P/N pins
7-2	RESERVED	R	0h	Reserved
1-0	OUT_CLKSEL	R/W	0h	Selects the PCIE0 REFCLK output clock source. Controls the ACSPCIE0 buffer PAD0 clock mux. 0h - SERDES0_REF_DER_OUT_CLK 1h - SERDES1_REF_DER_OUT_CLK 2h - SERDES0_REFCLK1_OUT 3h - SERDES1_REFCLK1_OUT

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6.175 CTRLMMR_PCIE_REFCLK1_CLKSEL Register (Proxy0 Offset = 8074h; Proxy1 Offset = A074h) [reset = 1h]

CTRLMMR_PCIE_REFCLK1_CLKSEL is shown in Figure 6-175 and described in Table 6-352.

Return to Summary Table.

Selects the ACSPCIE clock source for the PCIE_REFCLK1 P/N output pins PCIE_REFCLK[1:0] P/N are driven by ACSPCIE0 PAD[1:0] and PCIE_REFCLK[3:2] P/N are driven by ACSPCIE1 PAD[1:0].

Table 6-351. CTRLMMR_PCIE_REFCLK1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8074h	0010 A074h

Figure 6-175. CTRLMMR_PCIE_REFCLK1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							OUT_CLK_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						OUT_CLKSEL	
R-0h						R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-352. CTRLMMR_PCIE_REFCLK1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUT_CLK_EN	R/W	0h	Enables the output of the ACSPCIE buffer to drive the PCIE1 REFCLK P/N pins
7-2	RESERVED	R	0h	Reserved
1-0	OUT_CLKSEL	R/W	1h	Selects the PCIE1 REFCLK output clock source. Controls the ACSPCIE0 buffer PAD1 clock mux. 0h - SERDES0_REF_DER_OUT_CLK 1h - SERDES1_REF_DER_OUT_CLK 2h - SERDES0_REFCLK1_OUT 3h - SERDES1_REFCLK1_OUT

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6.176 CTRLMMR_PCIE_REFCLK2_CLKSEL Register (Proxy0 Offset = 8078h; Proxy1 Offset = A078h) [reset = 0h]

CTRLMMR_PCIE_REFCLK2_CLKSEL is shown in Figure 6-176 and described in Table 6-354.

Return to Summary Table.

Selects the ACSPCIE clock source for the PCIE_REFCLK2 P/N output pins PCIE_REFCLK[1:0] P/N are driven by ACSPCIE0 PAD[1:0] and PCIE_REFCLK[3:2] P/N are driven by ACSPCIE1 PAD[1:0].

Table 6-353. CTRLMMR_PCIE_REFCLK2_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8078h	0010 A078h

Figure 6-176. CTRLMMR_PCIE_REFCLK2_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							OUT_CLK_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						OUT_CLKSEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-354. CTRLMMR_PCIE_REFCLK2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUT_CLK_EN	R/W	0h	Enables the output of the ACSPCIE buffer to drive the PCIE2 REFCLK P/N pins
7-2	RESERVED	R	0h	Reserved
1-0	OUT_CLKSEL	R/W	0h	Selects the PCIE2 REFCLK output clock source. Controls the ACSPCIE1 buffer PAD0 clock mux. 0h - SERDES2_REF_DER_OUT_CLK 1h - SERDES3_REF_DER_OUT_CLK 2h - SERDES2_REFCLK1_OUT 3h - SERDES3_REFCLK1_OUT

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6.177 CTRLMMR_PCIE_REFCLK3_CLKSEL Register (Proxy0 Offset = 807Ch; Proxy1 Offset = A07Ch) [reset = 1h]

CTRLMMR_PCIE_REFCLK3_CLKSEL is shown in Figure 6-177 and described in Table 6-356.

Return to Summary Table.

Selects the ACSPCIE clock source for the PCIE_REFCLK3 P/N output pins PCIE_REFCLK[1:0] P/N are driven by ACSPCIE0 PAD[1:0] and PCIE_REFCLK[3:2] P/N are driven by ACSPCIE1 PAD[1:0].

Table 6-355. CTRLMMR_PCIE_REFCLK3_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 807Ch	0010 A07Ch

Figure 6-177. CTRLMMR_PCIE_REFCLK3_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							OUT_CLK_EN
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						OUT_CLKSEL	
R-0h						R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-356. CTRLMMR_PCIE_REFCLK3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	OUT_CLK_EN	R/W	0h	Enables the output of the ACSPCIE buffer to drive the PCIE3 REFCLK P/N pins
7-2	RESERVED	R	0h	Reserved
1-0	OUT_CLKSEL	R/W	1h	Selects the PCIE3 REFCLK output clock source. Controls the ACSPCIE1 buffer PAD0 clock mux. 0h - SERDES2_REF_DER_OUT_CLK 1h - SERDES3_REF_DER_OUT_CLK 2h - SERDES2_REFCLK1_OUT 3h - SERDES3_REFCLK1_OUT

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6.178 CTRLMMR_PCIE0_CLKSEL Register (Proxy0 Offset = 8080h; Proxy1 Offset = A080h) [reset = 0h]

CTRLMMR_PCIE0_CLKSEL is shown in Figure 6-178 and described in Table 6-358.

Return to Summary Table.

Selects PCIe0 functional clock sources.

Table 6-357. CTRLMMR_PCIE0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8080h	0010 A080h

Figure 6-178. CTRLMMR_PCIE0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CPTS_CLKSEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-358. CTRLMMR_PCIE0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CPTS_CLKSEL	R/W	0h	Selects the clock source for the PCIE0 Common Platform Time Stamp module 0h - MAIN_PLL3_HSDIV1_CLKOUT 1h - MAIN_PLL0_HSDIV6_CLKOUT 2h - MCU_CPTS_REF_CLK (pin) 3h - CPTS_RFT_CLK (pin) 4h - MCU_EXT_REFCLK0 (pin) 5h - EXT_REFCLK1 (pin) 6h - SERDES0_IP2_LN0_TXMCLK 7h - SERDES0_IP2_LN1_TXMCLK 8h - SERDES1_IP2_LN0_TXMCLK 9h - SERDES1_IP2_LN1_TXMCLK Ah - SERDES2_IP2_LN0_TXMCLK Bh - SERDES2_IP2_LN1_TXMCLK Ch - SERDES3_IP2_LN0_TXMCLK Dh - SERDES3_IP2_LN1_TXMCLK Eh - MCU_PLL2_HSDIV1_CLKOUT Fh - MAIN_SYSCLK0

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6.179 CTRLMMR_PCIE1_CLKSEL Register (Proxy0 Offset = 8084h; Proxy1 Offset = A084h) [reset = 0h]

CTRLMMR_PCIE1_CLKSEL is shown in Figure 6-179 and described in Table 6-360.

Return to Summary Table.

Selects PCIe1 functional clock sources.

Table 6-359. CTRLMMR_PCIE1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8084h	0010 A084h

Figure 6-179. CTRLMMR_PCIE1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CPTS_CLKSEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-360. CTRLMMR_PCIE1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CPTS_CLKSEL	R/W	0h	Selects the clock source for the PCIE1 Common Platform Time Stamp module 0h - MAIN_PLL3_HSDIV1_CLKOUT 1h - MAIN_PLL0_HSDIV6_CLKOUT 2h - MCU_CPTS_REF_CLK (pin) 3h - CPTS_RFT_CLK (pin) 4h - MCU_EXT_REFCLK0 (pin) 5h - EXT_REFCLK1 (pin) 6h - SERDES0_IP2_LN0_TXMCLK 7h - SERDES0_IP2_LN1_TXMCLK 8h - SERDES1_IP2_LN0_TXMCLK 9h - SERDES1_IP2_LN1_TXMCLK Ah - SERDES2_IP2_LN0_TXMCLK Bh - SERDES2_IP2_LN1_TXMCLK Ch - SERDES3_IP2_LN0_TXMCLK Dh - SERDES3_IP2_LN1_TXMCLK Eh - MCU_PLL2_HSDIV1_CLKOUT Fh - MAIN_SYSCLK0

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6.180 CTRLMMR_PCIE2_CLKSEL Register (Proxy0 Offset = 8088h; Proxy1 Offset = A088h) [reset = 0h]

CTRLMMR_PCIE2_CLKSEL is shown in Figure 6-180 and described in Table 6-362.

Return to Summary Table.

Selects PCIe2 functional clock sources.

Table 6-361. CTRLMMR_PCIE2_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8088h	0010 A088h

Figure 6-180. CTRLMMR_PCIE2_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CPTS_CLKSEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-362. CTRLMMR_PCIE2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CPTS_CLKSEL	R/W	0h	Selects the clock source for the PCIE2 Common Platform Time Stamp module 0h - MAIN_PLL3_HSDIV1_CLKOUT 1h - MAIN_PLL0_HSDIV6_CLKOUT 2h - MCU_CPTS_REF_CLK (pin) 3h - CPTS_RFT_CLK (pin) 4h - MCU_EXT_REFCLK0 (pin) 5h - EXT_REFCLK1 (pin) 6h - SERDES0_IP2_LN0_TXMCLK 7h - SERDES0_IP2_LN1_TXMCLK 8h - SERDES1_IP2_LN0_TXMCLK 9h - SERDES1_IP2_LN1_TXMCLK Ah - SERDES2_IP2_LN0_TXMCLK Bh - SERDES2_IP2_LN1_TXMCLK Ch - SERDES3_IP2_LN0_TXMCLK Dh - SERDES3_IP2_LN1_TXMCLK Eh - MCU_PLL2_HSDIV1_CLKOUT Fh - MAIN_SYSCLK0

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6.181 CTRLMMR_PCIE3_CLKSEL Register (Proxy0 Offset = 808Ch; Proxy1 Offset = A08Ch) [reset = 0h]

CTRLMMR_PCIE3_CLKSEL is shown in Figure 6-181 and described in Table 6-364.

Return to Summary Table.

Selects PCIe3 functional clock sources.

Table 6-363. CTRLMMR_PCIE3_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 808Ch	0010 A08Ch

Figure 6-181. CTRLMMR_PCIE3_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CPTS_CLKSEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-364. CTRLMMR_PCIE3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CPTS_CLKSEL	R/W	0h	Selects the clock source for the PCIE3 Common Platform Time Stamp module 0h - MAIN_PLL3_HSDIV1_CLKOUT 1h - MAIN_PLL0_HSDIV6_CLKOUT 2h - MCU_CPTS_REF_CLK (pin) 3h - CPTS_RFT_CLK (pin) 4h - MCU_EXT_REFCLK0 (pin) 5h - EXT_REFCLK1 (pin) 6h - SERDES0_IP2_LN0_TXMCLK 7h - SERDES0_IP2_LN1_TXMCLK 8h - SERDES1_IP2_LN0_TXMCLK 9h - SERDES1_IP2_LN1_TXMCLK Ah - SERDES2_IP2_LN0_TXMCLK Bh - SERDES2_IP2_LN1_TXMCLK Ch - SERDES3_IP2_LN0_TXMCLK Dh - SERDES3_IP2_LN1_TXMCLK Eh - MCU_PLL2_HSDIV1_CLKOUT Fh - MAIN_SYSCLK0

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6.182 CTRLMMR_CPSW_CLKSEL Register (Proxy0 Offset = 8090h; Proxy1 Offset = A090h) [reset = 0h]

CTRLMMR_CPSW_CLKSEL is shown in Figure 6-182 and described in Table 6-366.

Return to Summary Table.

Selects the 9X CP Switch clock sources.

Table 6-365. CTRLMMR_CPSW_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8090h	0010 A090h

Figure 6-182. CTRLMMR_CPSW_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CPTS_CLKSEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-366. CTRLMMR_CPSW_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CPTS_CLKSEL	R/W	0h	Selects the clock source for the CPSW9x Ethernet switch Common Platform Time Stamp module 0h - MAIN_PLL3_HSDIV1_CLKOUT 1h - MAIN_PLL0_HSDIV6_CLKOUT 2h - MCU_CPTS_REF_CLK (pin) 3h - CPTS_RFT_CLK (pin) 4h - MCU_EXT_REFCLK0 (pin) 5h - EXT_REFCLK1 (pin) 6h - SERDES0_IP2_LN0_TXMCLK 7h - SERDES0_IP2_LN1_TXMCLK 8h - SERDES1_IP2_LN0_TXMCLK 9h - SERDES1_IP2_LN1_TXMCLK Ah - SERDES2_IP2_LN0_TXMCLK Bh - SERDES2_IP2_LN1_TXMCLK Ch - SERDES3_IP2_LN0_TXMCLK Dh - SERDES3_IP2_LN1_TXMCLK Eh - MCU_PLL2_HSDIV1_CLKOUT Fh - MAIN_SYSCLK0

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6.183 CTRLMMR_NAVSS_CLKSEL Register (Proxy0 Offset = 8098h; Proxy1 Offset = A098h) [reset = 0h]

CTRLMMR_NAVSS_CLKSEL is shown in Figure 6-183 and described in Table 6-368.

Return to Summary Table.

Selects the clock source for the Nav Subsystem.

Table 6-367. CTRLMMR_NAVSS_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8098h	0010 A098h

Figure 6-183. CTRLMMR_NAVSS_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CPTS_CLKSEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-368. CTRLMMR_NAVSS_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CPTS_CLKSEL	R/W	0h	Selects the clock source for the SoC] Common Platform Time Stamp module located within the Nav Subsystem 0h - MAIN_PLL3_HSDIV1_CLKOUT 1h - MAIN_PLL0_HSDIV6_CLKOUT 2h - MCU_CPTS_REF_CLK (pin) 3h - CPTS_RFT_CLK (pin) 4h - MCU_EXT_REFCLK0 (pin) 5h - EXT_REFCLK1 (pin) 6h - SERDES0_IP2_LN0_TXMCLK 7h - SERDES0_IP2_LN1_TXMCLK 8h - SERDES1_IP2_LN0_TXMCLK 9h - SERDES1_IP2_LN1_TXMCLK Ah - SERDES2_IP2_LN0_TXMCLK Bh - SERDES2_IP2_LN1_TXMCLK Ch - SERDES3_IP2_LN0_TXMCLK Dh - SERDES3_IP2_LN1_TXMCLK Eh - MCU_PLL2_HSDIV1_CLKOUT Fh - MAIN_SYSCLK0

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6.184 CTRLMMR_EMMC0_CLKSEL Register (Proxy0 Offset = 80B0h; Proxy1 Offset = A0B0h) [reset = 0h]

CTRLMMR_EMMC0_CLKSEL is shown in Figure 6-184 and described in Table 6-370.

Return to Summary Table.

Selects the functional clock source for 8-bit eMMC0.

Table 6-369. CTRLMMR_EMMC0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 80B0h	0010 A0B0h

Figure 6-184. CTRLMMR_EMMC0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-370. CTRLMMR_EMMC0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	eMMC XIN_CLK selection 0h - MAIN_PLL0_HSDIV2_CLKOUT 1h - MAIN_PLL1_HSDIV2_CLKOUT 2h - MAIN_PLL2_HSDIV2_CLKOUT 3h - MAIN_PLL3_HSDIV2_CLKOUT

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6.185 CTRLMMR_EMMC1_CLKSEL Register (Proxy0 Offset = 80B4h; Proxy1 Offset = A0B4h) [reset = 1h]

CTRLMMR_EMMC1_CLKSEL is shown in Figure 6-185 and described in Table 6-372.

Return to Summary Table.

Selects the functional clock source for 4-bit eMMC1.

Table 6-371. CTRLMMR_EMMC1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 80B4h	0010 A0B4h

Figure 6-185. CTRLMMR_EMMC1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							LB_CLKSEL
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-1h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-372. CTRLMMR_EMMC1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	LB_CLKSEL	R/W	0h	eMMC Loopback clock selection 0h - Loopback clock from MMC1_CLKLB pad 1h - Loopback clock from MMC1_CLK pin **NOTE:** It is recommended to keep this bit to its default value of 0h.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	1h	eMMC XIN_CLK selection 0h - MAIN_PLL0_HSDIV2_CLKOUT 1h - MAIN_PLL1_HSDIV2_CLKOUT 2h - MAIN_PLL2_HSDIV2_CLKOUT 3h - MAIN_PLL3_HSDIV2_CLKOUT

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6.186 CTRLMMR_EMMC2_CLKSEL Register (Proxy0 Offset = 80B8h; Proxy1 Offset = A0B8h) [reset = 2h]

CTRLMMR_EMMC2_CLKSEL is shown in Figure 6-186 and described in Table 6-374.

Return to Summary Table.

Selects the functional clock source for 4-bit eMMC2.

Table 6-373. CTRLMMR_EMMC2_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 80B8h	0010 A0B8h

Figure 6-186. CTRLMMR_EMMC2_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							LB_CLKSEL
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-2h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-374. CTRLMMR_EMMC2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	LB_CLKSEL	R/W	0h	eMMC Loopback clock selection 0h - Loopback clock from MMC2_CLKLB pad 1h - Loopback clock from MMC2_CLK pin **NOTE:** It is recommended to keep this bit to its default value of 0h.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	2h	eMMC XIN_CLK selection 0h - MAIN_PLL0_HSDIV2_CLKOUT 1h - MAIN_PLL1_HSDIV2_CLKOUT 2h - MAIN_PLL2_HSDIV2_CLKOUT 3h - MAIN_PLL3_HSDIV2_CLKOUT

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6.187 CTRLMMR_UFS0_CLKSEL Register (Proxy0 Offset = 80C0h; Proxy1 Offset = A0C0h) [reset = 0h]

CTRLMMR_UFS0_CLKSEL is shown in Figure 6-187 and described in Table 6-376.

Return to Summary Table.

Selects the clocks for Universal Flash Storage 0 interface.

Table 6-375. CTRLMMR_UFS0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 80C0h	0010 A0C0h

Figure 6-187. CTRLMMR_UFS0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						MCLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-376. CTRLMMR_UFS0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	MCLK_SEL	R/W	0h	Selects the MPHY clock source 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL1_HSDIV6_CLKOUT 3h - EXT_REFCLK0 (pin)

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6.188 CTRLMMR_GPMC_CLKSEL Register (Proxy0 Offset = 80D0h; Proxy1 Offset = A0D0h) [reset = 0h]

CTRLMMR_GPMC_CLKSEL is shown in Figure 6-188 and described in Table 6-378.

Return to Summary Table.

Selects the bus and functional clock source for the GPMC module. This allows the GPMC to run asynchronously to the bus fabric in order to optimize parallel port performance.

Table 6-377. CTRLMMR_GPMC_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 80D0h	0010 A0D0h

Figure 6-188. CTRLMMR_GPMC_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-378. CTRLMMR_GPMC_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	Selects the GPMC clock source 0h - MAIN_PLL0_HSDIV3_CLKOUT 1h - MAIN_PLL2_HSDIV1_CLKOUT / 6 2h - MAIN_PLL2_HSDIV1_CLKOUT / 4 3h - MAIN_SYSCLK0 / 4

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6.189 CTRLMMR_USB0_CLKSEL Register (Proxy0 Offset = 80E0h; Proxy1 Offset = A0E0h) [reset = 0h]

CTRLMMR_USB0_CLKSEL is shown in Figure 6-189 and described in Table 6-380.

Return to Summary Table.

Selects the functional clock sources for USB0.

Table 6-379. CTRLMMR_USB0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 80E0h	0010 A0E0h

Figure 6-189. CTRLMMR_USB0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							REFCLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-380. CTRLMMR_USB0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	REFCLK_SEL	R/W	0h	Selects the clock source for the USB0 ref_clk. 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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6.190 CTRLMMR_USB1_CLKSEL Register (Proxy0 Offset = 80E4h; Proxy1 Offset = A0E4h) [reset = 0h]

CTRLMMR_USB1_CLKSEL is shown in Figure 6-190 and described in Table 6-382.

Return to Summary Table.

Selects the functional clock sources for USB1.

Table 6-381. CTRLMMR_USB1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 80E4h	0010 A0E4h

Figure 6-190. CTRLMMR_USB1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							REFCLK_SEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-382. CTRLMMR_USB1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	REFCLK_SEL	R/W	0h	Selects the clock source for the USB1 ref_clk. 0h - Use WKUP_HFOSC0_CLKOUT 1h - Use HFOSC1_CLKOUT

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6.191 CTRLMMR_TIMER0_CLKSEL Register (Proxy0 Offset = 8100h; Proxy1 Offset = A100h) [reset = 0h]

CTRLMMR_TIMER0_CLKSEL is shown in Figure 6-191 and described in Table 6-384.

Return to Summary Table.

Timer0 functional clock selection control.

Table 6-383. CTRLMMR_TIMER0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8100h	0010 A100h

Figure 6-191. CTRLMMR_TIMER0_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-384. CTRLMMR_TIMER0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.192 CTRLMMR_TIMER1_CLKSEL Register (Proxy0 Offset = 8104h; Proxy1 Offset = A104h) [reset = 0h]

CTRLMMR_TIMER1_CLKSEL is shown in Figure 6-192 and described in Table 6-386.

Return to Summary Table.

Timer1 functional clock selection control.

Table 6-385. CTRLMMR_TIMER1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8104h	0010 A104h

Figure 6-192. CTRLMMR_TIMER1_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-386. CTRLMMR_TIMER1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.193 CTRLMMR_TIMER2_CLKSEL Register (Proxy0 Offset = 8108h; Proxy1 Offset = A108h) [reset = 0h]

CTRLMMR_TIMER2_CLKSEL is shown in Figure 6-193 and described in Table 6-388.

Return to Summary Table.

Timer2 functional clock selection control.

Table 6-387. CTRLMMR_TIMER2_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8108h	0010 A108h

Figure 6-193. CTRLMMR_TIMER2_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-388. CTRLMMR_TIMER2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.194 CTRLMMR_TIMER3_CLKSEL Register (Proxy0 Offset = 810Ch; Proxy1 Offset = A10Ch) [reset = 0h]

CTRLMMR_TIMER3_CLKSEL is shown in Figure 6-194 and described in Table 6-390.

Return to Summary Table.

Timer3 functional clock selection control.

Table 6-389. CTRLMMR_TIMER3_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 810Ch	0010 A10Ch

Figure 6-194. CTRLMMR_TIMER3_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-390. CTRLMMR_TIMER3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.195 CTRLMMR_TIMER4_CLKSEL Register (Proxy0 Offset = 8110h; Proxy1 Offset = A110h) [reset = 0h]

CTRLMMR_TIMER4_CLKSEL is shown in Figure 6-195 and described in Table 6-392.

Return to Summary Table.

Timer4 functional clock selection control.

Table 6-391. CTRLMMR_TIMER4_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8110h	0010 A110h

Figure 6-195. CTRLMMR_TIMER4_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-392. CTRLMMR_TIMER4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.196 CTRLMMR_TIMER5_CLKSEL Register (Proxy0 Offset = 8114h; Proxy1 Offset = A114h) [reset = 0h]

CTRLMMR_TIMER5_CLKSEL is shown in Figure 6-196 and described in Table 6-394.

Return to Summary Table.

Timer5 functional clock selection control.

Table 6-393. CTRLMMR_TIMER5_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8114h	0010 A114h

Figure 6-196. CTRLMMR_TIMER5_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-394. CTRLMMR_TIMER5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.197 CTRLMMR_TIMER6_CLKSEL Register (Proxy0 Offset = 8118h; Proxy1 Offset = A118h) [reset = 0h]

CTRLMMR_TIMER6_CLKSEL is shown in Figure 6-197 and described in Table 6-396.

Return to Summary Table.

Timer6 functional clock selection control.

Table 6-395. CTRLMMR_TIMER6_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8118h	0010 A118h

Figure 6-197. CTRLMMR_TIMER6_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-396. CTRLMMR_TIMER6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.198 CTRLMMR_TIMER7_CLKSEL Register (Proxy0 Offset = 811Ch; Proxy1 Offset = A11Ch) [reset = 0h]

CTRLMMR_TIMER7_CLKSEL is shown in Figure 6-198 and described in Table 6-398.

Return to Summary Table.

Timer7 functional clock selection control.

Table 6-397. CTRLMMR_TIMER7_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 811Ch	0010 A11Ch

Figure 6-198. CTRLMMR_TIMER7_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-398. CTRLMMR_TIMER7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.199 CTRLMMR_TIMER8_CLKSEL Register (Proxy0 Offset = 8120h; Proxy1 Offset = A120h) [reset = 0h]

CTRLMMR_TIMER8_CLKSEL is shown in Figure 6-199 and described in Table 6-400.

Return to Summary Table.

Timer8 functional clock selection control.

Table 6-399. CTRLMMR_TIMER8_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8120h	0010 A120h

Figure 6-199. CTRLMMR_TIMER8_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-400. CTRLMMR_TIMER8_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.200 CTRLMMR_TIMER9_CLKSEL Register (Proxy0 Offset = 8124h; Proxy1 Offset = A124h) [reset = 0h]

CTRLMMR_TIMER9_CLKSEL is shown in Figure 6-200 and described in Table 6-402.

Return to Summary Table.

Timer9 functional clock selection control.

Table 6-401. CTRLMMR_TIMER9_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8124h	0010 A124h

Figure 6-200. CTRLMMR_TIMER9_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-402. CTRLMMR_TIMER9_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.201 CTRLMMR_TIMER10_CLKSEL Register (Proxy0 Offset = 8128h; Proxy1 Offset = A128h) [reset = 0h]

CTRLMMR_TIMER10_CLKSEL is shown in Figure 6-201 and described in Table 6-404.

Return to Summary Table.

Timer10 functional clock selection control.

Table 6-403. CTRLMMR_TIMER10_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8128h	0010 A128h

Figure 6-201. CTRLMMR_TIMER10_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-404. CTRLMMR_TIMER10_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.202 CTRLMMR_TIMER11_CLKSEL Register (Proxy0 Offset = 812Ch; Proxy1 Offset = A12Ch) [reset = 0h]

CTRLMMR_TIMER11_CLKSEL is shown in Figure 6-202 and described in Table 6-406.

Return to Summary Table.

Timer11 functional clock selection control.

Table 6-405. CTRLMMR_TIMER11_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 812Ch	0010 A12Ch

Figure 6-202. CTRLMMR_TIMER11_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-406. CTRLMMR_TIMER11_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.203 CTRLMMR_TIMER12_CLKSEL Register (Proxy0 Offset = 8130h; Proxy1 Offset = A130h) [reset = 0h]

CTRLMMR_TIMER12_CLKSEL is shown in Figure 6-203 and described in Table 6-408.

Return to Summary Table.

Timer12 functional clock selection control.

Table 6-407. CTRLMMR_TIMER12_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8130h	0010 A130h

Figure 6-203. CTRLMMR_TIMER12_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-408. CTRLMMR_TIMER12_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.204 CTRLMMR_TIMER13_CLKSEL Register (Proxy0 Offset = 8134h; Proxy1 Offset = A134h) [reset = 0h]

CTRLMMR_TIMER13_CLKSEL is shown in Figure 6-204 and described in Table 6-410.

Return to Summary Table.

Timer13 functional clock selection control.

Table 6-409. CTRLMMR_TIMER13_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8134h	0010 A134h

Figure 6-204. CTRLMMR_TIMER13_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-410. CTRLMMR_TIMER13_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.205 CTRLMMR_TIMER14_CLKSEL Register (Proxy0 Offset = 8138h; Proxy1 Offset = A138h) [reset = 0h]

CTRLMMR_TIMER14_CLKSEL is shown in Figure 6-205 and described in Table 6-412.

Return to Summary Table.

Timer14 functional clock selection control.

Table 6-411. CTRLMMR_TIMER14_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8138h	0010 A138h

Figure 6-205. CTRLMMR_TIMER14_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-412. CTRLMMR_TIMER14_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.206 CTRLMMR_TIMER15_CLKSEL Register (Proxy0 Offset = 813Ch; Proxy1 Offset = A13Ch) [reset = 0h]

CTRLMMR_TIMER15_CLKSEL is shown in Figure 6-206 and described in Table 6-414.

Return to Summary Table.

Timer15 functional clock selection control.

Table 6-413. CTRLMMR_TIMER15_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 813Ch	0010 A13Ch

Figure 6-206. CTRLMMR_TIMER15_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-414. CTRLMMR_TIMER15_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.207 CTRLMMR_TIMER16_CLKSEL Register (Proxy0 Offset = 8140h; Proxy1 Offset = A140h) [reset = 0h]

CTRLMMR_TIMER16_CLKSEL is shown in Figure 6-207 and described in Table 6-416.

Return to Summary Table.

Timer16 functional clock selection control.

Table 6-415. CTRLMMR_TIMER16_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8140h	0010 A140h

Figure 6-207. CTRLMMR_TIMER16_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-416. CTRLMMR_TIMER16_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.208 CTRLMMR_TIMER17_CLKSEL Register (Proxy0 Offset = 8144h; Proxy1 Offset = A144h) [reset = 0h]

CTRLMMR_TIMER17_CLKSEL is shown in Figure 6-208 and described in Table 6-418.

Return to Summary Table.

Timer17 functional clock selection control.

Table 6-417. CTRLMMR_TIMER17_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8144h	0010 A144h

Figure 6-208. CTRLMMR_TIMER17_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-418. CTRLMMR_TIMER17_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.209 CTRLMMR_TIMER18_CLKSEL Register (Proxy0 Offset = 8148h; Proxy1 Offset = A148h) [reset = 0h]

CTRLMMR_TIMER18_CLKSEL is shown in Figure 6-209 and described in Table 6-420.

Return to Summary Table.

Timer18 functional clock selection control.

Table 6-419. CTRLMMR_TIMER18_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8148h	0010 A148h

Figure 6-209. CTRLMMR_TIMER18_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-420. CTRLMMR_TIMER18_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.210 CTRLMMR_TIMER19_CLKSEL Register (Proxy0 Offset = 814Ch; Proxy1 Offset = A14Ch) [reset = 0h]

CTRLMMR_TIMER19_CLKSEL is shown in Figure 6-210 and described in Table 6-422.

Return to Summary Table.

Timer19 functional clock selection control.

Table 6-421. CTRLMMR_TIMER19_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 814Ch	0010 A14Ch

Figure 6-210. CTRLMMR_TIMER19_CLKSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												CLK_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-422. CTRLMMR_TIMER19_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	CLK_SEL	R/W	0h	Timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL0_HSDIV1_CLKOUT 3h - CLK_12M_RC 4h - MAIN_PLL3_HSDIV3_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - LPXOSC_CLKOUT 8h - CPTS_RFT_CLK (pin) 9h - MAIN_PLL1_HSDIV3_CLKOUT Ah - MAIN_PLL2_HSDIV6_CLKOUT Bh - MAIN_PLL4_HSDIV2_CLKOUT Ch - CPTS_GENF2 Dh - CPTS_GENF3 Eh - CPSW9G_CPTS_GENF0 Fh - MAIN_PLL15_HSDIV2_CLKOUT

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6.211 CTRLMMR_SPI0_CLKSEL Register (Proxy0 Offset = 8190h; Proxy1 Offset = A190h) [reset = 0h]

CTRLMMR_SPI0_CLKSEL is shown in Figure 6-211 and described in Table 6-424.

Return to Summary Table.

SPI0 clock control.

Table 6-423. CTRLMMR_SPI0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8190h	0010 A190h

Figure 6-211. CTRLMMR_SPI0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-424. CTRLMMR_SPI0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

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6.212 CTRLMMR_SPI1_CLKSEL Register (Proxy0 Offset = 8194h; Proxy1 Offset = A194h) [reset = 0h]

CTRLMMR_SPI1_CLKSEL is shown in Figure 6-212 and described in Table 6-426.

Return to Summary Table.

SPI1 clock control.

Table 6-425. CTRLMMR_SPI1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8194h	0010 A194h

Figure 6-212. CTRLMMR_SPI1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-426. CTRLMMR_SPI1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

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6.213 CTRLMMR_SPI2_CLKSEL Register (Proxy0 Offset = 8198h; Proxy1 Offset = A198h) [reset = 0h]

CTRLMMR_SPI2_CLKSEL is shown in Figure 6-213 and described in Table 6-428.

Return to Summary Table.

SPI2 clock control.

Table 6-427. CTRLMMR_SPI2_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8198h	0010 A198h

Figure 6-213. CTRLMMR_SPI2_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-428. CTRLMMR_SPI2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

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6.214 CTRLMMR_SPI3_CLKSEL Register (Proxy0 Offset = 819Ch; Proxy1 Offset = A19Ch) [reset = 0h]

CTRLMMR_SPI3_CLKSEL is shown in Figure 6-214 and described in Table 6-430.

Return to Summary Table.

SPI3 clock control.

Table 6-429. CTRLMMR_SPI3_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 819Ch	0010 A19Ch

Figure 6-214. CTRLMMR_SPI3_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-430. CTRLMMR_SPI3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

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6.215 CTRLMMR_SPI5_CLKSEL Register (Proxy0 Offset = 81A4h; Proxy1 Offset = A1A4h) [reset = 0h]

CTRLMMR_SPI5_CLKSEL is shown in Figure 6-215 and described in Table 6-432.

Return to Summary Table.

SPI5 clock control.

Table 6-431. CTRLMMR_SPI5_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81A4h	0010 A1A4h

Figure 6-215. CTRLMMR_SPI5_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-432. CTRLMMR_SPI5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

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6.216 CTRLMMR_SPI6_CLKSEL Register (Proxy0 Offset = 81A8h; Proxy1 Offset = A1A8h) [reset = 0h]

CTRLMMR_SPI6_CLKSEL is shown in Figure 6-216 and described in Table 6-434.

Return to Summary Table.

SPI6 clock control.

Table 6-433. CTRLMMR_SPI6_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81A8h	0010 A1A8h

Figure 6-216. CTRLMMR_SPI6_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-434. CTRLMMR_SPI6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

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6.217 CTRLMMR_SPI7_CLKSEL Register (Proxy0 Offset = 81ACh; Proxy1 Offset = A1ACh) [reset = 0h]

CTRLMMR_SPI7_CLKSEL is shown in Figure 6-217 and described in Table 6-436.

Return to Summary Table.

SPI7 clock control.

Table 6-435. CTRLMMR_SPI7_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81ACh	0010 A1ACh

Figure 6-217. CTRLMMR_SPI7_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							MSTR_LB_CLKSEL
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-436. CTRLMMR_SPI7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	MSTR_LB_CLKSEL	R/W	0h	Master mode receive capture clock loopback selection 0h - Internal clock loopback 1h - Loopback from pad
15-0	RESERVED	R	0h	Reserved

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6.218 CTRLMMR_USART0_CLK_CTRL Register (Proxy0 Offset = 81C0h; Proxy1 Offset = A1C0h) [reset = 3h]

CTRLMMR_USART0_CLK_CTRL is shown in Figure 6-218 and described in Table 6-438.

Return to Summary Table.

Selects the clock divider of the USART0 functional clock.

Table 6-437. CTRLMMR_USART0_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81C0h	0010 A1C0h

Figure 6-218. CTRLMMR_USART0_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						CLK_DIV	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-438. CTRLMMR_USART0_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART0 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. 0h - Divide by 1 1h - Divide by 2 2h - Divide by 3 3h - Divide by 4

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6.219 CTRLMMR_USART1_CLK_CTRL Register (Proxy0 Offset = 81C4h; Proxy1 Offset = A1C4h) [reset = 3h]

CTRLMMR_USART1_CLK_CTRL is shown in Figure 6-219 and described in Table 6-440.

Return to Summary Table.

Selects the clock divider of the USART1 functional clock.

Table 6-439. CTRLMMR_USART1_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81C4h	0010 A1C4h

Figure 6-219. CTRLMMR_USART1_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						CLK_DIV	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-440. CTRLMMR_USART1_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART1 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. 0h - Divide by 1 1h - Divide by 2 2h - Divide by 3 3h - Divide by 4

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6.220 CTRLMMR_USART2_CLK_CTRL Register (Proxy0 Offset = 81C8h; Proxy1 Offset = A1C8h) [reset = 3h]

CTRLMMR_USART2_CLK_CTRL is shown in Figure 6-220 and described in Table 6-442.

Return to Summary Table.

Selects the clock divider of the USART2 functional clock.

Table 6-441. CTRLMMR_USART2_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81C8h	0010 A1C8h

Figure 6-220. CTRLMMR_USART2_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_DIV	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-442. CTRLMMR_USART2_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART2 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. 0h - Divide by 1 1h - Divide by 2 2h - Divide by 3 3h - Divide by 4

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6.221 CTRLMMR_USART3_CLK_CTRL Register (Proxy0 Offset = 81CCh; Proxy1 Offset = A1CCh) [reset = 3h]

CTRLMMR_USART3_CLK_CTRL is shown in Figure 6-221 and described in Table 6-444.

Return to Summary Table.

Selects the clock divider of the USART3 functional clock.

Table 6-443. CTRLMMR_USART3_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81CCh	0010 A1CCh

Figure 6-221. CTRLMMR_USART3_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						CLK_DIV	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-444. CTRLMMR_USART3_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART3 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. 0h - Divide by 1 1h - Divide by 2 2h - Divide by 3 3h - Divide by 4

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6.222 CTRLMMR_USART4_CLK_CTRL Register (Proxy0 Offset = 81D0h; Proxy1 Offset = A1D0h) [reset = 3h]

CTRLMMR_USART4_CLK_CTRL is shown in Figure 6-222 and described in Table 6-446.

Return to Summary Table.

Selects the clock divider of the USART4 functional clock.

Table 6-445. CTRLMMR_USART4_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81D0h	0010 A1D0h

Figure 6-222. CTRLMMR_USART4_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_DIV	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-446. CTRLMMR_USART4_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART4 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. 0h - Divide by 1 1h - Divide by 2 2h - Divide by 3 3h - Divide by 4

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6.223 CTRLMMR_USART5_CLK_CTRL Register (Proxy0 Offset = 81D4h; Proxy1 Offset = A1D4h) [reset = 3h]

CTRLMMR_USART5_CLK_CTRL is shown in Figure 6-223 and described in Table 6-448.

Return to Summary Table.

Selects the clock divider of the USART5 functional clock.

Table 6-447. CTRLMMR_USART5_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81D4h	0010 A1D4h

Figure 6-223. CTRLMMR_USART5_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						CLK_DIV	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-448. CTRLMMR_USART5_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART5 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. 0h - Divide by 1 1h - Divide by 2 2h - Divide by 3 3h - Divide by 4

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6.224 CTRLMMR_USART6_CLK_CTRL Register (Proxy0 Offset = 81D8h; Proxy1 Offset = A1D8h) [reset = 3h]

CTRLMMR_USART6_CLK_CTRL is shown in Figure 6-224 and described in Table 6-450.

Return to Summary Table.

Selects the clock divider of the USART6 functional clock.

Table 6-449. CTRLMMR_USART6_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81D8h	0010 A1D8h

Figure 6-224. CTRLMMR_USART6_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							CLK_DIV_LD
R-0h							R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						CLK_DIV	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-450. CTRLMMR_USART6_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART6 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. 0h - Divide by 1 1h - Divide by 2 2h - Divide by 3 3h - Divide by 4

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6.225 CTRLMMR_USART7_CLK_CTRL Register (Proxy0 Offset = 81DCh; Proxy1 Offset = A1DCh) [reset = 3h]

CTRLMMR_USART7_CLK_CTRL is shown in Figure 6-225 and described in Table 6-452.

Return to Summary Table.

Selects the clock divider of the USART7 functional clock.

Table 6-451. CTRLMMR_USART7_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81DCh	0010 A1DCh

Figure 6-225. CTRLMMR_USART7_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						CLK_DIV	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-452. CTRLMMR_USART7_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART7 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. 0h - Divide by 1 1h - Divide by 2 2h - Divide by 3 3h - Divide by 4

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6.226 CTRLMMR_USART8_CLK_CTRL Register (Proxy0 Offset = 81E0h; Proxy1 Offset = A1E0h) [reset = 3h]

CTRLMMR_USART8_CLK_CTRL is shown in Figure 6-226 and described in Table 6-454.

Return to Summary Table.

Selects the clock divider of the USART8 functional clock.

Table 6-453. CTRLMMR_USART8_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81E0h	0010 A1E0h

Figure 6-226. CTRLMMR_USART8_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							CLK_DIV_LD
R-0h							R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						CLK_DIV	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-454. CTRLMMR_USART8_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART8 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. 0h - Divide by 1 1h - Divide by 2 2h - Divide by 3 3h - Divide by 4

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6.227 CTRLMMR_USART9_CLK_CTRL Register (Proxy0 Offset = 81E4h; Proxy1 Offset = A1E4h) [reset = 3h]

CTRLMMR_USART9_CLK_CTRL is shown in Figure 6-227 and described in Table 6-456.

Return to Summary Table.

Selects the clock divider of the USART9 functional clock.

Table 6-455. CTRLMMR_USART9_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 81E4h	0010 A1E4h

Figure 6-227. CTRLMMR_USART9_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							CLK_DIV_LD
R-0h							R/W-0h

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED						CLK_DIV	
R-0h						R/W-3h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-456. CTRLMMR_USART9_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	CLK_DIV_LD	R/W	0h	Load the output divider value Writing 1 to this bit will generate a load pulse to load the USART9 clock programmable divider value. This bit can be cleared but must not be set in the same write cycle in which the clk_div value is changed.
15-2	RESERVED	R	0h	Reserved
1-0	CLK_DIV	R/W	3h	Selects the clock divider value. Supports divide values of 1 to 4 Default is /4. To load the new divider value the clk_div_ld bit must be cleared and then set to 1. 0h - Divide by 1 1h - Divide by 2 2h - Divide by 3 3h - Divide by 4

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6.228 CTRLMMR_MCASP0_CLKSEL Register (Proxy0 Offset = 8200h; Proxy1 Offset = A200h) [reset = 0h]

CTRLMMR_MCASP0_CLKSEL is shown in Figure 6-228 and described in Table 6-458.

Return to Summary Table.

Selects the functional clock source for McASP0.

Table 6-457. CTRLMMR_MCASP0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8200h	0010 A200h

Figure 6-228. CTRLMMR_MCASP0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-458. CTRLMMR_MCASP0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP0 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.229 CTRLMMR_MCASP1_CLKSEL Register (Proxy0 Offset = 8204h; Proxy1 Offset = A204h) [reset = 0h]

CTRLMMR_MCASP1_CLKSEL is shown in Figure 6-229 and described in Table 6-460.

Return to Summary Table.

Selects the functional clock source for McASP1.

Table 6-459. CTRLMMR_MCASP1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8204h	0010 A204h

Figure 6-229. CTRLMMR_MCASP1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-460. CTRLMMR_MCASP1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP1 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.230 CTRLMMR_MCASP2_CLKSEL Register (Proxy0 Offset = 8208h; Proxy1 Offset = A208h) [reset = 0h]

CTRLMMR_MCASP2_CLKSEL is shown in Figure 6-230 and described in Table 6-462.

Return to Summary Table.

Selects the functional clock source for McASP2.

Table 6-461. CTRLMMR_MCASP2_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8208h	0010 A208h

Figure 6-230. CTRLMMR_MCASP2_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-462. CTRLMMR_MCASP2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP2 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.231 CTRLMMR_MCASP3_CLKSEL Register (Proxy0 Offset = 820Ch; Proxy1 Offset = A20Ch) [reset = 0h]

CTRLMMR_MCASP3_CLKSEL is shown in Figure 6-231 and described in Table 6-464.

Return to Summary Table.

Selects the functional clock source for McASP3.

Table 6-463. CTRLMMR_MCASP3_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 820Ch	0010 A20Ch

Figure 6-231. CTRLMMR_MCASP3_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-464. CTRLMMR_MCASP3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP3 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.232 CTRLMMR_MCASP4_CLKSEL Register (Proxy0 Offset = 8210h; Proxy1 Offset = A210h) [reset = 0h]

CTRLMMR_MCASP4_CLKSEL is shown in Figure 6-232 and described in Table 6-466.

Return to Summary Table.

Selects the functional clock source for McASP4.

Table 6-465. CTRLMMR_MCASP4_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8210h	0010 A210h

Figure 6-232. CTRLMMR_MCASP4_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-466. CTRLMMR_MCASP4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP4 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.233 CTRLMMR_MCASP5_CLKSEL Register (Proxy0 Offset = 8214h; Proxy1 Offset = A214h) [reset = 0h]

CTRLMMR_MCASP5_CLKSEL is shown in Figure 6-233 and described in Table 6-468.

Return to Summary Table.

Selects the functional clock source for McASP5.

Table 6-467. CTRLMMR_MCASP5_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8214h	0010 A214h

Figure 6-233. CTRLMMR_MCASP5_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-468. CTRLMMR_MCASP5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP5 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.234 CTRLMMR_MCASP6_CLKSEL Register (Proxy0 Offset = 8218h; Proxy1 Offset = A218h) [reset = 0h]

CTRLMMR_MCASP6_CLKSEL is shown in Figure 6-234 and described in Table 6-470.

Return to Summary Table.

Selects the functional clock source for McASP6.

Table 6-469. CTRLMMR_MCASP6_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8218h	0010 A218h

Figure 6-234. CTRLMMR_MCASP6_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-470. CTRLMMR_MCASP6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP6 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.235 CTRLMMR_MCASP7_CLKSEL Register (Proxy0 Offset = 821Ch; Proxy1 Offset = A21Ch) [reset = 0h]

CTRLMMR_MCASP7_CLKSEL is shown in Figure 6-235 and described in Table 6-472.

Return to Summary Table.

Selects the functional clock source for McASP7.

Table 6-471. CTRLMMR_MCASP7_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 821Ch	0010 A21Ch

Figure 6-235. CTRLMMR_MCASP7_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-472. CTRLMMR_MCASP7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP7 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.236 CTRLMMR_MCASP8_CLKSEL Register (Proxy0 Offset = 8220h; Proxy1 Offset = A220h) [reset = 0h]

CTRLMMR_MCASP8_CLKSEL is shown in Figure 6-236 and described in Table 6-474.

Return to Summary Table.

Selects the functional clock source for McASP8.

Table 6-473. CTRLMMR_MCASP8_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8220h	0010 A220h

Figure 6-236. CTRLMMR_MCASP8_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-474. CTRLMMR_MCASP8_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP8 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.237 CTRLMMR_MCASP9_CLKSEL Register (Proxy0 Offset = 8224h; Proxy1 Offset = A224h) [reset = 0h]

CTRLMMR_MCASP9_CLKSEL is shown in Figure 6-237 and described in Table 6-476.

Return to Summary Table.

Selects the functional clock source for McASP9.

Table 6-475. CTRLMMR_MCASP9_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8224h	0010 A224h

Figure 6-237. CTRLMMR_MCASP9_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-476. CTRLMMR_MCASP9_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP9 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.238 CTRLMMR_MCASP10_CLKSEL Register (Proxy0 Offset = 8228h; Proxy1 Offset = A228h) [reset = 0h]

CTRLMMR_MCASP10_CLKSEL is shown in Figure 6-238 and described in Table 6-478.

Return to Summary Table.

Selects the functional clock source for McASP10.

Table 6-477. CTRLMMR_MCASP10_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8228h	0010 A228h

Figure 6-238. CTRLMMR_MCASP10_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-478. CTRLMMR_MCASP10_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP10 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.239 CTRLMMR_MCASP11_CLKSEL Register (Proxy0 Offset = 822Ch; Proxy1 Offset = A22Ch) [reset = 0h]

CTRLMMR_MCASP11_CLKSEL is shown in Figure 6-239 and described in Table 6-480.

Return to Summary Table.

Selects the functional clock source for McASP11.

Table 6-479. CTRLMMR_MCASP11_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 822Ch	0010 A22Ch

Figure 6-239. CTRLMMR_MCASP11_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					AUXCLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-480. CTRLMMR_MCASP11_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	AUXCLK_SEL	R/W	0h	Selects the McASP11 auxclk clock source 0h - MAIN_PLL4_HSDIV0_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV0_CLKOUT 3h - "0" 4h - ATCLK0 5h - ATCLK1 6h - ATCLK2 7h - ATCLK3

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6.240 CTRLMMR_MCASP0_AHCLKSEL Register (Proxy0 Offset = 8240h; Proxy1 Offset = A240h) [reset = 0h]

CTRLMMR_MCASP0_AHCLKSEL is shown in Figure 6-240 and described in Table 6-482.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP0.

Table 6-481. CTRLMMR_MCASP0_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8240h	0010 A240h

Figure 6-240. CTRLMMR_MCASP0_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-482. CTRLMMR_MCASP0_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP0. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-482. CTRLMMR_MCASP0_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP0 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.241 CTRLMMR_MCASP1_AHCLKSEL Register (Proxy0 Offset = 8244h; Proxy1 Offset = A244h) [reset = 0h]

CTRLMMR_MCASP1_AHCLKSEL is shown in Figure 6-241 and described in Table 6-484.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP1.

Table 6-483. CTRLMMR_MCASP1_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8244h	0010 A244h

Figure 6-241. CTRLMMR_MCASP1_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-484. CTRLMMR_MCASP1_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP1. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-484. CTRLMMR_MCASP1_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP1 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.242 CTRLMMR_MCASP2_AHCLKSEL Register (Proxy0 Offset = 8248h; Proxy1 Offset = A248h) [reset = 0h]

CTRLMMR_MCASP2_AHCLKSEL is shown in Figure 6-242 and described in Table 6-486.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP2.

Table 6-485. CTRLMMR_MCASP2_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8248h	0010 A248h

Figure 6-242. CTRLMMR_MCASP2_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-486. CTRLMMR_MCASP2_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP2. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-486. CTRLMMR_MCASP2_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP2 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.243 CTRLMMR_MCASP3_AHCLKSEL Register (Proxy0 Offset = 824Ch; Proxy1 Offset = A24Ch) [reset = 0h]

CTRLMMR_MCASP3_AHCLKSEL is shown in Figure 6-243 and described in Table 6-488.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP3.

Table 6-487. CTRLMMR_MCASP3_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 824Ch	0010 A24Ch

Figure 6-243. CTRLMMR_MCASP3_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-488. CTRLMMR_MCASP3_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP3. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-488. CTRLMMR_MCASP3_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP3 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.244 CTRLMMR_MCASP4_AHCLKSEL Register (Proxy0 Offset = 8250h; Proxy1 Offset = A250h) [reset = 0h]

CTRLMMR_MCASP4_AHCLKSEL is shown in Figure 6-244 and described in Table 6-490.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP4.

Table 6-489. CTRLMMR_MCASP4_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8250h	0010 A250h

Figure 6-244. CTRLMMR_MCASP4_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-490. CTRLMMR_MCASP4_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP4. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-490. CTRLMMR_MCASP4_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP4 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.245 CTRLMMR_MCASP5_AHCLKSEL Register (Proxy0 Offset = 8254h; Proxy1 Offset = A254h) [reset = 0h]

CTRLMMR_MCASP5_AHCLKSEL is shown in Figure 6-245 and described in Table 6-492.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP5.

Table 6-491. CTRLMMR_MCASP5_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8254h	0010 A254h

Figure 6-245. CTRLMMR_MCASP5_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-492. CTRLMMR_MCASP5_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP5. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-492. CTRLMMR_MCASP5_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP5 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.246 CTRLMMR_MCASP6_AHCLKSEL Register (Proxy0 Offset = 8258h; Proxy1 Offset = A258h) [reset = 0h]

CTRLMMR_MCASP6_AHCLKSEL is shown in Figure 6-246 and described in Table 6-494.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP6.

Table 6-493. CTRLMMR_MCASP6_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8258h	0010 A258h

Figure 6-246. CTRLMMR_MCASP6_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-494. CTRLMMR_MCASP6_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP6. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-494. CTRLMMR_MCASP6_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP6 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.247 CTRLMMR_MCASP7_AHCLKSEL Register (Proxy0 Offset = 825Ch; Proxy1 Offset = A25Ch) [reset = 0h]

CTRLMMR_MCASP7_AHCLKSEL is shown in Figure 6-247 and described in Table 6-496.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP7.

Table 6-495. CTRLMMR_MCASP7_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 825Ch	0010 A25Ch

Figure 6-247. CTRLMMR_MCASP7_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-496. CTRLMMR_MCASP7_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP7. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-496. CTRLMMR_MCASP7_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP7 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.248 CTRLMMR_MCASP8_AHCLKSEL Register (Proxy0 Offset = 8260h; Proxy1 Offset = A260h) [reset = 0h]

CTRLMMR_MCASP8_AHCLKSEL is shown in Figure 6-248 and described in Table 6-498.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP8.

Table 6-497. CTRLMMR_MCASP8_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8260h	0010 A260h

Figure 6-248. CTRLMMR_MCASP8_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-498. CTRLMMR_MCASP8_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP8. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-498. CTRLMMR_MCASP8_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP8 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.249 CTRLMMR_MCASP9_AHCLKSEL Register (Proxy0 Offset = 8264h; Proxy1 Offset = A264h) [reset = 0h]

CTRLMMR_MCASP9_AHCLKSEL is shown in Figure 6-249 and described in Table 6-500.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP9.

Table 6-499. CTRLMMR_MCASP9_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8264h	0010 A264h

Figure 6-249. CTRLMMR_MCASP9_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-500. CTRLMMR_MCASP9_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP9. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-500. CTRLMMR_MCASP9_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP9 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.250 CTRLMMR_MCASP10_AHCLKSEL Register (Proxy0 Offset = 8268h; Proxy1 Offset = A268h) [reset = 0h]

CTRLMMR_MCASP10_AHCLKSEL is shown in Figure 6-250 and described in Table 6-502.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP10.

Table 6-501. CTRLMMR_MCASP10_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8268h	0010 A268h

Figure 6-250. CTRLMMR_MCASP10_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-502. CTRLMMR_MCASP10_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP10. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-502. CTRLMMR_MCASP10_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP10 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.251 CTRLMMR_MCASP11_AHCLKSEL Register (Proxy0 Offset = 826Ch; Proxy1 Offset = A26Ch) [reset = 0h]

CTRLMMR_MCASP11_AHCLKSEL is shown in Figure 6-251 and described in Table 6-504.

Return to Summary Table.

Selects the AHCLKX and AHCLKR clock source for McASP11.

Table 6-503. CTRLMMR_MCASP11_AHCLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 826Ch	0010 A26Ch

Figure 6-251. CTRLMMR_MCASP11_AHCLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED				AHCLKX_SEL			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESERVED				AHCLKR_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-504. CTRLMMR_MCASP11_AHCLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	0h	Reserved
11-8	AHCLKX_SEL	R/W	0h	Selects the AHCLKX input source for McASP11. Not shown values are reserved. 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3
7-4	RESERVED	R	0h	Reserved

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Table 6-504. CTRLMMR_MCASP11_AHCLKSEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	AHCLKR_SEL	R/W	0h	Selects the AHCLKR input source for McASP11 0h - HFOSC1_CLKOUT 1h - WKUP_HFOSC0_CLKOUT 2h - AUDIO_EXT_REFCLK0_IN 3h - AUDIO_EXT_REFCLK1_IN 4h - AUDIO_EXT_REFCLK2_IN 5h - AUDIO_EXT_REFCLK3_IN 6h - MLB_IO_CLK 7h - MLBP_IO_CLK / 2 8h - ATCLK0 9h - ATCLK1 Ah - ATCLK2 Bh - ATCLK3 Ch - "0" Dh - "0" Eh - "0" Fh - "0"

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6.252 CTRLMMR_ASRC_RXSYNC0_SEL Register (Proxy0 Offset = 8280h; Proxy1 Offset = A280h) [reset = 0h]

CTRLMMR_ASRC_RXSYNC0_SEL is shown in Figure 6-252 and described in Table 6-506.

Return to Summary Table.

Selects the source signal for the ASRC RXSYNC0 frame sync input.

Table 6-505. CTRLMMR_ASRC_RXSYNC0_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8280h	0010 A280h

Figure 6-252. CTRLMMR_ASRC_RXSYNC0_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										SYNC_SEL					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-506. CTRLMMR_ASRC_RXSYNC0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved

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Table 6-506. CTRLMMR_ASRC_RXSYNC0_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	SYNC_SEL	R/W	0h	RXSYNC source signal. Not shown values are reserved. 0h - McASP0 AFSR Pin Input 1h - McASP1 AFSR Pin Input 2h - McASP2 AFSR Pin Input 3h - McASP3 AFSR Pin Input 4h - McASP4 AFSR Pin Input 5h - McASP5 AFSR Pin Input 6h - McASP6 AFSR Pin Input 7h - McASP7 AFSR Pin Input 8h - McASP8 AFSR Pin Input 9h - McASP9 AFSR Pin Input Ah - McASP10 AFSR Pin Input Bh - McASP11 AFSR Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2 1Eh - MAIN_PLL4_HSDIV3_CLKOUT 1Fh - MAIN_PLL15_HSDIV3_CLKOUT 20h - ADC0_CLK 21h - ADC1_CLK 22h - MCU_EXT_REFCLK0 Pin 23h - EXT_REFCLK1 Pin

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6.253 CTRLMMR_ASRC_RXSYNC1_SEL Register (Proxy0 Offset = 8284h; Proxy1 Offset = A284h) [reset = 0h]

CTRLMMR_ASRC_RXSYNC1_SEL is shown in Figure 6-253 and described in Table 6-508.

Return to Summary Table.

Selects the source signal for the ASRC RXSYNC1 frame sync input.

Table 6-507. CTRLMMR_ASRC_RXSYNC1_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8284h	0010 A284h

Figure 6-253. CTRLMMR_ASRC_RXSYNC1_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										SYNC_SEL					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-508. CTRLMMR_ASRC_RXSYNC1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved

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Table 6-508. CTRLMMR_ASRC_RXSYNC1_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	SYNC_SEL	R/W	0h	RXSYNC source signal. Not shown values are reserved. 0h - McASP0 AFSR Pin Input 1h - McASP1 AFSR Pin Input 2h - McASP2 AFSR Pin Input 3h - McASP3 AFSR Pin Input 4h - McASP4 AFSR Pin Input 5h - McASP5 AFSR Pin Input 6h - McASP6 AFSR Pin Input 7h - McASP7 AFSR Pin Input 8h - McASP8 AFSR Pin Input 9h - McASP9 AFSR Pin Input Ah - McASP10 AFSR Pin Input Bh - McASP11 AFSR Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2 1Eh - MAIN_PLL4_HSDIV3_CLKOUT 1Fh - MAIN_PLL15_HSDIV3_CLKOUT 20h - ADC0_CLK 21h - ADC1_CLK 22h - MCU_EXT_REFCLK0 Pin 23h - EXT_REFCLK1 Pin

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6.254 CTRLMMR_ASRC_RXSYNC2_SEL Register (Proxy0 Offset = 8288h; Proxy1 Offset = A288h) [reset = 0h]

CTRLMMR_ASRC_RXSYNC2_SEL is shown in Figure 6-254 and described in Table 6-510.

Return to Summary Table.

Selects the source signal for the ASRC RXSYNC2 frame sync input.

Table 6-509. CTRLMMR_ASRC_RXSYNC2_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8288h	0010 A288h

Figure 6-254. CTRLMMR_ASRC_RXSYNC2_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										SYNC_SEL					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-510. CTRLMMR_ASRC_RXSYNC2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved

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Table 6-510. CTRLMMR_ASRC_RXSYNC2_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	SYNC_SEL	R/W	0h	RXSYNC source signal. Not shown values are reserved. 0h - McASP0 AFSR Pin Input 1h - McASP1 AFSR Pin Input 2h - McASP2 AFSR Pin Input 3h - McASP3 AFSR Pin Input 4h - McASP4 AFSR Pin Input 5h - McASP5 AFSR Pin Input 6h - McASP6 AFSR Pin Input 7h - McASP7 AFSR Pin Input 8h - McASP8 AFSR Pin Input 9h - McASP9 AFSR Pin Input Ah - McASP10 AFSR Pin Input Bh - McASP11 AFSR Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2 1Eh - MAIN_PLL4_HSDIV3_CLKOUT 1Fh - MAIN_PLL15_HSDIV3_CLKOUT 20h - ADC0_CLK 21h - ADC1_CLK 22h - MCU_EXT_REFCLK0 Pin 23h - EXT_REFCLK1 Pin

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6.255 CTRLMMR_ASRC_RXSYNC3_SEL Register (Proxy0 Offset = 828Ch; Proxy1 Offset = A28Ch) [reset = 0h]

CTRLMMR_ASRC_RXSYNC3_SEL is shown in Figure 6-255 and described in Table 6-512.

Return to Summary Table.

Selects the source signal for the ASRC RXSYNC3 frame sync input.

Table 6-511. CTRLMMR_ASRC_RXSYNC3_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 828Ch	0010 A28Ch

Figure 6-255. CTRLMMR_ASRC_RXSYNC3_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										SYNC_SEL					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-512. CTRLMMR_ASRC_RXSYNC3_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved

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Table 6-512. CTRLMMR_ASRC_RXSYNC3_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	SYNC_SEL	R/W	0h	RXSYNC source signal. Not shown values are reserved. 0h - McASP0 AFSR Pin Input 1h - McASP1 AFSR Pin Input 2h - McASP2 AFSR Pin Input 3h - McASP3 AFSR Pin Input 4h - McASP4 AFSR Pin Input 5h - McASP5 AFSR Pin Input 6h - McASP6 AFSR Pin Input 7h - McASP7 AFSR Pin Input 8h - McASP8 AFSR Pin Input 9h - McASP9 AFSR Pin Input Ah - McASP10 AFSR Pin Input Bh - McASP11 AFSR Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2 1Eh - MAIN_PLL4_HSDIV3_CLKOUT 1Fh - MAIN_PLL15_HSDIV3_CLKOUT 20h - ADC0_CLK 21h - ADC1_CLK 22h - MCU_EXT_REFCLK0 Pin 23h - EXT_REFCLK1 Pin

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6.256 CTRLMMR_ASRC_TXSYNC0_SEL Register (Proxy0 Offset = 8290h; Proxy1 Offset = A290h) [reset = 0h]

CTRLMMR_ASRC_TXSYNC0_SEL is shown in Figure 6-256 and described in Table 6-514.

Return to Summary Table.

Selects the source signal for the ASRC TXSYNC0 frame sync input.

Table 6-513. CTRLMMR_ASRC_TXSYNC0_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8290h	0010 A290h

Figure 6-256. CTRLMMR_ASRC_TXSYNC0_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										SYNC_SEL					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-514. CTRLMMR_ASRC_TXSYNC0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved

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Table 6-514. CTRLMMR_ASRC_TXSYNC0_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	SYNC_SEL	R/W	0h	TXSYNC source signal. Not shown values are reserved. 0h - McASP0 AFSX Pin Input 1h - McASP1 AFSX Pin Input 2h - McASP2 AFSX Pin Input 3h - McASP3 AFSX Pin Input 4h - McASP4 AFSX Pin Input 5h - McASP5 AFSX Pin Input 6h - McASP6 AFSX Pin Input 7h - McASP7 AFSX Pin Input 8h - McASP8 AFSX Pin Input 9h - McASP9 AFSX Pin Input Ah - McASP10 AFSX Pin Input Bh - McASP11 AFSX Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2 1Eh - MAIN_PLL4_HSDIV3_CLKOUT 1Fh - MAIN_PLL15_HSDIV3_CLKOUT 20h - ADC0_CLK 21h - ADC1_CLK 22h - MCU_EXT_REFCLK0 Pin 23h - EXT_REFCLK1 Pin

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6.257 CTRLMMR_ASRC_TXSYNC1_SEL Register (Proxy0 Offset = 8294h; Proxy1 Offset = A294h) [reset = 0h]

CTRLMMR_ASRC_TXSYNC1_SEL is shown in Figure 6-257 and described in Table 6-516.

Return to Summary Table.

Selects the source signal for the ASRC TXSYNC1 frame sync input.

Table 6-515. CTRLMMR_ASRC_TXSYNC1_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8294h	0010 A294h

Figure 6-257. CTRLMMR_ASRC_TXSYNC1_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										SYNC_SEL					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-516. CTRLMMR_ASRC_TXSYNC1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved

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Table 6-516. CTRLMMR_ASRC_TXSYNC1_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	SYNC_SEL	R/W	0h	TXSYNC source signal. Not shown values are reserved. 0h - McASP0 AFSX Pin Input 1h - McASP1 AFSX Pin Input 2h - McASP2 AFSX Pin Input 3h - McASP3 AFSX Pin Input 4h - McASP4 AFSX Pin Input 5h - McASP5 AFSX Pin Input 6h - McASP6 AFSX Pin Input 7h - McASP7 AFSX Pin Input 8h - McASP8 AFSX Pin Input 9h - McASP9 AFSX Pin Input Ah - McASP10 AFSX Pin Input Bh - McASP11 AFSX Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2 1Eh - MAIN_PLL4_HSDIV3_CLKOUT 1Fh - MAIN_PLL15_HSDIV3_CLKOUT 20h - ADC0_CLK 21h - ADC1_CLK 22h - MCU_EXT_REFCLK0 Pin 23h - EXT_REFCLK1 Pin

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6.258 CTRLMMR_ASRC_TXSYNC2_SEL Register (Proxy0 Offset = 8298h; Proxy1 Offset = A298h) [reset = 0h]

CTRLMMR_ASRC_TXSYNC2_SEL is shown in Figure 6-258 and described in Table 6-518.

Return to Summary Table.

Selects the source signal for the ASRC TXSYNC2 frame sync input.

Table 6-517. CTRLMMR_ASRC_TXSYNC2_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8298h	0010 A298h

Figure 6-258. CTRLMMR_ASRC_TXSYNC2_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										SYNC_SEL					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-518. CTRLMMR_ASRC_TXSYNC2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved

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Table 6-518. CTRLMMR_ASRC_TXSYNC2_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	SYNC_SEL	R/W	0h	TXSYNC source signal. Not shown values are reserved. 0h - McASP0 AFSX Pin Input 1h - McASP1 AFSX Pin Input 2h - McASP2 AFSX Pin Input 3h - McASP3 AFSX Pin Input 4h - McASP4 AFSX Pin Input 5h - McASP5 AFSX Pin Input 6h - McASP6 AFSX Pin Input 7h - McASP7 AFSX Pin Input 8h - McASP8 AFSX Pin Input 9h - McASP9 AFSX Pin Input Ah - McASP10 AFSX Pin Input Bh - McASP11 AFSX Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2 1Eh - MAIN_PLL4_HSDIV3_CLKOUT 1Fh - MAIN_PLL15_HSDIV3_CLKOUT 20h - ADC0_CLK 21h - ADC1_CLK 22h - MCU_EXT_REFCLK0 Pin 23h - EXT_REFCLK1 Pin

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6.259 CTRLMMR_ASRC_TXSYNC3_SEL Register (Proxy0 Offset = 829Ch; Proxy1 Offset = A29Ch) [reset = 0h]

CTRLMMR_ASRC_TXSYNC3_SEL is shown in Figure 6-259 and described in Table 6-520.

Return to Summary Table.

Selects the source signal for the ASRC TXSYNC3 frame sync input.

Table 6-519. CTRLMMR_ASRC_TXSYNC3_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 829Ch	0010 A29Ch

Figure 6-259. CTRLMMR_ASRC_TXSYNC3_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																										SYNC_SEL					
R-0h																										R/W-0h					

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-520. CTRLMMR_ASRC_TXSYNC3_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-6	RESERVED	R	0h	Reserved

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Table 6-520. CTRLMMR_ASRC_TXSYNC3_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	SYNC_SEL	R/W	0h	TXSYNC source signal. Not shown values are reserved. 0h - McASP0 AFSX Pin Input 1h - McASP1 AFSX Pin Input 2h - McASP2 AFSX Pin Input 3h - McASP3 AFSX Pin Input 4h - McASP4 AFSX Pin Input 5h - McASP5 AFSX Pin Input 6h - McASP6 AFSX Pin Input 7h - McASP7 AFSX Pin Input 8h - McASP8 AFSX Pin Input 9h - McASP9 AFSX Pin Input Ah - McASP10 AFSX Pin Input Bh - McASP11 AFSX Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2 1Eh - MAIN_PLL4_HSDIV3_CLKOUT 1Fh - MAIN_PLL15_HSDIV3_CLKOUT 20h - ADC0_CLK 21h - ADC1_CLK 22h - MCU_EXT_REFCLK0 Pin 23h - EXT_REFCLK1 Pin

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6.260 CTRLMMR_ATL_BWS0_SEL Register (Proxy0 Offset = 82A0h; Proxy1 Offset = A2A0h) [reset = 0h]

CTRLMMR_ATL_BWS0_SEL is shown in Figure 6-260 and described in Table 6-522.

Return to Summary Table.

Selects the source of ATL Baseband Word Select 0.

Table 6-521. CTRLMMR_ATL_BWS0_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82A0h	0010 A2A0h

Figure 6-260. CTRLMMR_ATL_BWS0_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WD_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-522. CTRLMMR_ATL_BWS0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	WD_SEL	R/W	0h	BWS source signal. Not shown values are reserved. 0h - McASP0 AFSR Pin Input 1h - McASP1 AFSR Pin Input 2h - McASP2 AFSR Pin Input 3h - McASP3 AFSR Pin Input 4h - McASP4 AFSR Pin Input 5h - McASP5 AFSR Pin Input 6h - McASP6 AFSR Pin Input 7h - McASP7 AFSR Pin Input 8h - McASP8 AFSR Pin Input 9h - McASP9 AFSR Pin Input Ah - McASP10 AFSR Pin Input Bh - McASP11 AFSR Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input

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6.261 CTRLMMR_ATL_BWS1_SEL Register (Proxy0 Offset = 82A4h; Proxy1 Offset = A2A4h) [reset = 0h]

CTRLMMR_ATL_BWS1_SEL is shown in Figure 6-261 and described in Table 6-524.

Return to Summary Table.

Selects the source of ATL Baseband Word Select 1.

Table 6-523. CTRLMMR_ATL_BWS1_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82A4h	0010 A2A4h

Figure 6-261. CTRLMMR_ATL_BWS1_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WD_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-524. CTRLMMR_ATL_BWS1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	WD_SEL	R/W	0h	BWS source signal. Not shown values are reserved. 0h - McASP0 AFSR Pin Input 1h - McASP1 AFSR Pin Input 2h - McASP2 AFSR Pin Input 3h - McASP3 AFSR Pin Input 4h - McASP4 AFSR Pin Input 5h - McASP5 AFSR Pin Input 6h - McASP6 AFSR Pin Input 7h - McASP7 AFSR Pin Input 8h - McASP8 AFSR Pin Input 9h - McASP9 AFSR Pin Input Ah - McASP10 AFSR Pin Input Bh - McASP11 AFSR Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input

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6.262 CTRLMMR_ATL_BWS2_SEL Register (Proxy0 Offset = 82A8h; Proxy1 Offset = A2A8h) [reset = 0h]

CTRLMMR_ATL_BWS2_SEL is shown in Figure 6-262 and described in Table 6-526.

Return to Summary Table.

Selects the source of ATL Baseband Word Select 2.

Table 6-525. CTRLMMR_ATL_BWS2_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82A8h	0010 A2A8h

Figure 6-262. CTRLMMR_ATL_BWS2_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WD_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-526. CTRLMMR_ATL_BWS2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	WD_SEL	R/W	0h	BWS source signal. Not shown values are reserved. 0h - McASP0 AFSR Pin Input 1h - McASP1 AFSR Pin Input 2h - McASP2 AFSR Pin Input 3h - McASP3 AFSR Pin Input 4h - McASP4 AFSR Pin Input 5h - McASP5 AFSR Pin Input 6h - McASP6 AFSR Pin Input 7h - McASP7 AFSR Pin Input 8h - McASP8 AFSR Pin Input 9h - McASP9 AFSR Pin Input Ah - McASP10 AFSR Pin Input Bh - McASP11 AFSR Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input

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6.263 CTRLMMR_ATL_BWS3_SEL Register (Proxy0 Offset = 82ACh; Proxy1 Offset = A2ACh) [reset = 0h]

CTRLMMR_ATL_BWS3_SEL is shown in Figure 6-263 and described in Table 6-528.

Return to Summary Table.

Selects the source of ATL Baseband Word Select 3.

Table 6-527. CTRLMMR_ATL_BWS3_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82ACh	0010 A2ACh

Figure 6-263. CTRLMMR_ATL_BWS3_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WD_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-528. CTRLMMR_ATL_BWS3_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	WD_SEL	R/W	0h	BWS source signal. Not shown values are reserved. 0h - McASP0 AFSR Pin Input 1h - McASP1 AFSR Pin Input 2h - McASP2 AFSR Pin Input 3h - McASP3 AFSR Pin Input 4h - McASP4 AFSR Pin Input 5h - McASP5 AFSR Pin Input 6h - McASP6 AFSR Pin Input 7h - McASP7 AFSR Pin Input 8h - McASP8 AFSR Pin Input 9h - McASP9 AFSR Pin Input Ah - McASP10 AFSR Pin Input Bh - McASP11 AFSR Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input

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6.264 CTRLMMR_ATL_AWS0_SEL Register (Proxy0 Offset = 82B0h; Proxy1 Offset = A2B0h) [reset = 0h]

CTRLMMR_ATL_AWS0_SEL is shown in Figure 6-264 and described in Table 6-530.

Return to Summary Table.

Selects the source of ATL Audio Word Select 0.

Table 6-529. CTRLMMR_ATL_AWS0_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82B0h	0010 A2B0h

Figure 6-264. CTRLMMR_ATL_AWS0_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WD_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-530. CTRLMMR_ATL_AWS0_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	WD_SEL	R/W	0h	AWS source signal. Not shown values are reserved. 0h - McASP0 AFSX Pin Input 1h - McASP1 AFSX Pin Input 2h - McASP2 AFSX Pin Input 3h - McASP3 AFSX Pin Input 4h - McASP4 AFSX Pin Input 5h - McASP5 AFSX Pin Input 6h - McASP6 AFSX Pin Input 7h - McASP7 AFSX Pin Input 8h - McASP8 AFSX Pin Input 9h - McASP9 AFSX Pin Input Ah - McASP10 AFSX Pin Input Bh - McASP11 AFSX Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2

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6.265 CTRLMMR_ATL_AWS1_SEL Register (Proxy0 Offset = 82B4h; Proxy1 Offset = A2B4h) [reset = 0h]

CTRLMMR_ATL_AWS1_SEL is shown in Figure 6-265 and described in Table 6-532.

Return to Summary Table.

Selects the source of ATL Audio Word Select 1.

Table 6-531. CTRLMMR_ATL_AWS1_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82B4h	0010 A2B4h

Figure 6-265. CTRLMMR_ATL_AWS1_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WD_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-532. CTRLMMR_ATL_AWS1_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	WD_SEL	R/W	0h	AWS source signal. Not shown values are reserved. 0h - McASP0 AFSX Pin Input 1h - McASP1 AFSX Pin Input 2h - McASP2 AFSX Pin Input 3h - McASP3 AFSX Pin Input 4h - McASP4 AFSX Pin Input 5h - McASP5 AFSX Pin Input 6h - McASP6 AFSX Pin Input 7h - McASP7 AFSX Pin Input 8h - McASP8 AFSX Pin Input 9h - McASP9 AFSX Pin Input Ah - McASP10 AFSX Pin Input Bh - McASP11 AFSX Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2

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6.266 CTRLMMR_ATL_AWS2_SEL Register (Proxy0 Offset = 82B8h; Proxy1 Offset = A2B8h) [reset = 0h]

CTRLMMR_ATL_AWS2_SEL is shown in Figure 6-266 and described in Table 6-534.

Return to Summary Table.

Selects the source of ATL Audio Word Select 2.

Table 6-533. CTRLMMR_ATL_AWS2_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82B8h	0010 A2B8h

Figure 6-266. CTRLMMR_ATL_AWS2_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WD_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-534. CTRLMMR_ATL_AWS2_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	WD_SEL	R/W	0h	AWS source signal. Not shown values are reserved. 0h - McASP0 AFSX Pin Input 1h - McASP1 AFSX Pin Input 2h - McASP2 AFSX Pin Input 3h - McASP3 AFSX Pin Input 4h - McASP4 AFSX Pin Input 5h - McASP5 AFSX Pin Input 6h - McASP6 AFSX Pin Input 7h - McASP7 AFSX Pin Input 8h - McASP8 AFSX Pin Input 9h - McASP9 AFSX Pin Input Ah - McASP10 AFSX Pin Input Bh - McASP11 AFSX Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2

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6.267 CTRLMMR_ATL_AWS3_SEL Register (Proxy0 Offset = 82BCh; Proxy1 Offset = A2BCh) [reset = 0h]

CTRLMMR_ATL_AWS3_SEL is shown in Figure 6-267 and described in Table 6-536.

Return to Summary Table.

Selects the source of ATL Audio Word Select 3.

Table 6-535. CTRLMMR_ATL_AWS3_SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82BCh	0010 A2BCh

Figure 6-267. CTRLMMR_ATL_AWS3_SEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												WD_SEL			
R-0h																												R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-536. CTRLMMR_ATL_AWS3_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	Reserved
4-0	WD_SEL	R/W	0h	AWS source signal. Not shown values are reserved. 0h - McASP0 AFSX Pin Input 1h - McASP1 AFSX Pin Input 2h - McASP2 AFSX Pin Input 3h - McASP3 AFSX Pin Input 4h - McASP4 AFSX Pin Input 5h - McASP5 AFSX Pin Input 6h - McASP6 AFSX Pin Input 7h - McASP7 AFSX Pin Input 8h - McASP8 AFSX Pin Input 9h - McASP9 AFSX Pin Input Ah - McASP10 AFSX Pin Input Bh - McASP11 AFSX Pin Input Ch - McASP0 AFSX Pin Input Dh - McASP1 AFSX Pin Input Eh - McASP2 AFSX Pin Input Fh - McASP3 AFSX Pin Input 10h - McASP4 AFSX Pin Input 11h - McASP5 AFSX Pin Input 12h - McASP6 AFSX Pin Input 13h - McASP7 AFSX Pin Input 14h - McASP8 AFSX Pin Input 15h - McASP9 AFSX Pin Input 16h - McASP10 AFSX Pin Input 17h - McASP11 AFSX Pin Input 18h - AUDIO_EXT_REFCLK0 Pin input 19h - AUDIO_EXT_REFCLK1 Pin input 1Ah - AUDIO_EXT_REFCLK2 Pin input 1Bh - AUDIO_EXT_REFCLK3 Pin input 1Ch - MLB_IO_CLK 1Dh - MLBP_IO_CLK /2

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6.268 CTRLMMR_ATL_CLKSEL Register (Proxy0 Offset = 82C0h; Proxy1 Offset = A2C0h) [reset = 0h]

CTRLMMR_ATL_CLKSEL is shown in Figure 6-268 and described in Table 6-538.

Return to Summary Table.

Selects the source of the ATL PCLK.

Table 6-537. CTRLMMR_ATL_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82C0h	0010 A2C0h

Figure 6-268. CTRLMMR_ATL_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				PCLK_SEL			
R-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-538. CTRLMMR_ATL_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3-0	PCLK_SEL	R/W	0h	Selects the PCLK clock source 0h - MAIN_PLL4_HSDIV1_CLKOUT 1h - MAIN_PLL2_HSDIV2_CLKOUT 2h - MAIN_PLL15_HSDIV1_CLKOUT 3h - "0" 4h - MAIN_PLL0_HSDIV7_CLKOUT 5h - MCU_EXT_REFCLK0 (pin) 6h - EXT_REFCLK1 (pin) 7h - "0"

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6.269 CTRLMMR_AUDIO_REFCLK0_CTRL Register (Proxy0 Offset = 82E0h; Proxy1 Offset = A2E0h) [reset = 1Fh]

CTRLMMR_AUDIO_REFCLK0_CTRL is shown in Figure 6-269 and described in Table 6-540.

Return to Summary Table.

Selects the clock source for the AUDIO_EXT_REFCLK0 output.

Table 6-539. CTRLMMR_AUDIO_REFCLK0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82E0h	0010 A2E0h

Figure 6-269. CTRLMMR_AUDIO_REFCLK0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED			CLK_SEL				
R-0h			R/W-1Fh				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-540. CTRLMMR_AUDIO_REFCLK0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	CLKOUT_EN	R/W	0h	AUDIO_REFCLK 0 output enable This bit is inverted to drive the active low output buffer enable 0h - AUDIO_EXT_REFCLK0 pin is configured as an input 1h - AUDIO_EXT_REFCLK0 pin is configured as an output
14-5	RESERVED	R	0h	Reserved

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Table 6-540. CTRLMMR_AUDIO_REFCLK0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CLK_SEL	R/W	1Fh	Clock source 0h - MCASP0 AHCLKR Output 1h - MCASP1 AHCLKR Output 2h - MCASP2 AHCLKR Output 3h - MCASP3 AHCLKR Output 4h - MCASP4 AHCLKR Output 5h - MCASP5 AHCLKR Output 6h - MCASP6 AHCLKR Output 7h - MCASP7 AHCLKR Output 8h - MCASP8 AHCLKR Output 9h - MCASP9 AHCLKR Output Ah - MCASP10 AHCLKR Output Bh - MCASP11 AHCLKR Output Ch - MCASP0 AHCLKX Output Dh - MCASP1 AHCLKX Output Eh - MCASP2 AHCLKX Output Fh - MCASP3 AHCLKX Output 10h - MCASP4 AHCLKX Output 11h - MCASP5 AHCLKX Output 12h - MCASP6 AHCLKX Output 13h - MCASP7 AHCLKX Output 14h - MCASP8 AHCLKX Output 15h - MCASP9 AHCLKX Output 16h - MCASP10 AHCLKX Output 17h - MCASP11 AHCLKX Output 18h - ATCLK0 19h - ATCLK1 1Ah - ATCLK2 1Bh - ATCLK3 1Ch - MAIN_PLL4_HSDIV2_CLKOUT 1Dh - MAIN_PLL15_HSDIV2_CLKOUT 1Eh - "0" 1Fh - "0"

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6.270 CTRLMMR_AUDIO_REFCLK1_CTRL Register (Proxy0 Offset = 82E4h; Proxy1 Offset = A2E4h) [reset = 1Fh]

CTRLMMR_AUDIO_REFCLK1_CTRL is shown in Figure 6-270 and described in Table 6-542.

Return to Summary Table.

Selects the clock source for the AUDIO_EXT_REFCLK1 output.

Table 6-541. CTRLMMR_AUDIO_REFCLK1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82E4h	0010 A2E4h

Figure 6-270. CTRLMMR_AUDIO_REFCLK1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						
R/W-0h	R-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CLK_SEL				
R-0h			R/W-1Fh				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-542. CTRLMMR_AUDIO_REFCLK1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	CLKOUT_EN	R/W	0h	AUDIO_REFCLK 1 output enable This bit is inverted to drive the active low output buffer enable 0h - AUDIO_EXT_REFCLK1 pin is configured as an input 1h - AUDIO_EXT_REFCLK1 pin is configured as an output
14-5	RESERVED	R	0h	Reserved

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Table 6-542. CTRLMMR_AUDIO_REFCLK1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CLK_SEL	R/W	1Fh	Clock source 0h - MCASP0 AHCLKR Output 1h - MCASP1 AHCLKR Output 2h - MCASP2 AHCLKR Output 3h - MCASP3 AHCLKR Output 4h - MCASP4 AHCLKR Output 5h - MCASP5 AHCLKR Output 6h - MCASP6 AHCLKR Output 7h - MCASP7 AHCLKR Output 8h - MCASP8 AHCLKR Output 9h - MCASP9 AHCLKR Output Ah - MCASP10 AHCLKR Output Bh - MCASP11 AHCLKR Output Ch - MCASP0 AHCLKX Output Dh - MCASP1 AHCLKX Output Eh - MCASP2 AHCLKX Output Fh - MCASP3 AHCLKX Output 10h - MCASP4 AHCLKX Output 11h - MCASP5 AHCLKX Output 12h - MCASP6 AHCLKX Output 13h - MCASP7 AHCLKX Output 14h - MCASP8 AHCLKX Output 15h - MCASP9 AHCLKX Output 16h - MCASP10 AHCLKX Output 17h - MCASP11 AHCLKX Output 18h - ATCLK0 19h - ATCLK1 1Ah - ATCLK2 1Bh - ATCLK3 1Ch - MAIN_PLL4_HSDIV2_CLKOUT 1Dh - MAIN_PLL15_HSDIV2_CLKOUT 1Eh - "0" 1Fh - "0"

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6.271 CTRLMMR_AUDIO_REFCLK2_CTRL Register (Proxy0 Offset = 82E8h; Proxy1 Offset = A2E8h) [reset = 1Fh]

CTRLMMR_AUDIO_REFCLK2_CTRL is shown in Figure 6-271 and described in Table 6-544.

Return to Summary Table.

Selects the clock source for the AUDIO_EXT_REFCLK2 output.

Table 6-543. CTRLMMR_AUDIO_REFCLK2_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82E8h	0010 A2E8h

Figure 6-271. CTRLMMR_AUDIO_REFCLK2_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						
R/W-0h	R-0h						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			CLK_SEL				
R-0h			R/W-1Fh				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-544. CTRLMMR_AUDIO_REFCLK2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	CLKOUT_EN	R/W	0h	AUDIO_REFCLK 2 output enable This bit is inverted to drive the active low output buffer enable 0h - AUDIO_EXT_REFCLK2 pin is configured as an input 1h - AUDIO_EXT_REFCLK2 pin is configured as an output
14-5	RESERVED	R	0h	Reserved

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Table 6-544. CTRLMMR_AUDIO_REFCLK2_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CLK_SEL	R/W	1Fh	Clock source 0h - MCASP0 AHCLKR Output 1h - MCASP1 AHCLKR Output 2h - MCASP2 AHCLKR Output 3h - MCASP3 AHCLKR Output 4h - MCASP4 AHCLKR Output 5h - MCASP5 AHCLKR Output 6h - MCASP6 AHCLKR Output 7h - MCASP7 AHCLKR Output 8h - MCASP8 AHCLKR Output 9h - MCASP9 AHCLKR Output Ah - MCASP10 AHCLKR Output Bh - MCASP11 AHCLKR Output Ch - MCASP0 AHCLKX Output Dh - MCASP1 AHCLKX Output Eh - MCASP2 AHCLKX Output Fh - MCASP3 AHCLKX Output 10h - MCASP4 AHCLKX Output 11h - MCASP5 AHCLKX Output 12h - MCASP6 AHCLKX Output 13h - MCASP7 AHCLKX Output 14h - MCASP8 AHCLKX Output 15h - MCASP9 AHCLKX Output 16h - MCASP10 AHCLKX Output 17h - MCASP11 AHCLKX Output 18h - ATCLK0 19h - ATCLK1 1Ah - ATCLK2 1Bh - ATCLK3 1Ch - MAIN_PLL4_HSDIV2_CLKOUT 1Dh - MAIN_PLL15_HSDIV2_CLKOUT 1Eh - "0" 1Fh - "0"

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6.272 CTRLMMR_AUDIO_REFCLK3_CTRL Register (Proxy0 Offset = 82ECh; Proxy1 Offset = A2ECh) [reset = 1Fh]

CTRLMMR_AUDIO_REFCLK3_CTRL is shown in Figure 6-272 and described in Table 6-546.

Return to Summary Table.

Selects the clock source for the AUDIO_EXT_REFCLK3 output.

Table 6-545. CTRLMMR_AUDIO_REFCLK3_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 82ECh	0010 A2ECh

Figure 6-272. CTRLMMR_AUDIO_REFCLK3_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						
R/W-0h	R-0h						
7	6	5	4	3	2	1	0
RESERVED			CLK_SEL				
R-0h			R/W-1Fh				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-546. CTRLMMR_AUDIO_REFCLK3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	CLKOUT_EN	R/W	0h	AUDIO_REFCLK 3 output enable This bit is inverted to drive the active low output buffer enable 0h - AUDIO_EXT_REFCLK3 pin is configured as an input 1h - AUDIO_EXT_REFCLK3 pin is configured as an output
14-5	RESERVED	R	0h	Reserved

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Table 6-546. CTRLMMR_AUDIO_REFCLK3_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CLK_SEL	R/W	1Fh	Clock source 0h - MCASP0 AHCLKR Output 1h - MCASP1 AHCLKR Output 2h - MCASP2 AHCLKR Output 3h - MCASP3 AHCLKR Output 4h - MCASP4 AHCLKR Output 5h - MCASP5 AHCLKR Output 6h - MCASP6 AHCLKR Output 7h - MCASP7 AHCLKR Output 8h - MCASP8 AHCLKR Output 9h - MCASP9 AHCLKR Output Ah - MCASP10 AHCLKR Output Bh - MCASP11 AHCLKR Output Ch - MCASP0 AHCLKX Output Dh - MCASP1 AHCLKX Output Eh - MCASP2 AHCLKX Output Fh - MCASP3 AHCLKX Output 10h - MCASP4 AHCLKX Output 11h - MCASP5 AHCLKX Output 12h - MCASP6 AHCLKX Output 13h - MCASP7 AHCLKX Output 14h - MCASP8 AHCLKX Output 15h - MCASP9 AHCLKX Output 16h - MCASP10 AHCLKX Output 17h - MCASP11 AHCLKX Output 18h - ATCLK0 19h - ATCLK1 1Ah - ATCLK2 1Bh - ATCLK3 1Ch - MAIN_PLL4_HSDIV2_CLKOUT 1Dh - MAIN_PLL15_HSDIV2_CLKOUT 1Eh - "0" 1Fh - "0"

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6.273 CTRLMMR_DPI0_CLK_CTRL Register (Proxy0 Offset = 8300h; Proxy1 Offset = A300h) [reset = 0h]

CTRLMMR_DPI0_CLK_CTRL is shown in Figure 6-273 and described in Table 6-548.

Return to Summary Table.

Selects the clock source for the DPI0 video output.

Table 6-547. CTRLMMR_DPI0_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8300h	0010 A300h

Figure 6-273. CTRLMMR_DPI0_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_CLKSEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-548. CTRLMMR_DPI0_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EXT_CLKSEL	R/W	0h	Selects whether to use DSS PLL3 or an external pin as a DPI clock source. 0h - Use internal clock : MAIN_PLL19_HSDIV0_CLKOUT 1h - Use external clock : VOUT1_EXTPCLKIN

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6.274 CTRLMMR_DPI1_CLK_CTRL Register (Proxy0 Offset = 8304h; Proxy1 Offset = A304h) [reset = 0h]

CTRLMMR_DPI1_CLK_CTRL is shown in Figure 6-274 and described in Table 6-550.

Return to Summary Table.

Selects the clock source for the DPI1 video output.

Table 6-549. CTRLMMR_DPI1_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8304h	0010 A304h

Figure 6-274. CTRLMMR_DPI1_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							EXT_CLKSEL
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-550. CTRLMMR_DPI1_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	EXT_CLKSEL	R/W	0h	Selects whether to use DSS PLL7 or an external pin as a DPI clock source. 0h - Use internal clock : MAIN_PLL23_HSDIV0_CLKOUT 1h - Use external clock : VOUT2_EXTPCLKIN

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6.275 CTRLMMR_DPHY0_CLKSEL Register (Proxy0 Offset = 8310h; Proxy1 Offset = A310h) [reset = 0h]

CTRLMMR_DPHY0_CLKSEL is shown in Figure 6-275 and described in Table 6-552.

Return to Summary Table.

Selects the clock source for the DSI0 transmit PHY.

Table 6-551. CTRLMMR_DPHY0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8310h	0010 A310h

Figure 6-275. CTRLMMR_DPHY0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						REF_CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-552. CTRLMMR_DPHY0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	REF_CLK_SEL	R/W	0h	DPHY reference clock source 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL3_HSDIV4_CLKOUT 3h - MAIN_PLL2_HSDIV4_CLKOUT

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6.276 CTRLMMR_DSS_DISPC0_CLKSEL1 Register (Proxy0 Offset = 8324h; Proxy1 Offset = A324h) [reset = 0h]

CTRLMMR_DSS_DISPC0_CLKSEL1 is shown in Figure 6-276 and described in Table 6-554.

Return to Summary Table.

Selects the clock source for DPI Lane 1 of Display Controller Instance 0.

Table 6-553. CTRLMMR_DSS_DISPC0_CLKSEL1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8324h	0010 A324h

Figure 6-276. CTRLMMR_DSS_DISPC0_CLKSEL1 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						DPI1_PCLK	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-554. CTRLMMR_DSS_DISPC0_CLKSEL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	DPI1_PCLK	R/W	0h	DPI lane 1 pixel clock source 0h - MAIN_PLL17_HSDIV0_CLKOUT 1h - MAIN_PLL19_HSDIV0_CLKOUT_EXTPCLKIN 2h - MAIN_PLL23_HSDIV0_CLKOUT_EXTPCLKIN 3h - MAIN_PLL16_HSDIV1_CLKOUT

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6.277 CTRLMMR_DSS_DISPC0_CLKSEL2 Register (Proxy0 Offset = 8328h; Proxy1 Offset = A328h) [reset = 0h]

CTRLMMR_DSS_DISPC0_CLKSEL2 is shown in Figure 6-277 and described in Table 6-556.

Return to Summary Table.

Selects the clock source for DPI Lane 2 of Display Controller Instance 0.

Table 6-555. CTRLMMR_DSS_DISPC0_CLKSEL2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8328h	0010 A328h

Figure 6-277. CTRLMMR_DSS_DISPC0_CLKSEL2 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							DPI2_PCLK
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-556. CTRLMMR_DSS_DISPC0_CLKSEL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	DPI2_PCLK	R/W	0h	DPI lane 2 pixel clock source 0h - MAIN_PLL16_HSDIV0_CLKOUT 1h - MAIN_PLL18_HSDIV0_CLKOUT

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6.278 CTRLMMR_DSS_DISPC0_CLKSEL3 Register (Proxy0 Offset = 832Ch; Proxy1 Offset = A32Ch) [reset = 0h]

CTRLMMR_DSS_DISPC0_CLKSEL3 is shown in Figure 6-278 and described in Table 6-558.

Return to Summary Table.

Selects the clock source for DPI Lane 3 of Display Controller Instance 0 Can also override the DPI Lane 0 and DPI Lane 2 clock source for certain values.

Table 6-557. CTRLMMR_DSS_DISPC0_CLKSEL3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 832Ch	0010 A32Ch

Figure 6-278. CTRLMMR_DSS_DISPC0_CLKSEL3 Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					DPI3_PCLK		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-558. CTRLMMR_DSS_DISPC0_CLKSEL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	0h	Reserved
2-0	DPI3_PCLK	R/W	0h	DPI lane 3 pixel clock source Note that values of 3'b1x1 also change the DPI lane 0 pixel clock source and values of 3'b11x change the DPI lane 2 pixel clock source 0h - MAIN_PLL16_HSDIV1_CLKOUT 1h - MAIN_PLL17_HSDIV1_CLKOUT 2h - MAIN_PLL18_HSDIV1_CLKOUT 3h - MAIN_PLL19_HSDIV0_CLKOUT_EXTPCLKIN 4h - MAIN_PLL23_HSDIV0_CLKOUT_EXTPCLKIN 5h - MAIN_PLL23_HSDIV0_CLKOUT_EXTPCLKIN and dpi0_pclk = dpi1_pclk 6h - MAIN_PLL23_HSDIV0_CLKOUT_EXTPCLKIN and dpi2_pclk = MAIN_PLL19_HSDIV0_CLKOUT_EXTPCLKIN 7h - MAIN_PLL23_HSDIV0_CLKOUT_EXTPCLKIN and dpi0_pclk = dpi1_pclk and dpi2_pclk = MAIN_PLL19_HSDIV0_CLKOUT_EXTPCLKIN

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6.279 CTRLMMR_EDP_PHY0_CLKSEL Register (Proxy0 Offset = 8340h; Proxy1 Offset = A340h) [reset = 0h]

CTRLMMR_EDP_PHY0_CLKSEL is shown in Figure 6-279 and described in Table 6-560.

Return to Summary Table.

Selects the Phy core clock for Embedded Display Port Phy0.

Table 6-559. CTRLMMR_EDP_PHY0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8340h	0010 A340h

Figure 6-279. CTRLMMR_EDP_PHY0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-560. CTRLMMR_EDP_PHY0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	EDP PHY CORE_REFCLK clock source 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL3_HSDIV4_CLKOUT 3h - MAIN_PLL2_HSDIV4_CLKOUT

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6.280 CTRLMMR_EDP0_CLK_CTRL Register (Proxy0 Offset = 8350h; Proxy1 Offset = A350h) [reset = 0h]

CTRLMMR_EDP0_CLK_CTRL is shown in Figure 6-280 and described in Table 6-562.

Return to Summary Table.

Controls clock operation for Embedded Display Port 0.

Table 6-561. CTRLMMR_EDP0_CLK_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8350h	0010 A350h

Figure 6-280. CTRLMMR_EDP0_CLK_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							DSI_CLK_DYN_SWTCH_DIS
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-562. CTRLMMR_EDP0_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	DSI_CLK_DYN_SWTCH_DIS	R/W	0h	EDP0 DSI clock dynamic switch disable. This bit controls whether the EDP source clock is dynamically switched (to MAIN_PLL2_HSDIV7_CLKOUT) on a warm reset event. 0h - Dynamic switching on warm reset is enabled 1h - Dynamic switching on warm reset is disabled
7-0	RESERVED	R	0h	Reserved

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6.281 CTRLMMR_WWD0_CLKSEL Register (Proxy0 Offset = 8380h; Proxy1 Offset = A380h) [reset = 0h]

CTRLMMR_WWD0_CLKSEL is shown in Figure 6-281 and described in Table 6-564.

Return to Summary Table.

ARM MPU Core 0 Windowed watchdog timer functional clock selection control.

Table 6-563. CTRLMMR_WWD0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8380h	0010 A380h

Figure 6-281. CTRLMMR_WWD0_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-564. CTRLMMR_WWD0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks CTRLMMR_WWD0_CLKSEL from further writes until the next module reset.
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K 4h - HFOSC1_CLKOUT 5h - reserved (HFOSC1_CLKOUT) 6h - reserved (HFOSC1_CLKOUT) 7h - reserved (HFOSC1_CLKOUT)

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6.282 CTRLMMR_WWD1_CLKSEL Register (Proxy0 Offset = 8384h; Proxy1 Offset = A384h) [reset = 0h]

CTRLMMR_WWD1_CLKSEL is shown in Figure 6-282 and described in Table 6-566.

Return to Summary Table.

ARM MPU Core 1 Windowed watchdog timer functional clock selection control.

Table 6-565. CTRLMMR_WWD1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8384h	0010 A384h

Figure 6-282. CTRLMMR_WWD1_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-566. CTRLMMR_WWD1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks CTRLMMR_WWD1_CLKSEL from further writes until the next module reset.
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K 4h - HFOSC1_CLKOUT 5h - reserved (HFOSC1_CLKOUT) 6h - reserved (HFOSC1_CLKOUT) 7h - reserved (HFOSC1_CLKOUT)

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6.283 CTRLMMR_WWD15_CLKSEL Register (Proxy0 Offset = 83BCh; Proxy1 Offset = A3BCh) [reset = 0h]

CTRLMMR_WWD15_CLKSEL is shown in Figure 6-283 and described in Table 6-568.

Return to Summary Table.

GPU Windowed watchdog timer functional clock selection control.

Table 6-567. CTRLMMR_WWD15_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 83BCh	0010 A3BCh

Figure 6-283. CTRLMMR_WWD15_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-568. CTRLMMR_WWD15_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks CTRLMMR_WWD15_CLKSEL from further writes until the next module reset.
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K 4h - HFOSC1_CLKOUT 5h - reserved (HFOSC1_CLKOUT) 6h - reserved (HFOSC1_CLKOUT) 7h - reserved (HFOSC1_CLKOUT)

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6.284 CTRLMMR_WWD16_CLKSEL Register (Proxy0 Offset = 83C0h; Proxy1 Offset = A3C0h) [reset = 0h]

CTRLMMR_WWD16_CLKSEL is shown in Figure 6-284 and described in Table 6-570.

Return to Summary Table.

C71x Core 0 Windowed watchdog timer functional clock selection control.

Table 6-569. CTRLMMR_WWD16_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 83C0h	0010 A3C0h

Figure 6-284. CTRLMMR_WWD16_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-570. CTRLMMR_WWD16_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks CTRLMMR_WWD16_CLKSEL from further writes until the next module reset.
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K 4h - HFOSC1_CLKOUT 5h - reserved (HFOSC1_CLKOUT) 6h - reserved (HFOSC1_CLKOUT) 7h - reserved (HFOSC1_CLKOUT)

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6.285 CTRLMMR_WWD24_CLKSEL Register (Proxy0 Offset = 83E0h; Proxy1 Offset = A3E0h) [reset = 0h]

CTRLMMR_WWD24_CLKSEL is shown in Figure 6-285 and described in Table 6-572.

Return to Summary Table.

C66x Core 0 Windowed watchdog timer functional clock selection control.

Table 6-571. CTRLMMR_WWD24_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 83E0h	0010 A3E0h

Figure 6-285. CTRLMMR_WWD24_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-572. CTRLMMR_WWD24_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks CTRLMMR_WWD24_CLKSEL from further writes until the next module reset.
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K 4h - HFOSC1_CLKOUT 5h - reserved (HFOSC1_CLKOUT) 6h - reserved (HFOSC1_CLKOUT) 7h - reserved (HFOSC1_CLKOUT)

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6.286 CTRLMMR_WWD25_CLKSEL Register (Proxy0 Offset = 83E4h; Proxy1 Offset = A3E4h) [reset = 0h]

CTRLMMR_WWD25_CLKSEL is shown in Figure 6-286 and described in Table 6-574.

Return to Summary Table.

C66x Core 1 Windowed watchdog timer functional clock selection control.

Table 6-573. CTRLMMR_WWD25_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 83E4h	0010 A3E4h

Figure 6-286. CTRLMMR_WWD25_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-574. CTRLMMR_WWD25_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks CTRLMMR_WWD25_CLKSEL from further writes until the next module reset.
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K 4h - HFOSC1_CLKOUT 5h - reserved (HFOSC1_CLKOUT) 6h - reserved (HFOSC1_CLKOUT) 7h - reserved (HFOSC1_CLKOUT)

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6.287 CTRLMMR_WWD28_CLKSEL Register (Proxy0 Offset = 83F0h; Proxy1 Offset = A3F0h) [reset = 0h]

CTRLMMR_WWD28_CLKSEL is shown in Figure 6-287 and described in Table 6-576.

Return to Summary Table.

Main R5 Core 0 Windowed watchdog timer functional clock selection control.

Table 6-575. CTRLMMR_WWD28_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 83F0h	0010 A3F0h

Figure 6-287. CTRLMMR_WWD28_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-576. CTRLMMR_WWD28_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks CTRLMMR_WWD28_CLKSEL from further writes until the next module reset.
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control These bits are warm reset isolated to preserve R5 RTI clock selection. 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K 4h - HFOSC1_CLKOUT 5h - reserved (HFOSC1_CLKOUT) 6h - reserved (HFOSC1_CLKOUT) 7h - reserved (HFOSC1_CLKOUT)

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6.288 CTRLMMR_WWD29_CLKSEL Register (Proxy0 Offset = 83F4h; Proxy1 Offset = A3F4h) [reset = 0h]

CTRLMMR_WWD29_CLKSEL is shown in Figure 6-288 and described in Table 6-578.

Return to Summary Table.

Main R5 Core 1 Windowed watchdog timer functional clock selection control.

Table 6-577. CTRLMMR_WWD29_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 83F4h	0010 A3F4h

Figure 6-288. CTRLMMR_WWD29_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED							
R-0h							

7	6	5	4	3	2	1	0
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-578. CTRLMMR_WWD29_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks CTRLMMR_WWD29_CLKSEL from further writes until the next module reset.
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control These bits are warm reset isolated to preserve R5 RTI clock selection. 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K 4h - HFOSC1_CLKOUT 5h - reserved (HFOSC1_CLKOUT) 6h - reserved (HFOSC1_CLKOUT) 7h - reserved (HFOSC1_CLKOUT)

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6.289 CTRLMMR_WWD30_CLKSEL Register (Proxy0 Offset = 83F8h; Proxy1 Offset = A3F8h) [reset = 0h]

CTRLMMR_WWD30_CLKSEL is shown in Figure 6-289 and described in Table 6-580.

Return to Summary Table.

Main R5 Core 2 Windowed watchdog timer functional clock selection control.

Table 6-579. CTRLMMR_WWD30_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 83F8h	0010 A3F8h

Figure 6-289. CTRLMMR_WWD30_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-580. CTRLMMR_WWD30_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks CTRLMMR_WWD30_CLKSEL from further writes until the next module reset.
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control These bits are warm reset isolated to preserve R5 RTI clock selection. 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K 4h - HFOSC1_CLKOUT 5h - reserved (HFOSC1_CLKOUT) 6h - reserved (HFOSC1_CLKOUT) 7h - reserved (HFOSC1_CLKOUT)

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6.290 CTRLMMR_WWD31_CLKSEL Register (Proxy0 Offset = 83FCh; Proxy1 Offset = A3FCh) [reset = 0h]

CTRLMMR_WWD31_CLKSEL is shown in Figure 6-290 and described in Table 6-582.

Return to Summary Table.

Main R5 Core 3 Windowed watchdog timer functional clock selection control.

Table 6-581. CTRLMMR_WWD31_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 83FCh	0010 A3FCh

Figure 6-290. CTRLMMR_WWD31_CLKSEL Register

31	30	29	28	27	26	25	24
WRTLOCK	RESERVED						
R/W-0h	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED					CLK_SEL		
R-0h					R/W-0h		

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-582. CTRLMMR_WWD31_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	WRTLOCK	R/W	0h	When set, locks CTRLMMR_WWD31_CLKSEL from further writes until the next module reset.
30-3	RESERVED	R	0h	Reserved
2-0	CLK_SEL	R/W	0h	Windowed watchdog timer functional clock input select mux control These bits are warm reset isolated to preserve R5 RTI clock selection. 0h - WKUP_HFOSC0_CLKOUT 1h - LPXOSC_CLKOUT 2h - CLK_12M_RC 3h - CLK_32K 4h - HFOSC1_CLKOUT 5h - reserved (HFOSC1_CLKOUT) 6h - reserved (HFOSC1_CLKOUT) 7h - reserved (HFOSC1_CLKOUT)

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6.291 CTRLMMR_SERDES0_CLKSEL Register (Proxy0 Offset = 8400h; Proxy1 Offset = A400h) [reset = 0h]

CTRLMMR_SERDES0_CLKSEL is shown in Figure 6-291 and described in Table 6-584.

Return to Summary Table.

Selects the clock source for Lane 0 when configured as 2 single lane PHYs and Lane 0-1 when configured as a dual lane PHY.

Table 6-583. CTRLMMR_SERDES0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8400h	0010 A400h

Figure 6-291. CTRLMMR_SERDES0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CORE_REFCLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-584. CTRLMMR_SERDES0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CORE_REFCLK_SEL	R/W	0h	Selects the source for the core_refclk input 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL3_HSDIV4_CLKOUT 3h - MAIN_PLL2_HSDIV4_CLKOUT

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6.292 CTRLMMR_SERDES0_CLK1SEL Register (Proxy0 Offset = 8404h; Proxy1 Offset = A404h) [reset = 0h]

CTRLMMR_SERDES0_CLK1SEL is shown in Figure 6-292 and described in Table 6-586.

Return to Summary Table.

Selects the clock source for Lane1 when configured as 2 single lane PHYs.

Table 6-585. CTRLMMR_SERDES0_CLK1SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8404h	0010 A404h

Figure 6-292. CTRLMMR_SERDES0_CLK1SEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CORE_REFCLK1_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-586. CTRLMMR_SERDES0_CLK1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CORE_REFCLK1_SEL	R/W	0h	Selects the source for the core_refclk1 input 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL3_HSDIV4_CLKOUT 3h - MAIN_PLL2_HSDIV4_CLKOUT

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6.293 CTRLMMR_SERDES1_CLKSEL Register (Proxy0 Offset = 8410h; Proxy1 Offset = A410h) [reset = 0h]

CTRLMMR_SERDES1_CLKSEL is shown in Figure 6-293 and described in Table 6-588.

Return to Summary Table.

Selects the clock source for Lane 0 when configured as 2 single lane PHYs and Lane 0-1 when configured as a dual lane PHY.

Table 6-587. CTRLMMR_SERDES1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8410h	0010 A410h

Figure 6-293. CTRLMMR_SERDES1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CORE_REFCLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-588. CTRLMMR_SERDES1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CORE_REFCLK_SEL	R/W	0h	Selects the source for the core_refclk input 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL3_HSDIV4_CLKOUT 3h - MAIN_PLL2_HSDIV4_CLKOUT

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6.294 CTRLMMR_SERDES1_CLK1SEL Register (Proxy0 Offset = 8414h; Proxy1 Offset = A414h) [reset = 0h]

CTRLMMR_SERDES1_CLK1SEL is shown in Figure 6-294 and described in Table 6-590.

Return to Summary Table.

Selects the clock source for Lane1 when configured as 2 single lane PHYs.

Table 6-589. CTRLMMR_SERDES1_CLK1SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8414h	0010 A414h

Figure 6-294. CTRLMMR_SERDES1_CLK1SEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CORE_REFCLK1_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-590. CTRLMMR_SERDES1_CLK1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CORE_REFCLK1_SEL	R/W	0h	Selects the source for the core_refclk1 input 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL3_HSDIV4_CLKOUT 3h - MAIN_PLL2_HSDIV4_CLKOUT

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6.295 CTRLMMR_SERDES2_CLKSEL Register (Proxy0 Offset = 8420h; Proxy1 Offset = A420h) [reset = 0h]

CTRLMMR_SERDES2_CLKSEL is shown in Figure 6-295 and described in Table 6-592.

Return to Summary Table.

Selects the clock source for Lane 0 when configured as 2 single lane PHYs and Lane 0-1 when configured as a dual lane PHY.

Table 6-591. CTRLMMR_SERDES2_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8420h	0010 A420h

Figure 6-295. CTRLMMR_SERDES2_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CORE_REFCLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-592. CTRLMMR_SERDES2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CORE_REFCLK_SEL	R/W	0h	Selects the source for the core_refclk input 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL3_HSDIV4_CLKOUT 3h - MAIN_PLL2_HSDIV4_CLKOUT

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6.296 CTRLMMR_SERDES2_CLK1SEL Register (Proxy0 Offset = 8424h; Proxy1 Offset = A424h) [reset = 0h]

CTRLMMR_SERDES2_CLK1SEL is shown in Figure 6-296 and described in Table 6-594.

Return to Summary Table.

Selects the clock source for Lane1 when configured as 2 single lane PHYs.

Table 6-593. CTRLMMR_SERDES2_CLK1SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8424h	0010 A424h

Figure 6-296. CTRLMMR_SERDES2_CLK1SEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CORE_REFCLK1_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-594. CTRLMMR_SERDES2_CLK1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CORE_REFCLK1_SEL	R/W	0h	Selects the source for the core_refclk1 input 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL3_HSDIV4_CLKOUT 3h - MAIN_PLL2_HSDIV4_CLKOUT

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6.297 CTRLMMR_SERDES3_CLKSEL Register (Proxy0 Offset = 8430h; Proxy1 Offset = A430h) [reset = 0h]

CTRLMMR_SERDES3_CLKSEL is shown in Figure 6-297 and described in Table 6-596.

Return to Summary Table.

Selects the clock source for Lane 0 when configured as 2 single lane PHYs and Lane 0-1 when configured as a dual lane PHY.

Table 6-595. CTRLMMR_SERDES3_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8430h	0010 A430h

Figure 6-297. CTRLMMR_SERDES3_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CORE_REFCLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-596. CTRLMMR_SERDES3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CORE_REFCLK_SEL	R/W	0h	Selects the source for the core_refclk input 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL3_HSDIV4_CLKOUT 3h - MAIN_PLL2_HSDIV4_CLKOUT

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6.298 CTRLMMR_SERDES3_CLK1SEL Register (Proxy0 Offset = 8434h; Proxy1 Offset = A434h) [reset = 0h]

CTRLMMR_SERDES3_CLK1SEL is shown in Figure 6-298 and described in Table 6-598.

Return to Summary Table.

Selects the clock source for Lane1 when configured as 2 single lane PHYs.

Table 6-597. CTRLMMR_SERDES3_CLK1SEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8434h	0010 A434h

Figure 6-298. CTRLMMR_SERDES3_CLK1SEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CORE_REFCLK1_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-598. CTRLMMR_SERDES3_CLK1SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CORE_REFCLK1_SEL	R/W	0h	Selects the source for the core_refclk1 input 0h - WKUP_HFOSC0_CLKOUT 1h - HFOSC1_CLKOUT 2h - MAIN_PLL3_HSDIV4_CLKOUT 3h - MAIN_PLL2_HSDIV4_CLKOUT

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6.299 CTRLMMR_MCAN0_CLKSEL Register (Proxy0 Offset = 8480h; Proxy1 Offset = A480h) [reset = 0h]

CTRLMMR_MCAN0_CLKSEL is shown in Figure 6-299 and described in Table 6-600.

Return to Summary Table.

Controls the functional clock source MCAN0.

Table 6-599. CTRLMMR_MCAN0_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8480h	0010 A480h

Figure 6-299. CTRLMMR_MCAN0_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-600. CTRLMMR_MCAN0_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.300 CTRLMMR_MCAN1_CLKSEL Register (Proxy0 Offset = 8484h; Proxy1 Offset = A484h) [reset = 0h]

CTRLMMR_MCAN1_CLKSEL is shown in Figure 6-300 and described in Table 6-602.

Return to Summary Table.

Controls the functional clock source MCAN1.

Table 6-601. CTRLMMR_MCAN1_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8484h	0010 A484h

Figure 6-300. CTRLMMR_MCAN1_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-602. CTRLMMR_MCAN1_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.301 CTRLMMR_MCAN2_CLKSEL Register (Proxy0 Offset = 8488h; Proxy1 Offset = A488h) [reset = 0h]

CTRLMMR_MCAN2_CLKSEL is shown in Figure 6-301 and described in Table 6-604.

Return to Summary Table.

Controls the functional clock source MCAN2.

Table 6-603. CTRLMMR_MCAN2_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8488h	0010 A488h

Figure 6-301. CTRLMMR_MCAN2_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-604. CTRLMMR_MCAN2_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.302 CTRLMMR_MCAN3_CLKSEL Register (Proxy0 Offset = 848Ch; Proxy1 Offset = A48Ch) [reset = 0h]

CTRLMMR_MCAN3_CLKSEL is shown in Figure 6-302 and described in Table 6-606.

Return to Summary Table.

Controls the functional clock source MCAN3.

Table 6-605. CTRLMMR_MCAN3_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 848Ch	0010 A48Ch

Figure 6-302. CTRLMMR_MCAN3_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-606. CTRLMMR_MCAN3_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.303 CTRLMMR_MCAN4_CLKSEL Register (Proxy0 Offset = 8490h; Proxy1 Offset = A490h) [reset = 0h]

CTRLMMR_MCAN4_CLKSEL is shown in Figure 6-303 and described in Table 6-608.

Return to Summary Table.

Controls the functional clock source MCAN4.

Table 6-607. CTRLMMR_MCAN4_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8490h	0010 A490h

Figure 6-303. CTRLMMR_MCAN4_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-608. CTRLMMR_MCAN4_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.304 CTRLMMR_MCAN5_CLKSEL Register (Proxy0 Offset = 8494h; Proxy1 Offset = A494h) [reset = 0h]

CTRLMMR_MCAN5_CLKSEL is shown in Figure 6-304 and described in Table 6-610.

Return to Summary Table.

Controls the functional clock source MCAN5.

Table 6-609. CTRLMMR_MCAN5_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8494h	0010 A494h

Figure 6-304. CTRLMMR_MCAN5_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-610. CTRLMMR_MCAN5_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.305 CTRLMMR_MCAN6_CLKSEL Register (Proxy0 Offset = 8498h; Proxy1 Offset = A498h) [reset = 0h]

CTRLMMR_MCAN6_CLKSEL is shown in Figure 6-305 and described in Table 6-612.

Return to Summary Table.

Controls the functional clock source MCAN6.

Table 6-611. CTRLMMR_MCAN6_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 8498h	0010 A498h

Figure 6-305. CTRLMMR_MCAN6_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-612. CTRLMMR_MCAN6_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.306 CTRLMMR_MCAN7_CLKSEL Register (Proxy0 Offset = 849Ch; Proxy1 Offset = A49Ch) [reset = 0h]

CTRLMMR_MCAN7_CLKSEL is shown in Figure 6-306 and described in Table 6-614.

Return to Summary Table.

Controls the functional clock source MCAN7.

Table 6-613. CTRLMMR_MCAN7_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 849Ch	0010 A49Ch

Figure 6-306. CTRLMMR_MCAN7_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-614. CTRLMMR_MCAN7_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.307 CTRLMMR_MCAN8_CLKSEL Register (Proxy0 Offset = 84A0h; Proxy1 Offset = A4A0h) [reset = 0h]

CTRLMMR_MCAN8_CLKSEL is shown in Figure 6-307 and described in Table 6-616.

Return to Summary Table.

Controls the functional clock source MCAN8.

Table 6-615. CTRLMMR_MCAN8_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 84A0h	0010 A4A0h

Figure 6-307. CTRLMMR_MCAN8_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-616. CTRLMMR_MCAN8_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.308 CTRLMMR_MCAN9_CLKSEL Register (Proxy0 Offset = 84A4h; Proxy1 Offset = A4A4h) [reset = 0h]

CTRLMMR_MCAN9_CLKSEL is shown in Figure 6-308 and described in Table 6-618.

Return to Summary Table.

Controls the functional clock source MCAN9.

Table 6-617. CTRLMMR_MCAN9_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 84A4h	0010 A4A4h

Figure 6-308. CTRLMMR_MCAN9_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-618. CTRLMMR_MCAN9_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.309 CTRLMMR_MCAN10_CLKSEL Register (Proxy0 Offset = 84A8h; Proxy1 Offset = A4A8h) [reset = 0h]

CTRLMMR_MCAN10_CLKSEL is shown in Figure 6-309 and described in Table 6-620.

Return to Summary Table.

Controls the functional clock source MCAN10.

Table 6-619. CTRLMMR_MCAN10_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 84A8h	0010 A4A8h

Figure 6-309. CTRLMMR_MCAN10_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-620. CTRLMMR_MCAN10_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.310 CTRLMMR_MCAN11_CLKSEL Register (Proxy0 Offset = 84ACh; Proxy1 Offset = A4ACh) [reset = 0h]

CTRLMMR_MCAN11_CLKSEL is shown in Figure 6-310 and described in Table 6-622.

Return to Summary Table.

Controls the functional clock source MCAN11.

Table 6-621. CTRLMMR_MCAN11_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 84ACh	0010 A4ACh

Figure 6-310. CTRLMMR_MCAN11_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-622. CTRLMMR_MCAN11_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.311 CTRLMMR_MCAN12_CLKSEL Register (Proxy0 Offset = 84B0h; Proxy1 Offset = A4B0h) [reset = 0h]

CTRLMMR_MCAN12_CLKSEL is shown in Figure 6-311 and described in Table 6-624.

Return to Summary Table.

Controls the functional clock source MCAN12.

Table 6-623. CTRLMMR_MCAN12_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 84B0h	0010 A4B0h

Figure 6-311. CTRLMMR_MCAN12_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-624. CTRLMMR_MCAN12_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.312 CTRLMMR_MCAN13_CLKSEL Register (Proxy0 Offset = 84B4h; Proxy1 Offset = A4B4h) [reset = 0h]

CTRLMMR_MCAN13_CLKSEL is shown in Figure 6-312 and described in Table 6-626.

Return to Summary Table.

Controls the functional clock source MCAN13.

Table 6-625. CTRLMMR_MCAN13_CLKSEL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 84B4h	0010 A4B4h

Figure 6-312. CTRLMMR_MCAN13_CLKSEL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						CLK_SEL	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-626. CTRLMMR_MCAN13_CLKSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	CLK_SEL	R/W	0h	MAIN MCAN_CLK selection 0h - MAIN_PLL0_HSDIV4_CLKOUT 1h - MCU_EXT_REFCLK0 (pin) 2h - HFOSC1_CLKOUT 3h - WKUP_HFOSC0_CLKOUT

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6.313 CTRLMMR_LOCK2_KICK0 Register (Proxy0 Offset = 9008h; Proxy1 Offset = B008h) [reset = 0h]

CTRLMMR_LOCK2_KICK0 is shown in Figure 6-313 and described in Table 6-628.

Return to Summary Table.

Lower 32-bits of Partition2 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_LOCK2_KICK1 with its key value before write-protected Partition 2 registers can be written.

Table 6-627. CTRLMMR_LOCK2_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 9008h	0010 B008h

Figure 6-313. CTRLMMR_LOCK2_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-628. CTRLMMR_LOCK2_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition2 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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6.314 CTRLMMR_LOCK2_KICK1 Register (Proxy0 Offset = 900Ch; Proxy1 Offset = B00Ch) [reset = 0h]

CTRLMMR_LOCK2_KICK1 is shown in Figure 6-314 and described in Table 6-630.

Return to Summary Table.

Upper 32-bits of Partition 2 write lock key. This register must be written with the designated key value after a write to CTRLMMR_LOCK2_KICK0 with its key value before write-protected Partition 2 registers can be written.

Table 6-629. CTRLMMR_LOCK2_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 900Ch	0010 B00Ch

Figure 6-314. CTRLMMR_LOCK2_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-630. CTRLMMR_LOCK2_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition2 registers

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6.315 CTRLMMR_P2_CLAIM0 Register (Proxy0 Offset = 9100h; Proxy1 Offset = B100h) [reset = 0h]

CTRLMMR_P2_CLAIM0 is shown in Figure 6-315 and described in Table 6-632.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 6-631. CTRLMMR_P2_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 9100h	0010 B100h

Figure 6-315. CTRLMMR_P2_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-632. CTRLMMR_P2_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x8000 + (0 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xA000 + (0 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.316 CTRLMMR_P2_CLAIM1 Register (Proxy0 Offset = 9104h; Proxy1 Offset = B104h) [reset = 0h]

CTRLMMR_P2_CLAIM1 is shown in Figure 6-316 and described in Table 6-634.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 6-633. CTRLMMR_P2_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 9104h	0010 B104h

Figure 6-316. CTRLMMR_P2_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-634. CTRLMMR_P2_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x8000 + (1 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xA000 + (1 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.317 CTRLMMR_P2_CLAIM2 Register (Proxy0 Offset = 9108h; Proxy1 Offset = B108h) [reset = 0h]

CTRLMMR_P2_CLAIM2 is shown in Figure 6-317 and described in Table 6-636.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 6-635. CTRLMMR_P2_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 9108h	0010 B108h

Figure 6-317. CTRLMMR_P2_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-636. CTRLMMR_P2_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x8000 + (2 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xA000 + (2 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.318 CTRLMMR_P2_CLAIM3 Register (Proxy0 Offset = 910Ch; Proxy1 Offset = B10Ch) [reset = 0h]

CTRLMMR_P2_CLAIM3 is shown in Figure 6-318 and described in Table 6-638.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 6-637. CTRLMMR_P2_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 910Ch	0010 B10Ch

Figure 6-318. CTRLMMR_P2_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-638. CTRLMMR_P2_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x8000 + (3 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xA000 + (3 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.319 CTRLMMR_P2_CLAIM4 Register (Proxy0 Offset = 9110h; Proxy1 Offset = B110h) [reset = 0h]

CTRLMMR_P2_CLAIM4 is shown in Figure 6-319 and described in Table 6-640.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 6-639. CTRLMMR_P2_CLAIM4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 9110h	0010 B110h

Figure 6-319. CTRLMMR_P2_CLAIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-640. CTRLMMR_P2_CLAIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x8000 + (4 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xA000 + (4 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.320 CTRLMMR_P2_CLAIM5 Register (Proxy0 Offset = 9114h; Proxy1 Offset = B114h) [reset = 0h]

CTRLMMR_P2_CLAIM5 is shown in Figure 6-320 and described in Table 6-642.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 6-641. CTRLMMR_P2_CLAIM5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 9114h	0010 B114h

Figure 6-320. CTRLMMR_P2_CLAIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-642. CTRLMMR_P2_CLAIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x8000 + (5 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xA000 + (5 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.321 CTRLMMR_P2_CLAIM6 Register (Proxy0 Offset = 9118h; Proxy1 Offset = B118h) [reset = 0h]

CTRLMMR_P2_CLAIM6 is shown in Figure 6-321 and described in Table 6-644.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 6-643. CTRLMMR_P2_CLAIM6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 9118h	0010 B118h

Figure 6-321. CTRLMMR_P2_CLAIM6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-644. CTRLMMR_P2_CLAIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x8000 + (6 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xA000 + (6 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.322 CTRLMMR_P2_CLAIM7 Register (Proxy0 Offset = 911Ch; Proxy1 Offset = B11Ch) [reset = 0h]

CTRLMMR_P2_CLAIM7 is shown in Figure 6-322 and described in Table 6-646.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 6-645. CTRLMMR_P2_CLAIM7 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 911Ch	0010 B11Ch

Figure 6-322. CTRLMMR_P2_CLAIM7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-646. CTRLMMR_P2_CLAIM7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x8000 + (7 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xA000 + (7 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.323 CTRLMMR_P2_CLAIM8 Register (Proxy0 Offset = 9120h; Proxy1 Offset = B120h) [reset = 0h]

CTRLMMR_P2_CLAIM8 is shown in Figure 6-323 and described in Table 6-648.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 6-647. CTRLMMR_P2_CLAIM8 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 9120h	0010 B120h

Figure 6-323. CTRLMMR_P2_CLAIM8 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-648. CTRLMMR_P2_CLAIM8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x8000 + (8 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xA000 + (8 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.324 CTRLMMR_P2_CLAIM9 Register (Proxy0 Offset = 9124h; Proxy1 Offset = B124h) [reset = 0h]

CTRLMMR_P2_CLAIM9 is shown in Figure 6-324 and described in Table 6-650.

Return to Summary Table.

Claim bits for Partition2 Registers.

Table 6-649. CTRLMMR_P2_CLAIM9 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 9124h	0010 B124h

Figure 6-324. CTRLMMR_P2_CLAIM9 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-650. CTRLMMR_P2_CLAIM9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x8000 + (9 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xA000 + (9 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.325 CTRLMMR_MCU0_LBIST_CTRL Register (Proxy0 Offset = C000h; Proxy1 Offset = E000h) [reset = 0h]

CTRLMMR_MCU0_LBIST_CTRL is shown in Figure 6-325 and described in Table 6-652.

Return to Summary Table.

Configures and enables LBIST operation.

Table 6-651. CTRLMMR_MCU0_LBIST_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C000h	0010 E000h

Figure 6-325. CTRLMMR_MCU0_LBIST_CTRL Register

31	30	29	28	27	26	25	24
BIST_RESET	RESERVED			BIST_RUN			
R/W-0h	R-0h			R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RUNBIST_MODE				RESERVED		DC_DEF	
R/W-0h				R-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOAD_DIV	RESERVED		DIVIDE_RATIO				
R/W-0h	R-0h		R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-652. CTRLMMR_MCU0_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_RESET	R/W	0h	Reset LBIST macro
30-28	RESERVED	R	0h	Reserved
27-24	BIST_RUN	R/W	0h	Starts LBIST if all bits are 1
23-16	RESERVED	R	0h	Reserved
15-12	RUNBIST_MODE	R/W	0h	Runbist mode enable if all bits are 1
11-10	RESERVED	R	0h	Reserved
9-8	DC_DEF	R/W	0h	Clock delay after scan_enable switching
7	LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1
6-5	RESERVED	R	0h	Reserved
4-0	DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio

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6.326 CTRLMMR_MCU0_LBIST_PATCOUNT Register (Proxy0 Offset = C004h; Proxy1 Offset = E004h) [reset = 0h]

CTRLMMR_MCU0_LBIST_PATCOUNT is shown in Figure 6-326 and described in Table 6-654.

Return to Summary Table.

Specifies the number of LBIST patterns to run.

Table 6-653. CTRLMMR_MCU0_LBIST_PATCOUNT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C004h	0010 E004h

Figure 6-326. CTRLMMR_MCU0_LBIST_PATCOUNT Register

31	30	29	28	27	26	25	24
RESERVED		STATIC_PC_DEF					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
STATIC_PC_DEF							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				SET_PC_DEF			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESET_PC_DEF				SCAN_PC_DEF			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-654. CTRLMMR_MCU0_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run
15-12	RESERVED	R	0h	Reserved
11-8	SET_PC_DEF	R/W	0h	Number of set patterns to run
7-4	RESET_PC_DEF	R/W	0h	Number of reset patterns to run
3-0	SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run

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6.327 CTRLMMR_MCU0_LBIST_SEED0 Register (Proxy0 Offset = C008h; Proxy1 Offset = E008h) [reset = 0h]

CTRLMMR_MCU0_LBIST_SEED0 is shown in Figure 6-327 and described in Table 6-656.

Return to Summary Table.

Specifies the 32 LSBs of the PRPG seed.

Table 6-655. CTRLMMR_MCU0_LBIST_SEED0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C008h	0010 E008h

Figure 6-327. CTRLMMR_MCU0_LBIST_SEED0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRPG_DEF																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-656. CTRLMMR_MCU0_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0)

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6.328 CTRLMMR_MCU0_LBIST_SEED1 Register (Proxy0 Offset = C00Ch; Proxy1 Offset = E00Ch) [reset = 0h]

CTRLMMR_MCU0_LBIST_SEED1 is shown in Figure 6-328 and described in Table 6-658.

Return to Summary Table.

Specifies the 21 MSBs of the PRPG seed.

Table 6-657. CTRLMMR_MCU0_LBIST_SEED1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C00Ch	0010 E00Ch

Figure 6-328. CTRLMMR_MCU0_LBIST_SEED1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRPG_DEF																				
R-0h											R/W-0h																				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-658. CTRLMMR_MCU0_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32)

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6.329 CTRLMMR_MCU0_LBIST_SPARE0 Register (Proxy0 Offset = C010h; Proxy1 Offset = E010h) [reset = 0h]

CTRLMMR_MCU0_LBIST_SPARE0 is shown in Figure 6-329 and described in Table 6-660.

Return to Summary Table.

Spare LBIST control bits.

Table 6-659. CTRLMMR_MCU0_LBIST_SPARE0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C010h	0010 E010h

Figure 6-329. CTRLMMR_MCU0_LBIST_SPARE0 Register

31	30	29	28	27	26	25	24
SPARE0							
R/W-0h							
23	22	21	20	19	18	17	16
SPARE0							
R/W-0h							
15	14	13	12	11	10	9	8
SPARE0							
R/W-0h							
7	6	5	4	3	2	1	0
SPARE0						PBIST_SELFTEST_EN	LBIST_SELFTEST_EN
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-660. CTRLMMR_MCU0_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	SPARE0	R/W	0h	LBIST spare bits
1	PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control
0	LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control

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6.330 CTRLMMR_MCU0_LBIST_SPARE1 Register (Proxy0 Offset = C014h; Proxy1 Offset = E014h) [reset = 0h]

CTRLMMR_MCU0_LBIST_SPARE1 is shown in Figure 6-330 and described in Table 6-662.

Return to Summary Table.

Spare LBIST control bits.

Table 6-661. CTRLMMR_MCU0_LBIST_SPARE1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C014h	0010 E014h

Figure 6-330. CTRLMMR_MCU0_LBIST_SPARE1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-662. CTRLMMR_MCU0_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE1	R/W	0h	LBIST spare bits

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6.331 CTRLMMR_MCU0_LBIST_STAT Register (Proxy0 Offset = C018h; Proxy1 Offset = E018h) [reset = X]

CTRLMMR_MCU0_LBIST_STAT is shown in Figure 6-331 and described in Table 6-664.

Return to Summary Table.

Indicates LBIST status and provides MISR selection control.

Table 6-663. CTRLMMR_MCU0_LBIST_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C018h	0010 E018h

Figure 6-331. CTRLMMR_MCU0_LBIST_STAT Register

31	30	29	28	27	26	25	24
BIST_DONE	RESERVED						
R-X	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
BIST_RUNNING	RESERVED					OUT_MUX_CTL	
R-X	R-0h					R/W-0h	

7	6	5	4	3	2	1	0
MISR_MUX_CTL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-664. CTRLMMR_MCU0_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_DONE	R	X	LBIST is done
30-16	RESERVED	R	0h	Reserved
15	BIST_RUNNING	R	X	LBIST is running
14-10	RESERVED	R	0h	Reserved
9-8	OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 0h - LBIST IP CTRLMMR_PID value 1h - LBIST CTRL ID value 1x - MISR value
7-0	MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR.

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6.332 CTRLMMR_MCU0_LBIST_MISR Register (Proxy0 Offset = C01Ch; Proxy1 Offset = E01Ch) [reset = X]

CTRLMMR_MCU0_LBIST_MISR is shown in Figure 6-332 and described in Table 6-666.

Return to Summary Table.

Contains LBIST MISR output value.

Table 6-665. CTRLMMR_MCU0_LBIST_MISR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C01Ch	0010 E01Ch

Figure 6-332. CTRLMMR_MCU0_LBIST_MISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_RESULT																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-666. CTRLMMR_MCU0_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl

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6.333 CTRLMMR_MCU1_LBIST_CTRL Register (Proxy0 Offset = C020h; Proxy1 Offset = E020h) [reset = 0h]

CTRLMMR_MCU1_LBIST_CTRL is shown in Figure 6-333 and described in Table 6-668.

Return to Summary Table.

Configures and enables LBIST operation.

Table 6-667. CTRLMMR_MCU1_LBIST_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C020h	0010 E020h

Figure 6-333. CTRLMMR_MCU1_LBIST_CTRL Register

31	30	29	28	27	26	25	24
BIST_RESET	RESERVED			BIST_RUN			
R/W-0h	R-0h			R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RUNBIST_MODE				RESERVED		DC_DEF	
R/W-0h				R-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOAD_DIV	RESERVED		DIVIDE_RATIO				
R/W-0h	R-0h		R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-668. CTRLMMR_MCU1_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_RESET	R/W	0h	Reset LBIST macro
30-28	RESERVED	R	0h	Reserved
27-24	BIST_RUN	R/W	0h	Starts LBIST if all bits are 1
23-16	RESERVED	R	0h	Reserved
15-12	RUNBIST_MODE	R/W	0h	Runbist mode enable if all bits are 1
11-10	RESERVED	R	0h	Reserved
9-8	DC_DEF	R/W	0h	Clock delay after scan_enable switching
7	LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1
6-5	RESERVED	R	0h	Reserved
4-0	DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio

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6.334 CTRLMMR_MCU1_LBIST_PATCOUNT Register (Proxy0 Offset = C024h; Proxy1 Offset = E024h) [reset = 0h]

CTRLMMR_MCU1_LBIST_PATCOUNT is shown in Figure 6-334 and described in Table 6-670.

Return to Summary Table.

Specifies the number of LBIST patterns to run.

Table 6-669. CTRLMMR_MCU1_LBIST_PATCOUNT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C024h	0010 E024h

Figure 6-334. CTRLMMR_MCU1_LBIST_PATCOUNT Register

31	30	29	28	27	26	25	24
RESERVED		STATIC_PC_DEF					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
STATIC_PC_DEF							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				SET_PC_DEF			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESET_PC_DEF				SCAN_PC_DEF			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-670. CTRLMMR_MCU1_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run
15-12	RESERVED	R	0h	Reserved
11-8	SET_PC_DEF	R/W	0h	Number of set patterns to run
7-4	RESET_PC_DEF	R/W	0h	Number of reset patterns to run
3-0	SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run

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6.335 CTRLMMR_MCU1_LBIST_SEED0 Register (Proxy0 Offset = C028h; Proxy1 Offset = E028h) [reset = 0h]

CTRLMMR_MCU1_LBIST_SEED0 is shown in Figure 6-335 and described in Table 6-672.

Return to Summary Table.

Specifies the 32 LSBs of the PRPG seed.

Table 6-671. CTRLMMR_MCU1_LBIST_SEED0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C028h	0010 E028h

Figure 6-335. CTRLMMR_MCU1_LBIST_SEED0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRPG_DEF																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-672. CTRLMMR_MCU1_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0)

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6.336 CTRLMMR_MCU1_LBIST_SEED1 Register (Proxy0 Offset = C02Ch; Proxy1 Offset = E02Ch) [reset = 0h]

CTRLMMR_MCU1_LBIST_SEED1 is shown in Figure 6-336 and described in Table 6-674.

Return to Summary Table.

Specifies the 21 MSBs of the PRPG seed.

Table 6-673. CTRLMMR_MCU1_LBIST_SEED1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C02Ch	0010 E02Ch

Figure 6-336. CTRLMMR_MCU1_LBIST_SEED1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRPG_DEF																				
R-0h											R/W-0h																				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-674. CTRLMMR_MCU1_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32)

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6.337 CTRLMMR_MCU1_LBIST_SPARE0 Register (Proxy0 Offset = C030h; Proxy1 Offset = E030h) [reset = 0h]

CTRLMMR_MCU1_LBIST_SPARE0 is shown in Figure 6-337 and described in Table 6-676.

Return to Summary Table.

Spare LBIST control bits.

Table 6-675. CTRLMMR_MCU1_LBIST_SPARE0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C030h	0010 E030h

Figure 6-337. CTRLMMR_MCU1_LBIST_SPARE0 Register

31	30	29	28	27	26	25	24
SPARE0							
R/W-0h							
23	22	21	20	19	18	17	16
SPARE0							
R/W-0h							
15	14	13	12	11	10	9	8
SPARE0							
R/W-0h							
7	6	5	4	3	2	1	0
SPARE0						PBIST_SELFTEST_EN	LBIST_SELFTEST_EN
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-676. CTRLMMR_MCU1_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	SPARE0	R/W	0h	LBIST spare bits
1	PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control
0	LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control

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6.338 CTRLMMR_MCU1_LBIST_SPARE1 Register (Proxy0 Offset = C034h; Proxy1 Offset = E034h) [reset = 0h]

CTRLMMR_MCU1_LBIST_SPARE1 is shown in Figure 6-338 and described in Table 6-678.

Return to Summary Table.

Spare LBIST control bits.

Table 6-677. CTRLMMR_MCU1_LBIST_SPARE1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C034h	0010 E034h

Figure 6-338. CTRLMMR_MCU1_LBIST_SPARE1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-678. CTRLMMR_MCU1_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE1	R/W	0h	LBIST spare bits

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6.339 CTRLMMR_MCU1_LBIST_STAT Register (Proxy0 Offset = C038h; Proxy1 Offset = E038h) [reset = X]

CTRLMMR_MCU1_LBIST_STAT is shown in Figure 6-339 and described in Table 6-680.

Return to Summary Table.

Indicates LBIST status and provides MISR selection control.

Table 6-679. CTRLMMR_MCU1_LBIST_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C038h	0010 E038h

Figure 6-339. CTRLMMR_MCU1_LBIST_STAT Register

31	30	29	28	27	26	25	24
BIST_DONE	RESERVED						
R-X	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
BIST_RUNNING	RESERVED					OUT_MUX_CTL	
R-X	R-0h					R/W-0h	

7	6	5	4	3	2	1	0
MISR_MUX_CTL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-680. CTRLMMR_MCU1_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_DONE	R	X	LBIST is done
30-16	RESERVED	R	0h	Reserved
15	BIST_RUNNING	R	X	LBIST is running
14-10	RESERVED	R	0h	Reserved
9-8	OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 0h - LBIST IP CTRLMMR_PID value 1h - LBIST CTRL ID value 1x - MISR value
7-0	MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR.

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6.340 CTRLMMR_MCU1_LBIST_MISR Register (Proxy0 Offset = C03Ch; Proxy1 Offset = E03Ch) [reset = X]

CTRLMMR_MCU1_LBIST_MISR is shown in Figure 6-340 and described in Table 6-682.

Return to Summary Table.

Contains LBIST MISR output value.

Table 6-681. CTRLMMR_MCU1_LBIST_MISR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C03Ch	0010 E03Ch

Figure 6-340. CTRLMMR_MCU1_LBIST_MISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_RESULT																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-682. CTRLMMR_MCU1_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl

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6.341 CTRLMMR_DMPAC_LBIST_CTRL Register (Proxy0 Offset = C040h; Proxy1 Offset = E040h) [reset = 0h]

CTRLMMR_DMPAC_LBIST_CTRL is shown in Figure 6-341 and described in Table 6-684.

Return to Summary Table.

Configures and enables LBIST operation.

Table 6-683. CTRLMMR_DMPAC_LBIST_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C040h	0010 E040h

Figure 6-341. CTRLMMR_DMPAC_LBIST_CTRL Register

31	30	29	28	27	26	25	24
BIST_RESET	RESERVED			BIST_RUN			
R/W-0h	R-0h			R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RUNBIST_MODE				RESERVED		DC_DEF	
R/W-0h				R-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOAD_DIV	RESERVED		DIVIDE_RATIO				
R/W-0h	R-0h		R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-684. CTRLMMR_DMPAC_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_RESET	R/W	0h	Reset LBIST macro
30-28	RESERVED	R	0h	Reserved
27-24	BIST_RUN	R/W	0h	Starts LBIST if all bits are 1
23-16	RESERVED	R	0h	Reserved
15-12	RUNBIST_MODE	R/W	0h	Runbist mode enable if all bits are 1
11-10	RESERVED	R	0h	Reserved
9-8	DC_DEF	R/W	0h	Clock delay after scan_enable switching
7	LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1
6-5	RESERVED	R	0h	Reserved
4-0	DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio

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6.342 CTRLMMR_DMPAC_LBIST_PATCOUNT Register (Proxy0 Offset = C044h; Proxy1 Offset = E044h) [reset = 0h]

CTRLMMR_DMPAC_LBIST_PATCOUNT is shown in Figure 6-342 and described in Table 6-686.

Return to Summary Table.

Specifies the number of LBIST patterns to run.

Table 6-685. CTRLMMR_DMPAC_LBIST_PATCOUNT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C044h	0010 E044h

Figure 6-342. CTRLMMR_DMPAC_LBIST_PATCOUNT Register

31	30	29	28	27	26	25	24
RESERVED		STATIC_PC_DEF					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
STATIC_PC_DEF							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				SET_PC_DEF			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESET_PC_DEF				SCAN_PC_DEF			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-686. CTRLMMR_DMPAC_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run
15-12	RESERVED	R	0h	Reserved
11-8	SET_PC_DEF	R/W	0h	Number of set patterns to run
7-4	RESET_PC_DEF	R/W	0h	Number of reset patterns to run
3-0	SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run

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6.343 CTRLMMR_DMPAC_LBIST_SEED0 Register (Proxy0 Offset = C048h; Proxy1 Offset = E048h) [reset = 0h]

CTRLMMR_DMPAC_LBIST_SEED0 is shown in Figure 6-343 and described in Table 6-688.

Return to Summary Table.

Specifies the 32 LSBs of the PRPG seed.

Table 6-687. CTRLMMR_DMPAC_LBIST_SEED0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C048h	0010 E048h

Figure 6-343. CTRLMMR_DMPAC_LBIST_SEED0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRPG_DEF																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-688. CTRLMMR_DMPAC_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0)

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6.344 CTRLMMR_DMPAC_LBIST_SEED1 Register (Proxy0 Offset = C04Ch; Proxy1 Offset = E04Ch) [reset = 0h]

CTRLMMR_DMPAC_LBIST_SEED1 is shown in Figure 6-344 and described in Table 6-690.

Return to Summary Table.

Specifies the 21 MSBs of the PRPG seed.

Table 6-689. CTRLMMR_DMPAC_LBIST_SEED1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C04Ch	0010 E04Ch

Figure 6-344. CTRLMMR_DMPAC_LBIST_SEED1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRPG_DEF																				
R-0h											R/W-0h																				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-690. CTRLMMR_DMPAC_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32)

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6.345 CTRLMMR_DMPAC_LBIST_SPARE0 Register (Proxy0 Offset = C050h; Proxy1 Offset = E050h) [reset = 0h]

CTRLMMR_DMPAC_LBIST_SPARE0 is shown in Figure 6-345 and described in Table 6-692.

Return to Summary Table.

Spare LBIST control bits.

Table 6-691. CTRLMMR_DMPAC_LBIST_SPARE0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C050h	0010 E050h

Figure 6-345. CTRLMMR_DMPAC_LBIST_SPARE0 Register

31	30	29	28	27	26	25	24
SPARE0							
R/W-0h							
23	22	21	20	19	18	17	16
SPARE0							
R/W-0h							
15	14	13	12	11	10	9	8
SPARE0							
R/W-0h							
7	6	5	4	3	2	1	0
SPARE0						PBIST_SELFTEST_EN	LBIST_SELFTEST_EN
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-692. CTRLMMR_DMPAC_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	SPARE0	R/W	0h	LBIST spare bits
1	PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control
0	LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control

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6.346 CTRLMMR_DMPAC_LBIST_SPARE1 Register (Proxy0 Offset = C054h; Proxy1 Offset = E054h) [reset = 0h]

CTRLMMR_DMPAC_LBIST_SPARE1 is shown in Figure 6-346 and described in Table 6-694.

Return to Summary Table.

Spare LBIST control bits.

Table 6-693. CTRLMMR_DMPAC_LBIST_SPARE1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C054h	0010 E054h

Figure 6-346. CTRLMMR_DMPAC_LBIST_SPARE1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-694. CTRLMMR_DMPAC_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE1	R/W	0h	LBIST spare bits

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6.347 CTRLMMR_DMPAC_LBIST_STAT Register (Proxy0 Offset = C058h; Proxy1 Offset = E058h) [reset = X]

CTRLMMR_DMPAC_LBIST_STAT is shown in Figure 6-347 and described in Table 6-696.

Return to Summary Table.

Indicates LBIST status and provides MISR selection control.

Table 6-695. CTRLMMR_DMPAC_LBIST_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C058h	0010 E058h

Figure 6-347. CTRLMMR_DMPAC_LBIST_STAT Register

31	30	29	28	27	26	25	24
BIST_DONE	RESERVED						
R-X	R-0h						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
BIST_RUNNING	RESERVED					OUT_MUX_CTL	
R-X	R-0h					R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MISR_MUX_CTL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-696. CTRLMMR_DMPAC_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_DONE	R	X	LBIST is done
30-16	RESERVED	R	0h	Reserved
15	BIST_RUNNING	R	X	LBIST is running
14-10	RESERVED	R	0h	Reserved
9-8	OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 0h - LBIST IP CTRLMMR_PID value 1h - LBIST CTRL ID value 1x - MISR value
7-0	MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR.

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6.348 CTRLMMR_DMPAC_LBIST_MISR Register (Proxy0 Offset = C05Ch; Proxy1 Offset = E05Ch) [reset = X]

CTRLMMR_DMPAC_LBIST_MISR is shown in Figure 6-348 and described in Table 6-698.

Return to Summary Table.

Contains LBIST MISR output value.

Table 6-697. CTRLMMR_DMPAC_LBIST_MISR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C05Ch	0010 E05Ch

Figure 6-348. CTRLMMR_DMPAC_LBIST_MISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_RESULT																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-698. CTRLMMR_DMPAC_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl

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6.349 CTRLMMR_VPAC_LBIST_CTRL Register (Proxy0 Offset = C060h; Proxy1 Offset = E060h) [reset = 0h]

CTRLMMR_VPAC_LBIST_CTRL is shown in Figure 6-349 and described in Table 6-700.

Return to Summary Table.

Configures and enables LBIST operation.

Table 6-699. CTRLMMR_VPAC_LBIST_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C060h	0010 E060h

Figure 6-349. CTRLMMR_VPAC_LBIST_CTRL Register

31	30	29	28	27	26	25	24
BIST_RESET	RESERVED			BIST_RUN			
R/W-0h	R-0h			R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RUNBIST_MODE				RESERVED		DC_DEF	
R/W-0h				R-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOAD_DIV	RESERVED		DIVIDE_RATIO				
R/W-0h	R-0h		R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-700. CTRLMMR_VPAC_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_RESET	R/W	0h	Reset LBIST macro
30-28	RESERVED	R	0h	Reserved
27-24	BIST_RUN	R/W	0h	Starts LBIST if all bits are 1
23-16	RESERVED	R	0h	Reserved
15-12	RUNBIST_MODE	R/W	0h	Runbist mode enable if all bits are 1
11-10	RESERVED	R	0h	Reserved
9-8	DC_DEF	R/W	0h	Clock delay after scan_enable switching
7	LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1
6-5	RESERVED	R	0h	Reserved
4-0	DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio

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6.350 CTRLMMR_VPAC_LBIST_PATCOUNT Register (Proxy0 Offset = C064h; Proxy1 Offset = E064h) [reset = 0h]

CTRLMMR_VPAC_LBIST_PATCOUNT is shown in Figure 6-350 and described in Table 6-702.

Return to Summary Table.

Specifies the number of LBIST patterns to run.

Table 6-701. CTRLMMR_VPAC_LBIST_PATCOUNT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C064h	0010 E064h

Figure 6-350. CTRLMMR_VPAC_LBIST_PATCOUNT Register

31	30	29	28	27	26	25	24
RESERVED		STATIC_PC_DEF					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
STATIC_PC_DEF							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				SET_PC_DEF			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESET_PC_DEF				SCAN_PC_DEF			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-702. CTRLMMR_VPAC_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run
15-12	RESERVED	R	0h	Reserved
11-8	SET_PC_DEF	R/W	0h	Number of set patterns to run
7-4	RESET_PC_DEF	R/W	0h	Number of reset patterns to run
3-0	SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run

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6.351 CTRLMMR_VPAC_LBIST_SEED0 Register (Proxy0 Offset = C068h; Proxy1 Offset = E068h) [reset = 0h]

CTRLMMR_VPAC_LBIST_SEED0 is shown in Figure 6-351 and described in Table 6-704.

Return to Summary Table.

Specifies the 32 LSBs of the PRPG seed.

Table 6-703. CTRLMMR_VPAC_LBIST_SEED0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C068h	0010 E068h

Figure 6-351. CTRLMMR_VPAC_LBIST_SEED0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRPG_DEF																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-704. CTRLMMR_VPAC_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0)

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6.352 CTRLMMR_VPAC_LBIST_SEED1 Register (Proxy0 Offset = C06Ch; Proxy1 Offset = E06Ch) [reset = 0h]

CTRLMMR_VPAC_LBIST_SEED1 is shown in Figure 6-352 and described in Table 6-706.

Return to Summary Table.

Specifies the 21 MSBs of the PRPG seed.

Table 6-705. CTRLMMR_VPAC_LBIST_SEED1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C06Ch	0010 E06Ch

Figure 6-352. CTRLMMR_VPAC_LBIST_SEED1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRPG_DEF																				
R-0h											R/W-0h																				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-706. CTRLMMR_VPAC_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32)

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6.353 CTRLMMR_VPAC_LBIST_SPARE0 Register (Proxy0 Offset = C070h; Proxy1 Offset = E070h) [reset = 0h]

CTRLMMR_VPAC_LBIST_SPARE0 is shown in Figure 6-353 and described in Table 6-708.

Return to Summary Table.

Spare LBIST control bits.

Table 6-707. CTRLMMR_VPAC_LBIST_SPARE0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C070h	0010 E070h

Figure 6-353. CTRLMMR_VPAC_LBIST_SPARE0 Register

31	30	29	28	27	26	25	24
SPARE0							
R/W-0h							
23	22	21	20	19	18	17	16
SPARE0							
R/W-0h							
15	14	13	12	11	10	9	8
SPARE0							
R/W-0h							
7	6	5	4	3	2	1	0
SPARE0						PBIST_SELFTEST_EN	LBIST_SELFTEST_EN
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-708. CTRLMMR_VPAC_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	SPARE0	R/W	0h	LBIST spare bits
1	PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control
0	LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control

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6.354 CTRLMMR_VPAC_LBIST_SPARE1 Register (Proxy0 Offset = C074h; Proxy1 Offset = E074h) [reset = 0h]

CTRLMMR_VPAC_LBIST_SPARE1 is shown in Figure 6-354 and described in Table 6-710.

Return to Summary Table.

Spare LBIST control bits.

Table 6-709. CTRLMMR_VPAC_LBIST_SPARE1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C074h	0010 E074h

Figure 6-354. CTRLMMR_VPAC_LBIST_SPARE1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-710. CTRLMMR_VPAC_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE1	R/W	0h	LBIST spare bits

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6.355 CTRLMMR_VPAC_LBIST_STAT Register (Proxy0 Offset = C078h; Proxy1 Offset = E078h) [reset = X]

CTRLMMR_VPAC_LBIST_STAT is shown in Figure 6-355 and described in Table 6-712.

Return to Summary Table.

Indicates LBIST status and provides MISR selection control.

Table 6-711. CTRLMMR_VPAC_LBIST_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C078h	0010 E078h

Figure 6-355. CTRLMMR_VPAC_LBIST_STAT Register

31	30	29	28	27	26	25	24
BIST_DONE	RESERVED						
R-X	R-0h						
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
BIST_RUNNING	RESERVED					OUT_MUX_CTL	
R-X	R-0h					R/W-0h	
7	6	5	4	3	2	1	0
MISR_MUX_CTL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-712. CTRLMMR_VPAC_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_DONE	R	X	LBIST is done
30-16	RESERVED	R	0h	Reserved
15	BIST_RUNNING	R	X	LBIST is running
14-10	RESERVED	R	0h	Reserved
9-8	OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 0h - LBIST IP CTRLMMR_PID value 1h - LBIST CTRL ID value 1x - MISR value
7-0	MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR.

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6.356 CTRLMMR_VPAC_LBIST_MISR Register (Proxy0 Offset = C07Ch; Proxy1 Offset = E07Ch) [reset = X]

CTRLMMR_VPAC_LBIST_MISR is shown in Figure 6-356 and described in Table 6-714.

Return to Summary Table.

Contains LBIST MISR output value.

Table 6-713. CTRLMMR_VPAC_LBIST_MISR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C07Ch	0010 E07Ch

Figure 6-356. CTRLMMR_VPAC_LBIST_MISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_RESULT																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-714. CTRLMMR_VPAC_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl

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6.357 CTRLMMR_DSP0_LBIST_CTRL Register (Proxy0 Offset = C080h; Proxy1 Offset = E080h) [reset = 0h]

CTRLMMR_DSP0_LBIST_CTRL is shown in Figure 6-357 and described in Table 6-716.

Return to Summary Table.

Configures and enables LBIST operation.

Table 6-715. CTRLMMR_DSP0_LBIST_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C080h	0010 E080h

Figure 6-357. CTRLMMR_DSP0_LBIST_CTRL Register

31	30	29	28	27	26	25	24
BIST_RESET	RESERVED			BIST_RUN			
R/W-0h	R-0h			R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RUNBIST_MODE				RESERVED		DC_DEF	
R/W-0h				R-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOAD_DIV	RESERVED		DIVIDE_RATIO				
R/W-0h	R-0h		R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-716. CTRLMMR_DSP0_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_RESET	R/W	0h	Reset LBIST macro
30-28	RESERVED	R	0h	Reserved
27-24	BIST_RUN	R/W	0h	Starts LBIST if all bits are 1
23-16	RESERVED	R	0h	Reserved
15-12	RUNBIST_MODE	R/W	0h	Runbist mode enable if all bits are 1
11-10	RESERVED	R	0h	Reserved
9-8	DC_DEF	R/W	0h	Clock delay after scan_enable switching
7	LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1
6-5	RESERVED	R	0h	Reserved
4-0	DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio

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6.358 CTRLMMR_DSP0_LBIST_PATCOUNT Register (Proxy0 Offset = C084h; Proxy1 Offset = E084h) [reset = 0h]

CTRLMMR_DSP0_LBIST_PATCOUNT is shown in Figure 6-358 and described in Table 6-718.

Return to Summary Table.

Specifies the number of LBIST patterns to run.

Table 6-717. CTRLMMR_DSP0_LBIST_PATCOUNT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C084h	0010 E084h

Figure 6-358. CTRLMMR_DSP0_LBIST_PATCOUNT Register

31	30	29	28	27	26	25	24
RESERVED		STATIC_PC_DEF					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
STATIC_PC_DEF							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				SET_PC_DEF			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESET_PC_DEF				SCAN_PC_DEF			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-718. CTRLMMR_DSP0_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run
15-12	RESERVED	R	0h	Reserved
11-8	SET_PC_DEF	R/W	0h	Number of set patterns to run
7-4	RESET_PC_DEF	R/W	0h	Number of reset patterns to run
3-0	SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run

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6.359 CTRLMMR_DSP0_LBIST_SEED0 Register (Proxy0 Offset = C088h; Proxy1 Offset = E088h) [reset = 0h]

CTRLMMR_DSP0_LBIST_SEED0 is shown in Figure 6-359 and described in Table 6-720.

Return to Summary Table.

Specifies the 32 LSBs of the PRPG seed.

Table 6-719. CTRLMMR_DSP0_LBIST_SEED0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C088h	0010 E088h

Figure 6-359. CTRLMMR_DSP0_LBIST_SEED0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRPG_DEF																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-720. CTRLMMR_DSP0_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0)

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6.360 CTRLMMR_DSP0_LBIST_SEED1 Register (Proxy0 Offset = C08Ch; Proxy1 Offset = E08Ch) [reset = 0h]

CTRLMMR_DSP0_LBIST_SEED1 is shown in Figure 6-360 and described in Table 6-722.

Return to Summary Table.

Specifies the 21 MSBs of the PRPG seed.

Table 6-721. CTRLMMR_DSP0_LBIST_SEED1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C08Ch	0010 E08Ch

Figure 6-360. CTRLMMR_DSP0_LBIST_SEED1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRPG_DEF																				
R-0h											R/W-0h																				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-722. CTRLMMR_DSP0_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32)

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6.361 CTRLMMR_DSP0_LBIST_SPARE0 Register (Proxy0 Offset = C090h; Proxy1 Offset = E090h) [reset = 0h]

CTRLMMR_DSP0_LBIST_SPARE0 is shown in Figure 6-361 and described in Table 6-724.

Return to Summary Table.

Spare LBIST control bits.

Table 6-723. CTRLMMR_DSP0_LBIST_SPARE0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C090h	0010 E090h

Figure 6-361. CTRLMMR_DSP0_LBIST_SPARE0 Register

31	30	29	28	27	26	25	24
SPARE0							
R/W-0h							
23	22	21	20	19	18	17	16
SPARE0							
R/W-0h							
15	14	13	12	11	10	9	8
SPARE0							
R/W-0h							
7	6	5	4	3	2	1	0
SPARE0						PBIST_SELFTEST_EN	LBIST_SELFTEST_EN
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-724. CTRLMMR_DSP0_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	SPARE0	R/W	0h	LBIST spare bits
1	PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control
0	LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control

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6.362 CTRLMMR_DSP0_LBIST_SPARE1 Register (Proxy0 Offset = C094h; Proxy1 Offset = E094h) [reset = 0h]

CTRLMMR_DSP0_LBIST_SPARE1 is shown in Figure 6-362 and described in Table 6-726.

Return to Summary Table.

Spare LBIST control bits.

Table 6-725. CTRLMMR_DSP0_LBIST_SPARE1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C094h	0010 E094h

Figure 6-362. CTRLMMR_DSP0_LBIST_SPARE1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-726. CTRLMMR_DSP0_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE1	R/W	0h	LBIST spare bits

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6.363 CTRLMMR_DSP0_LBIST_STAT Register (Proxy0 Offset = C098h; Proxy1 Offset = E098h) [reset = X]

CTRLMMR_DSP0_LBIST_STAT is shown in Figure 6-363 and described in Table 6-728.

Return to Summary Table.

Indicates LBIST status and provides MISR selection control.

Table 6-727. CTRLMMR_DSP0_LBIST_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C098h	0010 E098h

Figure 6-363. CTRLMMR_DSP0_LBIST_STAT Register

31	30	29	28	27	26	25	24
BIST_DONE	RESERVED						
R-X	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
BIST_RUNNING	RESERVED					OUT_MUX_CTL	
R-X	R-0h					R/W-0h	

7	6	5	4	3	2	1	0
MISR_MUX_CTL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-728. CTRLMMR_DSP0_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_DONE	R	X	LBIST is done
30-16	RESERVED	R	0h	Reserved
15	BIST_RUNNING	R	X	LBIST is running
14-10	RESERVED	R	0h	Reserved
9-8	OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 0h - LBIST IP CTRLMMR_PID value 1h - LBIST CTRL ID value 1x - MISR value
7-0	MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR.

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6.364 CTRLMMR_DSP0_LBIST_MISR Register (Proxy0 Offset = C09Ch; Proxy1 Offset = E09Ch) [reset = X]

CTRLMMR_DSP0_LBIST_MISR is shown in Figure 6-364 and described in Table 6-730.

Return to Summary Table.

Contains LBIST MISR output value.

Table 6-729. CTRLMMR_DSP0_LBIST_MISR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C09Ch	0010 E09Ch

Figure 6-364. CTRLMMR_DSP0_LBIST_MISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_RESULT																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-730. CTRLMMR_DSP0_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl

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6.365 CTRLMMR_MPU0_LBIST_CTRL Register (Proxy0 Offset = C100h; Proxy1 Offset = E100h) [reset = 0h]

CTRLMMR_MPU0_LBIST_CTRL is shown in Figure 6-365 and described in Table 6-732.

Return to Summary Table.

Configures and enables LBIST operation.

Table 6-731. CTRLMMR_MPU0_LBIST_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C100h	0010 E100h

Figure 6-365. CTRLMMR_MPU0_LBIST_CTRL Register

31	30	29	28	27	26	25	24
BIST_RESET	RESERVED			BIST_RUN			
R/W-0h	R-0h			R/W-0h			
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R-0h							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RUNBIST_MODE				RESERVED		DC_DEF	
R/W-0h				R-0h		R/W-0h	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LOAD_DIV	RESERVED		DIVIDE_RATIO				
R/W-0h	R-0h		R/W-0h				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-732. CTRLMMR_MPU0_LBIST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_RESET	R/W	0h	Reset LBIST macro
30-28	RESERVED	R	0h	Reserved
27-24	BIST_RUN	R/W	0h	Starts LBIST if all bits are 1
23-16	RESERVED	R	0h	Reserved
15-12	RUNBIST_MODE	R/W	0h	Runbist mode enable if all bits are 1
11-10	RESERVED	R	0h	Reserved
9-8	DC_DEF	R/W	0h	Clock delay after scan_enable switching
7	LOAD_DIV	R/W	0h	Loads LBIST clock divide ratio on transition from 0 to 1
6-5	RESERVED	R	0h	Reserved
4-0	DIVIDE_RATIO	R/W	0h	LBIST clock divide ratio

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6.366 CTRLMMR_MPU0_LBIST_PATCOUNT Register (Proxy0 Offset = C104h; Proxy1 Offset = E104h) [reset = 0h]

CTRLMMR_MPU0_LBIST_PATCOUNT is shown in Figure 6-366 and described in Table 6-734.

Return to Summary Table.

Specifies the number of LBIST patterns to run.

Table 6-733. CTRLMMR_MPU0_LBIST_PATCOUNT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C104h	0010 E104h

Figure 6-366. CTRLMMR_MPU0_LBIST_PATCOUNT Register

31	30	29	28	27	26	25	24
RESERVED		STATIC_PC_DEF					
R-0h		R/W-0h					
23	22	21	20	19	18	17	16
STATIC_PC_DEF							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED				SET_PC_DEF			
R-0h				R/W-0h			
7	6	5	4	3	2	1	0
RESET_PC_DEF				SCAN_PC_DEF			
R/W-0h				R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-734. CTRLMMR_MPU0_LBIST_PATCOUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	RESERVED	R	0h	Reserved
29-16	STATIC_PC_DEF	R/W	0h	Number of stuck-at patterns to run
15-12	RESERVED	R	0h	Reserved
11-8	SET_PC_DEF	R/W	0h	Number of set patterns to run
7-4	RESET_PC_DEF	R/W	0h	Number of reset patterns to run
3-0	SCAN_PC_DEF	R/W	0h	Number of chain test patterns to run

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6.367 CTRLMMR_MPU0_LBIST_SEED0 Register (Proxy0 Offset = C108h; Proxy1 Offset = E108h) [reset = 0h]

CTRLMMR_MPU0_LBIST_SEED0 is shown in Figure 6-367 and described in Table 6-736.

Return to Summary Table.

Specifies the 32 LSBs of the PRPG seed.

Table 6-735. CTRLMMR_MPU0_LBIST_SEED0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C108h	0010 E108h

Figure 6-367. CTRLMMR_MPU0_LBIST_SEED0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRPG_DEF																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-736. CTRLMMR_MPU0_LBIST_SEED0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 31:0)

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6.368 CTRLMMR_MPU0_LBIST_SEED1 Register (Proxy0 Offset = C10Ch; Proxy1 Offset = E10Ch) [reset = 0h]

CTRLMMR_MPU0_LBIST_SEED1 is shown in Figure 6-368 and described in Table 6-738.

Return to Summary Table.

Specifies the 21 MSBs of the PRPG seed.

Table 6-737. CTRLMMR_MPU0_LBIST_SEED1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C10Ch	0010 E10Ch

Figure 6-368. CTRLMMR_MPU0_LBIST_SEED1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											PRPG_DEF																				
R-0h											R/W-0h																				

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-738. CTRLMMR_MPU0_LBIST_SEED1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-0	PRPG_DEF	R/W	0h	Initial seed for PRPG (bits 52:32)

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6.369 CTRLMMR_MPU0_LBIST_SPARE0 Register (Proxy0 Offset = C110h; Proxy1 Offset = E110h) [reset = 0h]

CTRLMMR_MPU0_LBIST_SPARE0 is shown in Figure 6-369 and described in Table 6-740.

Return to Summary Table.

Spare LBIST control bits.

Table 6-739. CTRLMMR_MPU0_LBIST_SPARE0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C110h	0010 E110h

Figure 6-369. CTRLMMR_MPU0_LBIST_SPARE0 Register

31	30	29	28	27	26	25	24
SPARE0							
R/W-0h							
23	22	21	20	19	18	17	16
SPARE0							
R/W-0h							
15	14	13	12	11	10	9	8
SPARE0							
R/W-0h							
7	6	5	4	3	2	1	0
SPARE0						PBIST_SELFTEST_EN	LBIST_SELFTEST_EN
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-740. CTRLMMR_MPU0_LBIST_SPARE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	SPARE0	R/W	0h	LBIST spare bits
1	PBIST_SELFTEST_EN	R/W	0h	PBIST isolation control
0	LBIST_SELFTEST_EN	R/W	0h	LBIST isolation control

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6.370 CTRLMMR_MPU0_LBIST_SPARE1 Register (Proxy0 Offset = C114h; Proxy1 Offset = E114h) [reset = 0h]

CTRLMMR_MPU0_LBIST_SPARE1 is shown in Figure 6-370 and described in Table 6-742.

Return to Summary Table.

Spare LBIST control bits.

Table 6-741. CTRLMMR_MPU0_LBIST_SPARE1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C114h	0010 E114h

Figure 6-370. CTRLMMR_MPU0_LBIST_SPARE1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPARE1																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-742. CTRLMMR_MPU0_LBIST_SPARE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPARE1	R/W	0h	LBIST spare bits

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6.371 CTRLMMR_MPU0_LBIST_STAT Register (Proxy0 Offset = C118h; Proxy1 Offset = E118h) [reset = X]

CTRLMMR_MPU0_LBIST_STAT is shown in Figure 6-371 and described in Table 6-744.

Return to Summary Table.

Indicates LBIST status and provides MISR selection control.

Table 6-743. CTRLMMR_MPU0_LBIST_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C118h	0010 E118h

Figure 6-371. CTRLMMR_MPU0_LBIST_STAT Register

31	30	29	28	27	26	25	24
BIST_DONE	RESERVED						
R-X	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
BIST_RUNNING	RESERVED					OUT_MUX_CTL	
R-X	R-0h					R/W-0h	

7	6	5	4	3	2	1	0
MISR_MUX_CTL							
R/W-0h							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-744. CTRLMMR_MPU0_LBIST_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BIST_DONE	R	X	LBIST is done
30-16	RESERVED	R	0h	Reserved
15	BIST_RUNNING	R	X	LBIST is running
14-10	RESERVED	R	0h	Reserved
9-8	OUT_MUX_CTL	R/W	0h	Selects source of LBIST output 0h - LBIST IP CTRLMMR_PID value 1h - LBIST CTRL ID value 1x - MISR value
7-0	MISR_MUX_CTL	R/W	0h	Selects block of 32 MISR bits to read. A value of 0 selects a compacted 32-bit version of the full MISR. A value of 1-32 select a 32-bit segment of the MISR.

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6.372 CTRLMMR_MPU0_LBIST_MISR Register (Proxy0 Offset = C11Ch; Proxy1 Offset = E11Ch) [reset = X]

CTRLMMR_MPU0_LBIST_MISR is shown in Figure 6-372 and described in Table 6-746.

Return to Summary Table.

Contains LBIST MISR output value.

Table 6-745. CTRLMMR_MPU0_LBIST_MISR Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C11Ch	0010 E11Ch

Figure 6-372. CTRLMMR_MPU0_LBIST_MISR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_RESULT																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-746. CTRLMMR_MPU0_LBIST_MISR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_RESULT	R	X	32-bits of MISR value selected by misr_mux_ctl

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6.373 CTRLMMR_MCU0_LBIST_SIG Register (Proxy0 Offset = C280h; Proxy1 Offset = E280h) [reset = X]

CTRLMMR_MCU0_LBIST_SIG is shown in Figure 6-373 and described in Table 6-748.

Return to Summary Table.

Contains expected MISR output value.

Table 6-747. CTRLMMR_MCU0_LBIST_SIG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C280h	0010 E280h

Figure 6-373. CTRLMMR_MCU0_LBIST_SIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_SIG																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-748. CTRLMMR_MCU0_LBIST_SIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_SIG	R	X	MISR signature

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6.374 CTRLMMR_MCU1_LBIST_SIG Register (Proxy0 Offset = C284h; Proxy1 Offset = E284h) [reset = X]

CTRLMMR_MCU1_LBIST_SIG is shown in Figure 6-374 and described in Table 6-750.

Return to Summary Table.

Contains expected MISR output value.

Table 6-749. CTRLMMR_MCU1_LBIST_SIG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C284h	0010 E284h

Figure 6-374. CTRLMMR_MCU1_LBIST_SIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_SIG																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-750. CTRLMMR_MCU1_LBIST_SIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_SIG	R	X	MISR signature

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6.375 CTRLMMR_DMPAC_LBIST_SIG Register (Proxy0 Offset = C288h; Proxy1 Offset = E288h) [reset = X]

CTRLMMR_DMPAC_LBIST_SIG is shown in Figure 6-375 and described in Table 6-752.

Return to Summary Table.

Contains expected MISR output value.

Table 6-751. CTRLMMR_DMPAC_LBIST_SIG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C288h	0010 E288h

Figure 6-375. CTRLMMR_DMPAC_LBIST_SIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_SIG																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-752. CTRLMMR_DMPAC_LBIST_SIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_SIG	R	X	MISR signature

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6.376 CTRLMMR_VPAC_LBIST_SIG Register (Proxy0 Offset = C28Ch; Proxy1 Offset = E28Ch) [reset = X]

CTRLMMR_VPAC_LBIST_SIG is shown in Figure 6-376 and described in Table 6-754.

Return to Summary Table.

Contains expected MISR output value.

Table 6-753. CTRLMMR_VPAC_LBIST_SIG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C28Ch	0010 E28Ch

Figure 6-376. CTRLMMR_VPAC_LBIST_SIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_SIG																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-754. CTRLMMR_VPAC_LBIST_SIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_SIG	R	X	MISR signature

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6.377 CTRLMMR_DSP0_LBIST_SIG Register (Proxy0 Offset = C290h; Proxy1 Offset = E290h) [reset = X]

CTRLMMR_DSP0_LBIST_SIG is shown in Figure 6-377 and described in Table 6-756.

Return to Summary Table.

Contains expected MISR output value.

Table 6-755. CTRLMMR_DSP0_LBIST_SIG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C290h	0010 E290h

Figure 6-377. CTRLMMR_DSP0_LBIST_SIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_SIG																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-756. CTRLMMR_DSP0_LBIST_SIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_SIG	R	X	MISR signature

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6.378 CTRLMMR_MPU0_LBIST_SIG Register (Proxy0 Offset = C2A0h; Proxy1 Offset = E2A0h) [reset = X]

CTRLMMR_MPU0_LBIST_SIG is shown in Figure 6-378 and described in Table 6-758.

Return to Summary Table.

Contains expected MISR output value.

Table 6-757. CTRLMMR_MPU0_LBIST_SIG Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C2A0h	0010 E2A0h

Figure 6-378. CTRLMMR_MPU0_LBIST_SIG Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISR_SIG																															
R-X																															

LEGEND: R = Read Only; *-n* = value after reset

Table 6-758. CTRLMMR_MPU0_LBIST_SIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	MISR_SIG	R	X	MISR signature

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6.379 CTRLMMR_FUSE_CRC_STAT Register (Proxy0 Offset = C320h; Proxy1 Offset = E320h) [reset = X]

CTRLMMR_FUSE_CRC_STAT is shown in Figure 6-379 and described in Table 6-760.

Return to Summary Table.

Indicates status of fuse chain CRC.

Table 6-759. CTRLMMR_FUSE_CRC_STAT Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 C320h	0010 E320h

Figure 6-379. CTRLMMR_FUSE_CRC_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
GRP1_CRC_ERR_7	GRP1_CRC_ERR_6	GRP1_CRC_ERR_5	GRP1_CRC_ERR_4	GRP1_CRC_ERR_3	GRP1_CRC_ERR_2	GRP1_CRC_ERR_1	GRP1_CRC_ERR_0
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X
7	6	5	4	3	2	1	0
CRC_ERR_7	CRC_ERR_6	CRC_ERR_5	CRC_ERR_4	CRC_ERR_3	CRC_ERR_2	CRC_ERR_1	RESERVED
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 6-760. CTRLMMR_FUSE_CRC_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	GRP1_CRC_ERR_7	R	X	Indicates eFuse CRC error on group1 chain 7
14	GRP1_CRC_ERR_6	R	X	Indicates eFuse CRC error on group1 chain 6
13	GRP1_CRC_ERR_5	R	X	Indicates eFuse CRC error on group1 chain 5
12	GRP1_CRC_ERR_4	R	X	Indicates eFuse CRC error on group1 chain 4
11	GRP1_CRC_ERR_3	R	X	Indicates eFuse CRC error on group1 chain 3
10	GRP1_CRC_ERR_2	R	X	Indicates eFuse CRC error on group1 chain 2
9	GRP1_CRC_ERR_1	R	X	Indicates eFuse CRC error on group1 chain 1
8	GRP1_CRC_ERR_0	R	X	Indicates eFuse CRC error on group1 chain 0
7	CRC_ERR_7	R	X	Indicates eFuse CRC error on chain 7
6	CRC_ERR_6	R	X	Indicates eFuse CRC error on chain 6
5	CRC_ERR_5	R	X	Indicates eFuse CRC error on chain 5
4	CRC_ERR_4	R	X	Indicates eFuse CRC error on chain 4
3	CRC_ERR_3	R	X	Indicates eFuse CRC error on chain 3
2	CRC_ERR_2	R	X	Indicates eFuse CRC error on chain 2
1	CRC_ERR_1	R	X	Indicates eFuse CRC error on chain 1
0	RESERVED	R	0h	Reserved

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6.380 CTRLMMR_LOCK3_KICK0 Register (Proxy0 Offset = D008h; Proxy1 Offset = F008h) [reset = 0h]

CTRLMMR_LOCK3_KICK0 is shown in Figure 6-380 and described in Table 6-762.

Return to Summary Table.

Lower 32-bits of Partition3 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_LOCK3_KICK1 with its key value before write-protected Partition 3 registers can be written.

Table 6-761. CTRLMMR_LOCK3_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 D008h	0010 F008h

Figure 6-380. CTRLMMR_LOCK3_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-762. CTRLMMR_LOCK3_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition3 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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6.381 CTRLMMR_LOCK3_KICK1 Register (Proxy0 Offset = D00Ch; Proxy1 Offset = F00Ch) [reset = 0h]

CTRLMMR_LOCK3_KICK1 is shown in Figure 6-381 and described in Table 6-764.

Return to Summary Table.

Upper 32-bits of Partition 3 write lock key. This register must be written with the designated key value after a write to CTRLMMR_LOCK3_KICK0 with its key value before write-protected Partition 3 registers can be written.

Table 6-763. CTRLMMR_LOCK3_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 D00Ch	0010 F00Ch

Figure 6-381. CTRLMMR_LOCK3_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-764. CTRLMMR_LOCK3_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition3 registers

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6.382 CTRLMMR_P3_CLAIM0 Register (Proxy0 Offset = D100h; Proxy1 Offset = F100h) [reset = 0h]

CTRLMMR_P3_CLAIM0 is shown in Figure 6-382 and described in Table 6-766.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 6-765. CTRLMMR_P3_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 D100h	0010 F100h

Figure 6-382. CTRLMMR_P3_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-766. CTRLMMR_P3_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0xC000 + (0 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xE000 + (0 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.383 CTRLMMR_P3_CLAIM1 Register (Proxy0 Offset = D104h; Proxy1 Offset = F104h) [reset = 0h]

CTRLMMR_P3_CLAIM1 is shown in Figure 6-383 and described in Table 6-768.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 6-767. CTRLMMR_P3_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 D104h	0010 F104h

Figure 6-383. CTRLMMR_P3_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-768. CTRLMMR_P3_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0xC000 + (1 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xE000 + (1 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.384 CTRLMMR_P3_CLAIM2 Register (Proxy0 Offset = D108h; Proxy1 Offset = F108h) [reset = 0h]

CTRLMMR_P3_CLAIM2 is shown in Figure 6-384 and described in Table 6-770.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 6-769. CTRLMMR_P3_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 D108h	0010 F108h

Figure 6-384. CTRLMMR_P3_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-770. CTRLMMR_P3_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0xC000 + (2 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xE000 + (2 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.385 CTRLMMR_P3_CLAIM3 Register (Proxy0 Offset = D10Ch; Proxy1 Offset = F10Ch) [reset = 0h]

CTRLMMR_P3_CLAIM3 is shown in Figure 6-385 and described in Table 6-772.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 6-771. CTRLMMR_P3_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 D10Ch	0010 F10Ch

Figure 6-385. CTRLMMR_P3_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-772. CTRLMMR_P3_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0xC000 + (3 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xE000 + (3 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.386 CTRLMMR_P3_CLAIM4 Register (Proxy0 Offset = D110h; Proxy1 Offset = F110h) [reset = 0h]

CTRLMMR_P3_CLAIM4 is shown in Figure 6-386 and described in Table 6-774.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 6-773. CTRLMMR_P3_CLAIM4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 D110h	0010 F110h

Figure 6-386. CTRLMMR_P3_CLAIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-774. CTRLMMR_P3_CLAIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0xC000 + (4 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xE000 + (4 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.387 CTRLMMR_P3_CLAIM5 Register (Proxy0 Offset = D114h; Proxy1 Offset = F114h) [reset = 0h]

CTRLMMR_P3_CLAIM5 is shown in Figure 6-387 and described in Table 6-776.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 6-775. CTRLMMR_P3_CLAIM5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 D114h	0010 F114h

Figure 6-387. CTRLMMR_P3_CLAIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-776. CTRLMMR_P3_CLAIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0xC000 + (5 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xE000 + (5 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.388 CTRLMMR_P3_CLAIM6 Register (Proxy0 Offset = D118h; Proxy1 Offset = F118h) [reset = 0h]

CTRLMMR_P3_CLAIM6 is shown in Figure 6-388 and described in Table 6-778.

Return to Summary Table.

Claim bits for Partition3 Registers.

Table 6-777. CTRLMMR_P3_CLAIM6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0010 D118h	0010 F118h

Figure 6-388. CTRLMMR_P3_CLAIM6 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-778. CTRLMMR_P3_CLAIM6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0xC000 + (6 x 0x80) + (b x 0x4) and register Proxy1 address of: 0xE000 + (6 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.389 CTRLMMR_CHNG_DDR4_FSP_REQ Register (Proxy0 Offset = 14000h; Proxy1 Offset = 16000h) [reset = 0h]

CTRLMMR_CHNG_DDR4_FSP_REQ is shown in Figure 6-389 and described in Table 6-780.

Return to Summary Table.

This register is used to initiate a LPDDR4 frequency set point change to the DDR Controller.

Table 6-779. CTRLMMR_CHNG_DDR4_FSP_REQ Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 4000h	0011 6000h

Figure 6-389. CTRLMMR_CHNG_DDR4_FSP_REQ Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							REQ
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						REQ_TYPE	
R-0h						R/W-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-780. CTRLMMR_CHNG_DDR4_FSP_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-9	RESERVED	R	0h	Reserved
8	REQ	R/W	0h	Initiate FSP frequency change
7-2	RESERVED	R	0h	Reserved
1-0	REQ_TYPE	R/W	0h	Frequency request type Frequency request type which indicates which DDR4 frequency to select in the set point table in the SDRAM

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6.390 CTRLMMR_CHNG_DDR4_FSP_ACK Register (Proxy0 Offset = 14004h; Proxy1 Offset = 16004h) [reset = X]

CTRLMMR_CHNG_DDR4_FSP_ACK is shown in Figure 6-390 and described in Table 6-782.

Return to Summary Table.

This register is used by the DDR Controller to acknowledge the LPDDR4 frequency set point shange request.

Table 6-781. CTRLMMR_CHNG_DDR4_FSP_ACK Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 4004h	0011 6004h

Figure 6-390. CTRLMMR_CHNG_DDR4_FSP_ACK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
ACK	RESERVED						ERROR
R-X	R-0h						R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 6-782. CTRLMMR_CHNG_DDR4_FSP_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	ACK	R	X	Frequency change acknowledge. This bit is only valid when CHNG_DDR4_FSP_REQ_req = 1 Indication from the DDR Controller that the FSP change operation is complete 0h - FSP change operation in progress 1h - FSP change operation complete
6-1	RESERVED	R	0h	Reserved
0	ERROR	R	X	Frequency change error This bit is only valid when CHNG_DDR4_FSP_REQ_req = 1 0h - FSP change was sucessful 1h - FSP change was not sucessful

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6.391 CTRLMMR_DDR4_FSP_CLKCHNG_REQ Register (Proxy0 Offset = 14080h; Proxy1 Offset = 16080h) [reset = X]

CTRLMMR_DDR4_FSP_CLKCHNG_REQ is shown in Figure 6-391 and described in Table 6-784.

Return to Summary Table.

This register is used by the DDR Controller to request the DDR PLL clock frequency change. This can occur as part of DDR4 initialization and training or in response to a LPDDR4 FSP change request.

Table 6-783. CTRLMMR_DDR4_FSP_CLKCHNG_REQ Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 4080h	0011 6080h

Figure 6-391. CTRLMMR_DDR4_FSP_CLKCHNG_REQ Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
REQ	RESERVED					REQ_TYPE	
R-X	R-0h					R-X	

LEGEND: R = Read Only; *-n* = value after reset

Table 6-784. CTRLMMR_DDR4_FSP_CLKCHNG_REQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	REQ	R	X	DDR Controller FSP clock change request Indicates that the DDR controller needs the DDR clock changed to the frequency indicated by the req_type field. This bit is cleared when the DDR4_FSP_CLKCHNG_ACK_ack bit is set.
6-2	RESERVED	R	0h	Reserved
1-0	REQ_TYPE	R	X	Frequency request type Indicates which LPDDR4 FSP (frequency set point) to which the DDR Controller wants the DDR clock set

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6.392 CTRLMMR_DDR4_FSP_CLKCHNG_ACK Register (Proxy0 Offset = 140C0h; Proxy1 Offset = 160C0h) [reset = 0h]

CTRLMMR_DDR4_FSP_CLKCHNG_ACK is shown in Figure 6-392 and described in Table 6-786.

Return to Summary Table.

This register is used to acknowledge a DDR PLL clock frequency change to the DDR Controller.

Table 6-785. CTRLMMR_DDR4_FSP_CLKCHNG_ACK Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 40C0h	0011 60C0h

Figure 6-392. CTRLMMR_DDR4_FSP_CLKCHNG_ACK Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							ACK
R-0h							R/W-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-786. CTRLMMR_DDR4_FSP_CLKCHNG_ACK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	ACK	R/W	0h	DDR FSP clock change ackowledge This bit should be set once the DDR clock has been sucessfully changed to the value requested by DDR4_FSP_CLKCHNG_REQ_req_type. Setting this bit will clear the DDR4_FSP_CLKCHNG_REQ_req bit and the associated change request interrupt.

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6.393 CTRLMMR_LOCK5_KICK0 Register (Proxy0 Offset = 15008h; Proxy1 Offset = 17008h) [reset = 0h]

CTRLMMR_LOCK5_KICK0 is shown in Figure 6-393 and described in Table 6-788.

Return to Summary Table.

Lower 32-bits of Partition5 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_LOCK5_KICK1 with its key value before write-protected Partition 5 registers can be written.

Table 6-787. CTRLMMR_LOCK5_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 5008h	0011 7008h

Figure 6-393. CTRLMMR_LOCK5_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-788. CTRLMMR_LOCK5_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition5 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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6.394 CTRLMMR_LOCK5_KICK1 Register (Proxy0 Offset = 1500Ch; Proxy1 Offset = 1700Ch) [reset = 0h]

CTRLMMR_LOCK5_KICK1 is shown in Figure 6-394 and described in Table 6-790.

Return to Summary Table.

Upper 32-bits of Partition 5 write lock key. This register must be written with the designated key value after a write to CTRLMMR_LOCK5_KICK0 with its key value before write-protected Partition 5 registers can be written.

Table 6-789. CTRLMMR_LOCK5_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 500Ch	0011 700Ch

Figure 6-394. CTRLMMR_LOCK5_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-790. CTRLMMR_LOCK5_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition5 registers

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6.395 CTRLMMR_P5_CLAIM0 Register (Proxy0 Offset = 15100h; Proxy1 Offset = 17100h) [reset = 0h]

CTRLMMR_P5_CLAIM0 is shown in Figure 6-395 and described in Table 6-792.

Return to Summary Table.

Claim bits for Partition5 Registers.

Table 6-791. CTRLMMR_P5_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 5100h	0011 7100h

Figure 6-395. CTRLMMR_P5_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-792. CTRLMMR_P5_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x14000 + (0 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x16000 + (0 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.396 CTRLMMR_P5_CLAIM1 Register (Proxy0 Offset = 15104h; Proxy1 Offset = 17104h) [reset = 0h]

CTRLMMR_P5_CLAIM1 is shown in Figure 6-396 and described in Table 6-794.

Return to Summary Table.

Claim bits for Partition5 Registers.

Table 6-793. CTRLMMR_P5_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 5104h	0011 7104h

Figure 6-396. CTRLMMR_P5_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-794. CTRLMMR_P5_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x14000 + (1 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x16000 + (1 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.397 CTRLMMR_ACSPCIE0_CTRL Register (Proxy0 Offset = 18090h; Proxy1 Offset = 1A090h) [reset = X]

CTRLMMR_ACSPCIE0_CTRL is shown in Figure 6-397 and described in Table 6-796.

Return to Summary Table.

Controls the ACSPCIE0 module.

Table 6-795. CTRLMMR_ACSPCIE0_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 8090h	0011 A090h

Figure 6-397. CTRLMMR_ACSPCIE0_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							BANDGAP_OK
R-0h							R-X
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							AIPOFF
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PWRDN1	PWRDN0
R-0h						R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-796. CTRLMMR_ACSPCIE0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	BANDGAP_OK	R	X	Bandgap output okay
23-9	RESERVED	R	0h	Reserved
8	AIPOFF	R/W	0h	Testmode enable
7-2	RESERVED	R	0h	Reserved
1	PWRDN1	R/W	1h	Disable (tristate) PAD1 IO buffers
0	PWRDN0	R/W	1h	Disable (tristate) PAD0 IO buffers

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6.398 CTRLMMR_ACSPCIE1_CTRL Register (Proxy0 Offset = 18094h; Proxy1 Offset = 1A094h) [reset = X]

CTRLMMR_ACSPCIE1_CTRL is shown in Figure 6-398 and described in Table 6-798.

Return to Summary Table.

Controls the ACSPCIE1 module.

Table 6-797. CTRLMMR_ACSPCIE1_CTRL Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 8094h	0011 A094h

Figure 6-398. CTRLMMR_ACSPCIE1_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							BANDGAP_OK
R-0h							R-X
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							AIPOFF
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PWRDN1	PWRDN0
R-0h						R/W-1h	R/W-1h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-798. CTRLMMR_ACSPCIE1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R	0h	Reserved
24	BANDGAP_OK	R	X	Bandgap output okay when set
23-9	RESERVED	R	0h	Reserved
8	AIPOFF	R/W	0h	Testmode enable when set
7-2	RESERVED	R	0h	Reserved
1	PWRDN1	R/W	1h	Disable (tristate) PAD1 IO buffers when set
0	PWRDN0	R/W	1h	Disable (tristate) PAD0 IO buffers when set

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6.399 CTRLMMR_LOCK6_KICK0 Register (Proxy0 Offset = 19008h; Proxy1 Offset = 1B008h) [reset = 0h]

CTRLMMR_LOCK6_KICK0 is shown in Figure 6-399 and described in Table 6-800.

Return to Summary Table.

Lower 32-bits of Partition6 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_LOCK6_KICK1 with its key value before write-protected Partition 6 registers can be written.

Table 6-799. CTRLMMR_LOCK6_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 9008h	0011 B008h

Figure 6-399. CTRLMMR_LOCK6_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-800. CTRLMMR_LOCK6_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition6 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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6.400 CTRLMMR_LOCK6_KICK1 Register (Proxy0 Offset = 1900Ch; Proxy1 Offset = 1B00Ch) [reset = 0h]

CTRLMMR_LOCK6_KICK1 is shown in Figure 6-400 and described in Table 6-802.

Return to Summary Table.

Upper 32-bits of Partition 6 write lock key. This register must be written with the designated key value after a write to CTRLMMR_LOCK6_KICK0 with its key value before write-protected Partition 6 registers can be written.

Table 6-801. CTRLMMR_LOCK6_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 900Ch	0011 B00Ch

Figure 6-400. CTRLMMR_LOCK6_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-802. CTRLMMR_LOCK6_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition6 registers

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6.401 CTRLMMR_P6_CLAIM0 Register (Proxy0 Offset = 19100h; Proxy1 Offset = 1B100h) [reset = 0h]

CTRLMMR_P6_CLAIM0 is shown in Figure 6-401 and described in Table 6-804.

Return to Summary Table.

Claim bits for Partition6 Registers.

Table 6-803. CTRLMMR_P6_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 9100h	0011 B100h

Figure 6-401. CTRLMMR_P6_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-804. CTRLMMR_P6_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x18000 + (0 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x1A000 + (0 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.402 CTRLMMR_P6_CLAIM1 Register (Proxy0 Offset = 19104h; Proxy1 Offset = 1B104h) [reset = 0h]

CTRLMMR_P6_CLAIM1 is shown in Figure 6-402 and described in Table 6-806.

Return to Summary Table.

Claim bits for Partition6 Registers.

Table 6-805. CTRLMMR_P6_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 9104h	0011 B104h

Figure 6-402. CTRLMMR_P6_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-806. CTRLMMR_P6_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x18000 + (1 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x1A000 + (1 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.403 CTRLMMR_PADCONFIG0 Register (Proxy0 Offset = 1C000h; Proxy1 Offset = 1E000h) [reset = 4007h]

CTRLMMR_PADCONFIG0 is shown in Figure 6-403 and described in Table 6-808.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-807. CTRLMMR_PADCONFIG0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C000h	0011 E000h

Figure 6-403. CTRLMMR_PADCONFIG0 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	RESERVED		DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h	R-0h	

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-808. CTRLMMR_PADCONFIG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28-27	RESERVED	R	0h	Reserved
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active

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Table 6-808. CTRLMMR_PADCONFIG0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17-16	RESERVED	R	0h	Reserved
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.404 CTRLMMR_PADCONFIG1 Register (Proxy0 Offset = 1C004h; Proxy1 Offset = 1E004h) [reset = 8214007h]

CTRLMMR_PADCONFIG1 is shown in Figure 6-404 and described in Table 6-810.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-809. CTRLMMR_PADCONFIG1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C004h	0011 E004h

Figure 6-404. CTRLMMR_PADCONFIG1 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-810. CTRLMMR_PADCONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-810. CTRLMMR_PADCONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-810. CTRLMMR_PADCONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.405 CTRLMMR_PADCONFIG2 Register (Proxy0 Offset = 1C008h; Proxy1 Offset = 1E008h) [reset = 8214007h]

CTRLMMR_PADCONFIG2 is shown in Figure 6-405 and described in Table 6-812.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-811. CTRLMMR_PADCONFIG2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C008h	0011 E008h

Figure 6-405. CTRLMMR_PADCONFIG2 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-812. CTRLMMR_PADCONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-812. CTRLMMR_PADCONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-812. CTRLMMR_PADCONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.406 CTRLMMR_PADCONFIG3 Register (Proxy0 Offset = 1C00Ch; Proxy1 Offset = 1E00Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG3 is shown in Figure 6-406 and described in Table 6-814.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-813. CTRLMMR_PADCONFIG3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C00Ch	0011 E00Ch

Figure 6-406. CTRLMMR_PADCONFIG3 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-814. CTRLMMR_PADCONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-814. CTRLMMR_PADCONFIG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-814. CTRLMMR_PADCONFIG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.407 CTRLMMR_PADCONFIG4 Register (Proxy0 Offset = 1C010h; Proxy1 Offset = 1E010h) [reset = 8214007h]

CTRLMMR_PADCONFIG4 is shown in Figure 6-407 and described in Table 6-816.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-815. CTRLMMR_PADCONFIG4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C010h	0011 E010h

Figure 6-407. CTRLMMR_PADCONFIG4 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-816. CTRLMMR_PADCONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-816. CTRLMMR_PADCONFIG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-816. CTRLMMR_PADCONFIG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.408 CTRLMMR_PADCONFIG5 Register (Proxy0 Offset = 1C014h; Proxy1 Offset = 1E014h) [reset = 8214007h]

CTRLMMR_PADCONFIG5 is shown in Figure 6-408 and described in Table 6-818.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-817. CTRLMMR_PADCONFIG5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C014h	0011 E014h

Figure 6-408. CTRLMMR_PADCONFIG5 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-818. CTRLMMR_PADCONFIG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-818. CTRLMMR_PADCONFIG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-818. CTRLMMR_PADCONFIG5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.409 CTRLMMR_PADCONFIG6 Register (Proxy0 Offset = 1C018h; Proxy1 Offset = 1E018h) [reset = 8254007h]

CTRLMMR_PADCONFIG6 is shown in Figure 6-409 and described in Table 6-820.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-819. CTRLMMR_PADCONFIG6 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C018h	0011 E018h

Figure 6-409. CTRLMMR_PADCONFIG6 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-820. CTRLMMR_PADCONFIG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-820. CTRLMMR_PADCONFIG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-820. CTRLMMR_PADCONFIG6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.410 CTRLMMR_PADCONFIG7 Register (Proxy0 Offset = 1C01Ch; Proxy1 Offset = 1E01Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG7 is shown in Figure 6-410 and described in Table 6-822.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-821. CTRLMMR_PADCONFIG7 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C01Ch	0011 E01Ch

Figure 6-410. CTRLMMR_PADCONFIG7 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-822. CTRLMMR_PADCONFIG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-822. CTRLMMR_PADCONFIG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-822. CTRLMMR_PADCONFIG7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.411 CTRLMMR_PADCONFIG8 Register (Proxy0 Offset = 1C020h; Proxy1 Offset = 1E020h) [reset = 8214007h]

CTRLMMR_PADCONFIG8 is shown in Figure 6-411 and described in Table 6-824.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-823. CTRLMMR_PADCONFIG8 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C020h	0011 E020h

Figure 6-411. CTRLMMR_PADCONFIG8 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-824. CTRLMMR_PADCONFIG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-824. CTRLMMR_PADCONFIG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-824. CTRLMMR_PADCONFIG8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.412 CTRLMMR_PADCONFIG9 Register (Proxy0 Offset = 1C024h; Proxy1 Offset = 1E024h) [reset = 8214007h]

CTRLMMR_PADCONFIG9 is shown in Figure 6-412 and described in Table 6-826.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-825. CTRLMMR_PADCONFIG9 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C024h	0011 E024h

Figure 6-412. CTRLMMR_PADCONFIG9 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-826. CTRLMMR_PADCONFIG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-826. CTRLMMR_PADCONFIG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-826. CTRLMMR_PADCONFIG9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.413 CTRLMMR_PADCONFIG10 Register (Proxy0 Offset = 1C028h; Proxy1 Offset = 1E028h) [reset = 8214007h]

CTRLMMR_PADCONFIG10 is shown in Figure 6-413 and described in Table 6-828.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-827. CTRLMMR_PADCONFIG10 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C028h	0011 E028h

Figure 6-413. CTRLMMR_PADCONFIG10 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-828. CTRLMMR_PADCONFIG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-828. CTRLMMR_PADCONFIG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-828. CTRLMMR_PADCONFIG10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.414 CTRLMMR_PADCONFIG11 Register (Proxy0 Offset = 1C02Ch; Proxy1 Offset = 1E02Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG11 is shown in Figure 6-414 and described in Table 6-830.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-829. CTRLMMR_PADCONFIG11 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C02Ch	0011 E02Ch

Figure 6-414. CTRLMMR_PADCONFIG11 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-830. CTRLMMR_PADCONFIG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-830. CTRLMMR_PADCONFIG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-830. CTRLMMR_PADCONFIG11 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.415 CTRLMMR_PADCONFIG12 Register (Proxy0 Offset = 1C030h; Proxy1 Offset = 1E030h) [reset = 8214007h]

CTRLMMR_PADCONFIG12 is shown in Figure 6-415 and described in Table 6-832.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-831. CTRLMMR_PADCONFIG12 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C030h	0011 E030h

Figure 6-415. CTRLMMR_PADCONFIG12 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-832. CTRLMMR_PADCONFIG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-832. CTRLMMR_PADCONFIG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-832. CTRLMMR_PADCONFIG12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.416 CTRLMMR_PADCONFIG13 Register (Proxy0 Offset = 1C034h; Proxy1 Offset = 1E034h) [reset = 8214007h]

CTRLMMR_PADCONFIG13 is shown in Figure 6-416 and described in Table 6-834.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-833. CTRLMMR_PADCONFIG13 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C034h	0011 E034h

Figure 6-416. CTRLMMR_PADCONFIG13 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-834. CTRLMMR_PADCONFIG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-834. CTRLMMR_PADCONFIG13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-834. CTRLMMR_PADCONFIG13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.417 CTRLMMR_PADCONFIG14 Register (Proxy0 Offset = 1C038h; Proxy1 Offset = 1E038h) [reset = 8214007h]

CTRLMMR_PADCONFIG14 is shown in Figure 6-417 and described in Table 6-836.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-835. CTRLMMR_PADCONFIG14 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C038h	0011 E038h

Figure 6-417. CTRLMMR_PADCONFIG14 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-836. CTRLMMR_PADCONFIG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-836. CTRLMMR_PADCONFIG14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-836. CTRLMMR_PADCONFIG14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.418 CTRLMMR_PADCONFIG15 Register (Proxy0 Offset = 1C03Ch; Proxy1 Offset = 1E03Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG15 is shown in Figure 6-418 and described in Table 6-838.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-837. CTRLMMR_PADCONFIG15 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C03Ch	0011 E03Ch

Figure 6-418. CTRLMMR_PADCONFIG15 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-838. CTRLMMR_PADCONFIG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-838. CTRLMMR_PADCONFIG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-838. CTRLMMR_PADCONFIG15 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.419 CTRLMMR_PADCONFIG16 Register (Proxy0 Offset = 1C040h; Proxy1 Offset = 1E040h) [reset = 8214007h]

CTRLMMR_PADCONFIG16 is shown in Figure 6-419 and described in Table 6-840.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-839. CTRLMMR_PADCONFIG16 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C040h	0011 E040h

Figure 6-419. CTRLMMR_PADCONFIG16 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-840. CTRLMMR_PADCONFIG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-840. CTRLMMR_PADCONFIG16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-840. CTRLMMR_PADCONFIG16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.420 CTRLMMR_PADCONFIG17 Register (Proxy0 Offset = 1C044h; Proxy1 Offset = 1E044h) [reset = 8214007h]

CTRLMMR_PADCONFIG17 is shown in Figure 6-420 and described in Table 6-842.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-841. CTRLMMR_PADCONFIG17 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C044h	0011 E044h

Figure 6-420. CTRLMMR_PADCONFIG17 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-842. CTRLMMR_PADCONFIG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-842. CTRLMMR_PADCONFIG17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-842. CTRLMMR_PADCONFIG17 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.421 CTRLMMR_PADCONFIG18 Register (Proxy0 Offset = 1C048h; Proxy1 Offset = 1E048h) [reset = 8054000h]

CTRLMMR_PADCONFIG18 is shown in Figure 6-421 and described in Table 6-844.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-843. CTRLMMR_PADCONFIG18 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C048h	0011 E048h

Figure 6-421. CTRLMMR_PADCONFIG18 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-844. CTRLMMR_PADCONFIG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-844. CTRLMMR_PADCONFIG18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-844. CTRLMMR_PADCONFIG18 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.422 CTRLMMR_PADCONFIG19 Register (Proxy0 Offset = 1C04Ch; Proxy1 Offset = 1E04Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG19 is shown in Figure 6-422 and described in Table 6-846.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-845. CTRLMMR_PADCONFIG19 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C04Ch	0011 E04Ch

Figure 6-422. CTRLMMR_PADCONFIG19 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-846. CTRLMMR_PADCONFIG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-846. CTRLMMR_PADCONFIG19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-846. CTRLMMR_PADCONFIG19 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.423 CTRLMMR_PADCONFIG20 Register (Proxy0 Offset = 1C050h; Proxy1 Offset = 1E050h) [reset = 8214007h]

CTRLMMR_PADCONFIG20 is shown in Figure 6-423 and described in Table 6-848.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-847. CTRLMMR_PADCONFIG20 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C050h	0011 E050h

Figure 6-423. CTRLMMR_PADCONFIG20 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-848. CTRLMMR_PADCONFIG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-848. CTRLMMR_PADCONFIG20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-848. CTRLMMR_PADCONFIG20 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.424 CTRLMMR_PADCONFIG21 Register (Proxy0 Offset = 1C054h; Proxy1 Offset = 1E054h) [reset = 8214007h]

CTRLMMR_PADCONFIG21 is shown in Figure 6-424 and described in Table 6-850.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-849. CTRLMMR_PADCONFIG21 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C054h	0011 E054h

Figure 6-424. CTRLMMR_PADCONFIG21 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-850. CTRLMMR_PADCONFIG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-850. CTRLMMR_PADCONFIG21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-850. CTRLMMR_PADCONFIG21 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.425 CTRLMMR_PADCONFIG22 Register (Proxy0 Offset = 1C058h; Proxy1 Offset = 1E058h) [reset = 8214007h]

CTRLMMR_PADCONFIG22 is shown in Figure 6-425 and described in Table 6-852.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-851. CTRLMMR_PADCONFIG22 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C058h	0011 E058h

Figure 6-425. CTRLMMR_PADCONFIG22 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-852. CTRLMMR_PADCONFIG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-852. CTRLMMR_PADCONFIG22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-852. CTRLMMR_PADCONFIG22 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.426 CTRLMMR_PADCONFIG23 Register (Proxy0 Offset = 1C05Ch; Proxy1 Offset = 1E05Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG23 is shown in Figure 6-426 and described in Table 6-854.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-853. CTRLMMR_PADCONFIG23 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C05Ch	0011 E05Ch

Figure 6-426. CTRLMMR_PADCONFIG23 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-854. CTRLMMR_PADCONFIG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-854. CTRLMMR_PADCONFIG23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-854. CTRLMMR_PADCONFIG23 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.427 CTRLMMR_PADCONFIG24 Register (Proxy0 Offset = 1C060h; Proxy1 Offset = 1E060h) [reset = 8214007h]

CTRLMMR_PADCONFIG24 is shown in Figure 6-427 and described in Table 6-856.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-855. CTRLMMR_PADCONFIG24 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C060h	0011 E060h

Figure 6-427. CTRLMMR_PADCONFIG24 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-856. CTRLMMR_PADCONFIG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-856. CTRLMMR_PADCONFIG24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-856. CTRLMMR_PADCONFIG24 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.428 CTRLMMR_PADCONFIG25 Register (Proxy0 Offset = 1C064h; Proxy1 Offset = 1E064h) [reset = 8214007h]

CTRLMMR_PADCONFIG25 is shown in Figure 6-428 and described in Table 6-858.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-857. CTRLMMR_PADCONFIG25 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C064h	0011 E064h

Figure 6-428. CTRLMMR_PADCONFIG25 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-858. CTRLMMR_PADCONFIG25 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-858. CTRLMMR_PADCONFIG25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-858. CTRLMMR_PADCONFIG25 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.429 CTRLMMR_PADCONFIG26 Register (Proxy0 Offset = 1C068h; Proxy1 Offset = 1E068h) [reset = 8214007h]

CTRLMMR_PADCONFIG26 is shown in Figure 6-429 and described in Table 6-860.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-859. CTRLMMR_PADCONFIG26 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C068h	0011 E068h

Figure 6-429. CTRLMMR_PADCONFIG26 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-860. CTRLMMR_PADCONFIG26 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-860. CTRLMMR_PADCONFIG26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-860. CTRLMMR_PADCONFIG26 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.430 CTRLMMR_PADCONFIG27 Register (Proxy0 Offset = 1C06Ch; Proxy1 Offset = 1E06Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG27 is shown in Figure 6-430 and described in Table 6-862.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-861. CTRLMMR_PADCONFIG27 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C06Ch	0011 E06Ch

Figure 6-430. CTRLMMR_PADCONFIG27 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-862. CTRLMMR_PADCONFIG27 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-862. CTRLMMR_PADCONFIG27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-862. CTRLMMR_PADCONFIG27 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.431 CTRLMMR_PADCONFIG28 Register (Proxy0 Offset = 1C070h; Proxy1 Offset = 1E070h) [reset = 8214007h]

CTRLMMR_PADCONFIG28 is shown in Figure 6-431 and described in Table 6-864.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-863. CTRLMMR_PADCONFIG28 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C070h	0011 E070h

Figure 6-431. CTRLMMR_PADCONFIG28 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-864. CTRLMMR_PADCONFIG28 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-864. CTRLMMR_PADCONFIG28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-864. CTRLMMR_PADCONFIG28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.432 CTRLMMR_PADCONFIG29 Register (Proxy0 Offset = 1C074h; Proxy1 Offset = 1E074h) [reset = 8214007h]

CTRLMMR_PADCONFIG29 is shown in Figure 6-432 and described in Table 6-866.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-865. CTRLMMR_PADCONFIG29 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C074h	0011 E074h

Figure 6-432. CTRLMMR_PADCONFIG29 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-866. CTRLMMR_PADCONFIG29 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-866. CTRLMMR_PADCONFIG29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-866. CTRLMMR_PADCONFIG29 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.433 CTRLMMR_PADCONFIG30 Register (Proxy0 Offset = 1C078h; Proxy1 Offset = 1E078h) [reset = 8214007h]

CTRLMMR_PADCONFIG30 is shown in Figure 6-433 and described in Table 6-868.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-867. CTRLMMR_PADCONFIG30 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C078h	0011 E078h

Figure 6-433. CTRLMMR_PADCONFIG30 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-868. CTRLMMR_PADCONFIG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-868. CTRLMMR_PADCONFIG30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-868. CTRLMMR_PADCONFIG30 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.434 CTRLMMR_PADCONFIG31 Register (Proxy0 Offset = 1C07Ch; Proxy1 Offset = 1E07Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG31 is shown in Figure 6-434 and described in Table 6-870.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-869. CTRLMMR_PADCONFIG31 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C07Ch	0011 E07Ch

Figure 6-434. CTRLMMR_PADCONFIG31 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-870. CTRLMMR_PADCONFIG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-870. CTRLMMR_PADCONFIG31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-870. CTRLMMR_PADCONFIG31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.435 CTRLMMR_PADCONFIG32 Register (Proxy0 Offset = 1C080h; Proxy1 Offset = 1E080h) [reset = 8214007h]

CTRLMMR_PADCONFIG32 is shown in Figure 6-435 and described in Table 6-872.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-871. CTRLMMR_PADCONFIG32 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C080h	0011 E080h

Figure 6-435. CTRLMMR_PADCONFIG32 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-872. CTRLMMR_PADCONFIG32 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-872. CTRLMMR_PADCONFIG32 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-872. CTRLMMR_PADCONFIG32 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.436 CTRLMMR_PADCONFIG33 Register (Proxy0 Offset = 1C084h; Proxy1 Offset = 1E084h) [reset = 8214007h]

CTRLMMR_PADCONFIG33 is shown in Figure 6-436 and described in Table 6-874.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-873. CTRLMMR_PADCONFIG33 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C084h	0011 E084h

Figure 6-436. CTRLMMR_PADCONFIG33 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-874. CTRLMMR_PADCONFIG33 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-874. CTRLMMR_PADCONFIG33 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-874. CTRLMMR_PADCONFIG33 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.437 CTRLMMR_PADCONFIG34 Register (Proxy0 Offset = 1C088h; Proxy1 Offset = 1E088h) [reset = 8214007h]

CTRLMMR_PADCONFIG34 is shown in Figure 6-437 and described in Table 6-876.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-875. CTRLMMR_PADCONFIG34 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C088h	0011 E088h

Figure 6-437. CTRLMMR_PADCONFIG34 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-876. CTRLMMR_PADCONFIG34 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-876. CTRLMMR_PADCONFIG34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-876. CTRLMMR_PADCONFIG34 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.438 CTRLMMR_PADCONFIG35 Register (Proxy0 Offset = 1C08Ch; Proxy1 Offset = 1E08Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG35 is shown in Figure 6-438 and described in Table 6-878.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-877. CTRLMMR_PADCONFIG35 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C08Ch	0011 E08Ch

Figure 6-438. CTRLMMR_PADCONFIG35 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-878. CTRLMMR_PADCONFIG35 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-878. CTRLMMR_PADCONFIG35 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-878. CTRLMMR_PADCONFIG35 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.439 CTRLMMR_PADCONFIG36 Register (Proxy0 Offset = 1C090h; Proxy1 Offset = 1E090h) [reset = 8214007h]

CTRLMMR_PADCONFIG36 is shown in Figure 6-439 and described in Table 6-880.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-879. CTRLMMR_PADCONFIG36 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C090h	0011 E090h

Figure 6-439. CTRLMMR_PADCONFIG36 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-880. CTRLMMR_PADCONFIG36 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-880. CTRLMMR_PADCONFIG36 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-880. CTRLMMR_PADCONFIG36 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.440 CTRLMMR_PADCONFIG37 Register (Proxy0 Offset = 1C094h; Proxy1 Offset = 1E094h) [reset = 8214007h]

CTRLMMR_PADCONFIG37 is shown in Figure 6-440 and described in Table 6-882.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-881. CTRLMMR_PADCONFIG37 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C094h	0011 E094h

Figure 6-440. CTRLMMR_PADCONFIG37 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-882. CTRLMMR_PADCONFIG37 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-882. CTRLMMR_PADCONFIG37 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-882. CTRLMMR_PADCONFIG37 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.441 CTRLMMR_PADCONFIG38 Register (Proxy0 Offset = 1C098h; Proxy1 Offset = 1E098h) [reset = 8214007h]

CTRLMMR_PADCONFIG38 is shown in Figure 6-441 and described in Table 6-884.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-883. CTRLMMR_PADCONFIG38 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C098h	0011 E098h

Figure 6-441. CTRLMMR_PADCONFIG38 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-884. CTRLMMR_PADCONFIG38 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-884. CTRLMMR_PADCONFIG38 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-884. CTRLMMR_PADCONFIG38 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.442 CTRLMMR_PADCONFIG39 Register (Proxy0 Offset = 1C09Ch; Proxy1 Offset = 1E09Ch) [reset = 8254007h]

CTRLMMR_PADCONFIG39 is shown in Figure 6-442 and described in Table 6-886.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-885. CTRLMMR_PADCONFIG39 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C09Ch	0011 E09Ch

Figure 6-442. CTRLMMR_PADCONFIG39 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-886. CTRLMMR_PADCONFIG39 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-886. CTRLMMR_PADCONFIG39 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-886. CTRLMMR_PADCONFIG39 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.443 CTRLMMR_PADCONFIG40 Register (Proxy0 Offset = 1C0A0h; Proxy1 Offset = 1E0A0h) [reset = 8214007h]

CTRLMMR_PADCONFIG40 is shown in Figure 6-443 and described in Table 6-888.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-887. CTRLMMR_PADCONFIG40 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0A0h	0011 E0A0h

Figure 6-443. CTRLMMR_PADCONFIG40 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-888. CTRLMMR_PADCONFIG40 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-888. CTRLMMR_PADCONFIG40 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-888. CTRLMMR_PADCONFIG40 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.444 CTRLMMR_PADCONFIG41 Register (Proxy0 Offset = 1C0A4h; Proxy1 Offset = 1E0A4h) [reset = 8214007h]

CTRLMMR_PADCONFIG41 is shown in Figure 6-444 and described in Table 6-890.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-889. CTRLMMR_PADCONFIG41 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0A4h	0011 E0A4h

Figure 6-444. CTRLMMR_PADCONFIG41 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-890. CTRLMMR_PADCONFIG41 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-890. CTRLMMR_PADCONFIG41 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-890. CTRLMMR_PADCONFIG41 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.445 CTRLMMR_PADCONFIG42 Register (Proxy0 Offset = 1C0A8h; Proxy1 Offset = 1E0A8h) [reset = 8214007h]

CTRLMMR_PADCONFIG42 is shown in Figure 6-445 and described in Table 6-892.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-891. CTRLMMR_PADCONFIG42 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0A8h	0011 E0A8h

Figure 6-445. CTRLMMR_PADCONFIG42 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-892. CTRLMMR_PADCONFIG42 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-892. CTRLMMR_PADCONFIG42 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-892. CTRLMMR_PADCONFIG42 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.446 CTRLMMR_PADCONFIG43 Register (Proxy0 Offset = 1C0ACh; Proxy1 Offset = 1E0ACh) [reset = 8214007h]

CTRLMMR_PADCONFIG43 is shown in Figure 6-446 and described in Table 6-894.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-893. CTRLMMR_PADCONFIG43 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0ACh	0011 E0ACh

Figure 6-446. CTRLMMR_PADCONFIG43 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-894. CTRLMMR_PADCONFIG43 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-894. CTRLMMR_PADCONFIG43 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-894. CTRLMMR_PADCONFIG43 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.447 CTRLMMR_PADCONFIG44 Register (Proxy0 Offset = 1C0B0h; Proxy1 Offset = 1E0B0h) [reset = 8214007h]

CTRLMMR_PADCONFIG44 is shown in Figure 6-447 and described in Table 6-896.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-895. CTRLMMR_PADCONFIG44 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0B0h	0011 E0B0h

Figure 6-447. CTRLMMR_PADCONFIG44 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-896. CTRLMMR_PADCONFIG44 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-896. CTRLMMR_PADCONFIG44 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-896. CTRLMMR_PADCONFIG44 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.448 CTRLMMR_PADCONFIG45 Register (Proxy0 Offset = 1C0B4h; Proxy1 Offset = 1E0B4h) [reset = 8214007h]

CTRLMMR_PADCONFIG45 is shown in Figure 6-448 and described in Table 6-898.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-897. CTRLMMR_PADCONFIG45 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0B4h	0011 E0B4h

Figure 6-448. CTRLMMR_PADCONFIG45 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-898. CTRLMMR_PADCONFIG45 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-898. CTRLMMR_PADCONFIG45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-898. CTRLMMR_PADCONFIG45 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.449 CTRLMMR_PADCONFIG46 Register (Proxy0 Offset = 1C0B8h; Proxy1 Offset = 1E0B8h) [reset = 8214007h]

CTRLMMR_PADCONFIG46 is shown in Figure 6-449 and described in Table 6-900.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-899. CTRLMMR_PADCONFIG46 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0B8h	0011 E0B8h

Figure 6-449. CTRLMMR_PADCONFIG46 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-900. CTRLMMR_PADCONFIG46 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-900. CTRLMMR_PADCONFIG46 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-900. CTRLMMR_PADCONFIG46 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.450 CTRLMMR_PADCONFIG47 Register (Proxy0 Offset = 1C0BCh; Proxy1 Offset = 1E0BCh) [reset = 8214007h]

CTRLMMR_PADCONFIG47 is shown in Figure 6-450 and described in Table 6-902.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-901. CTRLMMR_PADCONFIG47 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0BCh	0011 E0BCh

Figure 6-450. CTRLMMR_PADCONFIG47 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-902. CTRLMMR_PADCONFIG47 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-902. CTRLMMR_PADCONFIG47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-902. CTRLMMR_PADCONFIG47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.451 CTRLMMR_PADCONFIG48 Register (Proxy0 Offset = 1C0C0h; Proxy1 Offset = 1E0C0h) [reset = 8214007h]

CTRLMMR_PADCONFIG48 is shown in Figure 6-451 and described in Table 6-904.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-903. CTRLMMR_PADCONFIG48 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0C0h	0011 E0C0h

Figure 6-451. CTRLMMR_PADCONFIG48 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-904. CTRLMMR_PADCONFIG48 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-904. CTRLMMR_PADCONFIG48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-904. CTRLMMR_PADCONFIG48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.452 CTRLMMR_PADCONFIG49 Register (Proxy0 Offset = 1C0C4h; Proxy1 Offset = 1E0C4h) [reset = 8254007h]

CTRLMMR_PADCONFIG49 is shown in Figure 6-452 and described in Table 6-906.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-905. CTRLMMR_PADCONFIG49 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0C4h	0011 E0C4h

Figure 6-452. CTRLMMR_PADCONFIG49 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-906. CTRLMMR_PADCONFIG49 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-906. CTRLMMR_PADCONFIG49 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-906. CTRLMMR_PADCONFIG49 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.453 CTRLMMR_PADCONFIG50 Register (Proxy0 Offset = 1C0C8h; Proxy1 Offset = 1E0C8h) [reset = 8214007h]

CTRLMMR_PADCONFIG50 is shown in Figure 6-453 and described in Table 6-908.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-907. CTRLMMR_PADCONFIG50 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0C8h	0011 E0C8h

Figure 6-453. CTRLMMR_PADCONFIG50 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-908. CTRLMMR_PADCONFIG50 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-908. CTRLMMR_PADCONFIG50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-908. CTRLMMR_PADCONFIG50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.454 CTRLMMR_PADCONFIG51 Register (Proxy0 Offset = 1C0CCh; Proxy1 Offset = 1E0CCh) [reset = 8214007h]

CTRLMMR_PADCONFIG51 is shown in Figure 6-454 and described in Table 6-910.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-909. CTRLMMR_PADCONFIG51 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0CCh	0011 E0CCh

Figure 6-454. CTRLMMR_PADCONFIG51 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-910. CTRLMMR_PADCONFIG51 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-910. CTRLMMR_PADCONFIG51 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-910. CTRLMMR_PADCONFIG51 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.455 CTRLMMR_PADCONFIG52 Register (Proxy0 Offset = 1C0D0h; Proxy1 Offset = 1E0D0h) [reset = 8214007h]

CTRLMMR_PADCONFIG52 is shown in Figure 6-455 and described in Table 6-912.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-911. CTRLMMR_PADCONFIG52 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0D0h	0011 E0D0h

Figure 6-455. CTRLMMR_PADCONFIG52 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-912. CTRLMMR_PADCONFIG52 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-912. CTRLMMR_PADCONFIG52 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-912. CTRLMMR_PADCONFIG52 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.456 CTRLMMR_PADCONFIG53 Register (Proxy0 Offset = 1C0D4h; Proxy1 Offset = 1E0D4h) [reset = 8214007h]

CTRLMMR_PADCONFIG53 is shown in Figure 6-456 and described in Table 6-914.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-913. CTRLMMR_PADCONFIG53 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0D4h	0011 E0D4h

Figure 6-456. CTRLMMR_PADCONFIG53 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-914. CTRLMMR_PADCONFIG53 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-914. CTRLMMR_PADCONFIG53 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-914. CTRLMMR_PADCONFIG53 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.457 CTRLMMR_PADCONFIG54 Register (Proxy0 Offset = 1C0D8h; Proxy1 Offset = 1E0D8h) [reset = 8214007h]

CTRLMMR_PADCONFIG54 is shown in Figure 6-457 and described in Table 6-916.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-915. CTRLMMR_PADCONFIG54 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0D8h	0011 E0D8h

Figure 6-457. CTRLMMR_PADCONFIG54 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-916. CTRLMMR_PADCONFIG54 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-916. CTRLMMR_PADCONFIG54 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-916. CTRLMMR_PADCONFIG54 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.458 CTRLMMR_PADCONFIG55 Register (Proxy0 Offset = 1C0DCh; Proxy1 Offset = 1E0DCh) [reset = 8214007h]

CTRLMMR_PADCONFIG55 is shown in Figure 6-458 and described in Table 6-918.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-917. CTRLMMR_PADCONFIG55 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0DCh	0011 E0DCh

Figure 6-458. CTRLMMR_PADCONFIG55 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-918. CTRLMMR_PADCONFIG55 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-918. CTRLMMR_PADCONFIG55 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-918. CTRLMMR_PADCONFIG55 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.459 CTRLMMR_PADCONFIG56 Register (Proxy0 Offset = 1C0E0h; Proxy1 Offset = 1E0E0h) [reset = 8214007h]

CTRLMMR_PADCONFIG56 is shown in Figure 6-459 and described in Table 6-920.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-919. CTRLMMR_PADCONFIG56 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0E0h	0011 E0E0h

Figure 6-459. CTRLMMR_PADCONFIG56 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-920. CTRLMMR_PADCONFIG56 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-920. CTRLMMR_PADCONFIG56 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-920. CTRLMMR_PADCONFIG56 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.460 CTRLMMR_PADCONFIG57 Register (Proxy0 Offset = 1C0E4h; Proxy1 Offset = 1E0E4h) [reset = 8214007h]

CTRLMMR_PADCONFIG57 is shown in Figure 6-460 and described in Table 6-922.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-921. CTRLMMR_PADCONFIG57 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0E4h	0011 E0E4h

Figure 6-460. CTRLMMR_PADCONFIG57 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-922. CTRLMMR_PADCONFIG57 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-922. CTRLMMR_PADCONFIG57 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-922. CTRLMMR_PADCONFIG57 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.461 CTRLMMR_PADCONFIG58 Register (Proxy0 Offset = 1C0E8h; Proxy1 Offset = 1E0E8h) [reset = 8214007h]

CTRLMMR_PADCONFIG58 is shown in Figure 6-461 and described in Table 6-924.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-923. CTRLMMR_PADCONFIG58 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0E8h	0011 E0E8h

Figure 6-461. CTRLMMR_PADCONFIG58 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-924. CTRLMMR_PADCONFIG58 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-924. CTRLMMR_PADCONFIG58 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-924. CTRLMMR_PADCONFIG58 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.462 CTRLMMR_PADCONFIG59 Register (Proxy0 Offset = 1C0ECh; Proxy1 Offset = 1E0ECh) [reset = 8214007h]

CTRLMMR_PADCONFIG59 is shown in Figure 6-462 and described in Table 6-926.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-925. CTRLMMR_PADCONFIG59 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0ECh	0011 E0ECh

Figure 6-462. CTRLMMR_PADCONFIG59 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-926. CTRLMMR_PADCONFIG59 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-926. CTRLMMR_PADCONFIG59 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-926. CTRLMMR_PADCONFIG59 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.463 CTRLMMR_PADCONFIG60 Register (Proxy0 Offset = 1C0F0h; Proxy1 Offset = 1E0F0h) [reset = 8214007h]

CTRLMMR_PADCONFIG60 is shown in Figure 6-463 and described in Table 6-928.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-927. CTRLMMR_PADCONFIG60 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0F0h	0011 E0F0h

Figure 6-463. CTRLMMR_PADCONFIG60 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-928. CTRLMMR_PADCONFIG60 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-928. CTRLMMR_PADCONFIG60 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-928. CTRLMMR_PADCONFIG60 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.464 CTRLMMR_PADCONFIG61 Register (Proxy0 Offset = 1C0F4h; Proxy1 Offset = 1E0F4h) [reset = 8254007h]

CTRLMMR_PADCONFIG61 is shown in Figure 6-464 and described in Table 6-930.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-929. CTRLMMR_PADCONFIG61 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0F4h	0011 E0F4h

Figure 6-464. CTRLMMR_PADCONFIG61 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-930. CTRLMMR_PADCONFIG61 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-930. CTRLMMR_PADCONFIG61 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-930. CTRLMMR_PADCONFIG61 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.465 CTRLMMR_PADCONFIG62 Register (Proxy0 Offset = 1C0F8h; Proxy1 Offset = 1E0F8h) [reset = 8214007h]

CTRLMMR_PADCONFIG62 is shown in Figure 6-465 and described in Table 6-932.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-931. CTRLMMR_PADCONFIG62 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0F8h	0011 E0F8h

Figure 6-465. CTRLMMR_PADCONFIG62 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-932. CTRLMMR_PADCONFIG62 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-932. CTRLMMR_PADCONFIG62 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-932. CTRLMMR_PADCONFIG62 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.466 CTRLMMR_PADCONFIG63 Register (Proxy0 Offset = 1C0FCh; Proxy1 Offset = 1E0FCh) [reset = 8214007h]

CTRLMMR_PADCONFIG63 is shown in Figure 6-466 and described in Table 6-934.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-933. CTRLMMR_PADCONFIG63 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C0FCh	0011 E0FCh

Figure 6-466. CTRLMMR_PADCONFIG63 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-934. CTRLMMR_PADCONFIG63 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-934. CTRLMMR_PADCONFIG63 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-934. CTRLMMR_PADCONFIG63 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.467 CTRLMMR_PADCONFIG64 Register (Proxy0 Offset = 1C100h; Proxy1 Offset = 1E100h) [reset = 8214007h]

CTRLMMR_PADCONFIG64 is shown in Figure 6-467 and described in Table 6-936.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-935. CTRLMMR_PADCONFIG64 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C100h	0011 E100h

Figure 6-467. CTRLMMR_PADCONFIG64 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-936. CTRLMMR_PADCONFIG64 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-936. CTRLMMR_PADCONFIG64 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-936. CTRLMMR_PADCONFIG64 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.468 CTRLMMR_PADCONFIG65 Register (Proxy0 Offset = 1C104h; Proxy1 Offset = 1E104h) [reset = 8214007h]

CTRLMMR_PADCONFIG65 is shown in Figure 6-468 and described in Table 6-938.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-937. CTRLMMR_PADCONFIG65 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C104h	0011 E104h

Figure 6-468. CTRLMMR_PADCONFIG65 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-938. CTRLMMR_PADCONFIG65 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-938. CTRLMMR_PADCONFIG65 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-938. CTRLMMR_PADCONFIG65 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.469 CTRLMMR_PADCONFIG66 Register (Proxy0 Offset = 1C108h; Proxy1 Offset = 1E108h) [reset = 8214007h]

CTRLMMR_PADCONFIG66 is shown in Figure 6-469 and described in Table 6-940.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-939. CTRLMMR_PADCONFIG66 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C108h	0011 E108h

Figure 6-469. CTRLMMR_PADCONFIG66 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-940. CTRLMMR_PADCONFIG66 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-940. CTRLMMR_PADCONFIG66 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-940. CTRLMMR_PADCONFIG66 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.470 CTRLMMR_PADCONFIG67 Register (Proxy0 Offset = 1C10Ch; Proxy1 Offset = 1E10Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG67 is shown in Figure 6-470 and described in Table 6-942.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-941. CTRLMMR_PADCONFIG67 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C10Ch	0011 E10Ch

Figure 6-470. CTRLMMR_PADCONFIG67 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-942. CTRLMMR_PADCONFIG67 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-942. CTRLMMR_PADCONFIG67 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-942. CTRLMMR_PADCONFIG67 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.471 CTRLMMR_PADCONFIG68 Register (Proxy0 Offset = 1C110h; Proxy1 Offset = 1E110h) [reset = 8214007h]

CTRLMMR_PADCONFIG68 is shown in Figure 6-471 and described in Table 6-944.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-943. CTRLMMR_PADCONFIG68 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C110h	0011 E110h

Figure 6-471. CTRLMMR_PADCONFIG68 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-944. CTRLMMR_PADCONFIG68 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-944. CTRLMMR_PADCONFIG68 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-944. CTRLMMR_PADCONFIG68 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.472 CTRLMMR_PADCONFIG69 Register (Proxy0 Offset = 1C114h; Proxy1 Offset = 1E114h) [reset = 8254007h]

CTRLMMR_PADCONFIG69 is shown in Figure 6-472 and described in Table 6-946.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-945. CTRLMMR_PADCONFIG69 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C114h	0011 E114h

Figure 6-472. CTRLMMR_PADCONFIG69 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-946. CTRLMMR_PADCONFIG69 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-946. CTRLMMR_PADCONFIG69 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-946. CTRLMMR_PADCONFIG69 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.473 CTRLMMR_PADCONFIG70 Register (Proxy0 Offset = 1C118h; Proxy1 Offset = 1E118h) [reset = 8214007h]

CTRLMMR_PADCONFIG70 is shown in Figure 6-473 and described in Table 6-948.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-947. CTRLMMR_PADCONFIG70 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C118h	0011 E118h

Figure 6-473. CTRLMMR_PADCONFIG70 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-948. CTRLMMR_PADCONFIG70 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-948. CTRLMMR_PADCONFIG70 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-948. CTRLMMR_PADCONFIG70 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.474 CTRLMMR_PADCONFIG71 Register (Proxy0 Offset = 1C11Ch; Proxy1 Offset = 1E11Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG71 is shown in Figure 6-474 and described in Table 6-950.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-949. CTRLMMR_PADCONFIG71 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C11Ch	0011 E11Ch

Figure 6-474. CTRLMMR_PADCONFIG71 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-950. CTRLMMR_PADCONFIG71 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-950. CTRLMMR_PADCONFIG71 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-950. CTRLMMR_PADCONFIG71 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.475 CTRLMMR_PADCONFIG72 Register (Proxy0 Offset = 1C120h; Proxy1 Offset = 1E120h) [reset = 8214007h]

CTRLMMR_PADCONFIG72 is shown in Figure 6-475 and described in Table 6-952.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-951. CTRLMMR_PADCONFIG72 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C120h	0011 E120h

Figure 6-475. CTRLMMR_PADCONFIG72 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-952. CTRLMMR_PADCONFIG72 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-952. CTRLMMR_PADCONFIG72 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-952. CTRLMMR_PADCONFIG72 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.476 CTRLMMR_PADCONFIG73 Register (Proxy0 Offset = 1C124h; Proxy1 Offset = 1E124h) [reset = 8214007h]

CTRLMMR_PADCONFIG73 is shown in Figure 6-476 and described in Table 6-954.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-953. CTRLMMR_PADCONFIG73 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C124h	0011 E124h

Figure 6-476. CTRLMMR_PADCONFIG73 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-954. CTRLMMR_PADCONFIG73 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-954. CTRLMMR_PADCONFIG73 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-954. CTRLMMR_PADCONFIG73 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.477 CTRLMMR_PADCONFIG74 Register (Proxy0 Offset = 1C128h; Proxy1 Offset = 1E128h) [reset = 8214007h]

CTRLMMR_PADCONFIG74 is shown in Figure 6-477 and described in Table 6-956.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-955. CTRLMMR_PADCONFIG74 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C128h	0011 E128h

Figure 6-477. CTRLMMR_PADCONFIG74 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-956. CTRLMMR_PADCONFIG74 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-956. CTRLMMR_PADCONFIG74 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-956. CTRLMMR_PADCONFIG74 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.478 CTRLMMR_PADCONFIG75 Register (Proxy0 Offset = 1C12Ch; Proxy1 Offset = 1E12Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG75 is shown in Figure 6-478 and described in Table 6-958.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-957. CTRLMMR_PADCONFIG75 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C12Ch	0011 E12Ch

Figure 6-478. CTRLMMR_PADCONFIG75 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-958. CTRLMMR_PADCONFIG75 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-958. CTRLMMR_PADCONFIG75 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-958. CTRLMMR_PADCONFIG75 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.479 CTRLMMR_PADCONFIG76 Register (Proxy0 Offset = 1C130h; Proxy1 Offset = 1E130h) [reset = 8214007h]

CTRLMMR_PADCONFIG76 is shown in Figure 6-479 and described in Table 6-960.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-959. CTRLMMR_PADCONFIG76 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C130h	0011 E130h

Figure 6-479. CTRLMMR_PADCONFIG76 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-960. CTRLMMR_PADCONFIG76 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-960. CTRLMMR_PADCONFIG76 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-960. CTRLMMR_PADCONFIG76 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.480 CTRLMMR_PADCONFIG77 Register (Proxy0 Offset = 1C134h; Proxy1 Offset = 1E134h) [reset = 8214007h]

CTRLMMR_PADCONFIG77 is shown in Figure 6-480 and described in Table 6-962.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-961. CTRLMMR_PADCONFIG77 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C134h	0011 E134h

Figure 6-480. CTRLMMR_PADCONFIG77 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-962. CTRLMMR_PADCONFIG77 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-962. CTRLMMR_PADCONFIG77 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-962. CTRLMMR_PADCONFIG77 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.481 CTRLMMR_PADCONFIG78 Register (Proxy0 Offset = 1C138h; Proxy1 Offset = 1E138h) [reset = 8214007h]

CTRLMMR_PADCONFIG78 is shown in Figure 6-481 and described in Table 6-964.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-963. CTRLMMR_PADCONFIG78 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C138h	0011 E138h

Figure 6-481. CTRLMMR_PADCONFIG78 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-964. CTRLMMR_PADCONFIG78 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-964. CTRLMMR_PADCONFIG78 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-964. CTRLMMR_PADCONFIG78 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.482 CTRLMMR_PADCONFIG79 Register (Proxy0 Offset = 1C13Ch; Proxy1 Offset = 1E13Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG79 is shown in Figure 6-482 and described in Table 6-966.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-965. CTRLMMR_PADCONFIG79 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C13Ch	0011 E13Ch

Figure 6-482. CTRLMMR_PADCONFIG79 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-966. CTRLMMR_PADCONFIG79 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-966. CTRLMMR_PADCONFIG79 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-966. CTRLMMR_PADCONFIG79 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.483 CTRLMMR_PADCONFIG80 Register (Proxy0 Offset = 1C140h; Proxy1 Offset = 1E140h) [reset = 8214007h]

CTRLMMR_PADCONFIG80 is shown in Figure 6-483 and described in Table 6-968.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-967. CTRLMMR_PADCONFIG80 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C140h	0011 E140h

Figure 6-483. CTRLMMR_PADCONFIG80 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-968. CTRLMMR_PADCONFIG80 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-968. CTRLMMR_PADCONFIG80 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-968. CTRLMMR_PADCONFIG80 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.484 CTRLMMR_PADCONFIG81 Register (Proxy0 Offset = 1C144h; Proxy1 Offset = 1E144h) [reset = 8254007h]

CTRLMMR_PADCONFIG81 is shown in Figure 6-484 and described in Table 6-970.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-969. CTRLMMR_PADCONFIG81 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C144h	0011 E144h

Figure 6-484. CTRLMMR_PADCONFIG81 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-970. CTRLMMR_PADCONFIG81 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-970. CTRLMMR_PADCONFIG81 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-970. CTRLMMR_PADCONFIG81 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.485 CTRLMMR_PADCONFIG82 Register (Proxy0 Offset = 1C148h; Proxy1 Offset = 1E148h) [reset = 8214007h]

CTRLMMR_PADCONFIG82 is shown in Figure 6-485 and described in Table 6-972.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-971. CTRLMMR_PADCONFIG82 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C148h	0011 E148h

Figure 6-485. CTRLMMR_PADCONFIG82 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-972. CTRLMMR_PADCONFIG82 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-972. CTRLMMR_PADCONFIG82 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-972. CTRLMMR_PADCONFIG82 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.486 CTRLMMR_PADCONFIG83 Register (Proxy0 Offset = 1C14Ch; Proxy1 Offset = 1E14Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG83 is shown in Figure 6-486 and described in Table 6-974.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-973. CTRLMMR_PADCONFIG83 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C14Ch	0011 E14Ch

Figure 6-486. CTRLMMR_PADCONFIG83 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-974. CTRLMMR_PADCONFIG83 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-974. CTRLMMR_PADCONFIG83 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-974. CTRLMMR_PADCONFIG83 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.487 CTRLMMR_PADCONFIG84 Register (Proxy0 Offset = 1C150h; Proxy1 Offset = 1E150h) [reset = 8214007h]

CTRLMMR_PADCONFIG84 is shown in Figure 6-487 and described in Table 6-976.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-975. CTRLMMR_PADCONFIG84 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C150h	0011 E150h

Figure 6-487. CTRLMMR_PADCONFIG84 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-976. CTRLMMR_PADCONFIG84 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-976. CTRLMMR_PADCONFIG84 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-976. CTRLMMR_PADCONFIG84 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.488 CTRLMMR_PADCONFIG85 Register (Proxy0 Offset = 1C154h; Proxy1 Offset = 1E154h) [reset = 8214007h]

CTRLMMR_PADCONFIG85 is shown in Figure 6-488 and described in Table 6-978.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-977. CTRLMMR_PADCONFIG85 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C154h	0011 E154h

Figure 6-488. CTRLMMR_PADCONFIG85 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-978. CTRLMMR_PADCONFIG85 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-978. CTRLMMR_PADCONFIG85 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-978. CTRLMMR_PADCONFIG85 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.489 CTRLMMR_PADCONFIG86 Register (Proxy0 Offset = 1C158h; Proxy1 Offset = 1E158h) [reset = 8214007h]

CTRLMMR_PADCONFIG86 is shown in Figure 6-489 and described in Table 6-980.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-979. CTRLMMR_PADCONFIG86 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C158h	0011 E158h

Figure 6-489. CTRLMMR_PADCONFIG86 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-980. CTRLMMR_PADCONFIG86 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-980. CTRLMMR_PADCONFIG86 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-980. CTRLMMR_PADCONFIG86 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.490 CTRLMMR_PADCONFIG87 Register (Proxy0 Offset = 1C15Ch; Proxy1 Offset = 1E15Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG87 is shown in Figure 6-490 and described in Table 6-982.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-981. CTRLMMR_PADCONFIG87 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C15Ch	0011 E15Ch

Figure 6-490. CTRLMMR_PADCONFIG87 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-982. CTRLMMR_PADCONFIG87 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-982. CTRLMMR_PADCONFIG87 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-982. CTRLMMR_PADCONFIG87 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.491 CTRLMMR_PADCONFIG88 Register (Proxy0 Offset = 1C160h; Proxy1 Offset = 1E160h) [reset = 8214007h]

CTRLMMR_PADCONFIG88 is shown in Figure 6-491 and described in Table 6-984.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-983. CTRLMMR_PADCONFIG88 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C160h	0011 E160h

Figure 6-491. CTRLMMR_PADCONFIG88 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-984. CTRLMMR_PADCONFIG88 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-984. CTRLMMR_PADCONFIG88 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-984. CTRLMMR_PADCONFIG88 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.492 CTRLMMR_PADCONFIG89 Register (Proxy0 Offset = 1C164h; Proxy1 Offset = 1E164h) [reset = 8214007h]

CTRLMMR_PADCONFIG89 is shown in Figure 6-492 and described in Table 6-986.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-985. CTRLMMR_PADCONFIG89 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C164h	0011 E164h

Figure 6-492. CTRLMMR_PADCONFIG89 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-986. CTRLMMR_PADCONFIG89 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-986. CTRLMMR_PADCONFIG89 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-986. CTRLMMR_PADCONFIG89 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.493 CTRLMMR_PADCONFIG90 Register (Proxy0 Offset = 1C168h; Proxy1 Offset = 1E168h) [reset = 8214007h]

CTRLMMR_PADCONFIG90 is shown in Figure 6-493 and described in Table 6-988.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-987. CTRLMMR_PADCONFIG90 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C168h	0011 E168h

Figure 6-493. CTRLMMR_PADCONFIG90 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-988. CTRLMMR_PADCONFIG90 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-988. CTRLMMR_PADCONFIG90 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-988. CTRLMMR_PADCONFIG90 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.494 CTRLMMR_PADCONFIG91 Register (Proxy0 Offset = 1C16Ch; Proxy1 Offset = 1E16Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG91 is shown in Figure 6-494 and described in Table 6-990.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-989. CTRLMMR_PADCONFIG91 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C16Ch	0011 E16Ch

Figure 6-494. CTRLMMR_PADCONFIG91 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-990. CTRLMMR_PADCONFIG91 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-990. CTRLMMR_PADCONFIG91 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-990. CTRLMMR_PADCONFIG91 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.495 CTRLMMR_PADCONFIG92 Register (Proxy0 Offset = 1C170h; Proxy1 Offset = 1E170h) [reset = 8214007h]

CTRLMMR_PADCONFIG92 is shown in Figure 6-495 and described in Table 6-992.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-991. CTRLMMR_PADCONFIG92 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C170h	0011 E170h

Figure 6-495. CTRLMMR_PADCONFIG92 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-992. CTRLMMR_PADCONFIG92 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-992. CTRLMMR_PADCONFIG92 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-992. CTRLMMR_PADCONFIG92 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.496 CTRLMMR_PADCONFIG93 Register (Proxy0 Offset = 1C174h; Proxy1 Offset = 1E174h) [reset = 8214007h]

CTRLMMR_PADCONFIG93 is shown in Figure 6-496 and described in Table 6-994.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-993. CTRLMMR_PADCONFIG93 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C174h	0011 E174h

Figure 6-496. CTRLMMR_PADCONFIG93 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-994. CTRLMMR_PADCONFIG93 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-994. CTRLMMR_PADCONFIG93 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-994. CTRLMMR_PADCONFIG93 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.497 CTRLMMR_PADCONFIG94 Register (Proxy0 Offset = 1C178h; Proxy1 Offset = 1E178h) [reset = 8214007h]

CTRLMMR_PADCONFIG94 is shown in Figure 6-497 and described in Table 6-996.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-995. CTRLMMR_PADCONFIG94 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C178h	0011 E178h

Figure 6-497. CTRLMMR_PADCONFIG94 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-996. CTRLMMR_PADCONFIG94 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-996. CTRLMMR_PADCONFIG94 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-996. CTRLMMR_PADCONFIG94 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.498 CTRLMMR_PADCONFIG95 Register (Proxy0 Offset = 1C17Ch; Proxy1 Offset = 1E17Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG95 is shown in Figure 6-498 and described in Table 6-998.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-997. CTRLMMR_PADCONFIG95 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C17Ch	0011 E17Ch

Figure 6-498. CTRLMMR_PADCONFIG95 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-998. CTRLMMR_PADCONFIG95 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-998. CTRLMMR_PADCONFIG95 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-998. CTRLMMR_PADCONFIG95 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.499 CTRLMMR_PADCONFIG96 Register (Proxy0 Offset = 1C180h; Proxy1 Offset = 1E180h) [reset = 8214007h]

CTRLMMR_PADCONFIG96 is shown in Figure 6-499 and described in Table 6-1000.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-999. CTRLMMR_PADCONFIG96 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C180h	0011 E180h

Figure 6-499. CTRLMMR_PADCONFIG96 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1000. CTRLMMR_PADCONFIG96 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1000. CTRLMMR_PADCONFIG96 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1000. CTRLMMR_PADCONFIG96 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.500 CTRLMMR_PADCONFIG97 Register (Proxy0 Offset = 1C184h; Proxy1 Offset = 1E184h) [reset = 8214007h]

CTRLMMR_PADCONFIG97 is shown in Figure 6-500 and described in Table 6-1002.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1001. CTRLMMR_PADCONFIG97 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C184h	0011 E184h

Figure 6-500. CTRLMMR_PADCONFIG97 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1002. CTRLMMR_PADCONFIG97 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1002. CTRLMMR_PADCONFIG97 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1002. CTRLMMR_PADCONFIG97 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.501 CTRLMMR_PADCONFIG98 Register (Proxy0 Offset = 1C188h; Proxy1 Offset = 1E188h) [reset = 8214007h]

CTRLMMR_PADCONFIG98 is shown in Figure 6-501 and described in Table 6-1004.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1003. CTRLMMR_PADCONFIG98 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C188h	0011 E188h

Figure 6-501. CTRLMMR_PADCONFIG98 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1004. CTRLMMR_PADCONFIG98 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1004. CTRLMMR_PADCONFIG98 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1004. CTRLMMR_PADCONFIG98 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.502 CTRLMMR_PADCONFIG99 Register (Proxy0 Offset = 1C18Ch; Proxy1 Offset = 1E18Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG99 is shown in Figure 6-502 and described in Table 6-1006.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1005. CTRLMMR_PADCONFIG99 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C18Ch	0011 E18Ch

Figure 6-502. CTRLMMR_PADCONFIG99 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1006. CTRLMMR_PADCONFIG99 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1006. CTRLMMR_PADCONFIG99 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1006. CTRLMMR_PADCONFIG99 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.503 CTRLMMR_PADCONFIG100 Register (Proxy0 Offset = 1C190h; Proxy1 Offset = 1E190h) [reset = 8214007h]

CTRLMMR_PADCONFIG100 is shown in Figure 6-503 and described in Table 6-1008.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1007. CTRLMMR_PADCONFIG100 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C190h	0011 E190h

Figure 6-503. CTRLMMR_PADCONFIG100 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1008. CTRLMMR_PADCONFIG100 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1008. CTRLMMR_PADCONFIG100 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1008. CTRLMMR_PADCONFIG100 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.504 CTRLMMR_PADCONFIG101 Register (Proxy0 Offset = 1C194h; Proxy1 Offset = 1E194h) [reset = 8214007h]

CTRLMMR_PADCONFIG101 is shown in Figure 6-504 and described in Table 6-1010.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1009. CTRLMMR_PADCONFIG101 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C194h	0011 E194h

Figure 6-504. CTRLMMR_PADCONFIG101 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1010. CTRLMMR_PADCONFIG101 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1010. CTRLMMR_PADCONFIG101 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1010. CTRLMMR_PADCONFIG101 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.505 CTRLMMR_PADCONFIG102 Register (Proxy0 Offset = 1C198h; Proxy1 Offset = 1E198h) [reset = 8214007h]

CTRLMMR_PADCONFIG102 is shown in Figure 6-505 and described in Table 6-1012.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1011. CTRLMMR_PADCONFIG102 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C198h	0011 E198h

Figure 6-505. CTRLMMR_PADCONFIG102 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1012. CTRLMMR_PADCONFIG102 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1012. CTRLMMR_PADCONFIG102 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1012. CTRLMMR_PADCONFIG102 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.506 CTRLMMR_PADCONFIG103 Register (Proxy0 Offset = 1C19Ch; Proxy1 Offset = 1E19Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG103 is shown in Figure 6-506 and described in Table 6-1014.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1013. CTRLMMR_PADCONFIG103 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C19Ch	0011 E19Ch

Figure 6-506. CTRLMMR_PADCONFIG103 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1014. CTRLMMR_PADCONFIG103 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1014. CTRLMMR_PADCONFIG103 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1014. CTRLMMR_PADCONFIG103 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.507 CTRLMMR_PADCONFIG104 Register (Proxy0 Offset = 1C1A0h; Proxy1 Offset = 1E1A0h) [reset = 8214007h]

CTRLMMR_PADCONFIG104 is shown in Figure 6-507 and described in Table 6-1016.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1015. CTRLMMR_PADCONFIG104 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1A0h	0011 E1A0h

Figure 6-507. CTRLMMR_PADCONFIG104 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1016. CTRLMMR_PADCONFIG104 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1016. CTRLMMR_PADCONFIG104 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1016. CTRLMMR_PADCONFIG104 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.508 CTRLMMR_PADCONFIG105 Register (Proxy0 Offset = 1C1A4h; Proxy1 Offset = 1E1A4h) [reset = 8214007h]

CTRLMMR_PADCONFIG105 is shown in Figure 6-508 and described in Table 6-1018.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1017. CTRLMMR_PADCONFIG105 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1A4h	0011 E1A4h

Figure 6-508. CTRLMMR_PADCONFIG105 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1018. CTRLMMR_PADCONFIG105 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1018. CTRLMMR_PADCONFIG105 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1018. CTRLMMR_PADCONFIG105 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.509 CTRLMMR_PADCONFIG106 Register (Proxy0 Offset = 1C1A8h; Proxy1 Offset = 1E1A8h) [reset = 8214007h]

CTRLMMR_PADCONFIG106 is shown in Figure 6-509 and described in Table 6-1020.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1019. CTRLMMR_PADCONFIG106 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1A8h	0011 E1A8h

Figure 6-509. CTRLMMR_PADCONFIG106 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1020. CTRLMMR_PADCONFIG106 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1020. CTRLMMR_PADCONFIG106 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1020. CTRLMMR_PADCONFIG106 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.510 CTRLMMR_PADCONFIG107 Register (Proxy0 Offset = 1C1ACh; Proxy1 Offset = 1E1ACh) [reset = 8214007h]

CTRLMMR_PADCONFIG107 is shown in Figure 6-510 and described in Table 6-1022.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1021. CTRLMMR_PADCONFIG107 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1ACh	0011 E1ACh

Figure 6-510. CTRLMMR_PADCONFIG107 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1022. CTRLMMR_PADCONFIG107 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1022. CTRLMMR_PADCONFIG107 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1022. CTRLMMR_PADCONFIG107 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.511 CTRLMMR_PADCONFIG108 Register (Proxy0 Offset = 1C1B0h; Proxy1 Offset = 1E1B0h) [reset = 8214007h]

CTRLMMR_PADCONFIG108 is shown in Figure 6-511 and described in Table 6-1024.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1023. CTRLMMR_PADCONFIG108 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1B0h	0011 E1B0h

Figure 6-511. CTRLMMR_PADCONFIG108 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1024. CTRLMMR_PADCONFIG108 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1024. CTRLMMR_PADCONFIG108 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1024. CTRLMMR_PADCONFIG108 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.512 CTRLMMR_PADCONFIG109 Register (Proxy0 Offset = 1C1B4h; Proxy1 Offset = 1E1B4h) [reset = 8214007h]

CTRLMMR_PADCONFIG109 is shown in Figure 6-512 and described in Table 6-1026.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1025. CTRLMMR_PADCONFIG109 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1B4h	0011 E1B4h

Figure 6-512. CTRLMMR_PADCONFIG109 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1026. CTRLMMR_PADCONFIG109 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1026. CTRLMMR_PADCONFIG109 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1026. CTRLMMR_PADCONFIG109 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.513 CTRLMMR_PADCONFIG110 Register (Proxy0 Offset = 1C1B8h; Proxy1 Offset = 1E1B8h) [reset = 8214007h]

CTRLMMR_PADCONFIG110 is shown in Figure 6-513 and described in Table 6-1028.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1027. CTRLMMR_PADCONFIG110 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1B8h	0011 E1B8h

Figure 6-513. CTRLMMR_PADCONFIG110 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1028. CTRLMMR_PADCONFIG110 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1028. CTRLMMR_PADCONFIG110 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1028. CTRLMMR_PADCONFIG110 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.514 CTRLMMR_PADCONFIG111 Register (Proxy0 Offset = 1C1BCh; Proxy1 Offset = 1E1BCh) [reset = 8214007h]

CTRLMMR_PADCONFIG111 is shown in Figure 6-514 and described in Table 6-1030.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1029. CTRLMMR_PADCONFIG111 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1BCh	0011 E1BCh

Figure 6-514. CTRLMMR_PADCONFIG111 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1030. CTRLMMR_PADCONFIG111 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1030. CTRLMMR_PADCONFIG111 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1030. CTRLMMR_PADCONFIG111 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.515 CTRLMMR_PADCONFIG112 Register (Proxy0 Offset = 1C1C0h; Proxy1 Offset = 1E1C0h) [reset = 8214007h]

CTRLMMR_PADCONFIG112 is shown in Figure 6-515 and described in Table 6-1032.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1031. CTRLMMR_PADCONFIG112 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1C0h	0011 E1C0h

Figure 6-515. CTRLMMR_PADCONFIG112 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1032. CTRLMMR_PADCONFIG112 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1032. CTRLMMR_PADCONFIG112 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1032. CTRLMMR_PADCONFIG112 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.516 CTRLMMR_PADCONFIG113 Register (Proxy0 Offset = 1C1C4h; Proxy1 Offset = 1E1C4h) [reset = 8214007h]

CTRLMMR_PADCONFIG113 is shown in Figure 6-516 and described in Table 6-1034.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1033. CTRLMMR_PADCONFIG113 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1C4h	0011 E1C4h

Figure 6-516. CTRLMMR_PADCONFIG113 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1034. CTRLMMR_PADCONFIG113 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1034. CTRLMMR_PADCONFIG113 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1034. CTRLMMR_PADCONFIG113 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.517 CTRLMMR_PADCONFIG114 Register (Proxy0 Offset = 1C1C8h; Proxy1 Offset = 1E1C8h) [reset = 8214007h]

CTRLMMR_PADCONFIG114 is shown in Figure 6-517 and described in Table 6-1036.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1035. CTRLMMR_PADCONFIG114 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1C8h	0011 E1C8h

Figure 6-517. CTRLMMR_PADCONFIG114 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1036. CTRLMMR_PADCONFIG114 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1036. CTRLMMR_PADCONFIG114 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1036. CTRLMMR_PADCONFIG114 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.518 CTRLMMR_PADCONFIG115 Register (Proxy0 Offset = 1C1CCh; Proxy1 Offset = 1E1CCh) [reset = 8214007h]

CTRLMMR_PADCONFIG115 is shown in Figure 6-518 and described in Table 6-1038.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1037. CTRLMMR_PADCONFIG115 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1CCh	0011 E1CCh

Figure 6-518. CTRLMMR_PADCONFIG115 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1038. CTRLMMR_PADCONFIG115 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1038. CTRLMMR_PADCONFIG115 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1038. CTRLMMR_PADCONFIG115 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.519 CTRLMMR_PADCONFIG116 Register (Proxy0 Offset = 1C1D0h; Proxy1 Offset = 1E1D0h) [reset = 8214007h]

CTRLMMR_PADCONFIG116 is shown in Figure 6-519 and described in Table 6-1040.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1039. CTRLMMR_PADCONFIG116 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1D0h	0011 E1D0h

Figure 6-519. CTRLMMR_PADCONFIG116 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1040. CTRLMMR_PADCONFIG116 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1040. CTRLMMR_PADCONFIG116 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1040. CTRLMMR_PADCONFIG116 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.520 CTRLMMR_PADCONFIG117 Register (Proxy0 Offset = 1C1D4h; Proxy1 Offset = 1E1D4h) [reset = 8214007h]

CTRLMMR_PADCONFIG117 is shown in Figure 6-520 and described in Table 6-1042.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1041. CTRLMMR_PADCONFIG117 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1D4h	0011 E1D4h

Figure 6-520. CTRLMMR_PADCONFIG117 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1042. CTRLMMR_PADCONFIG117 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1042. CTRLMMR_PADCONFIG117 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1042. CTRLMMR_PADCONFIG117 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.521 CTRLMMR_PADCONFIG118 Register (Proxy0 Offset = 1C1D8h; Proxy1 Offset = 1E1D8h) [reset = 8214007h]

CTRLMMR_PADCONFIG118 is shown in Figure 6-521 and described in Table 6-1044.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1043. CTRLMMR_PADCONFIG118 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1D8h	0011 E1D8h

Figure 6-521. CTRLMMR_PADCONFIG118 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1044. CTRLMMR_PADCONFIG118 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1044. CTRLMMR_PADCONFIG118 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1044. CTRLMMR_PADCONFIG118 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.522 CTRLMMR_PADCONFIG119 Register (Proxy0 Offset = 1C1DCh; Proxy1 Offset = 1E1DCh) [reset = 8214007h]

CTRLMMR_PADCONFIG119 is shown in Figure 6-522 and described in Table 6-1046.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1045. CTRLMMR_PADCONFIG119 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1DCh	0011 E1DCh

Figure 6-522. CTRLMMR_PADCONFIG119 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1046. CTRLMMR_PADCONFIG119 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1046. CTRLMMR_PADCONFIG119 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1046. CTRLMMR_PADCONFIG119 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.523 CTRLMMR_PADCONFIG120 Register (Proxy0 Offset = 1C1E0h; Proxy1 Offset = 1E1E0h) [reset = 8214007h]

CTRLMMR_PADCONFIG120 is shown in Figure 6-523 and described in Table 6-1048.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1047. CTRLMMR_PADCONFIG120 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1E0h	0011 E1E0h

Figure 6-523. CTRLMMR_PADCONFIG120 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1048. CTRLMMR_PADCONFIG120 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1048. CTRLMMR_PADCONFIG120 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1048. CTRLMMR_PADCONFIG120 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.524 CTRLMMR_PADCONFIG121 Register (Proxy0 Offset = 1C1E4h; Proxy1 Offset = 1E1E4h) [reset = 8214007h]

CTRLMMR_PADCONFIG121 is shown in Figure 6-524 and described in Table 6-1050.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1049. CTRLMMR_PADCONFIG121 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1E4h	0011 E1E4h

Figure 6-524. CTRLMMR_PADCONFIG121 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1050. CTRLMMR_PADCONFIG121 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1050. CTRLMMR_PADCONFIG121 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1050. CTRLMMR_PADCONFIG121 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.525 CTRLMMR_PADCONFIG122 Register (Proxy0 Offset = 1C1E8h; Proxy1 Offset = 1E1E8h) [reset = 8214007h]

CTRLMMR_PADCONFIG122 is shown in Figure 6-525 and described in Table 6-1052.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1051. CTRLMMR_PADCONFIG122 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1E8h	0011 E1E8h

Figure 6-525. CTRLMMR_PADCONFIG122 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1052. CTRLMMR_PADCONFIG122 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1052. CTRLMMR_PADCONFIG122 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1052. CTRLMMR_PADCONFIG122 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.526 CTRLMMR_PADCONFIG123 Register (Proxy0 Offset = 1C1ECh; Proxy1 Offset = 1E1ECh) [reset = 8214007h]

CTRLMMR_PADCONFIG123 is shown in Figure 6-526 and described in Table 6-1054.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1053. CTRLMMR_PADCONFIG123 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1ECh	0011 E1ECh

Figure 6-526. CTRLMMR_PADCONFIG123 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1054. CTRLMMR_PADCONFIG123 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1054. CTRLMMR_PADCONFIG123 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1054. CTRLMMR_PADCONFIG123 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.527 CTRLMMR_PADCONFIG124 Register (Proxy0 Offset = 1C1F0h; Proxy1 Offset = 1E1F0h) [reset = 8214007h]

CTRLMMR_PADCONFIG124 is shown in Figure 6-527 and described in Table 6-1056.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1055. CTRLMMR_PADCONFIG124 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1F0h	0011 E1F0h

Figure 6-527. CTRLMMR_PADCONFIG124 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1056. CTRLMMR_PADCONFIG124 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1056. CTRLMMR_PADCONFIG124 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1056. CTRLMMR_PADCONFIG124 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.528 CTRLMMR_PADCONFIG125 Register (Proxy0 Offset = 1C1F4h; Proxy1 Offset = 1E1F4h) [reset = 8214007h]

CTRLMMR_PADCONFIG125 is shown in Figure 6-528 and described in Table 6-1058.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1057. CTRLMMR_PADCONFIG125 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1F4h	0011 E1F4h

Figure 6-528. CTRLMMR_PADCONFIG125 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1058. CTRLMMR_PADCONFIG125 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1058. CTRLMMR_PADCONFIG125 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1058. CTRLMMR_PADCONFIG125 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.529 CTRLMMR_PADCONFIG126 Register (Proxy0 Offset = 1C1F8h; Proxy1 Offset = 1E1F8h) [reset = 8214007h]

CTRLMMR_PADCONFIG126 is shown in Figure 6-529 and described in Table 6-1060.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1059. CTRLMMR_PADCONFIG126 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1F8h	0011 E1F8h

Figure 6-529. CTRLMMR_PADCONFIG126 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1060. CTRLMMR_PADCONFIG126 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1060. CTRLMMR_PADCONFIG126 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1060. CTRLMMR_PADCONFIG126 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.530 CTRLMMR_PADCONFIG127 Register (Proxy0 Offset = 1C1FCh; Proxy1 Offset = 1E1FCh) [reset = 8214007h]

CTRLMMR_PADCONFIG127 is shown in Figure 6-530 and described in Table 6-1062.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1061. CTRLMMR_PADCONFIG127 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C1FCh	0011 E1FCh

Figure 6-530. CTRLMMR_PADCONFIG127 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1062. CTRLMMR_PADCONFIG127 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1062. CTRLMMR_PADCONFIG127 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1062. CTRLMMR_PADCONFIG127 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.531 CTRLMMR_PADCONFIG128 Register (Proxy0 Offset = 1C200h; Proxy1 Offset = 1E200h) [reset = 8214007h]

CTRLMMR_PADCONFIG128 is shown in Figure 6-531 and described in Table 6-1064.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1063. CTRLMMR_PADCONFIG128 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C200h	0011 E200h

Figure 6-531. CTRLMMR_PADCONFIG128 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1064. CTRLMMR_PADCONFIG128 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1064. CTRLMMR_PADCONFIG128 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1064. CTRLMMR_PADCONFIG128 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.532 CTRLMMR_PADCONFIG129 Register (Proxy0 Offset = 1C204h; Proxy1 Offset = 1E204h) [reset = 8214007h]

CTRLMMR_PADCONFIG129 is shown in Figure 6-532 and described in Table 6-1066.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1065. CTRLMMR_PADCONFIG129 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C204h	0011 E204h

Figure 6-532. CTRLMMR_PADCONFIG129 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1066. CTRLMMR_PADCONFIG129 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1066. CTRLMMR_PADCONFIG129 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1066. CTRLMMR_PADCONFIG129 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.533 CTRLMMR_PADCONFIG130 Register (Proxy0 Offset = 1C208h; Proxy1 Offset = 1E208h) [reset = 8214007h]

CTRLMMR_PADCONFIG130 is shown in Figure 6-533 and described in Table 6-1068.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1067. CTRLMMR_PADCONFIG130 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C208h	0011 E208h

Figure 6-533. CTRLMMR_PADCONFIG130 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1068. CTRLMMR_PADCONFIG130 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1068. CTRLMMR_PADCONFIG130 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1068. CTRLMMR_PADCONFIG130 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.534 CTRLMMR_PADCONFIG131 Register (Proxy0 Offset = 1C20Ch; Proxy1 Offset = 1E20Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG131 is shown in Figure 6-534 and described in Table 6-1070.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1069. CTRLMMR_PADCONFIG131 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C20Ch	0011 E20Ch

Figure 6-534. CTRLMMR_PADCONFIG131 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1070. CTRLMMR_PADCONFIG131 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1070. CTRLMMR_PADCONFIG131 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1070. CTRLMMR_PADCONFIG131 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.535 CTRLMMR_PADCONFIG132 Register (Proxy0 Offset = 1C210h; Proxy1 Offset = 1E210h) [reset = 8214007h]

CTRLMMR_PADCONFIG132 is shown in Figure 6-535 and described in Table 6-1072.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1071. CTRLMMR_PADCONFIG132 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C210h	0011 E210h

Figure 6-535. CTRLMMR_PADCONFIG132 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1072. CTRLMMR_PADCONFIG132 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1072. CTRLMMR_PADCONFIG132 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1072. CTRLMMR_PADCONFIG132 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.536 CTRLMMR_PADCONFIG133 Register (Proxy0 Offset = 1C214h; Proxy1 Offset = 1E214h) [reset = 8214007h]

CTRLMMR_PADCONFIG133 is shown in Figure 6-536 and described in Table 6-1074.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1073. CTRLMMR_PADCONFIG133 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C214h	0011 E214h

Figure 6-536. CTRLMMR_PADCONFIG133 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1074. CTRLMMR_PADCONFIG133 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1074. CTRLMMR_PADCONFIG133 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1074. CTRLMMR_PADCONFIG133 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.537 CTRLMMR_PADCONFIG134 Register (Proxy0 Offset = 1C218h; Proxy1 Offset = 1E218h) [reset = 8214007h]

CTRLMMR_PADCONFIG134 is shown in Figure 6-537 and described in Table 6-1076.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1075. CTRLMMR_PADCONFIG134 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C218h	0011 E218h

Figure 6-537. CTRLMMR_PADCONFIG134 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1076. CTRLMMR_PADCONFIG134 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1076. CTRLMMR_PADCONFIG134 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1076. CTRLMMR_PADCONFIG134 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.538 CTRLMMR_PADCONFIG135 Register (Proxy0 Offset = 1C21Ch; Proxy1 Offset = 1E21Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG135 is shown in Figure 6-538 and described in Table 6-1078.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1077. CTRLMMR_PADCONFIG135 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C21Ch	0011 E21Ch

Figure 6-538. CTRLMMR_PADCONFIG135 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1078. CTRLMMR_PADCONFIG135 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1078. CTRLMMR_PADCONFIG135 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1078. CTRLMMR_PADCONFIG135 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.539 CTRLMMR_PADCONFIG136 Register (Proxy0 Offset = 1C220h; Proxy1 Offset = 1E220h) [reset = 44007h]

CTRLMMR_PADCONFIG136 is shown in Figure 6-539 and described in Table 6-1080.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1079. CTRLMMR_PADCONFIG136 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C220h	0011 E220h

Figure 6-539. CTRLMMR_PADCONFIG136 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	RESERVED		DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R-0h	

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1080. CTRLMMR_PADCONFIG136 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28-27	RESERVED	R	0h	Reserved
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active

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Table 6-1080. CTRLMMR_PADCONFIG136 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17-16	RESERVED	R	0h	Reserved
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.540 CTRLMMR_PADCONFIG137 Register (Proxy0 Offset = 1C224h; Proxy1 Offset = 1E224h) [reset = 44007h]

CTRLMMR_PADCONFIG137 is shown in Figure 6-540 and described in Table 6-1082.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1081. CTRLMMR_PADCONFIG137 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C224h	0011 E224h

Figure 6-540. CTRLMMR_PADCONFIG137 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	RESERVED		DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R-0h	

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1082. CTRLMMR_PADCONFIG137 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28-27	RESERVED	R	0h	Reserved
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active

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Table 6-1082. CTRLMMR_PADCONFIG137 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17-16	RESERVED	R	0h	Reserved
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.541 CTRLMMR_PADCONFIG138 Register (Proxy0 Offset = 1C228h; Proxy1 Offset = 1E228h) [reset = 44007h]

CTRLMMR_PADCONFIG138 is shown in Figure 6-541 and described in Table 6-1084.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1083. CTRLMMR_PADCONFIG138 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C228h	0011 E228h

Figure 6-541. CTRLMMR_PADCONFIG138 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	RESERVED		DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R-0h	

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1084. CTRLMMR_PADCONFIG138 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28-27	RESERVED	R	0h	Reserved
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active

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Table 6-1084. CTRLMMR_PADCONFIG138 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17-16	RESERVED	R	0h	Reserved
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.542 CTRLMMR_PADCONFIG139 Register (Proxy0 Offset = 1C22Ch; Proxy1 Offset = 1E22Ch) [reset = 44007h]

CTRLMMR_PADCONFIG139 is shown in Figure 6-542 and described in Table 6-1086.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1085. CTRLMMR_PADCONFIG139 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C22Ch	0011 E22Ch

Figure 6-542. CTRLMMR_PADCONFIG139 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	RESERVED		DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R-0h		R/W-0h	R/W-0h	R/W-0h

23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	RESERVED	
R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-1h	R-0h	

15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1086. CTRLMMR_PADCONFIG139 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28-27	RESERVED	R	0h	Reserved
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active

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Table 6-1086. CTRLMMR_PADCONFIG139 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17-16	RESERVED	R	0h	Reserved
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.543 CTRLMMR_PADCONFIG140 Register (Proxy0 Offset = 1C230h; Proxy1 Offset = 1E230h) [reset = 8214007h]

CTRLMMR_PADCONFIG140 is shown in Figure 6-543 and described in Table 6-1088.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1087. CTRLMMR_PADCONFIG140 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C230h	0011 E230h

Figure 6-543. CTRLMMR_PADCONFIG140 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1088. CTRLMMR_PADCONFIG140 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1088. CTRLMMR_PADCONFIG140 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1088. CTRLMMR_PADCONFIG140 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.544 CTRLMMR_PADCONFIG141 Register (Proxy0 Offset = 1C234h; Proxy1 Offset = 1E234h) [reset = 8214007h]

CTRLMMR_PADCONFIG141 is shown in Figure 6-544 and described in Table 6-1090.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1089. CTRLMMR_PADCONFIG141 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C234h	0011 E234h

Figure 6-544. CTRLMMR_PADCONFIG141 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1090. CTRLMMR_PADCONFIG141 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1090. CTRLMMR_PADCONFIG141 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1090. CTRLMMR_PADCONFIG141 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.545 CTRLMMR_PADCONFIG142 Register (Proxy0 Offset = 1C238h; Proxy1 Offset = 1E238h) [reset = 8254007h]

CTRLMMR_PADCONFIG142 is shown in Figure 6-545 and described in Table 6-1092.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1091. CTRLMMR_PADCONFIG142 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C238h	0011 E238h

Figure 6-545. CTRLMMR_PADCONFIG142 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1092. CTRLMMR_PADCONFIG142 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1092. CTRLMMR_PADCONFIG142 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1092. CTRLMMR_PADCONFIG142 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.546 CTRLMMR_PADCONFIG143 Register (Proxy0 Offset = 1C23Ch; Proxy1 Offset = 1E23Ch) [reset = 8254007h]

CTRLMMR_PADCONFIG143 is shown in Figure 6-546 and described in Table 6-1094.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1093. CTRLMMR_PADCONFIG143 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C23Ch	0011 E23Ch

Figure 6-546. CTRLMMR_PADCONFIG143 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1094. CTRLMMR_PADCONFIG143 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1094. CTRLMMR_PADCONFIG143 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1094. CTRLMMR_PADCONFIG143 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.547 CTRLMMR_PADCONFIG144 Register (Proxy0 Offset = 1C240h; Proxy1 Offset = 1E240h) [reset = 8214007h]

CTRLMMR_PADCONFIG144 is shown in Figure 6-547 and described in Table 6-1096.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1095. CTRLMMR_PADCONFIG144 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C240h	0011 E240h

Figure 6-547. CTRLMMR_PADCONFIG144 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1096. CTRLMMR_PADCONFIG144 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1096. CTRLMMR_PADCONFIG144 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1096. CTRLMMR_PADCONFIG144 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.548 CTRLMMR_PADCONFIG145 Register (Proxy0 Offset = 1C244h; Proxy1 Offset = 1E244h) [reset = 8214007h]

CTRLMMR_PADCONFIG145 is shown in Figure 6-548 and described in Table 6-1098.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1097. CTRLMMR_PADCONFIG145 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C244h	0011 E244h

Figure 6-548. CTRLMMR_PADCONFIG145 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1098. CTRLMMR_PADCONFIG145 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1098. CTRLMMR_PADCONFIG145 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1098. CTRLMMR_PADCONFIG145 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.549 CTRLMMR_PADCONFIG146 Register (Proxy0 Offset = 1C248h; Proxy1 Offset = 1E248h) [reset = 8214007h]

CTRLMMR_PADCONFIG146 is shown in Figure 6-549 and described in Table 6-1100.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1099. CTRLMMR_PADCONFIG146 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C248h	0011 E248h

Figure 6-549. CTRLMMR_PADCONFIG146 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1100. CTRLMMR_PADCONFIG146 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1100. CTRLMMR_PADCONFIG146 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1100. CTRLMMR_PADCONFIG146 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.550 CTRLMMR_PADCONFIG147 Register (Proxy0 Offset = 1C24Ch; Proxy1 Offset = 1E24Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG147 is shown in Figure 6-550 and described in Table 6-1102.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1101. CTRLMMR_PADCONFIG147 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C24Ch	0011 E24Ch

Figure 6-550. CTRLMMR_PADCONFIG147 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1102. CTRLMMR_PADCONFIG147 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1102. CTRLMMR_PADCONFIG147 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1102. CTRLMMR_PADCONFIG147 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.551 CTRLMMR_PADCONFIG148 Register (Proxy0 Offset = 1C250h; Proxy1 Offset = 1E250h) [reset = 8214007h]

CTRLMMR_PADCONFIG148 is shown in Figure 6-551 and described in Table 6-1104.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1103. CTRLMMR_PADCONFIG148 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C250h	0011 E250h

Figure 6-551. CTRLMMR_PADCONFIG148 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1104. CTRLMMR_PADCONFIG148 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1104. CTRLMMR_PADCONFIG148 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1104. CTRLMMR_PADCONFIG148 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.552 CTRLMMR_PADCONFIG149 Register (Proxy0 Offset = 1C254h; Proxy1 Offset = 1E254h) [reset = 8214007h]

CTRLMMR_PADCONFIG149 is shown in Figure 6-552 and described in Table 6-1106.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1105. CTRLMMR_PADCONFIG149 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C254h	0011 E254h

Figure 6-552. CTRLMMR_PADCONFIG149 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1106. CTRLMMR_PADCONFIG149 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1106. CTRLMMR_PADCONFIG149 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1106. CTRLMMR_PADCONFIG149 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.553 CTRLMMR_PADCONFIG150 Register (Proxy0 Offset = 1C258h; Proxy1 Offset = 1E258h) [reset = 8214007h]

CTRLMMR_PADCONFIG150 is shown in Figure 6-553 and described in Table 6-1108.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1107. CTRLMMR_PADCONFIG150 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C258h	0011 E258h

Figure 6-553. CTRLMMR_PADCONFIG150 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1108. CTRLMMR_PADCONFIG150 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1108. CTRLMMR_PADCONFIG150 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1108. CTRLMMR_PADCONFIG150 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.554 CTRLMMR_PADCONFIG151 Register (Proxy0 Offset = 1C25Ch; Proxy1 Offset = 1E25Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG151 is shown in Figure 6-554 and described in Table 6-1110.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1109. CTRLMMR_PADCONFIG151 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C25Ch	0011 E25Ch

Figure 6-554. CTRLMMR_PADCONFIG151 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1110. CTRLMMR_PADCONFIG151 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1110. CTRLMMR_PADCONFIG151 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1110. CTRLMMR_PADCONFIG151 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.555 CTRLMMR_PADCONFIG152 Register (Proxy0 Offset = 1C260h; Proxy1 Offset = 1E260h) [reset = 8214007h]

CTRLMMR_PADCONFIG152 is shown in Figure 6-555 and described in Table 6-1112.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1111. CTRLMMR_PADCONFIG152 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C260h	0011 E260h

Figure 6-555. CTRLMMR_PADCONFIG152 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1112. CTRLMMR_PADCONFIG152 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1112. CTRLMMR_PADCONFIG152 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1112. CTRLMMR_PADCONFIG152 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.556 CTRLMMR_PADCONFIG153 Register (Proxy0 Offset = 1C264h; Proxy1 Offset = 1E264h) [reset = 8214007h]

CTRLMMR_PADCONFIG153 is shown in Figure 6-556 and described in Table 6-1114.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1113. CTRLMMR_PADCONFIG153 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C264h	0011 E264h

Figure 6-556. CTRLMMR_PADCONFIG153 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1114. CTRLMMR_PADCONFIG153 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1114. CTRLMMR_PADCONFIG153 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1114. CTRLMMR_PADCONFIG153 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.557 CTRLMMR_PADCONFIG154 Register (Proxy0 Offset = 1C268h; Proxy1 Offset = 1E268h) [reset = 8214007h]

CTRLMMR_PADCONFIG154 is shown in Figure 6-557 and described in Table 6-1116.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1115. CTRLMMR_PADCONFIG154 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C268h	0011 E268h

Figure 6-557. CTRLMMR_PADCONFIG154 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1116. CTRLMMR_PADCONFIG154 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1116. CTRLMMR_PADCONFIG154 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1116. CTRLMMR_PADCONFIG154 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.558 CTRLMMR_PADCONFIG155 Register (Proxy0 Offset = 1C26Ch; Proxy1 Offset = 1E26Ch) [reset = 8214007h]

CTRLMMR_PADCONFIG155 is shown in Figure 6-558 and described in Table 6-1118.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1117. CTRLMMR_PADCONFIG155 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C26Ch	0011 E26Ch

Figure 6-558. CTRLMMR_PADCONFIG155 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1118. CTRLMMR_PADCONFIG155 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1118. CTRLMMR_PADCONFIG155 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1118. CTRLMMR_PADCONFIG155 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.559 CTRLMMR_PADCONFIG156 Register (Proxy0 Offset = 1C270h; Proxy1 Offset = 1E270h) [reset = 8214007h]

CTRLMMR_PADCONFIG156 is shown in Figure 6-559 and described in Table 6-1120.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1119. CTRLMMR_PADCONFIG156 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C270h	0011 E270h

Figure 6-559. CTRLMMR_PADCONFIG156 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1120. CTRLMMR_PADCONFIG156 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1120. CTRLMMR_PADCONFIG156 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1120. CTRLMMR_PADCONFIG156 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.560 CTRLMMR_PADCONFIG157 Register (Proxy0 Offset = 1C274h; Proxy1 Offset = 1E274h) [reset = 8214007h]

CTRLMMR_PADCONFIG157 is shown in Figure 6-560 and described in Table 6-1122.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1121. CTRLMMR_PADCONFIG157 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C274h	0011 E274h

Figure 6-560. CTRLMMR_PADCONFIG157 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1122. CTRLMMR_PADCONFIG157 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1122. CTRLMMR_PADCONFIG157 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1122. CTRLMMR_PADCONFIG157 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.561 CTRLMMR_PADCONFIG158 Register (Proxy0 Offset = 1C278h; Proxy1 Offset = 1E278h) [reset = 8014000h]

CTRLMMR_PADCONFIG158 is shown in Figure 6-561 and described in Table 6-1124.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1123. CTRLMMR_PADCONFIG158 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C278h	0011 E278h

Figure 6-561. CTRLMMR_PADCONFIG158 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1124. CTRLMMR_PADCONFIG158 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1124. CTRLMMR_PADCONFIG158 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1124. CTRLMMR_PADCONFIG158 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.562 CTRLMMR_PADCONFIG159 Register (Proxy0 Offset = 1C27Ch; Proxy1 Offset = 1E27Ch) [reset = 8014000h]

CTRLMMR_PADCONFIG159 is shown in Figure 6-562 and described in Table 6-1126.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1125. CTRLMMR_PADCONFIG159 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C27Ch	0011 E27Ch

Figure 6-562. CTRLMMR_PADCONFIG159 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1126. CTRLMMR_PADCONFIG159 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1126. CTRLMMR_PADCONFIG159 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1126. CTRLMMR_PADCONFIG159 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.563 CTRLMMR_PADCONFIG160 Register (Proxy0 Offset = 1C280h; Proxy1 Offset = 1E280h) [reset = 44000h]

CTRLMMR_PADCONFIG160 is shown in Figure 6-563 and described in Table 6-1128.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1127. CTRLMMR_PADCONFIG160 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C280h	0011 E280h

Figure 6-563. CTRLMMR_PADCONFIG160 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	22	21	20	19	18	17	16
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-1h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1128. CTRLMMR_PADCONFIG160 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1128. CTRLMMR_PADCONFIG160 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1128. CTRLMMR_PADCONFIG160 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.564 CTRLMMR_PADCONFIG161 Register (Proxy0 Offset = 1C284h; Proxy1 Offset = 1E284h) [reset = 10264000h]

CTRLMMR_PADCONFIG161 is shown in Figure 6-564 and described in Table 6-1130.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1129. CTRLMMR_PADCONFIG161 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C284h	0011 E284h

Figure 6-564. CTRLMMR_PADCONFIG161 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1130. CTRLMMR_PADCONFIG161 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	1h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1130. CTRLMMR_PADCONFIG161 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1130. CTRLMMR_PADCONFIG161 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.565 CTRLMMR_PADCONFIG162 Register (Proxy0 Offset = 1C288h; Proxy1 Offset = 1E288h) [reset = 10024000h]

CTRLMMR_PADCONFIG162 is shown in Figure 6-565 and described in Table 6-1132.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1131. CTRLMMR_PADCONFIG162 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C288h	0011 E288h

Figure 6-565. CTRLMMR_PADCONFIG162 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1132. CTRLMMR_PADCONFIG162 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	1h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1132. CTRLMMR_PADCONFIG162 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	0h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1132. CTRLMMR_PADCONFIG162 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.566 CTRLMMR_PADCONFIG163 Register (Proxy0 Offset = 1C28Ch; Proxy1 Offset = 1E28Ch) [reset = 10264000h]

CTRLMMR_PADCONFIG163 is shown in Figure 6-566 and described in Table 6-1134.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1133. CTRLMMR_PADCONFIG163 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C28Ch	0011 E28Ch

Figure 6-566. CTRLMMR_PADCONFIG163 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-1h	R/W-1h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1134. CTRLMMR_PADCONFIG163 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	1h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1134. CTRLMMR_PADCONFIG163 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	1h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	1h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1134. CTRLMMR_PADCONFIG163 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.567 CTRLMMR_PADCONFIG164 Register (Proxy0 Offset = 1C290h; Proxy1 Offset = 1E290h) [reset = 204007h]

CTRLMMR_PADCONFIG164 is shown in Figure 6-567 and described in Table 6-1136.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1135. CTRLMMR_PADCONFIG164 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C290h	0011 E290h

Figure 6-567. CTRLMMR_PADCONFIG164 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	DRV_STR		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R/W-0h		R/W-0h	R/W-0h	R/W-0h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-7h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1136. CTRLMMR_PADCONFIG164 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	0h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1136. CTRLMMR_PADCONFIG164 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	DRV_STR	R/W	0h	Drive Strength Control . Selects the drive strength value for LVCMOS pins. (Does not apply to other pin types)
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	0h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1136. CTRLMMR_PADCONFIG164 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	7h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.568 CTRLMMR_PADCONFIG165 Register (Proxy0 Offset = 1C294h; Proxy1 Offset = 1E294h) [reset = 0h]

CTRLMMR_PADCONFIG165 is shown in Figure 6-568 and described in Table 6-1138.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1137. CTRLMMR_PADCONFIG165 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C294h	0011 E294h

Figure 6-568. CTRLMMR_PADCONFIG165 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED	ST_EN	RESERVED					
R-0h	R/W-0h	R-0h					

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1138. CTRLMMR_PADCONFIG165 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	0h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1138. CTRLMMR_PADCONFIG165 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.569 CTRLMMR_PADCONFIG166 Register (Proxy0 Offset = 1C298h; Proxy1 Offset = 1E298h) [reset = 0h]

CTRLMMR_PADCONFIG166 is shown in Figure 6-569 and described in Table 6-1140.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1139. CTRLMMR_PADCONFIG166 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C298h	0011 E298h

Figure 6-569. CTRLMMR_PADCONFIG166 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED	ST_EN	RESERVED					
R-0h	R/W-0h	R-0h					

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1140. CTRLMMR_PADCONFIG166 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	0h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1140. CTRLMMR_PADCONFIG166 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.570 CTRLMMR_PADCONFIG167 Register (Proxy0 Offset = 1C29Ch; Proxy1 Offset = 1E29Ch) [reset = 0h]

CTRLMMR_PADCONFIG167 is shown in Figure 6-570 and described in Table 6-1142.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1141. CTRLMMR_PADCONFIG167 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C29Ch	0011 E29Ch

Figure 6-570. CTRLMMR_PADCONFIG167 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED	ST_EN	RESERVED					
R-0h	R/W-0h	R-0h					

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1142. CTRLMMR_PADCONFIG167 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	0h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1142. CTRLMMR_PADCONFIG167 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.571 CTRLMMR_PADCONFIG168 Register (Proxy0 Offset = 1C2A0h; Proxy1 Offset = 1E2A0h) [reset = 0h]

CTRLMMR_PADCONFIG168 is shown in Figure 6-571 and described in Table 6-1144.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1143. CTRLMMR_PADCONFIG168 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C2A0h	0011 E2A0h

Figure 6-571. CTRLMMR_PADCONFIG168 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED	ST_EN	RESERVED					
R-0h	R/W-0h	R-0h					

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1144. CTRLMMR_PADCONFIG168 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	0h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1144. CTRLMMR_PADCONFIG168 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.572 CTRLMMR_PADCONFIG169 Register (Proxy0 Offset = 1C2A4h; Proxy1 Offset = 1E2A4h) [reset = 0h]

CTRLMMR_PADCONFIG169 is shown in Figure 6-572 and described in Table 6-1146.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1145. CTRLMMR_PADCONFIG169 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C2A4h	0011 E2A4h

Figure 6-572. CTRLMMR_PADCONFIG169 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED	ST_EN	RESERVED					
R-0h	R/W-0h	R-0h					

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1146. CTRLMMR_PADCONFIG169 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	0h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1146. CTRLMMR_PADCONFIG169 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.573 CTRLMMR_PADCONFIG170 Register (Proxy0 Offset = 1C2A8h; Proxy1 Offset = 1E2A8h) [reset = 0h]

CTRLMMR_PADCONFIG170 is shown in Figure 6-573 and described in Table 6-1148.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1147. CTRLMMR_PADCONFIG170 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C2A8h	0011 E2A8h

Figure 6-573. CTRLMMR_PADCONFIG170 Register

31	30	29	28	27	26	25	24
LOCK	RESERVED						
R/W-0h	R-0h						

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
RESERVED	ST_EN	RESERVED					
R-0h	R/W-0h	R-0h					

7	6	5	4	3	2	1	0
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1148. CTRLMMR_PADCONFIG170 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30-15	RESERVED	R	0h	Reserved
14	ST_EN	R/W	0h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1148. CTRLMMR_PADCONFIG170 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.574 CTRLMMR_PADCONFIG171 Register (Proxy0 Offset = 1C2ACh; Proxy1 Offset = 1E2ACh) [reset = 8214000h]

CTRLMMR_PADCONFIG171 is shown in Figure 6-574 and described in Table 6-1150.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1149. CTRLMMR_PADCONFIG171 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C2ACh	0011 E2ACh

Figure 6-574. CTRLMMR_PADCONFIG171 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1150. CTRLMMR_PADCONFIG171 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1150. CTRLMMR_PADCONFIG171 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1150. CTRLMMR_PADCONFIG171 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.575 CTRLMMR_PADCONFIG172 Register (Proxy0 Offset = 1C2B0h; Proxy1 Offset = 1E2B0h) [reset = 8214000h]

CTRLMMR_PADCONFIG172 is shown in Figure 6-575 and described in Table 6-1152.

Return to Summary Table.

Register to control pin configuration and muxing.

Table 6-1151. CTRLMMR_PADCONFIG172 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 C2B0h	0011 E2B0h

Figure 6-575. CTRLMMR_PADCONFIG172 Register

31	30	29	28	27	26	25	24
LOCK	WKUP_EVT	WKUP_EN	DS_PULLTYPE_SEL	DS_PULLUD_EN	DSOUT_VAL	DSOUT_DIS	DS_EN
R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ISO_BYP	ISO_OVR	TX_DIS	RESERVED		RXACTIVE	PULLTYPESEL	PULLUDEN
R/W-0h	R/W-0h	R/W-1h	R-0h		R/W-0h	R/W-0h	R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FORCE_DS_EN	ST_EN	DEBOUNCE_SEL			RESERVED		
R/W-0h	R/W-1h	R/W-0h			R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		VGPIO_SEL		MUXMODE			
R-0h		R/W-0h		R/W-0h			

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1152. CTRLMMR_PADCONFIG172 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	LOCK	R/W	0h	Lock 0h - Padconfig register is unlocked 1h - Padconfig register is locked from further writes
30	WKUP_EVT	R	0h	Wakeup event status 0h - No wake event on pin 1h - Wake event occurred on pin
29	WKUP_EN	R/W	0h	Wakeup enable. Supported for I/O group CANUART. 0h - Wakeup operation disabled 1h - Wakeup operation enabled
28	DS_PULLTYPE_SEL	R/W	0h	Deep Sleep pull-up/down selection 0h - Offmode pulldown selected 1h - Offmode pullup selected
27	DS_PULLUD_EN	R/W	1h	Deep Sleep pull-up/down enable (active low) 0h - Pullup / pulldown is enabled 1h - Pullup / pulldown is disabled
26	DSOUT_VAL	R/W	0h	Deep Sleep output value 0h - Output value is 0 1h - Output value is 1

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Table 6-1152. CTRLMMR_PADCONFIG172 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
25	DSOUT_DIS	R/W	0h	Deep Sleep output disable 0h - Output enabled 1h - Output disabled
24	DS_EN	R/W	0h	Deep Sleep override control 0h - IO keeps its previous state when Deep Sleep mode is active 1h - IO state is forced to OFF mode value when Deep Sleep mode is active
23	ISO_BYP	R/W	0h	Isolation Bypass 0h - IO isolation is preserved 1h - IO isolation is bypassed
22	ISO_OVR	R/W	0h	Isolation Override 0h - IO isolation is preserved 1h - IO isolation is overridden
21	TX_DIS	R/W	1h	Driver Disable 0h - Driver is enabled 1h - Driver is disabled
20-19	RESERVED	R	0h	Reserved
18	RXACTIVE	R/W	0h	Input enable for the Pad 0h - Receiver disabled 1h - Receiver enabled
17	PULLTYPESEL	R/W	0h	Pad Pullup / Pulldown type selection 0h - Pulldown selected 1h - Pullup selected
16	PULLUDEN	R/W	1h	Pad Pullup / Pulldown enable. This is an active low signal. 0h - Pullup / Pulldown enabled 1h - Pullup / Pulldown disabled
15	FORCE_DS_EN	R/W	0h	Enable pad Deep Sleep controls by overriding DMSC gating 0h - Deep Sleep pad controls are gated by the DMSC 1h - Activate Deep Sleep pad controls (override DMSC gating logic)
14	ST_EN	R/W	1h	Receiver Schmitt Trigger enable 0h - Schmitt trigger input disabled 1h - Schmitt trigger input enabled
13-11	DEBOUNCE_SEL	R/W	0h	Selects the debouce period for the pad.
10-6	RESERVED	R	0h	Reserved
5-4	VGPIO_SEL	R/W	0h	Virtual MAIN_GPIO instance select. These bits select which instance of GPIO is used for this I/O pad. This allows protection between two different Processor virtual worlds. These bits have no effect if GPIO mode (muxmode=7) is not selected for the PAD. 0h - Implement GPIO in GPIO_0/1 instance 1h - Implement GPIO in GPIO_2/3 instance 2h - Implement GPIO in GPIO_4/5 instance 3h - Implement GPIO in GPIO_6/7 instance

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Table 6-1152. CTRLMMR_PADCONFIG172 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	MUXMODE	R/W	0h	Pad functional signal mux selection 0h - Mux Mode 0 1h - Mux Mode 1 2h - Mux Mode 2 3h - Mux Mode 3 4h - Mux Mode 4 5h - Mux Mode 5 6h - Mux Mode 6 7h - Mux Mode 7 8h - Mux Mode 8 9h - Mux Mode 9 Ah - Mux Mode 10 Bh - Mux Mode 11 Ch - Mux Mode 12 Dh - Mux Mode 13 Eh - Mux Mode 14 Fh - Mux Mode 15

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6.576 CTRLMMR_LOCK7_KICK0 Register (Proxy0 Offset = 1D008h; Proxy1 Offset = 1F008h) [reset = 0h]

CTRLMMR_LOCK7_KICK0 is shown in Figure 6-576 and described in Table 6-1154.

Return to Summary Table.

Lower 32-bits of Partition7 write lock key. This register must be written with the designated key value followed by a write to CTRLMMR_LOCK7_KICK1 with its key value before write-protected Partition 7 registers can be written.

Table 6-1153. CTRLMMR_LOCK7_KICK0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 D008h	0011 F008h

Figure 6-576. CTRLMMR_LOCK7_KICK0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 6-1154. CTRLMMR_LOCK7_KICK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition7 registers
0	UNLOCKED	R	0h	Unlock status. When set indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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6.577 CTRLMMR_LOCK7_KICK1 Register (Proxy0 Offset = 1D00Ch; Proxy1 Offset = 1F00Ch) [reset = 0h]

CTRLMMR_LOCK7_KICK1 is shown in Figure 6-577 and described in Table 6-1156.

Return to Summary Table.

Upper 32-bits of Partition 7 write lock key. This register must be written with the designated key value after a write to CTRLMMR_LOCK7_KICK0 with its key value before write-protected Partition 7 registers can be written.

Table 6-1155. CTRLMMR_LOCK7_KICK1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 D00Ch	0011 F00Ch

Figure 6-577. CTRLMMR_LOCK7_KICK1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-1156. CTRLMMR_LOCK7_KICK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	KEY	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition7 registers

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6.578 CTRLMMR_P7_CLAIM0 Register (Proxy0 Offset = 1D100h; Proxy1 Offset = 1F100h) [reset = 0h]

CTRLMMR_P7_CLAIM0 is shown in Figure 6-578 and described in Table 6-1158.

Return to Summary Table.

Claim bits for Partition7 Registers.

Table 6-1157. CTRLMMR_P7_CLAIM0 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 D100h	0011 F100h

Figure 6-578. CTRLMMR_P7_CLAIM0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-1158. CTRLMMR_P7_CLAIM0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x1C000 + (0 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x1E000 + (0 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.579 CTRLMMR_P7_CLAIM1 Register (Proxy0 Offset = 1D104h; Proxy1 Offset = 1F104h) [reset = 0h]

CTRLMMR_P7_CLAIM1 is shown in Figure 6-579 and described in Table 6-1160.

Return to Summary Table.

Claim bits for Partition7 Registers.

Table 6-1159. CTRLMMR_P7_CLAIM1 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 D104h	0011 F104h

Figure 6-579. CTRLMMR_P7_CLAIM1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-1160. CTRLMMR_P7_CLAIM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x1C000 + (1 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x1E000 + (1 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.580 CTRLMMR_P7_CLAIM2 Register (Proxy0 Offset = 1D108h; Proxy1 Offset = 1F108h) [reset = 0h]

CTRLMMR_P7_CLAIM2 is shown in Figure 6-580 and described in Table 6-1162.

Return to Summary Table.

Claim bits for Partition7 Registers.

Table 6-1161. CTRLMMR_P7_CLAIM2 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 D108h	0011 F108h

Figure 6-580. CTRLMMR_P7_CLAIM2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-1162. CTRLMMR_P7_CLAIM2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x1C000 + (2 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x1E000 + (2 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.581 CTRLMMR_P7_CLAIM3 Register (Proxy0 Offset = 1D10Ch; Proxy1 Offset = 1F10Ch) [reset = 0h]

CTRLMMR_P7_CLAIM3 is shown in Figure 6-581 and described in Table 6-1164.

Return to Summary Table.

Claim bits for Partition7 Registers.

Table 6-1163. CTRLMMR_P7_CLAIM3 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 D10Ch	0011 F10Ch

Figure 6-581. CTRLMMR_P7_CLAIM3 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 6-1164. CTRLMMR_P7_CLAIM3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x1C000 + (3 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x1E000 + (3 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.582 CTRLMMR_P7_CLAIM4 Register (Proxy0 Offset = 1D110h; Proxy1 Offset = 1F110h) [reset = 0h]

CTRLMMR_P7_CLAIM4 is shown in Figure 6-582 and described in Table 6-1166.

Return to Summary Table.

Claim bits for Partition7 Registers.

Table 6-1165. CTRLMMR_P7_CLAIM4 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 D110h	0011 F110h

Figure 6-582. CTRLMMR_P7_CLAIM4 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-1166. CTRLMMR_P7_CLAIM4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x1C000 + (4 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x1E000 + (4 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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6.583 CTRLMMR_P7_CLAIM5 Register (Proxy0 Offset = 1D114h; Proxy1 Offset = 1F114h) [reset = 0h]

CTRLMMR_P7_CLAIM5 is shown in Figure 6-583 and described in Table 6-1168.

Return to Summary Table.

Claim bits for Partition7 Registers.

Table 6-1167. CTRLMMR_P7_CLAIM5 Instances

Instance	Proxy0 Physical Address	Proxy1 Physical Address
CTRL_MMR0	0011 D114h	0011 F114h

Figure 6-583. CTRLMMR_P7_CLAIM5 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROXY1_CLAIMED																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 6-1168. CTRLMMR_P7_CLAIM5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PROXY1_CLAIMED	R/W	0h	Proxy1 register claim bit Bit position b corresponds to register Proxy0 address of: 0x1C000 + (5 x 0x80) + (b x 0x4) and register Proxy1 address of: 0x1E000 + (5 x 0x80) + (b x 0x4) Write 1 through Proxy1 address to claim the associated register. This will disable all write accesses through the Proxy0 address of the register. Write 0 through Proxy1 address to release the claim and allow Proxy0 writes of the associated register.

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7 SEC_MMR0_BOOT_CTRL Registers

Table 7-2 lists the memory-mapped registers for the SEC_MMR0_BOOT_CTRL. All register offset addresses not listed in Table 7-2 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. SEC_MMR0_BOOT_CTRL Instances

Instance	Base Address
SEC_MMR0_BOOT_CTRL	45A4 0000h

Table 7-2. SEC_MMR0_BOOT_CTRL Registers

Offset	Acronym	Register Name	SEC_MMR0_BOOT_CTRL Physical Address
20h	CTRLMMR_SEC_CLSTR0_DEF	Cluster0 Definition Register	45A4 0020h
40h	CTRLMMR_SEC_CLSTR0_CFG	Cluster0 Configuration Register	45A4 0040h
100h	CTRLMMR_SEC_CLSTR0_CORE0_CFG	Cluster0 Core0 Configuration Register	45A4 0100h
110h	CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_LO	Cluster0 Core0 Boot Vector Lo Register	45A4 0110h
114h	CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_HI	Cluster0 Core0 Boot Vector Hi Register	45A4 0114h
120h	CTRLMMR_SEC_CLSTR0_CORE0_PMCTRL	Cluster0 Core0 Power Management Control	45A4 0120h
130h	CTRLMMR_SEC_CLSTR0_CORE0_PMSTAT	Cluster0 Core0 Power Management Status Register	45A4 0130h
180h	CTRLMMR_SEC_CLSTR0_CORE1_CFG	Cluster0 Core1 Configuration Register 0	45A4 0180h
190h	CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_LO	Cluster0 Core1 Boot Vector Lo Register	45A4 0190h
194h	CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_HI	Cluster0 Core1 Boot Vector Hi Register	45A4 0194h
1A0h	CTRLMMR_SEC_CLSTR0_CORE1_PMCTRL	Cluster0 Core1 Power Management Control	45A4 01A0h
1B0h	CTRLMMR_SEC_CLSTR0_CORE1_PMSTAT	Cluster0 Core1 Power Management Status Register	45A4 01B0h
1020h	CTRLMMR_SEC_CLSTR1_DEF	Cluster1 Definition Register	45A4 1020h
1040h	CTRLMMR_SEC_CLSTR1_CFG	Cluster1 Configuration Register	45A4 1040h
1100h	CTRLMMR_SEC_CLSTR1_CORE0_CFG	Cluster1 Core0 Configuration Register	45A4 1100h
1110h	CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_LO	Cluster1 Core0 Boot Vector Lo Register	45A4 1110h
1114h	CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_HI	Cluster1 Core0 Boot Vector Hi Register	45A4 1114h
1120h	CTRLMMR_SEC_CLSTR1_CORE0_PMCTRL	Cluster1 Core0 Power Management Control	45A4 1120h
1130h	CTRLMMR_SEC_CLSTR1_CORE0_PMSTAT	Cluster1 Core0 Power Management Status Register	45A4 1130h
1180h	CTRLMMR_SEC_CLSTR1_CORE1_CFG	Cluster1 Core1 Configuration Register 0	45A4 1180h
1190h	CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_LO	Cluster1 Core1 Boot Vector Lo Register	45A4 1190h
1194h	CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_HI	Cluster1 Core1 Boot Vector Hi Register	45A4 1194h
11A0h	CTRLMMR_SEC_CLSTR1_CORE1_PMCTRL	Cluster1 Core1 Power Management Control	45A4 11A0h
11B0h	CTRLMMR_SEC_CLSTR1_CORE1_PMSTAT	Cluster1 Core1 Power Management Status Register	45A4 11B0h
2020h	CTRLMMR_SEC_CLSTR2_DEF	Cluster2 Definition Register	45A4 2020h

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Table 7-2. SEC_MMR0_BOOT_CTRL Registers (continued)

Offset	Acronym	Register Name	SEC_MMR0_BOOT_CTRL Physical Address
2040h	CTRLMMR_SEC_CLSTR2_CFG	Cluster2 Configuration Register	45A4 2040h
2100h	CTRLMMR_SEC_CLSTR2_CORE0_CFG	Cluster2 Core0 Configuration Register	45A4 2100h
2110h	CTRLMMR_SEC_CLSTR2_CORE0_BOOTVECT_LO	Cluster2 Core0 Boot Vector Lo Register	45A4 2110h
3020h	CTRLMMR_SEC_CLSTR3_DEF	Cluster3 Definition Register	45A4 3020h
3040h	CTRLMMR_SEC_CLSTR3_CFG	Cluster3 Configuration Register	45A4 3040h
3100h	CTRLMMR_SEC_CLSTR3_CORE0_CFG	Cluster3 Core0 Configuration Register	45A4 3100h
3110h	CTRLMMR_SEC_CLSTR3_CORE0_BOOTVECT_LO	Cluster3 Core0 Boot Vector Lo Register	45A4 3110h

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7.1 CTRLMMR_SEC_CLSTR0_DEF Register (Offset = 20h) [reset = 2FF10h]

CTRLMMR_SEC_CLSTR0_DEF is shown in Figure 7-1 and described in Table 7-4.

Return to Summary Table.

Defines the type of the processor cluster.

Table 7-3. CTRLMMR_SEC_CLSTR0_DEF Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 0020h

Figure 7-1. CTRLMMR_SEC_CLSTR0_DEF Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED					CORE_NUM		
R-0h					R-2h		
15	14	13	12	11	10	9	8
DSP_CORE_TYPE							
R-FFh							
7	6	5	4	3	2	1	0
ARM_CORE_TYPE							
R-10h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-4. CTRLMMR_SEC_CLSTR0_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	CORE_NUM	R	2h	Number of cores in cluster 1h - Single Core 2h - Dual Core 4h - Quad Core
15-8	DSP_CORE_TYPE	R	FFh	DSP core type configuration. Not shown values are reserved. 0h - C7x 1h - C6x FFh - Not DSP
7-0	ARM_CORE_TYPE	R	10h	ARM core type configuration. Not shown values are reserved. 0h - A53 1h - A57 10h - R5 FFh - Not ARM

Table 7-5. Register Call Summary for CTRLMMR_SEC_CLSTR0_DEF

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_DEF Register (Offset = 20h) [reset = 2FF10h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.2 CTRLMMR_SEC_CLSTR0_CFG Register (Offset = 40h) [reset = X]

CTRLMMR_SEC_CLSTR0_CFG is shown in Figure 7-2 and described in Table 7-7.

Return to Summary Table.

Configures cluster level characteristics.

Table 7-6. CTRLMMR_SEC_CLSTR0_CFG Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 0040h

Figure 7-2. CTRLMMR_SEC_CLSTR0_CFG Register

31	30	29	28	27	26	25	24
CLSTR_CFG_RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
CLSTR_CFG_RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
CLSTR_CFG_RSVD							
R/W-0h							
7	6	5	4	3	2	1	0
CLSTR_CFG_RSVD				LOCKSTEP_EN	DBG_NO_CLKSTOP	TEINIT	LOCKSTEP
R/W-0h				R-X	R/W-0h	R/W-0h	R/W-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-7. CTRLMMR_SEC_CLSTR0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	CLSTR_CFG_RSVD	R/W	0h	Reserved for future use. Write '0' to ensure compatibility with future devices.
3	LOCKSTEP_EN	R	X	Lockstep enable. Indicates if R5 lockstep operation is supported on the device
2	DBG_NO_CLKSTOP	R/W	0h	CPU clockstop behavior 0h - CPU clocks stopped and nCLOCKSTOPPED asserted in standby mode 1h - CPU clocks not stopped in standby mode
1	TEINIT	R/W	0h	Exception handling state at reset: 0h - ARM mode 1h - Thumb mode
0	LOCKSTEP	R/W	X	When set, Core0 and Core1 operate in lockstep mode. Can only be changed if lockstep operation is supported as indicated by CLSTR0_CFG_lockstep_en = 1. If CLSTR0_CFG_lockstep_en = 0, lockstep is not supported, this bit will be read only with a value of 0.

Table 7-8. Register Call Summary for CTRLMMR_SEC_CLSTR0_CFG

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CFG Register (Offset = 40h) [reset = X]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.3 CTRLMMR_SEC_CLSTR0_CORE0_CFG Register (Offset = 100h) [reset = 880h]

CTRLMMR_SEC_CLSTR0_CORE0_CFG is shown in Figure 7-3 and described in Table 7-10.

Return to Summary Table.

Configures the TCM and interrupt operation of R5 Core0.

Table 7-9. CTRLMMR_SEC_CLSTR0_CORE0_CFG Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 0100h

Figure 7-3. CTRLMMR_SEC_CLSTR0_CORE0_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
NMFI_EN	RESERVED			TCM_RSTBASE	RESERVED		
R/W-0h	R-0h			R/W-1h	R-0h		

7	6	5	4	3	2	1	0
BTCM_EN	RESERVED			ATCM_EN	RESERVED		
R/W-1h	R-0h			R/W-0h	R-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-10. CTRLMMR_SEC_CLSTR0_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NMFI_EN	R/W	0h	Enable Core0 Non-Maskable Fast Interrupts when set
14-12	RESERVED	R	0h	Reserved
11	TCM_RSTBASE	R/W	1h	Core0 A/BTCM Reset Base Address Indicator 0h - BTCM located at address 0x0 1h - ATCM located at address 0x0
10-8	RESERVED	R	0h	Reserved
7	BTCM_EN	R/W	1h	Enable Core0 BTCM RAM at reset when set
6-4	RESERVED	R	0h	Reserved
3	ATCM_EN	R/W	0h	Enable Core0 ATCM RAM at reset when set
2-0	RESERVED	R	0h	Reserved

Table 7-11. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE0_CFG

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE0_CFG Register (Offset = 100h) [reset = 880h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.4 CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_LO Register (Offset = 110h) [reset = 200h]

CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_LO is shown in Figure 7-4 and described in Table 7-13.

Return to Summary Table.

Contains the lower 32 bits of the boot vector location for R5 Core0. Bits 4:0 are not used and are always 0.

Table 7-12. CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_LO Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 0110h

Figure 7-4. CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VECT_ADDR																									RESERVED						
R/W-4h																									R-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-13. CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0.
6-0	RESERVED	R	0h	Reserved

Table 7-14. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_LO

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_LO Register (Offset = 110h) [reset = 200h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.5 CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_HI Register (Offset = 114h) [reset = 0h]

CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_HI is shown in Figure 7-5 and described in Table 7-16.

Return to Summary Table.

Contains the lower 16 bits of the boot vector location for R5 Core0.

Table 7-15. CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_HI Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 0114h

Figure 7-5. CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VECT_ADDR															
R-0h																R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-16. CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32].

Table 7-17. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_HI

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE0_BOOTVECT_HI Register (Offset = 114h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.6 CTRLMMR_SEC_CLSTR0_CORE0_PMCTRL Register (Offset = 120h) [reset = 0h]

CTRLMMR_SEC_CLSTR0_CORE0_PMCTRL is shown in Figure 7-6 and described in Table 7-19.

Return to Summary Table.

Configures Cluster Core0 power state.

Table 7-18. CTRLMMR_SEC_CLSTR0_CORE0_PMCTRL Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 0120h

Figure 7-6. CTRLMMR_SEC_CLSTR0_CORE0_PMCTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CORE_HALT
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-19. CTRLMMR_SEC_CLSTR0_CORE0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CORE_HALT	R/W	0h	Halt Core0. When 0, indicates that Core0 is in the Halt state.

Table 7-20. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE0_PMCTRL

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE0_PMCTRL Register (Offset = 120h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.7 CTRLMMR_SEC_CLSTR0_CORE0_PMSTAT Register (Offset = 130h) [reset = X]

CTRLMMR_SEC_CLSTR0_CORE0_PMSTAT is shown in Figure 7-7 and described in Table 7-22.

Return to Summary Table.

Shows Cluster Core0 power status.

Table 7-21. CTRLMMR_SEC_CLSTR0_CORE0_PMSTAT Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 0130h

Figure 7-7. CTRLMMR_SEC_CLSTR0_CORE0_PMSTAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CLK_GATE	RESERVED	WFE	WFI
R-0h				R-X	R-0h	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 7-22. CTRLMMR_SEC_CLSTR0_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CLK_GATE	R	X	Core0 Clock Stopped When 0, indicates clock stopped due to WFI or WFE state
2	RESERVED	R	0h	Reserved
1	WFE	R	X	Core0 WFE When 0, indicates that Core0 is in the WFE state
0	WFI	R	X	Core0 WFI When 0, indicates that Core0 is in the WFI state

Table 7-23. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE0_PMSTAT

SEC_MMR0_BOOT_CTRL Registers
- CTRLMMR_SEC_CLSTR0_CORE0_PMSTAT Register (Offset = 130h) [reset = X]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.8 CTRLMMR_SEC_CLSTR0_CORE1_CFG Register (Offset = 180h) [reset = 880h]

CTRLMMR_SEC_CLSTR0_CORE1_CFG is shown in Figure 7-8 and described in Table 7-25.

Return to Summary Table.

Configures the TCM and interrupt operation of R5 Core1.

Table 7-24. CTRLMMR_SEC_CLSTR0_CORE1_CFG Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 0180h

Figure 7-8. CTRLMMR_SEC_CLSTR0_CORE1_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
NMFI_EN	RESERVED			TCM_RSTBASE	RESERVED		
R/W-0h	R-0h			R/W-1h	R-0h		
7	6	5	4	3	2	1	0
BTCM_EN	RESERVED			ATCM_EN	RESERVED		
R/W-1h	R-0h			R/W-0h	R-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-25. CTRLMMR_SEC_CLSTR0_CORE1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NMFI_EN	R/W	0h	Enable Core1 Non-Maskable Fast Interrupts when set
14-12	RESERVED	R	0h	Reserved
11	TCM_RSTBASE	R/W	1h	Core1 A/BTCM Reset Base Address Indicator 0h - BTCM located at address 0x0 1h - ATCM located at address 0x0
10-8	RESERVED	R	0h	Reserved
7	BTCM_EN	R/W	1h	Enable Core1 BTCM RAM at reset when set
6-4	RESERVED	R	0h	Reserved
3	ATCM_EN	R/W	0h	Enable Core1 ATCM RAM at reset when set
2-0	RESERVED	R	0h	Reserved

Table 7-26. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE1_CFG

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE1_CFG Register (Offset = 180h) [reset = 880h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.9 CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_LO Register (Offset = 190h) [reset = 200h]

CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_LO is shown in Figure 7-9 and described in Table 7-28.

Return to Summary Table.

Contains the lower 32 bits of the boot vector location for R5 Core1. Bits 4:0 are not used and are always 0.

Table 7-27. CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_LO Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 0190h

Figure 7-9. CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VECT_ADDR																									RESERVED						
R/W-4h																									R-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-28. CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0.
6-0	RESERVED	R	0h	Reserved

Table 7-29. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_LO

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_LO Register (Offset = 190h) [reset = 200h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.10 CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_HI Register (Offset = 194h) [reset = 0h]

CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_HI is shown in Figure 7-10 and described in Table 7-31.

Return to Summary Table.

Contains the lower 16 bits of the boot vector location for R5 Core1.

Table 7-30. CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_HI Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 0194h

Figure 7-10. CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VECT_ADDR															
R-0h																R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-31. CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32].

Table 7-32. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_HI

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE1_BOOTVECT_HI Register (Offset = 194h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.11 CTRLMMR_SEC_CLSTR0_CORE1_PMCTRL Register (Offset = 1A0h) [reset = 0h]

CTRLMMR_SEC_CLSTR0_CORE1_PMCTRL is shown in Figure 7-11 and described in Table 7-34.

Return to Summary Table.

Configures Cluster Core1 power state.

Table 7-33. CTRLMMR_SEC_CLSTR0_CORE1_PMCTRL Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 01A0h

Figure 7-11. CTRLMMR_SEC_CLSTR0_CORE1_PMCTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CORE_HALT
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-34. CTRLMMR_SEC_CLSTR0_CORE1_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CORE_HALT	R/W	0h	Halt Core1. When 0, indicates that Core1 is in the Halt state.

Table 7-35. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE1_PMCTRL

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE1_PMCTRL Register (Offset = 1A0h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.12 CTRLMMR_SEC_CLSTR0_CORE1_PMSTAT Register (Offset = 1B0h) [reset = X]

CTRLMMR_SEC_CLSTR0_CORE1_PMSTAT is shown in Figure 7-12 and described in Table 7-37.

Return to Summary Table.

Shows Cluster Core1 power status.

Table 7-36. CTRLMMR_SEC_CLSTR0_CORE1_PMSTAT Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 01B0h

Figure 7-12. CTRLMMR_SEC_CLSTR0_CORE1_PMSTAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CLK_GATE	RESERVED	WFE	WFI
R-0h				R-X	R-0h	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 7-37. CTRLMMR_SEC_CLSTR0_CORE1_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CLK_GATE	R	X	Core1 Clock Stopped When 0, indicates clock stopped due to WFI or WFE state
2	RESERVED	R	0h	Reserved
1	WFE	R	X	Core1 WFE When 0, indicates that Core1 is in the WFE state
0	WFI	R	X	Core1 WFI When 0, indicates that Core1 is in the WFI state

Table 7-38. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE1_PMSTAT

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE1_PMSTAT Register (Offset = 1B0h) [reset = X]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.13 CTRLMMR_SEC_CLSTR1_DEF Register (Offset = 1020h) [reset = 2FF10h]

CTRLMMR_SEC_CLSTR1_DEF is shown in Figure 7-13 and described in Table 7-40.

Return to Summary Table.

Defines the type of the processor cluster.

Table 7-39. CTRLMMR_SEC_CLSTR1_DEF Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 1020h

Figure 7-13. CTRLMMR_SEC_CLSTR1_DEF Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED					CORE_NUM		
R-0h					R-2h		
15	14	13	12	11	10	9	8
DSP_CORE_TYPE							
R-FFh							
7	6	5	4	3	2	1	0
ARM_CORE_TYPE							
R-10h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-40. CTRLMMR_SEC_CLSTR1_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	CORE_NUM	R	2h	Number of cores in cluster 1h - Single Core 2h - Dual Core 4h - Quad Core
15-8	DSP_CORE_TYPE	R	FFh	DSP core type configuration. Not shown values are reserved. 0h - C7x 1h - C6x FFh - Not DSP
7-0	ARM_CORE_TYPE	R	10h	ARM core type configuration. Not shown values are reserved. 0h - A53 1h - A57 10h - R5 FFh - Not ARM

Table 7-41. Register Call Summary for CTRLMMR_SEC_CLSTR1_DEF

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR1_DEF Register (Offset = 1020h) [reset = 2FF10h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.14 CTRLMMR_SEC_CLSTR1_CFG Register (Offset = 1040h) [reset = X]

CTRLMMR_SEC_CLSTR1_CFG is shown in Figure 7-14 and described in Table 7-43.

Return to Summary Table.

Configures cluster level characteristics.

Table 7-42. CTRLMMR_SEC_CLSTR1_CFG Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 1040h

Figure 7-14. CTRLMMR_SEC_CLSTR1_CFG Register

31	30	29	28	27	26	25	24
CLSTR_CFG_RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
CLSTR_CFG_RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
CLSTR_CFG_RSVD							
R/W-0h							
7	6	5	4	3	2	1	0
CLSTR_CFG_RSVD				LOCKSTEP_EN	DBG_NO_CLKSTOP	TEINIT	LOCKSTEP
R/W-0h				R-X	R/W-0h	R/W-0h	R/W-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-43. CTRLMMR_SEC_CLSTR1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	CLSTR_CFG_RSVD	R/W	0h	Reserved for future use. Write '0' to ensure compatibility with future devices.
3	LOCKSTEP_EN	R	X	Lockstep enable. Indicates if R5 lockstep operation is supported on the device
2	DBG_NO_CLKSTOP	R/W	0h	CPU clockstop behavior 0h - CPU clocks stopped and nCLOCKSTOPPED asserted in standby mode 1h - CPU clocks not stopped in standby mode
1	TEINIT	R/W	0h	Exception handling state at reset: 0h - ARM mode 1h - Thumb mode
0	LOCKSTEP	R/W	X	When set, Core0 and Core1 operate in lockstep mode. Can only be changed if lockstep operation is supported as indicated by CLSTR1_CFG_lockstep_en = 1. If CLSTR1_CFG_lockstep_en = 0, lockstep is not supported, this bit will be read only with a value of 0.

Table 7-44. Register Call Summary for CTRLMMR_SEC_CLSTR1_CFG

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR1_CFG Register (Offset = 1040h) [reset = X]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.15 CTRLMMR_SEC_CLSTR1_CORE0_CFG Register (Offset = 1100h) [reset = 880h]

CTRLMMR_SEC_CLSTR1_CORE0_CFG is shown in Figure 7-15 and described in Table 7-46.

Return to Summary Table.

Configures the TCM and interrupt operation of R5 Core0.

Table 7-45. CTRLMMR_SEC_CLSTR1_CORE0_CFG Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 1100h

Figure 7-15. CTRLMMR_SEC_CLSTR1_CORE0_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							

23	22	21	20	19	18	17	16
RESERVED							
R-0h							

15	14	13	12	11	10	9	8
NMFI_EN	RESERVED			TCM_RSTBASE	RESERVED		
R/W-0h	R-0h			R/W-1h	R-0h		

7	6	5	4	3	2	1	0
BTCM_EN	RESERVED			ATCM_EN	RESERVED		
R/W-1h	R-0h			R/W-0h	R-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-46. CTRLMMR_SEC_CLSTR1_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NMFI_EN	R/W	0h	Enable Core0 Non-Maskable Fast Interrupts when set
14-12	RESERVED	R	0h	Reserved
11	TCM_RSTBASE	R/W	1h	Core0 A/BTCM Reset Base Address Indicator 0h - BTCM located at address 0x0 1h - ATCM located at address 0x0
10-8	RESERVED	R	0h	Reserved
7	BTCM_EN	R/W	1h	Enable Core0 BTCM RAM at reset when set
6-4	RESERVED	R	0h	Reserved
3	ATCM_EN	R/W	0h	Enable Core0 ATCM RAM at reset when set
2-0	RESERVED	R	0h	Reserved

Table 7-47. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE0_CFG

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR1_CORE0_CFG Register (Offset = 1100h) [reset = 880h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.16 CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_LO Register (Offset = 1110h) [reset = 200h]

CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_LO is shown in Figure 7-16 and described in Table 7-49.

Return to Summary Table.

Contains the lower 32 bits of the boot vector location for R5 Core0. Bits 4:0 are not used and are always 0.

Table 7-48. CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_LO Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 1110h

Figure 7-16. CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VECT_ADDR																									RESERVED						
R/W-4h																									R-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-49. CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0.
6-0	RESERVED	R	0h	Reserved

Table 7-50. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_LO

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_LO Register (Offset = 1110h) [reset = 200h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.17 CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_HI Register (Offset = 1114h) [reset = 0h]

CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_HI is shown in Figure 7-17 and described in Table 7-52.

Return to Summary Table.

Contains the lower 16 bits of the boot vector location for R5 Core0.

Table 7-51. CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_HI Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 1114h

Figure 7-17. CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VECT_ADDR															
R-0h																R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-52. CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32].

Table 7-53. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_HI

SEC_MMR0_BOOT_CTRL Registers
- CTRLMMR_SEC_CLSTR1_CORE0_BOOTVECT_HI Register (Offset = 1114h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.18 CTRLMMR_SEC_CLSTR1_CORE0_PMCTRL Register (Offset = 1120h) [reset = 0h]

CTRLMMR_SEC_CLSTR1_CORE0_PMCTRL is shown in Figure 7-18 and described in Table 7-55.

Return to Summary Table.

Configures Cluster Core0 power state.

Table 7-54. CTRLMMR_SEC_CLSTR1_CORE0_PMCTRL Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 1120h

Figure 7-18. CTRLMMR_SEC_CLSTR1_CORE0_PMCTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CORE_HALT
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-55. CTRLMMR_SEC_CLSTR1_CORE0_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CORE_HALT	R/W	0h	Halt Core0. When 0, indicates that Core0 is in the Halt state.

Table 7-56. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE0_PMCTRL

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR1_CORE0_PMCTRL Register (Offset = 1120h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.19 CTRLMMR_SEC_CLSTR1_CORE0_PMSTAT Register (Offset = 1130h) [reset = X]

CTRLMMR_SEC_CLSTR1_CORE0_PMSTAT is shown in Figure 7-19 and described in Table 7-58.

Return to Summary Table.

Shows Cluster Core0 power status.

Table 7-57. CTRLMMR_SEC_CLSTR1_CORE0_PMSTAT Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 1130h

Figure 7-19. CTRLMMR_SEC_CLSTR1_CORE0_PMSTAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CLK_GATE	RESERVED	WFE	WFI
R-0h				R-X	R-0h	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-58. CTRLMMR_SEC_CLSTR1_CORE0_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CLK_GATE	R	X	Core0 Clock Stopped When 0, indicates clock stopped due to WFI or WFE state
2	RESERVED	R	0h	Reserved
1	WFE	R	X	Core0 WFE When 0, indicates that Core0 is in the WFE state
0	WFI	R	X	Core0 WFI When 0, indicates that Core0 is in the WFI state

Table 7-59. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE0_PMSTAT

SEC_MMR0_BOOT_CTRL Registers
- CTRLMMR_SEC_CLSTR1_CORE0_PMSTAT Register (Offset = 1130h) [reset = X]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.20 CTRLMMR_SEC_CLSTR1_CORE1_CFG Register (Offset = 1180h) [reset = 880h]

CTRLMMR_SEC_CLSTR1_CORE1_CFG is shown in Figure 7-20 and described in Table 7-61.

Return to Summary Table.

Configures the TCM and interrupt operation of R5 Core1.

Table 7-60. CTRLMMR_SEC_CLSTR1_CORE1_CFG Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 1180h

Figure 7-20. CTRLMMR_SEC_CLSTR1_CORE1_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
NMFI_EN	RESERVED			TCM_RSTBASE	RESERVED		
R/W-0h	R-0h			R/W-1h	R-0h		
7	6	5	4	3	2	1	0
BTCM_EN	RESERVED			ATCM_EN	RESERVED		
R/W-1h	R-0h			R/W-0h	R-0h		

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-61. CTRLMMR_SEC_CLSTR1_CORE1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	NMFI_EN	R/W	0h	Enable Core1 Non-Maskable Fast Interrupts when set
14-12	RESERVED	R	0h	Reserved
11	TCM_RSTBASE	R/W	1h	Core1 A/BTCM Reset Base Address Indicator 0h - BTCM located at address 0x0 1h - ATCM located at address 0x0
10-8	RESERVED	R	0h	Reserved
7	BTCM_EN	R/W	1h	Enable Core1 BTCM RAM at reset when set
6-4	RESERVED	R	0h	Reserved
3	ATCM_EN	R/W	0h	Enable Core1 ATCM RAM at reset when set
2-0	RESERVED	R	0h	Reserved

Table 7-62. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE1_CFG

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR1_CORE1_CFG Register (Offset = 1180h) [reset = 880h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.21 CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_LO Register (Offset = 1190h) [reset = 200h]

CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_LO is shown in Figure 7-21 and described in Table 7-64.

Return to Summary Table.

Contains the lower 32 bits of the boot vector location for R5 Core1. Bits 4:0 are not used and are always 0.

Table 7-63. CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_LO Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 1190h

Figure 7-21. CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VECT_ADDR																									RESERVED						
R/W-4h																									R-0h						

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-64. CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-7	VECT_ADDR	R/W	4h	Specifies the lower 25 bits of the 41-bit vector address corresponding to Vector Table address bits[31:7]. Note bits 6:0 of the Vector Table address are always 0.
6-0	RESERVED	R	0h	Reserved

Table 7-65. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_LO

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_LO Register (Offset = 1190h) [reset = 200h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.22 CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_HI Register (Offset = 1194h) [reset = 0h]

CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_HI is shown in Figure 7-22 and described in Table 7-67.

Return to Summary Table.

Contains the lower 16 bits of the boot vector location for R5 Core1.

Table 7-66. CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_HI Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 1194h

Figure 7-22. CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_HI Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																VECT_ADDR															
R-0h																R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-67. CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_HI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-0	VECT_ADDR	R/W	0h	Specifies the upper 16 bits of the 41-bit vector address corresponding to Vector Table address bits[47:32].

Table 7-68. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_HI

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR1_CORE1_BOOTVECT_HI Register (Offset = 1194h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.23 CTRLMMR_SEC_CLSTR1_CORE1_PMCTRL Register (Offset = 11A0h) [reset = 0h]

CTRLMMR_SEC_CLSTR1_CORE1_PMCTRL is shown in Figure 7-23 and described in Table 7-70.

Return to Summary Table.

Configures Cluster Core1 power state.

Table 7-69. CTRLMMR_SEC_CLSTR1_CORE1_PMCTRL Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 11A0h

Figure 7-23. CTRLMMR_SEC_CLSTR1_CORE1_PMCTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							CORE_HALT
R-0h							R/W-0h

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-70. CTRLMMR_SEC_CLSTR1_CORE1_PMCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	0h	Reserved
0	CORE_HALT	R/W	0h	Halt Core1. When 0, indicates that Core1 is in the Halt state.

Table 7-71. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE1_PMCTRL

SEC_MMR0_BOOT_CTRL Registers
- CTRLMMR_SEC_CLSTR1_CORE1_PMCTRL Register (Offset = 11A0h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.24 CTRLMMR_SEC_CLSTR1_CORE1_PMSTAT Register (Offset = 11B0h) [reset = X]

CTRLMMR_SEC_CLSTR1_CORE1_PMSTAT is shown in Figure 7-24 and described in Table 7-73.

Return to Summary Table.

Shows Cluster Core1 power status.

Table 7-72. CTRLMMR_SEC_CLSTR1_CORE1_PMSTAT Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 11B0h

Figure 7-24. CTRLMMR_SEC_CLSTR1_CORE1_PMSTAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				CLK_GATE	RESERVED	WFE	WFI
R-0h				R-X	R-0h	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 7-73. CTRLMMR_SEC_CLSTR1_CORE1_PMSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	CLK_GATE	R	X	Core1 Clock Stopped When 0, indicates clock stopped due to WFI or WFE state
2	RESERVED	R	0h	Reserved
1	WFE	R	X	Core1 WFE When 0, indicates that Core1 is in the WFE state
0	WFI	R	X	Core1 WFI When 0, indicates that Core1 is in the WFI state

Table 7-74. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE1_PMSTAT

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR1_CORE1_PMSTAT Register (Offset = 11B0h) [reset = X]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.25 CTRLMMR_SEC_CLSTR2_DEF Register (Offset = 2020h) [reset = 101FFh]

CTRLMMR_SEC_CLSTR2_DEF is shown in Figure 7-25 and described in Table 7-76.

Return to Summary Table.

Defines the type of the processor cluster.

Table 7-75. CTRLMMR_SEC_CLSTR2_DEF Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 2020h

Figure 7-25. CTRLMMR_SEC_CLSTR2_DEF Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED					CORE_NUM		
R-0h					R-1h		
15	14	13	12	11	10	9	8
DSP_CORE_TYPE							
R-1h							
7	6	5	4	3	2	1	0
ARM_CORE_TYPE							
R-FFh							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; *-n* = value after reset

Table 7-76. CTRLMMR_SEC_CLSTR2_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	CORE_NUM	R	1h	Number of cores in cluster 1h - Single Core 2h - Dual Core 4h - Quad Core
15-8	DSP_CORE_TYPE	R	1h	DSP core type configuration. Not shown values are reserved. 0h - C7x 1h - C6x FFh - Not DSP
7-0	ARM_CORE_TYPE	R	FFh	ARM core type configuration. Not shown values are reserved. 0h - A53 1h - A57 10h - R5 FFh - Not ARM

Table 7-77. Register Call Summary for CTRLMMR_SEC_CLSTR2_DEF

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR2_DEF Register (Offset = 2020h) [reset = 101FFh]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.26 CTRLMMR_SEC_CLSTR2_CFG Register (Offset = 2040h) [reset = 0h]

CTRLMMR_SEC_CLSTR2_CFG is shown in Figure 7-26 and described in Table 7-79.

Return to Summary Table.

Configures cluster level characteristics.

Table 7-78. CTRLMMR_SEC_CLSTR2_CFG Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 2040h

Figure 7-26. CTRLMMR_SEC_CLSTR2_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						SSCLK_MODE	
R-0h						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-79. CTRLMMR_SEC_CLSTR2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	SSCLK_MODE	R/W	0h	Controls the C66 clock rate for cluster logic and bus interfaces 0h - Div2 clock mode 1h - Div3 clock mode 2h - Div4 clock mode 3h - Reserved

Table 7-80. Register Call Summary for CTRLMMR_SEC_CLSTR2_CFG

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR2_CFG Register (Offset = 2040h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.27 CTRLMMR_SEC_CLSTR2_CORE0_CFG Register (Offset = 2100h) [reset = 0h]

CTRLMMR_SEC_CLSTR2_CORE0_CFG is shown in Figure 7-27 and described in Table 7-82.

Return to Summary Table.

Configures the C66 operation.

Table 7-81. CTRLMMR_SEC_CLSTR2_CORE0_CFG Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 2100h

Figure 7-27. CTRLMMR_SEC_CLSTR2_CORE0_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							BIG_ENDIAN
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-82. CTRLMMR_SEC_CLSTR2_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	BIG_ENDIAN	R/W	0h	When big endian operation is selected, C66 core operates in big endian and corepac bridges will swzzle the data in from and out to the SoC (which is always little endian) 0h - Little Endian mode 1h - Big Endian mode
15-0	RESERVED	R	0h	Reserved

Table 7-83. Register Call Summary for CTRLMMR_SEC_CLSTR2_CORE0_CFG

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR2_CORE0_CFG Register (Offset = 2100h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.28 CTRLMMR_SEC_CLSTR2_CORE0_BOOTVECT_LO Register (Offset = 2110h) [reset = 2000h]

CTRLMMR_SEC_CLSTR2_CORE0_BOOTVECT_LO is shown in Figure 7-28 and described in Table 7-85.

Return to Summary Table.

Contains the boot vector for the C66 core.

Table 7-84. CTRLMMR_SEC_CLSTR2_CORE0_BOOTVECT_LO Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 2110h

Figure 7-28. CTRLMMR_SEC_CLSTR2_CORE0_BOOTVECT_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										GEM_ISTP_RST_VAL																					
R-0h										R/W-2000h																					

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-85. CTRLMMR_SEC_CLSTR2_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21-0	GEM_ISTP_RST_VAL	R/W	2000h	C66 interrupt service table pointer Specifies the upper 22 bits of the 32-bit initial fetch address. Default value points to C66 L2 SRAM at 0x0080_0000

Table 7-86. Register Call Summary for CTRLMMR_SEC_CLSTR2_CORE0_BOOTVECT_LO

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR2_CORE0_BOOTVECT_LO Register (Offset = 2110h) [reset = 2000h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.29 CTRLMMR_SEC_CLSTR3_DEF Register (Offset = 3020h) [reset = 101FFh]

CTRLMMR_SEC_CLSTR3_DEF is shown in Figure 7-29 and described in Table 7-88.

Return to Summary Table.

Defines the type of the processor cluster.

Table 7-87. CTRLMMR_SEC_CLSTR3_DEF Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 3020h

Figure 7-29. CTRLMMR_SEC_CLSTR3_DEF Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED					CORE_NUM		
R-0h					R-1h		
15	14	13	12	11	10	9	8
DSP_CORE_TYPE							
R-1h							
7	6	5	4	3	2	1	0
ARM_CORE_TYPE							
R-FFh							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-88. CTRLMMR_SEC_CLSTR3_DEF Register Field Descriptions

Bit	Field	Type	Reset	Description
31-19	RESERVED	R	0h	Reserved
18-16	CORE_NUM	R	1h	Number of cores in cluster 1h - Single Core 2h - Dual Core 4h - Quad Core
15-8	DSP_CORE_TYPE	R	1h	DSP core type configuration. Not shown values are reserved. 0h - C7x 1h - C6x FFh - Not DSP
7-0	ARM_CORE_TYPE	R	FFh	ARM core type configuration. Not shown values are reserved. 0h - A53 1h - A57 10h - R5 FFh - Not ARM

Table 7-89. Register Call Summary for CTRLMMR_SEC_CLSTR3_DEF

SEC_MMR0_BOOT_CTRL Registers
- CTRLMMR_SEC_CLSTR3_DEF Register (Offset = 3020h) [reset = 101FFh]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.30 CTRLMMR_SEC_CLSTR3_CFG Register (Offset = 3040h) [reset = 0h]

CTRLMMR_SEC_CLSTR3_CFG is shown in Figure 7-30 and described in Table 7-91.

Return to Summary Table.

Configures cluster level characteristics.

Table 7-90. CTRLMMR_SEC_CLSTR3_CFG Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 3040h

Figure 7-30. CTRLMMR_SEC_CLSTR3_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						SSCLK_MODE	
R-0h						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-91. CTRLMMR_SEC_CLSTR3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R	0h	Reserved
1-0	SSCLK_MODE	R/W	0h	Controls the C66 clock rate for cluster logic and bus interfaces 0h - Div2 clock mode 1h - Div3 clock mode 2h - Div4 clock mode 3h - Reserved

Table 7-92. Register Call Summary for CTRLMMR_SEC_CLSTR3_CFG

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR3_CFG Register (Offset = 3040h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.31 CTRLMMR_SEC_CLSTR3_CORE0_CFG Register (Offset = 3100h) [reset = 0h]

CTRLMMR_SEC_CLSTR3_CORE0_CFG is shown in Figure 7-31 and described in Table 7-94.

Return to Summary Table.

Configures the C66 operation.

Table 7-93. CTRLMMR_SEC_CLSTR3_CORE0_CFG Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 3100h

Figure 7-31. CTRLMMR_SEC_CLSTR3_CORE0_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							BIG_ENDIAN
R-0h							R/W-0h
15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-94. CTRLMMR_SEC_CLSTR3_CORE0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-17	RESERVED	R	0h	Reserved
16	BIG_ENDIAN	R/W	0h	When big endian operation is selected, C66 core operates in big endian and corepac bridges will swzzle the data in from and out to the SoC (which is always little endian) 0h - Little Endian mode 1h - Big Endian mode
15-0	RESERVED	R	0h	Reserved

Table 7-95. Register Call Summary for CTRLMMR_SEC_CLSTR3_CORE0_CFG

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR3_CORE0_CFG Register (Offset = 3100h) [reset = 0h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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7.32 CTRLMMR_SEC_CLSTR3_CORE0_BOOTVECT_LO Register (Offset = 3110h) [reset = 2000h]

CTRLMMR_SEC_CLSTR3_CORE0_BOOTVECT_LO is shown in Figure 7-32 and described in Table 7-97.

Return to Summary Table.

Contains the boot vector for the C66 core.

Table 7-96. CTRLMMR_SEC_CLSTR3_CORE0_BOOTVECT_LO Instances

Instance	Physical Address
SEC_MMR0_BOOT_CTRL	45A4 3110h

Figure 7-32. CTRLMMR_SEC_CLSTR3_CORE0_BOOTVECT_LO Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										GEM_ISTP_RST_VAL																					
R-0h										R/W-2000h																					

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 7-97. CTRLMMR_SEC_CLSTR3_CORE0_BOOTVECT_LO Register Field Descriptions

Bit	Field	Type	Reset	Description
31-22	RESERVED	R	0h	Reserved
21-0	GEM_ISTP_RST_VAL	R/W	2000h	C66 interrupt service table pointer Specifies the upper 22 bits of the 32-bit initial fetch address. Default value points to C66 L2 SRAM at 0x0080_0000

Table 7-98. Register Call Summary for CTRLMMR_SEC_CLSTR3_CORE0_BOOTVECT_LO

SEC_MMR0_BOOT_CTRL Registers

- CTRLMMR_SEC_CLSTR3_CORE0_BOOTVECT_LO Register (Offset = 3110h) [reset = 2000h]: [0]
- SEC_MMR0_BOOT_CTRL Registers: [0]

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8 SEC_MMR0_DBG_CTRL Registers

Table 8-2 lists the memory-mapped registers for the SEC_MMR0_DBG_CTRL. All register offset addresses not listed in Table 8-2 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. SEC_MMR0_DBG_CTRL Instances

Instance	Base Address
SEC_MMR0_DBG_CTRL	4594 4000h

Table 8-2. SEC_MMR0_DBG_CTRL Registers

Offset	Acronym	Register Name	SEC_MMR0_DBG_CTRL Physical Address
0h	CTRLMMR_SEC_CLSTR0_CORE0_DBG_CFG	Cluster0 Core0 Debug Configuration Register	4594 4000h
40h	CTRLMMR_SEC_CLSTR0_CORE1_DBG_CFG	Cluster0 Core1 Debug Configuration Register	4594 4040h
1000h	CTRLMMR_SEC_CLSTR1_CORE0_DBG_CFG	Cluster1 Core0 Debug Configuration Register	4594 5000h
1040h	CTRLMMR_SEC_CLSTR1_CORE1_DBG_CFG	Cluster1 Core1 Debug Configuration Register	4594 5040h

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8.1 CTRLMMR_SEC_CLSTR0_CORE0_DBG_CFG Register (Offset = 0h) [reset = AA00h]

CTRLMMR_SEC_CLSTR0_CORE0_DBG_CFG is shown in Figure 8-1 and described in Table 8-4.

Return to Summary Table.

Configures debug operation for Cluster Core0.

Table 8-3. CTRLMMR_SEC_CLSTR0_CORE0_DBG_CFG Instances

Instance	Physical Address
SEC_MMR0_DBG_CTRL	4594 4000h

Figure 8-1. CTRLMMR_SEC_CLSTR0_CORE0_DBG_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
DBGEN				NIDEN			
R/W-Ah				R/W-Ah			
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 8-4. CTRLMMR_SEC_CLSTR0_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	DBGEN	R/W	Ah	Core0 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable Ah - Enabled others - Disabled
11-8	NIDEN	R/W	Ah	Core0 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable Ah - Enabled others - Disabled
7-0	RESERVED	R	0h	Reserved

Table 8-5. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE0_DBG_CFG

SEC_MMR0_DBG_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE0_DBG_CFG Register (Offset = 0h) [reset = AA00h]: [0]
- SEC_MMR0_DBG_CTRL Registers: [0]

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8.2 CTRLMMR_SEC_CLSTR0_CORE1_DBG_CFG Register (Offset = 40h) [reset = AA00h]

CTRLMMR_SEC_CLSTR0_CORE1_DBG_CFG is shown in Figure 8-2 and described in Table 8-7.

Return to Summary Table.

Configures debug operation for Cluster Core1.

Table 8-6. CTRLMMR_SEC_CLSTR0_CORE1_DBG_CFG Instances

Instance	Physical Address
SEC_MMR0_DBG_CTRL	4594 4040h

Figure 8-2. CTRLMMR_SEC_CLSTR0_CORE1_DBG_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
DBGEN				NIDEN			
R/W-Ah				R/W-Ah			
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 8-7. CTRLMMR_SEC_CLSTR0_CORE1_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	DBGEN	R/W	Ah	Core1 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable Ah - Enabled others - Disabled
11-8	NIDEN	R/W	Ah	Core1 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable Ah - Enabled others - Disabled
7-0	RESERVED	R	0h	Reserved

Table 8-8. Register Call Summary for CTRLMMR_SEC_CLSTR0_CORE1_DBG_CFG

SEC_MMR0_DBG_CTRL Registers

- CTRLMMR_SEC_CLSTR0_CORE1_DBG_CFG Register (Offset = 40h) [reset = AA00h]: [0]
- SEC_MMR0_DBG_CTRL Registers: [0]

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8.3 CTRLMMR_SEC_CLSTR1_CORE0_DBG_CFG Register (Offset = 1000h) [reset = AA00h]

CTRLMMR_SEC_CLSTR1_CORE0_DBG_CFG is shown in Figure 8-3 and described in Table 8-10.

Return to Summary Table.

Configures debug operation for Cluster Core0.

Table 8-9. CTRLMMR_SEC_CLSTR1_CORE0_DBG_CFG Instances

Instance	Physical Address
SEC_MMR0_DBG_CTRL	4594 5000h

Figure 8-3. CTRLMMR_SEC_CLSTR1_CORE0_DBG_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
DBGEN				NIDEN			
R/W-Ah				R/W-Ah			
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 8-10. CTRLMMR_SEC_CLSTR1_CORE0_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	DBGEN	R/W	Ah	Core0 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable Ah - Enabled others - Disabled
11-8	NIDEN	R/W	Ah	Core0 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable Ah - Enabled others - Disabled
7-0	RESERVED	R	0h	Reserved

Table 8-11. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE0_DBG_CFG

SEC_MMR0_DBG_CTRL Registers

- CTRLMMR_SEC_CLSTR1_CORE0_DBG_CFG Register (Offset = 1000h) [reset = AA00h]: [0]
- SEC_MMR0_DBG_CTRL Registers: [0]

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8.4 CTRLMMR_SEC_CLSTR1_CORE1_DBG_CFG Register (Offset = 1040h) [reset = AA00h]

CTRLMMR_SEC_CLSTR1_CORE1_DBG_CFG is shown in Figure 8-4 and described in Table 8-13.

Return to Summary Table.

Configures debug operation for Cluster Core1.

Table 8-12. CTRLMMR_SEC_CLSTR1_CORE1_DBG_CFG Instances

Instance	Physical Address
SEC_MMR0_DBG_CTRL	4594 5040h

Figure 8-4. CTRLMMR_SEC_CLSTR1_CORE1_DBG_CFG Register

31	30	29	28	27	26	25	24
RESERVED							
R-0h							
23	22	21	20	19	18	17	16
RESERVED							
R-0h							
15	14	13	12	11	10	9	8
DBGEN				NIDEN			
R/W-Ah				R/W-Ah			
7	6	5	4	3	2	1	0
RESERVED							
R-0h							

LEGEND: R/W = Read/Write; R = Read only; W1toCl = Write 1 to clear bit; -*n* = value after reset

Table 8-13. CTRLMMR_SEC_CLSTR1_CORE1_DBG_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15-12	DBGEN	R/W	Ah	Core1 Invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable Ah - Enabled others - Disabled
11-8	NIDEN	R/W	Ah	Core1 Non-invasive debug enable. This is a fault tolerant bitfield that must be set 4'hA to enable Ah - Enabled others - Disabled
7-0	RESERVED	R	0h	Reserved

Table 8-14. Register Call Summary for CTRLMMR_SEC_CLSTR1_CORE1_DBG_CFG

SEC_MMR0_DBG_CTRL Registers

- CTRLMMR_SEC_CLSTR1_CORE1_DBG_CFG Register (Offset = 1040h) [reset = AA00h]: [0]
- SEC_MMR0_DBG_CTRL Registers: [0]

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9 WKUP_VTM0 Registers

9.1 WKUP_VTM0_MMR_VBUSP_CFG1 Registers

Table 9-2 lists the memory-mapped registers for the WKUP_VTM0_MMR_VBUSP_CFG1 registers. All register offset addresses not listed in Table 9-2 should be considered as reserved locations and the register contents should not be modified.

All the MMRs in this region by default use mod_g_rst_n as their reset unless specified otherwise.

Table 9-1. WKUP_VTM0_MMR_VBUSP_CFG1 Instances

Instance	Base Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0000h

Table 9-2. WKUP_VTM0_MMR_VBUSP_CFG1 Registers

Offset	Acronym	Register Name	WKUP_VTM0_MMR_VBUSP_CFG1 Physical Address
0h	WKUP_VTM_PID		4204 0000h
4h	WKUP_VTM_DEVINFO_PWR0		4204 0004h
100h + formula	WKUP_VTM_VD_DEVINFO_j		4204 0100h + formula
104h + formula	WKUP_VTM_VD_OPPVID_j		4204 0104h + formula
204h	WKUP_VTM_GT_TH1_INT_RAW_STAT_SET		4204 0204h
108h + formula	WKUP_VTM_VD_EVT_STAT_j		4204 0108h + formula
208h	WKUP_VTM_GT_TH1_INT_EN_STAT_CLR		4204 0208h
10Ch + formula	WKUP_VTM_VD_EVT_SEL_SET_j		4204 010Ch + formula
110h + formula	WKUP_VTM_VD_EVT_SEL_CLR_j		4204 0110h + formula
214h	WKUP_VTM_GT_TH1_INT_EN_SET		4204 0214h
218h	WKUP_VTM_GT_TH1_INT_EN_CLR		4204 0218h
224h	WKUP_VTM_GT_TH2_INT_RAW_STAT_SET		4204 0224h
228h	WKUP_VTM_GT_TH2_INT_EN_STAT_CLR		4204 0228h
234h	WKUP_VTM_GT_TH2_INT_EN_SET		4204 0234h
238h	WKUP_VTM_GT_TH2_INT_EN_CLR		4204 0238h
244h	WKUP_VTM_LT_TH0_INT_RAW_STAT_SET		4204 0244h
248h	WKUP_VTM_LT_TH0_INT_EN_STAT_CLR		4204 0248h
254h	WKUP_VTM_LT_TH0_INT_EN_SET		4204 0254h
258h	WKUP_VTM_LT_TH0_INT_EN_CLR		4204 0258h
300h + formula	WKUP_VTM_TMPSENS_CTRL_j		4204 0300h + formula
308h + formula	WKUP_VTM_TMPSENS_STAT_j		4204 0308h + formula
30Ch + formula	WKUP_VTM_TMPSENS_TH_j		4204 030Ch + formula
310h + formula	WKUP_VTM_TMPSENS_TH2_j		4204 0310h + formula

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9.2 WKUP_VTM_PID Register (Offset = 0h) [reset = 661B4901h]

WKUP_VTM_PID is shown in Figure 9-1 and described in Table 9-4.

Return to Summary Table.

VTM Peripheral Identification Register

Table 9-3. WKUP_VTM_PID Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0000h

Figure 9-1. WKUP_VTM_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R-1h		R-2h		R-61Bh											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R_RTL					X_MAJOR			CUSTOM		Y_MINOR					
R-9h					R-1h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 9-4. WKUP_VTM_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID scheme
29-28	BU	R	2h	BU
27-16	FUNC	R	61Bh	Module functional identifier
15-11	R_RTL	R	9h	RTL revision number
10-8	X_MAJOR	R	1h	Major revision number
7-6	CUSTOM	R	0h	Custom revision number
5-0	Y_MINOR	R	1h	Minor revision number

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9.3 WKUP_VTM_DEVINFO_PWR0 Register (Offset = 4h) [reset = X]

WKUP_VTM_DEVINFO_PWR0 is shown in Figure 9-2 and described in Table 9-6.

Return to Summary Table.

Device specific voltage domain and temp sensor information register.

Table 9-5. WKUP_VTM_DEVINFO_PWR0 Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0004h

Figure 9-2. WKUP_VTM_DEVINFO_PWR0 Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED				VTM_VD_MAP			
R-X				R-X			
15	14	13	12	11	10	9	8
RESERVED			VD_RTC	RESERVED			
R-X			R-X	R-X			
7	6	5	4	3	2	1	0
TMPSENS_CT				CVD_CT			
R-X				R-X			

LEGEND: R = Read Only; *-n* = value after reset

Table 9-6. WKUP_VTM_DEVINFO_PWR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19-16	VTM_VD_MAP	R	X	Core voltage domain, cVD, global mapping 4-bit code, in the context of this SoC. It shows in which cVD this VTM is instantiated/placed. This field indicates in which core voltage domain, cVD, has been physically placed this VTM. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SoCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SoCs, 0x4-0xE = Mapping varies between SoCs, 0xF = not implemented. Reset value is a VTM tieoff, d_vtm_vd_map.
15-13	RESERVED	R	X	
12	VD_RTC	R	X	RTC voltage domain presence. 0: There is NO VD_RTC in this SoC. 1: There is a VD_RTC in this SoC. Reset value is a VTM tieoff, d_vd_rtc.
11-8	RESERVED	R	X	

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Table 9-6. WKUP_VTM_DEVINFO_PWR0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-4	TMPSENS_CT	R	X	Number of temperature sensors associated with this VTM. Valid values are 4'h 0 - 4'h8. 0x 0: NO temp-sensor associated to this VTM. 0x 8: 8 temp-sensors associated to this VTM. 0x9 to 0xF: invalid values. Reset value is a VTM tieoff, d_vtm_tmpsens_ct.
3-0	CVD_CT	R	X	Number of core voltage domains in device. VD0 is always allocated to VD_RTC, if it exists, and VD1 always to VD_WKUP. The maximum number of cVDs in an SoC is 15, 0xF. Reset value is a VTM tieoff, d_device_cvd_ct.

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9.4 WKUP_VTM_VD_DEVINFO_j Register (Offset = 100h + formula) [reset = X]

WKUP_VTM_VD_DEVINFO_j is shown in Figure 9-3 and described in Table 9-8.

Return to Summary Table.

Voltage domain a information register. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

Offset = 100h + (j * 20h); where j = 0h to 7h

Table 9-7. WKUP_VTM_VD_DEVINFO_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0100h + formula

Figure 9-3. WKUP_VTM_VD_DEVINFO_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			AVS0_SUP	VD_MAP			
R/W-X			R/W-X	R-X			
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 9-8. WKUP_VTM_VD_DEVINFO_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-13	RESERVED	R/W	X	
12	AVS0_SUP	R/W	X	Indicates VD0 AVS class0 support. Indicates if the cVD associated with this VTM's VD MMR supports AVS-Class 0: 0: No AVS-Class0. 1: Supports-AVS-Class0. Reset value is from e-fuse at module reset, efuse_vd[a]_avs_sup.
11-8	VD_MAP	R	X	Indicates the core voltage domain mapping of VTM VD. Device specific field. This field indicates to which SoC cVD is this VD of this VTM map to. Valid values: 0x0 to 0xE where: 0x 0 = VD_RTC, not present is some SoCs, 0x 1 = VD_WKUP, 0x 2 = VD_MCU, 0x 3 = VD_CORE, not present is some SoCs, 0x 4-0xE = Mapping varies between SoCs, 0xF = not implemented.
7-0	RESERVED	R/W	X	

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9.5 WKUP_VTM_VD_OPPVID_j Register (Offset = 104h + formula) [reset = X]

WKUP_VTM_VD_OPPVID_j is shown in Figure 9-4 and described in Table 9-10.

Return to Summary Table.

Voltage domain a VID actual code used as reference by Firmware to set the various voltage domain supply voltages. Reset defaults are sourced from efuse for each OPP. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

Offset = 104h + (j * 20h); where j = 0h to 7h

Table 9-9. WKUP_VTM_VD_OPPVID_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0104h + formula

Figure 9-4. WKUP_VTM_VD_OPPVID_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPP_3								OPP_2								OPP_1								OPP_0							
R/W-X								R/W-X								R/W-X								R/W-X							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-10. WKUP_VTM_VD_OPPVID_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	OPP_3	R/W	X	OPP 3 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SoC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[a]_opp_3.
23-16	OPP_2	R/W	X	OPP 2 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SoC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[a]_opp_2.
15-8	OPP_1	R/W	X	OPP 1 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SoC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[a]_opp_1.

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Table 9-10. WKUP_VTM_VD_OPPVID_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	OPP_0	R/W	X	OPP 0 default VID. VID code that represents the required VD value in this Voltage domain to operate at. Valid values are from 0x1e to 0x91. Any value outside that range indicates not implemented including 0x0. This is SoC and device/chip specific. Reset value is from e-fuse at POR, efuse_vd[a]_opp_0.

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9.6 WKUP_VTM_GT_TH1_INT_RAW_STAT_SET Register (Offset = 204h) [reset = X]

WKUP_VTM_GT_TH1_INT_RAW_STAT_SET is shown in Figure 9-5 and described in Table 9-12.

Return to Summary Table.

Interrupt RAW event status and set MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_GT_TH1_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

Table 9-11. WKUP_VTM_GT_TH1_INT_RAW_STAT_SET Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0204h

Figure 9-5. WKUP_VTM_GT_TH1_INT_RAW_STAT_SET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1S-0h							

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-12. WKUP_VTM_GT_TH1_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1S	0h	Interrupt pending bit set for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the pending stats regardless of the corresponding enable setting.

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9.7 WKUP_VTM_VD_EVT_STAT_j Register (Offset = 108h + formula) [reset = X]

WKUP_VTM_VD_EVT_STAT_j is shown in Figure 9-6 and described in Table 9-14.

Return to Summary Table.

Voltage domain a event and control status register.

Offset = 108h + (j * 20h); where j = 0h to 7h

Table 9-13. WKUP_VTM_VD_EVT_STAT_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0108h + formula

Figure 9-6. WKUP_VTM_VD_EVT_STAT_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED					LT_TH0_ALERT	GT_TH2_ALERT	GT_TH1_ALERT
R-X					R-X	R-X	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 9-14. WKUP_VTM_VD_EVT_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RESERVED	R	X	
2	LT_TH0_ALERT	R	X	This bit reflects the status of the TH0 undertemp alert resulting from the AND of all the similar alerts produced by the temp sensors selected by VTM_VD[a]_EVT_SEL_SET.tsens_evt_sel.
1	GT_TH2_ALERT	R	X	This bit reflects the status of the merged temperature alert resulting from the combination of all the similar alerts produced by the temp-monitors selected as showed in field VTM_VD[a]_EVT_SEL_SET.tsens_evt_sel. This field shows the actual present level of the resulting OR function of the combined selected signals.
0	GT_TH1_ALERT	R	X	This bit reflects the status of the merged temperature alert resulting from the OR of all the similar alerts produced by the temp-monitors selected as showed in field VTM_VD[a]_EVT_SEL_SET.tsens_evt_sel. This field shows the actual present value of the resulting OR function of the combined selected signals.

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9.8 WKUP_VTM_GT_TH1_INT_EN_STAT_CLR Register (Offset = 208h) [reset = X]

WKUP_VTM_GT_TH1_INT_EN_STAT_CLR is shown in Figure 9-7 and described in Table 9-16.

Return to Summary Table.

Enabled interrupt event status and clear MMR for interrupt GT_TH1 per voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_GT_TH1_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

Table 9-15. WKUP_VTM_GT_TH1_INT_EN_STAT_CLR Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0208h

Figure 9-7. WKUP_VTM_GT_TH1_INT_EN_STAT_CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1C-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 9-16. WKUP_VTM_GT_TH1_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1C	0h	Interrupt masked pending bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status that includes the corresponding enable setting.

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9.9 WKUP_VTM_VD_EVT_SEL_SET_j Register (Offset = 10Ch + formula) [reset = X]

WKUP_VTM_VD_EVT_SEL_SET_j is shown in Figure 9-8 and described in Table 9-18.

Return to Summary Table.

Voltage domain a event select and control set register. NOTE: This MMR and the companion MMR VTM_VD[a]_EVT_SEL_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Offset = 10Ch + (j * 20h); where j = 0h to 7h

Table 9-17. WKUP_VTM_VD_EVT_SEL_SET_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 010Ch + formula

Figure 9-8. WKUP_VTM_VD_EVT_SEL_SET_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								TSENS_EVT_SEL							
R/W-X								R/W1S-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-X															

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-18. WKUP_VTM_VD_EVT_SEL_SET_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	TSENS_EVT_SEL	R/W1S	0h	In this field we select which of the event contributions of the 8-maximum possible temp-monitors controlled by this VTM will contribute to generate the merged event/alerts of this VD. Any combination of them could be selected and varies between SoCs and VDs. Eg: 0x00 : No temp-monitor event contributes to generate the temperature events of this VD. 0x06: Temp-monitors[2,1] contribute to generate the temperature events of this VD. ... 0xFF: All 8 temp-monitors contribute to generate the temperature events of this VD. 0: Writing 0 to this field produces no effect. 1: Writing 1 to any of the bits in this field sets to 1 the corresponding bit in that field.
15-0	RESERVED	R/W	X	

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9.10 WKUP_VTM_VD_EVT_SEL_CLR_j Register (Offset = 110h + formula) [reset = X]

WKUP_VTM_VD_EVT_SEL_CLR_j is shown in Figure 9-9 and described in Table 9-20.

Return to Summary Table.

Voltage domain a event select and control clear register. NOTE: This MMR and the companion MMR VTM_VD[a]_EVT_SEL_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Offset = 110h + (j * 20h); where j = 0h to 7h

Table 9-19. WKUP_VTM_VD_EVT_SEL_CLR_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0110h + formula

Figure 9-9. WKUP_VTM_VD_EVT_SEL_CLR_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED								TSENS_EVT_SEL							
R/W-X								R/W1C-0h							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R/W-X															

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 9-20. WKUP_VTM_VD_EVT_SEL_CLR_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-16	TSENS_EVT_SEL	R/W1C	0h	In this field we select which of the event contributions of the 8-maximum possible temp-monitors controlled by this VTM will contribute to generate the merged event/alerts of this VD. Any combination of them could be selected and varies between SoCs and VDs. Eg: 0x00 : No temp-monitor event contributes to generate the temperature events of this VD. 0x06: Temp-monitors[2,1] contribute to generate the temperature events of this VD. ... 0xFF: All 8 temp-monitors contribute to generate the temperature events of this VD. 0: Writing 0 to this field produces no effect. 1: Writing 1 to any of the bits in this field clears, = 0, the corresponding bit in that field.
15-0	RESERVED	R/W	X	

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9.11 WKUP_VTM_GT_TH1_INT_EN_SET Register (Offset = 214h) [reset = X]

WKUP_VTM_GT_TH1_INT_EN_SET is shown in Figure 9-10 and described in Table 9-22.

Return to Summary Table.

Enable set MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_GT_TH1_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Table 9-21. WKUP_VTM_GT_TH1_INT_EN_SET Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0214h

Figure 9-10. WKUP_VTM_GT_TH1_INT_EN_SET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1S-0h							

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-22. WKUP_VTM_GT_TH1_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1S	0h	Interrupt enable bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings.

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9.12 WKUP_VTM_GT_TH1_INT_EN_CLR Register (Offset = 218h) [reset = X]

WKUP_VTM_GT_TH1_INT_EN_CLR is shown in Figure 9-11 and described in Table 9-24.

Return to Summary Table.

Enable clear MMR for interrupt GT_TH1 for each voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_GT_TH1_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Table 9-23. WKUP_VTM_GT_TH1_INT_EN_CLR Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0218h

Figure 9-11. WKUP_VTM_GT_TH1_INT_EN_CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1C-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 9-24. WKUP_VTM_GT_TH1_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1C	0h	Interrupt enable bit for gt_th1_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings.

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9.13 WKUP_VTM_GT_TH2_INT_RAW_STAT_SET Register (Offset = 224h) [reset = X]

WKUP_VTM_GT_TH2_INT_RAW_STAT_SET is shown in Figure 9-12 and described in Table 9-26.

Return to Summary Table.

Interrupt RAW event status and set MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_GT_TH2_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

Table 9-25. WKUP_VTM_GT_TH2_INT_RAW_STAT_SET Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0224h

Figure 9-12. WKUP_VTM_GT_TH2_INT_RAW_STAT_SET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1S-0h							

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-26. WKUP_VTM_GT_TH2_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1S	0h	Interrupt pending bit set for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the pending status regardless of the enable setting.

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9.14 WKUP_VTM_GT_TH2_INT_EN_STAT_CLR Register (Offset = 228h) [reset = X]

WKUP_VTM_GT_TH2_INT_EN_STAT_CLR is shown in Figure 9-13 and described in Table 9-28.

Return to Summary Table.

Enabled interrupt event status and clear MMR for interrupt GT_TH2 per voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_GT_TH2_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

Table 9-27. WKUP_VTM_GT_TH2_INT_EN_STAT_CLR Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0228h

Figure 9-13. WKUP_VTM_GT_TH2_INT_EN_STAT_CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1C-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 9-28. WKUP_VTM_GT_TH2_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1C	0h	Interrupt enabled pending bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status including the corresponding enable setting.

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9.15 WKUP_VTM_GT_TH2_INT_EN_SET Register (Offset = 234h) [reset = X]

WKUP_VTM_GT_TH2_INT_EN_SET is shown in Figure 9-14 and described in Table 9-30.

Return to Summary Table.

Enable set MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_GT_TH2_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Table 9-29. WKUP_VTM_GT_TH2_INT_EN_SET Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0234h

Figure 9-14. WKUP_VTM_GT_TH2_INT_EN_SET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1S-0h							

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-30. WKUP_VTM_GT_TH2_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1S	0h	Interrupt enable bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings.

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9.16 WKUP_VTM_GT_TH2_INT_EN_CLR Register (Offset = 238h) [reset = X]

WKUP_VTM_GT_TH2_INT_EN_CLR is shown in Figure 9-15 and described in Table 9-32.

Return to Summary Table.

Enable clear MMR for interrupt GT_TH2 for each voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_GT_TH2_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Table 9-31. WKUP_VTM_GT_TH2_INT_EN_CLR Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0238h

Figure 9-15. WKUP_VTM_GT_TH2_INT_EN_CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1C-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 9-32. WKUP_VTM_GT_TH2_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1C	0h	Interrupt enable bit for gt_th2_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings.

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9.17 WKUP_VTM_LT_TH0_INT_RAW_STAT_SET Register (Offset = 244h) [reset = X]

WKUP_VTM_LT_TH0_INT_RAW_STAT_SET is shown in Figure 9-16 and described in Table 9-34.

Return to Summary Table.

Interrupt RAW event status and set MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_LT_TH0_INT_EN_STAT_CLR are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

Table 9-33. WKUP_VTM_LT_TH0_INT_RAW_STAT_SET Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0244h

Figure 9-16. WKUP_VTM_LT_TH0_INT_RAW_STAT_SET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1S-0h							

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-34. WKUP_VTM_LT_TH0_INT_RAW_STAT_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1S	0h	Interrupt pending bit set for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the interrupt flag to be set. Used to manually force/drive an interrupt pending event. Reads return the raw pending status regardless of the corresponding enable setting.

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9.18 WKUP_VTM_LT_TH0_INT_EN_STAT_CLR Register (Offset = 248h) [reset = X]

WKUP_VTM_LT_TH0_INT_EN_STAT_CLR is shown in Figure 9-17 and described in Table 9-36.

Return to Summary Table.

Enabled interrupt event status and clear MMR for interrupt LT_TH0 per voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_LT_TH0_INT_RAW_STAT_SET are fully linked for write operation, but partially linked for reads, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR. However the reads to these 2 MMRs don't yield the same read data. Reads to *_INT_RAW_STAT_SET return the full "raw" events contents of the common linked MMR, whereas reads to MMR *_INT_EN_STAT_CLR will yield the masked-content of the linked MMR. The mask for the read is defined by the contents of the related MMR *_INT_EN_SET/CLR.

Table 9-35. WKUP_VTM_LT_TH0_INT_EN_STAT_CLR Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0248h

Figure 9-17. WKUP_VTM_LT_TH0_INT_EN_STAT_CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1C-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 9-36. WKUP_VTM_LT_TH0_INT_EN_STAT_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1C	0h	Interrupt enabled pending status bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the pending bit to be cleared. Reads return the enabled pending status that factors in the corresponding enable along with the pending status.

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9.19 WKUP_VTM_LT_TH0_INT_EN_SET Register (Offset = 254h) [reset = X]

WKUP_VTM_LT_TH0_INT_EN_SET is shown in Figure 9-18 and described in Table 9-38.

Return to Summary Table.

Enable set MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_LT_TH0_INT_EN_CLR are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Table 9-37. WKUP_VTM_LT_TH0_INT_EN_SET Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0254h

Figure 9-18. WKUP_VTM_LT_TH0_INT_EN_SET Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1S-0h							

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-38. WKUP_VTM_LT_TH0_INT_EN_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1S	0h	Interrupt enable bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be set to 1. Reads return the enable settings.

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9.20 WKUP_VTM_LT_TH0_INT_EN_CLR Register (Offset = 258h) [reset = X]

WKUP_VTM_LT_TH0_INT_EN_CLR is shown in Figure 9-19 and described in Table 9-40.

Return to Summary Table.

Enable clear MMR for interrupt LT_TH0 for each voltage domain. NOTE: This MMR and the companion MMR, WKUP_VTM_LT_TH0_INT_EN_SET are linked, which means that they are in fact a single common MMR, with 2 different write addresses/mechanisms, and thus the single common MMR updates with the writes to either MMR and reads to either of these 2 MMRs read the same content.

Table 9-39. WKUP_VTM_LT_TH0_INT_EN_CLR Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0258h

Figure 9-19. WKUP_VTM_LT_TH0_INT_EN_CLR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INT_VD							
R/W-X																								R/W1C-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 9-40. WKUP_VTM_LT_TH0_INT_EN_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7-0	INT_VD	R/W1C	0h	Interrupt enable bit for lt_th0_int from VD[7:0]. Write-operation: 0: Nothing happens. 1: Causes the bit to be cleared. Reads return the enable settings.

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9.21 WKUP_VTM_TMPSENS_CTRL_j Register (Offset = 300h + formula) [reset = X]

WKUP_VTM_TMPSENS_CTRL_j is shown in Figure 9-20 and described in Table 9-42.

Return to Summary Table.

Temperature Sensor Band-gap control register for sensor a.

Offset = 300h + (j * 20h); where j = 0h to 7h

Table 9-41. WKUP_VTM_TMPSENS_CTRL_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0300h + formula

Figure 9-20. WKUP_VTM_TMPSENS_CTRL_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED					LT_TH0_EN	GT_TH2_EN	GT_TH1_EN
R/W-X					R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED							
R/W-X							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-42. WKUP_VTM_TMPSENS_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R/W	X	
10	LT_TH0_EN	R/W	0h	Enable under-threshold0 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is < value set for threshold point 0. Reset value is POR only.
9	GT_TH2_EN	R/W	0h	Enable over-threshold2 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is > value set for threshold point 2. Reset value is POR only.
8	GT_TH1_EN	R/W	0h	Enable over-threshold1 event. Temp event/level control: 0 = Don't generate output level. 1 = Enable generation of event/level high when temperature reading is > value set for threshold point 1. Reset value is POR only.
7-0	RESERVED	R/W	X	

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9.22 WKUP_VTM_TMPSENS_STAT_j Register (Offset = 308h + formula) [reset = X]

WKUP_VTM_TMPSENS_STAT_j is shown in Figure 9-21 and described in Table 9-44.

Return to Summary Table.

Temperature Sensor Band-gap Status register for sensor a.

Offset = 308h + (j * 20h); where j = 0h to 7h

Table 9-43. WKUP_VTM_TMPSENS_STAT_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0308h + formula

Figure 9-21. WKUP_VTM_TMPSENS_STAT_j Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED				VD_MAP			
R-X				R-X			
15	14	13	12	11	10	9	8
MAXT_OUTRG_ALERT	LT_TH0_ALERT	GT_TH2_ALERT	GT_TH1_ALERT	EOC_FC_UPDATE	DATA_VALID	DATA_OUT	
R-X	R-0h	R-0h	R-0h	R-0h	R-X	R-X	
7	6	5	4	3	2	1	0
DATA_OUT							
R-X							

LEGEND: R = Read Only; *-n* = value after reset

Table 9-44. WKUP_VTM_TMPSENS_STAT_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R	X	
19-16	VD_MAP	R	X	Indicates the core voltage domain placement of the temp sensor. Device specific field. This field indicates in which core voltage domain, cVD, has been physically placed the temp-monitor. Valid values: 0x0 to 0xE where: 0x0 = VD_RTC, not present is some SoCs, 0x1 = VD_WKUP, 0x2 = VD_MCU, 0x3 = VD_CORE, not present is some SoCs, 0x4-0xE = Mapping varies between SoCs, 0xF = not implemented.
15	MAXT_OUTRG_ALERT	R	X	This bit will be driven to a level 1 for a given temperature monitor if it has its corresponding bit maxt_outrg_en = 1, and the temperature reading is reporting to be outside the max temperature supported, temp > programmed value. The level of this signal is a reflection, with some clock delays, of the temperature code reading. This is NOT an sticky bit. Reset value is POR only.

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Table 9-44. WKUP_VTM_TMPSENS_STAT_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	LT_TH0_ALERT	R	0h	This field reflects the status of the lt_th0_alert comparator result. The control MMR field lt_th0_en = 1 is required for this field to become 1. Reset value is at POR or clrz.
13	GT_TH2_ALERT	R	0h	This field reflects the status of the gt_th2_alert comparator result. The control MMR field gt_th2_en = 1 is required for this field to become 1. Reset value is at POR or clrz.
12	GT_TH1_ALERT	R	0h	This field reflects the status of the gt_th1_alert comparator result. The control MMR field gt_th1_en = 1 is required for this field to become 1. Reset value is at POR or clrz.
11	EOC_FC_UPDATE	R	0h	First time end of conversion. This field is reset to 0 every time VTM.mod_rst_n or VTM_TMPSENS[a]_CTRL.clrz are active. This bit will be set to 1 after the first time after reset release that data_valid transitions from 0 to 1, and remain at 1 until next time either of mod_rst_n or VTM_TMPSENS[a]_CTRL.clrz are active. Reset value is at POR or VTM_TMPSENS[a]_CTRL.clrz.
10	DATA_VALID	R	X	Data_valid signal value from sensor: ADC End of Conversion. End of conversion indicated by 0 to 1 transition. When high data_out(9:0) out of the temp-monitor is valid. This field doesn't reflect the instantaneous output from the temp-monitor. This field gets latched/updated in this VTM register when the data_valid value from temp-monitor toggles. Reset value is at POR or VTM_TMPSENS[a]_CTRL.clrz.
9-0	DATA_OUT	R	X	Data_out signal value from sensor: Temperature data from the ADC in monitor. Valid after VTM_TMPSENS[a]_STAT.eoc_fc_update = 1. This value will be latched in this VTM register every time monitor output data_valid transitions from 0 to 1. Reset value is POR only.

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9.23 WKUP_VTM_TMPSENS_TH_j Register (Offset = 30Ch + formula) [reset = X]

WKUP_VTM_TMPSENS_TH_j is shown in Figure 9-22 and described in Table 9-46.

Return to Summary Table.

Temperature Sensor Band-gap Threshold register for sensor a.

Offset = 30Ch + (j * 20h); where j = 0h to 7h

Table 9-45. WKUP_VTM_TMPSENS_TH_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 030Ch + formula

Figure 9-22. WKUP_VTM_TMPSENS_TH_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						TH1_VAL									
R/W-X						R/W-0h									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						TH0_VAL									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-46. WKUP_VTM_TMPSENS_TH_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	TH1_VAL	R/W	0h	Threshold point-1, thpt1, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is > th1_val[9:0] and gt_th1_en=1, that will cause the VTM to set the gt_th1_alert output. Once the current temp reading =< th1_val[9:0] then gt_th1_alert output will go to 0. Reset value is at POR only.
15-10	RESERVED	R/W	X	
9-0	TH0_VAL	R/W	0h	Threshold point-0, thpt0, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is < th0_val[9:0] and lt_th0_en=1, that will cause the VTM to set the lt_th0_alert output. Once the current temp reading => th0_val[9:0] then lt_th0_alert output will go to 0. Reset value is at POR only.

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9.24 WKUP_VTM_TMPSENS_TH2_j Register (Offset = 310h + formula) [reset = X]

WKUP_VTM_TMPSENS_TH2_j is shown in Figure 9-23 and described in Table 9-48.

Return to Summary Table.

Temperature Sensor Band-gap Threshold register 2 for sensor a.

Offset = 310h + (j * 20h); where j = 0h to 7h

Table 9-47. WKUP_VTM_TMPSENS_TH2_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG1	4204 0310h + formula

Figure 9-23. WKUP_VTM_TMPSENS_TH2_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						TH2_VAL									
R/W-X																						R/W-0h									

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-48. WKUP_VTM_TMPSENS_TH2_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RESERVED	R/W	X	
9-0	TH2_VAL	R/W	0h	Threshold point-2, thpt2, temp-value. Is a 10-bit temperature reference value. This is the 10-bit value that represents a high temperature point, as per sensor spec, with which to compare the present temperature reading, same 10-bit format. If the current temperature reading is > th2_val[9:0] and gt_th2_en=1, that will cause the VTM to set the gt_th2_alert output. Once the current temp reading =< th2_val[9:0] then gt_th2_alert output will go to 0. Reset value is at POR only.

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9.25 WKUP_VTM0_MMR_VBUSP_CFG2 Registers

Table 9-50 lists the memory-mapped registers for the WKUP_VTM0_MMR_VBUSP_CFG2 registers. All register offset addresses not listed in Table 9-50 should be considered as reserved locations and the register contents should not be modified.

This region contains critical control MMRs that should be protected and only accessed by a trusted entity. All the MMRs in this region by default use mod_g_rst_n as their reset unless specified otherwise.

Table 9-49. WKUP_VTM0_MMR_VBUSP_CFG2 Instances

Instance	Base Address
WKUP_VTM0_MMR_VBUSP_CFG2	4204 0000h

Table 9-50. WKUP_VTM0_MMR_VBUSP_CFG2 Registers

Offset	Acronym	Register Name	WKUP_VTM0_MMR_VBUSP_CFG2 Physical Address
8h	WKUP_VTM_CLK_CTRL		4205 0008h
Ch	WKUP_VTM_MISC_CTRL		4205 000Ch
10h	WKUP_VTM_MISC_CTRL2		4205 0010h
20h	WKUP_VTM_SAMPLE_CTRL		4205 0020h
300h + formula	WKUP_VTM_TMPSENS_CTRL_j		4205 0300h + formula
304h + formula	WKUP_VTM_TMPSENS_TRIM_j		4205 0304h + formula

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9.26 WKUP_VTM_CLK_CTRL Register (Offset = 8h) [reset = X]

WKUP_VTM_CLK_CTRL is shown in Figure 9-24 and described in Table 9-52.

Return to Summary Table.

VTM clock related control MMR. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary. The e-fuse value is sampled from input port efuse_tsens_clk_src_div. The tsens_clks_src_div field is Device specific.

Table 9-51. WKUP_VTM_CLK_CTRL Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG2	4205 0008h

Figure 9-24. WKUP_VTM_CLK_CTRL Register

31	30	29	28	27	26	25	24
TSENS_CLK_SEL	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED			TSENS_CLK_DIV				
R/W-X			R/W-0h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-52. WKUP_VTM_CLK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	TSENS_CLK_SEL	R/W	0h	Temperature sensor clock source selector. Device specific. 0 = fix_ref_clk as source. 1 = fix_ref2_clk as source. Reset value is at POR only.
30-5	RESERVED	R/W	X	
4-0	TSENS_CLK_DIV	R/W	0h	Temperature sensor clock source divider selector. Device specific. Divider uses select reference clock as source. 0 = 1x divide. 1 = 2x divide. ... 15 = 16x divide. ... 63 = 64x divide. Reset value is from e-fuse at POR, efuse_tsens_clk_src_div.

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9.27 WKUP_VTM_MISC_CTRL Register (Offset = Ch) [reset = X]

WKUP_VTM_MISC_CTRL is shown in Figure 9-25 and described in Table 9-54.

Return to Summary Table.

VTM miscellaneous control bits.

Table 9-53. WKUP_VTM_MISC_CTRL Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG2	4205 000Ch

Figure 9-25. WKUP_VTM_MISC_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							ANY_MAXT_OUTRG_ALERT_EN
R/W-X							R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-54. WKUP_VTM_MISC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	ANY_MAXT_OUTRG_ALERT_EN	R/W	0h	This bit when enabled will cause the VTM's output therm_maxtemp_outrange_alert to be driven high, if any of the sources for the maxt_outrg_alert, is set high. Whenever all the maxt_outrg_alert enabled sensor alerts, out of the 8 possible are back to 0 then the output, therm_maxtemp_outrange_alert, will also return to 0. Reset is at POR only.

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9.28 WKUP_VTM_MISC_CTRL2 Register (Offset = 10h) [reset = X]

WKUP_VTM_MISC_CTRL2 is shown in Figure 9-26 and described in Table 9-56.

Return to Summary Table.

VTM miscellaneous control bits.

Table 9-55. WKUP_VTM_MISC_CTRL2 Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG2	4205 0010h

Figure 9-26. WKUP_VTM_MISC_CTRL2 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED						MAXT_OUTRG_ALERT_THR0									
R/W-X						R/W-0h									
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						MAXT_OUTRG_ALERT_THR									
R/W-X						R/W-0h									

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-56. WKUP_VTM_MISC_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-26	RESERVED	R/W	X	
25-16	MAXT_OUTRG_ALERT_THR0	R/W	0h	This defines the global max temperature out of range safe sample value. If the alert is enabled globally and for the sensor and the sensor reads a value <= this value then the alert is cleared after being triggered. This safe threshold defines at what temp the alert can be cleared. Reset is at POR only.
15-10	RESERVED	R/W	X	
9-0	MAXT_OUTRG_ALERT_THR	R/W	0h	This defines the global max temperature out of range sample value. If the alert is enabled globally and for the sensor and the sensor reads a value >= this value then the alert is triggered. Reset is at POR only.

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9.29 WKUP_VTM_SAMPLE_CTRL Register (Offset = 20h) [reset = X]

WKUP_VTM_SAMPLE_CTRL is shown in Figure 9-27 and described in Table 9-58.

Return to Summary Table.

VTM sample related control MMR. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary. The e-fuse value is sampled from input port efuse_sample_clk_cnt. The sample_clk_cnt field is Device specific.

Table 9-57. WKUP_VTM_SAMPLE_CTRL Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG2	4205 0020h

Figure 9-27. WKUP_VTM_SAMPLE_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SAMPLE_PER_CNT															
R/W-X																R/W-0h															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-58. WKUP_VTM_SAMPLE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-0	SAMPLE_PER_CNT	R/W	0h	Temperature sensor sample period count selector. Device specific. This defines the sample period or number of sensor clocks between consecutive samples of the sensor allowed, from the start of the previous sample request to the start of the next sample request. After the sample is received the sensor status MMR fields will not be updated and the sensor will remain disabled. Reset value is from e-fuse at POR, efuse_sample_per_cnt.

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9.30 WKUP_VTM_TMPSENS_CTRL_j Register (Offset = 300h + formula) [reset = X]

WKUP_VTM_TMPSENS_CTRL_j is shown in Figure 9-28 and described in Table 9-60.

Return to Summary Table.

Temperature Sensor Band-gap control register for sensor a.

Offset = 300h + (j * 20h); where j = 0h to 7h

Table 9-59. WKUP_VTM_TMPSENS_CTRL_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG2	4205 0300h + formula

Figure 9-28. WKUP_VTM_TMPSENS_CTRL_j Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED				MAXT_OUTRG_EN	RESERVED		
R/W-X				R/W-0h	R/W-X		
7	6	5	4	3	2	1	0
RESERVED	CLRZ	SOC	CONT	RESERVED			
R/W-X	R/W-1h	R/W-0h	R/W-0h	R/W-X			

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-60. WKUP_VTM_TMPSENS_CTRL_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11	MAXT_OUTRG_EN	R/W	0h	Enable out-of-range event. This bit enables generation of the alert in case the given temperature sensors generates a temp code above a programmed max. 0 = Don't generate alert. 1 = Generate alert. Reset value is POR only.
10-7	RESERVED	R/W	X	
6	CLRZ	R/W	1h	Temp-Monitor control: 0 = Reset all Temp-monitor digital outputs. 1 = Allow operation of sensor. Reset value is POR only.
5	SOC	R/W	0h	Temp-Monitor control: ADC Start of Conversion. A transition from 0 to 1 starts a new ADC conversion cycle. The bit with automatically clear when the conversion has completed. This mode is not valid when already in continuous mode. Reset value is POR only.

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Table 9-60. WKUP_VTM_TMPSENS_CTRL_j Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	CONT	R/W	0h	Temp-Monitor control: ADC Continuous mode. Setting this mode enables the VTM to continuously monitor the sensor automatically. Each sample period the sensor will be accessed and the results captured. Reset value is POR only.
3-0	RESERVED	R/W	X	

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9.31 WKUP_VTM_TMPSENS_TRIM_j Register (Offset = 304h + formula) [reset = X]

WKUP_VTM_TMPSENS_TRIM_j is shown in Figure 9-29 and described in Table 9-62.

Return to Summary Table.

Temperature Sensor Band-gap trim values register for sensor a. The default reset values will not be necessarily overwritten. The write capability in the MMR is for having the option to debug and have software driven adjustments if necessary.

Offset = 304h + (j * 20h); where j = 0h to 7h

Table 9-61. WKUP_VTM_TMPSENS_TRIM_j Instances

Instance	Physical Address
WKUP_VTM0_MMR_VBUSP_CFG2	4205 0304h + formula

Figure 9-29. WKUP_VTM_TMPSENS_TRIM_j Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R/W-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TRIMO						RESERVED			TRIMG				
R/W-X		R/W-X						R/W-X			R/W-X				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-62. WKUP_VTM_TMPSENS_TRIM_j Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-8	TRIMO	R/W	X	Trim offset bits in the temp sensor. Reset value is from e-fuse at POR, efuse_tmpsens[a]_trimo.
7-5	RESERVED	R/W	X	
4-0	TRIMG	R/W	X	Trim gain bits in the temp sensor. Reset value is from e-fuse at POR, efuse_tmpsens[a]_trimg.

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9.32 WKUP_VTM0_ECCAGGR_CFG Registers

Table 9-64 lists the memory-mapped registers for the WKUP_VTM0_ECCAGGR_CFG registers. All register offset addresses not listed in Table 9-64 should be considered as reserved locations and the register contents should not be modified.

Note

For more information about ECC Aggregator functionality, see *ECC Aggregator*.

Table 9-63. WKUP_VTM0_ECCAGGR_CFG Instances

Instance	Base Address
WKUP_VTM0_ECCAGGR_CFG	4281 0000h

Table 9-64. WKUP_VTM0_ECCAGGR_CFG Registers

Offset	Acronym	Register Name	WKUP_VTM0_ECCAGGR_CFG Physical Address
0h	WKUP_VTM_REV	Aggregator Revision Register	4281 0000h
8h	WKUP_VTM_VECTOR	ECC WKUP_VTM_VECTOR Register	4281 0008h
Ch	WKUP_VTM_STAT	Misc Status	4281 000Ch
10h + formula	WKUP_VTM_RESERVED_SVBUS_y	Reserved Area for Serial VBUS Registers	4281 0010h + formula
3Ch	WKUP_VTM_SEC_EOI_REG	EOI Register	4281 003Ch
40h	WKUP_VTM_SEC_STATUS_REG0	Interrupt Status Register 0	4281 0040h
80h	WKUP_VTM_SEC_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4281 0080h
C0h	WKUP_VTM_SEC_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4281 00C0h
13Ch	WKUP_VTM_DED_EOI_REG	EOI Register	4281 013Ch
140h	WKUP_VTM_DED_STATUS_REG0	Interrupt Status Register 0	4281 0140h
180h	WKUP_VTM_DED_ENABLE_SET_REG0	Interrupt Enable Set Register 0	4281 0180h
1C0h	WKUP_VTM_DED_ENABLE_CLR_REG0	Interrupt Enable Clear Register 0	4281 01C0h
200h	WKUP_VTM_AGGR_ENABLE_SET	AGGR interrupt enable set Register	4281 0200h
204h	WKUP_VTM_AGGR_ENABLE_CLR	AGGR interrupt enable clear Register	4281 0204h
208h	WKUP_VTM_AGGR_STATUS_SET	AGGR interrupt status set Register	4281 0208h
20Ch	WKUP_VTM_AGGR_STATUS_CLR	AGGR interrupt status clear Register	4281 020Ch

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9.33 WKUP_VTM_REV Register (Offset = 0h) [reset = 66A0EA00h]

WKUP_VTM_REV is shown in Figure 9-30 and described in Table 9-66.

Return to Summary Table.

Revision parameters

Table 9-65. WKUP_VTM_REV Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 0000h

Figure 9-30. WKUP_VTM_REV Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE_ID											
R-1h		R-2h		R-6A0h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REVRTL					REVMAJ			CUSTOM		REVMIN					
R-1Dh					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 9-66. WKUP_VTM_REV Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	Scheme
29-28	BU	R	2h	bu
27-16	MODULE_ID	R	6A0h	Module ID
15-11	REVRTL	R	1Dh	RTL version
10-8	REVMAJ	R	2h	Major version
7-6	CUSTOM	R	0h	Custom version
5-0	REVMIN	R	0h	Minor version

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9.34 WKUP_VTM_VECTOR Register (Offset = 8h) [reset = X]

WKUP_VTM_VECTOR is shown in Figure 9-31 and described in Table 9-68.

Return to Summary Table.

ECC WKUP_VTM_VECTOR Register

Table 9-67. WKUP_VTM_VECTOR Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 0008h

Figure 9-31. WKUP_VTM_VECTOR Register

31	30	29	28	27	26	25	24
RESERVED							RD_SVBUS_DONE
R/W-X							R/W1C-0h
23	22	21	20	19	18	17	16
RD_SVBUS_ADDRESS							
R/W-0h							
15	14	13	12	11	10	9	8
RD_SVBUS	RESERVED				ECC_VECTOR		
R/W1S-0h	R/W-X				R/W-0h		
7	6	5	4	3	2	1	0
ECC_VECTOR							
R/W-0h							

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; R/W1S = Read/Write 1 to Set Bit; -*n* = value after reset

Table 9-68. WKUP_VTM_VECTOR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	X	
24	RD_SVBUS_DONE	R/W1C	0h	Status to indicate if read on serial VBUS is complete, write of any value will clear this bit.
23-16	RD_SVBUS_ADDRESS	R/W	0h	Read address
15	RD_SVBUS	R/W1S	0h	Write 1 to trigger a read on the serial VBUS
14-11	RESERVED	R/W	X	
10-0	ECC_VECTOR	R/W	0h	Value written to select the corresponding ECC RAM for control or status

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9.35 WKUP_VTM_STAT Register (Offset = Ch) [reset = X]

WKUP_VTM_STAT is shown in Figure 9-32 and described in Table 9-70.

Return to Summary Table.

Misc Status

Table 9-69. WKUP_VTM_STAT Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 000Ch

Figure 9-32. WKUP_VTM_STAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					NUM_RAMS										
R-X																					R-4h										

LEGEND: R = Read Only; *-n* = value after reset

Table 9-70. WKUP_VTM_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	X	
10-0	NUM_RAMS	R	4h	Indicates the number of RAMS serviced by the ECC aggregator

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9.36 WKUP_VTM_RESERVED_SVBUS_y Register (Offset = 10h + formula) [reset = 0h]

WKUP_VTM_RESERVED_SVBUS_y is shown in Figure 9-33 and described in Table 9-72.

Return to Summary Table.

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Offset = 10h + (y * 4h); where y = 0h to 7h

Table 9-71. WKUP_VTM_RESERVED_SVBUS_y Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 0010h + formula

Figure 9-33. WKUP_VTM_RESERVED_SVBUS_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 9-72. WKUP_VTM_RESERVED_SVBUS_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	DATA	R/W	0h	Serial VBUS register data

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9.37 WKUP_VTM_SEC_EOI_REG Register (Offset = 3Ch) [reset = X]

WKUP_VTM_SEC_EOI_REG is shown in Figure 9-34 and described in Table 9-74.

Return to Summary Table.

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 9-73. WKUP_VTM_SEC_EOI_REG Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 003Ch

Figure 9-34. WKUP_VTM_SEC_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-74. WKUP_VTM_SEC_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

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9.38 WKUP_VTM_SEC_STATUS_REG0 Register (Offset = 40h) [reset = X]

WKUP_VTM_SEC_STATUS_REG0 is shown in Figure 9-35 and described in Table 9-76.

Return to Summary Table.

Interrupt Status Register 0

Table 9-75. WKUP_VTM_SEC_STATUS_REG0 Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 0040h

Figure 9-35. WKUP_VTM_SEC_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	ECCAGG_PEND
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-76. WKUP_VTM_SEC_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_PEND	R/W1S	0h	Interrupt Pending Status for eccagg_pend

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9.39 WKUP_VTM_SEC_ENABLE_SET_REG0 Register (Offset = 80h) [reset = X]

WKUP_VTM_SEC_ENABLE_SET_REG0 is shown in Figure 9-36 and described in Table 9-78.

Return to Summary Table.

Interrupt Enable Set Register 0

Table 9-77. WKUP_VTM_SEC_ENABLE_SET_REG0 Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 0080h

Figure 9-36. WKUP_VTM_SEC_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	ECCAGG_ENABLE_SET
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-78. WKUP_VTM_SEC_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for eccagg_pend

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9.40 WKUP_VTM_SEC_ENABLE_CLR_REG0 Register (Offset = C0h) [reset = X]

WKUP_VTM_SEC_ENABLE_CLR_REG0 is shown in Figure 9-37 and described in Table 9-80.

Return to Summary Table.

Interrupt Enable Clear Register 0

Table 9-79. WKUP_VTM_SEC_ENABLE_CLR_REG0 Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 00C0h

Figure 9-37. WKUP_VTM_SEC_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
R/W-X				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 9-80. WKUP_VTM_SEC_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for eccagg_pend

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9.41 WKUP_VTM_DED_EOI_REG Register (Offset = 13Ch) [reset = X]

WKUP_VTM_DED_EOI_REG is shown in Figure 9-38 and described in Table 9-82.

Return to Summary Table.

EOI Register

The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. The software interrupt handler must write to the EOI register at the end of the current interrupt processing routine, so that new events can re-trigger the pulse interrupt signal again. For level interrupt signals the EOI register is not functional and must not be used.

Table 9-81. WKUP_VTM_DED_EOI_REG Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 013Ch

Figure 9-38. WKUP_VTM_DED_EOI_REG Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED							EOI_WR
R/W-X							R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-82. WKUP_VTM_DED_EOI_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R/W	X	
0	EOI_WR	R/W1S	0h	EOI Register

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9.42 WKUP_VTM_DED_STATUS_REG0 Register (Offset = 140h) [reset = X]

WKUP_VTM_DED_STATUS_REG0 is shown in Figure 9-39 and described in Table 9-84.

Return to Summary Table.

Interrupt Status Register 0

Table 9-83. WKUP_VTM_DED_STATUS_REG0 Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 0140h

Figure 9-39. WKUP_VTM_DED_STATUS_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	ECCAGG_PEND
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-84. WKUP_VTM_DED_STATUS_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_PEND	R/W1S	0h	Interrupt Pending Status for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_PEND	R/W1S	0h	Interrupt Pending Status for eccagg_pend

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9.43 WKUP_VTM_DED_ENABLE_SET_REG0 Register (Offset = 180h) [reset = X]

WKUP_VTM_DED_ENABLE_SET_REG0 is shown in Figure 9-40 and described in Table 9-86.

Return to Summary Table.

Interrupt Enable Set Register 0

Table 9-85. WKUP_VTM_DED_ENABLE_SET_REG0 Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 0180h

Figure 9-40. WKUP_VTM_DED_ENABLE_SET_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	ECCAGG_ENABLE_SET
R/W-X				R/W1S-0h	R/W1S-0h	R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-86. WKUP_VTM_DED_ENABLE_SET_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_ENABLE_SET	R/W1S	0h	Interrupt Enable Set Register for eccagg_pend

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9.44 WKUP_VTM_DED_ENABLE_CLR_REG0 Register (Offset = 1C0h) [reset = X]

WKUP_VTM_DED_ENABLE_CLR_REG0 is shown in Figure 9-41 and described in Table 9-88.

Return to Summary Table.

Interrupt Enable Clear Register 0

Table 9-87. WKUP_VTM_DED_ENABLE_CLR_REG0 Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 01C0h

Figure 9-41. WKUP_VTM_DED_ENABLE_CLR_REG0 Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	ECCAGG_ENABLE_CLR
R/W-X				R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; *-n* = value after reset

Table 9-88. WKUP_VTM_DED_ENABLE_CLR_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3	K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_K3VTM_N16FFC_CFG_CBASS_CFG_SCR_SCR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_k3vtm_n16ffc_cfg_cbass_cfg_scr_scr_edc_ctrl_busecc_pend
2	K3VTM_N16FFC_CFG_CBASS_VBUSP_P2P_BRIDGE_VBUSP_BRIDGE_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_cfg_cbass_vbusp_p2p_bridge_vbusp_bridge_busecc_pend
1	K3VTM_N16FFC_MMR_EDC_CTRL_BUSECC_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for k3vtm_n16ffc_mmr_edc_ctrl_busecc_pend
0	ECCAGG_ENABLE_CLR	R/W1C	0h	Interrupt Enable Clear Register for eccagg_pend

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9.45 WKUP_VTM_AGGR_ENABLE_SET Register (Offset = 200h) [reset = X]

WKUP_VTM_AGGR_ENABLE_SET is shown in Figure 9-42 and described in Table 9-90.

Return to Summary Table.

AGGR interrupt enable set Register

Table 9-89. WKUP_VTM_AGGR_ENABLE_SET Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 0200h

Figure 9-42. WKUP_VTM_AGGR_ENABLE_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1S-0h	R/W1S-0h

LEGEND: R/W = Read/Write; R/W1S = Read/Write 1 to Set Bit; *-n* = value after reset

Table 9-90. WKUP_VTM_AGGR_ENABLE_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1S	0h	interrupt enable set for svbus timeout errors
0	PARITY	R/W1S	0h	interrupt enable set for parity errors

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9.46 WKUP_VTM_AGGR_ENABLE_CLR Register (Offset = 204h) [reset = X]

WKUP_VTM_AGGR_ENABLE_CLR is shown in Figure 9-43 and described in Table 9-92.

Return to Summary Table.

AGGR interrupt enable clear Register

Table 9-91. WKUP_VTM_AGGR_ENABLE_CLR Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 0204h

Figure 9-43. WKUP_VTM_AGGR_ENABLE_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED						TIMEOUT	PARITY
R/W-X						R/W1C-0h	R/W1C-0h

LEGEND: R/W = Read/Write; R/W1C = Read/Write 1 to Clear Bit; -*n* = value after reset

Table 9-92. WKUP_VTM_AGGR_ENABLE_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RESERVED	R/W	X	
1	TIMEOUT	R/W1C	0h	interrupt enable clear for svbus timeout errors
0	PARITY	R/W1C	0h	interrupt enable clear for parity errors

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9.47 WKUP_VTM_AGGR_STATUS_SET Register (Offset = 208h) [reset = X]

WKUP_VTM_AGGR_STATUS_SET is shown in Figure 9-44 and described in Table 9-94.

Return to Summary Table.

AGGR interrupt status set Register

Table 9-93. WKUP_VTM_AGGR_STATUS_SET Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 0208h

Figure 9-44. WKUP_VTM_AGGR_STATUS_SET Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wincr-0h		R/Wincr-0h	

LEGEND: R/W = Read/Write; R/Wincr = Read/Write to Increment Field; -*n* = value after reset

Table 9-94. WKUP_VTM_AGGR_STATUS_SET Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wincr	0h	interrupt status set for svbus timeout errors
1-0	PARITY	R/Wincr	0h	interrupt status set for parity errors

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9.48 WKUP_VTM_AGGR_STATUS_CLR Register (Offset = 20Ch) [reset = X]

WKUP_VTM_AGGR_STATUS_CLR is shown in Figure 9-45 and described in Table 9-96.

Return to Summary Table.

AGGR interrupt status clear Register

Table 9-95. WKUP_VTM_AGGR_STATUS_CLR Instances

Instance	Physical Address
WKUP_VTM0_ECCAGGR_CFG	4281 020Ch

Figure 9-45. WKUP_VTM_AGGR_STATUS_CLR Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED				TIMEOUT		PARITY	
R/W-X				R/Wdecr-0h		R/Wdecr-0h	

LEGEND: R/W = Read/Write; R/Wdecr = Read/Write to Decrement Field; *-n* = value after reset

Table 9-96. WKUP_VTM_AGGR_STATUS_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R/W	X	
3-2	TIMEOUT	R/Wdecr	0h	interrupt status clear for svbus timeout errors
1-0	PARITY	R/Wdecr	0h	interrupt status clear for parity errors

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10 PSC Registers

10.1 WKUP_PSC0 Registers

Table 10-2 lists the memory-mapped registers for the WKUP_PSC0 registers. All register offset addresses not listed in Table 10-2 should be considered as reserved locations and the register contents should not be modified.

MMRs in region 0

Note

PSC functions are controlled via DMSC. For more information how to use DMSC, see TISCI API available at ti.com **(the TISCI API is under development)**.

Table 10-1. WKUP_PSC0 Instances

Instance	Base Address
WKUP_PSC0	4200 0000h

Table 10-2. WKUP_PSC0 Registers

Offset	Acronym	Register Name	WKUP_PSC0 Physical Address
0h	WKUP_PSC0_PID	WKUP_PSC0_PID register	4200 0000h
10h	WKUP_PSC0_GBLCTL	Global Control Register	4200 0010h
14h	WKUP_PSC0_GBLSTAT	Global Status Register	4200 0014h
18h	WKUP_PSC0_INTEVAL	Interrupt Evaluation Register	4200 0018h
40h	WKUP_PSC0_MERRPR	Module Error Pending Register	4200 0040h
50h	WKUP_PSC0_MERRCR	Module Error Clear Register	4200 0050h
60h	WKUP_PSC0_PERRPR	Power Error Pending Register	4200 0060h
68h	WKUP_PSC0_PERRCR	Power Error Clear Register	4200 0068h
70h	WKUP_PSC0_EPCPR	External Power Error Pending Register	4200 0070h
78h	WKUP_PSC0_EPCCR	External Power Control Clear Register	4200 0078h
100h	WKUP_PSC0_RAILSTAT	Power Rail Status Register	4200 0100h
104h	WKUP_PSC0_RAILCTL	Power Rail Counter Control Register	4200 0104h
108h	WKUP_PSC0_RAILSEL	Power Rail Counter Select Register	4200 0108h
120h	WKUP_PSC0_PTCMD	Power Domain Transition Command Register	4200 0120h
128h	WKUP_PSC0_PTSTAT	Power Domain Transition Status Register	4200 0128h
200h + formula	WKUP_PSC0_PDSTAT_y	Power Domain Status Register	4200 0200h + formula
300h + formula	WKUP_PSC0_PDCTL_y	Power Domain Control Register	4200 0300h + formula
400h + formula	WKUP_PSC0_PDCFG_y	Power Domain Configuration Register	4200 0400h + formula
600h + formula	WKUP_PSC0_MDCFG_y	Module Configuration Register	4200 0600h + formula
800h + formula	WKUP_PSC0_MDSTAT_y	Module Status Register	4200 0800h + formula
A00h + formula	WKUP_PSC0_MDCTL_y	Module Control Register	4200 0A00h + formula

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10.2 WKUP_PSC0_PID Register (Offset = 0h) [reset = 44820200h]

WKUP_PSC0_PID is shown in Figure 10-1 and described in Table 10-4.

Return to Summary Table.

The peripheral identification register is a constant register that contains the ID and ID revision number for that module. The WKUP_PSC0_PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect) meaning that the values within this register should be hard-coded with the appropriate values and must not change from their hard-coded values.

Table 10-3. WKUP_PSC0_PID Instances

Instance	Physical Address
WKUP_PSC0	4200 0000h

Figure 10-1. WKUP_PSC0_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R-1h		R-0h		R-482h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-0h					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 10-4. WKUP_PSC0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	WKUP_PSC0_PID register scheme
29-28	BU	R	0h	Business Unit
27-16	FUNC	R	482h	Module ID
15-11	RTL	R	0h	RTL revision. Will vary depending on release
10-8	MAJOR	R	2h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

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10.3 WKUP_PSC0_GBLCTL Register (Offset = 10h) [reset = X]

WKUP_PSC0_GBLCTL is shown in Figure 10-2 and described in Table 10-6.

Return to Summary Table.

This register contains global control to PSC.

Table 10-5. WKUP_PSC0_GBLCTL Instances

Instance	Physical Address
WKUP_PSC0	4200 0010h

Figure 10-2. WKUP_PSC0_GBLCTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IO_ANA_CTL								RESERVED							
R-0h								R-X							

LEGEND: R = Read Only; *-n* = value after reset

Table 10-6. WKUP_PSC0_GBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-8	IO_ANA_CTL	R	0h	General purpose IO/Analog PowerDown control. Directly drives io_ana_pdctl_po [7:0] outputs.
7-0	RESERVED	R	X	

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10.4 WKUP_PSC0_GBLSTAT Register (Offset = 14h) [reset = X]

WKUP_PSC0_GBLSTAT is shown in Figure 10-3 and described in Table 10-8.

Return to Summary Table.

This register shows the PSC global status.

Table 10-7. WKUP_PSC0_GBLSTAT Instances

Instance	Physical Address
WKUP_PSC0	4200 0014h

Figure 10-3. WKUP_PSC0_GBLSTAT Register

31	30	29	28	27	26	25	24
RESERVED				EF_SMRFLEX			
R-X				R-0h			
23	22	21	20	19	18	17	16
EF_SMRFLEX							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							OVRIDE
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 10-8. WKUP_PSC0_GBLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	EF_SMRFLEX	R	0h	Smart reflex class0 bits
15-1	RESERVED	R	X	
0	OVRIDE	R	0h	PSC Override Status

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10.5 WKUP_PSC0_INTEVAL Register (Offset = 18h) [reset = X]

WKUP_PSC0_INTEVAL is shown in Figure 10-4 and described in Table 10-10.

Return to Summary Table.

This register has no storage. Read from this register returns 0.

Table 10-9. WKUP_PSC0_INTEVAL Instances

Instance	Physical Address
WKUP_PSC0	4200 0018h

Figure 10-4. WKUP_PSC0_INTEVAL Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED				GOSET	EPCSET	ERRSET	RESERVED
W-X				W-0h	W-0h	W-0h	W-X
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED					EPCEV	ERREV	ALLEV
W-X					W-0h	W-0h	W-0h

LEGEND: W = Write Only; *-n* = value after reset

Table 10-10. WKUP_PSC0_INTEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	W	X	
19	GOSET	W	0h	GOSTAT Interrupt Set
18	EPCSET	W	0h	External Power Control Interrupt Set
17	ERRSET	W	0h	Combined Interrupt Set
16-3	RESERVED	W	X	
2	EPCEV	W	0h	External Power Control Interrupt Set
1	ERREV	W	0h	Re_evaluate Error Interrupt
0	ALLEV	W	0h	Re_evaluate combined PSC interrupt 0h = Write of 0 has no effect 1h = Re-evaluate the combined PSC interrupt PSC_ALLINT

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10.6 WKUP_PSC0_MERRPR Register (Offset = 40h) [reset = 0h]

WKUP_PSC0_MERRPR is shown in Figure 10-5 and described in Table 10-12.

Return to Summary Table.

This register records pending error conditions for all modules. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Table 10-11. WKUP_PSC0_MERRPR Instances

Instance	Physical Address
WKUP_PSC0	4200 0040h

Figure 10-5. WKUP_PSC0_MERRPR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M																															
R-0h																															

LEGEND: R = Read Only; -*n* = value after reset

Table 10-12. WKUP_PSC0_MERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	M	R	0h	Records pending error conditions. Each bit n represents a module.

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10.7 WKUP_PSC0_MERRCR Register (Offset = 50h) [reset = 0h]

WKUP_PSC0_MERRCR is shown in Figure 10-6 and described in Table 10-14.

Return to Summary Table.

This register has no storage. Read from this register returns 0. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Table 10-13. WKUP_PSC0_MERRCR Instances

Instance	Physical Address
WKUP_PSC0	4200 0050h

Figure 10-6. WKUP_PSC0_MERRCR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M																															
W1C-0h																															

LEGEND: W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 10-14. WKUP_PSC0_MERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	M	W1C	0h	Write of 1 clears the corresponding WKUP_PSC0_MERRPR bit.

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10.8 WKUP_PSC0_PERRPR Register (Offset = 60h) [reset = 0h]

WKUP_PSC0_PERRPR is shown in Figure 10-7 and described in Table 10-16.

Return to Summary Table.

This register records pending error conditions for each power domain. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-15. WKUP_PSC0_PERRPR Instances

Instance	Physical Address
WKUP_PSC0	4200 0060h

Figure 10-7. WKUP_PSC0_PERRPR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 10-16. WKUP_PSC0_PERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	P	R	0h	Power Domain n Error Condition. Each bit n represents a power domain.

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10.9 WKUP_PSC0_PERRCR Register (Offset = 68h) [reset = 0h]

WKUP_PSC0_PERRCR is shown in Figure 10-8 and described in Table 10-18.

Return to Summary Table.

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-17. WKUP_PSC0_PERRCR Instances

Instance	Physical Address
WKUP_PSC0	4200 0068h

Figure 10-8. WKUP_PSC0_PERRCR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P																															
W1C-0h																															

LEGEND: W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 10-18. WKUP_PSC0_PERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	P	W1C	0h	Write of 1 clears the corresponding WKUP_PSC0_PERRPR bit.

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10.10 WKUP_PSC0_EPCPR Register (Offset = 70h) [reset = 0h]

WKUP_PSC0_EPCPR is shown in Figure 10-9 and described in Table 10-20.

Return to Summary Table.

This register records pending external power control conditions. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-19. WKUP_PSC0_EPCPR Instances

Instance	Physical Address
WKUP_PSC0	4200 0070h

Figure 10-9. WKUP_PSC0_EPCPR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 10-20. WKUP_PSC0_EPCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EPC	R	0h	External Power Control Intervention Request for Power Domain n

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10.11 WKUP_PSC0_EPCCR Register (Offset = 78h) [reset = 0h]

WKUP_PSC0_EPCCR is shown in Figure 10-10 and described in Table 10-22.

Return to Summary Table.

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-21. WKUP_PSC0_EPCCR Instances

Instance	Physical Address
WKUP_PSC0	4200 0078h

Figure 10-10. WKUP_PSC0_EPCCR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC																															
W1C-0h																															

LEGEND: W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 10-22. WKUP_PSC0_EPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EPC	W1C	0h	Write of 1 clears the corresponding WKUP_PSC0_EPCPR bit

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10.12 WKUP_PSC0_RAILSTAT Register (Offset = 100h) [reset = X]

WKUP_PSC0_RAILSTAT is shown in Figure 10-11 and described in Table 10-24.

Return to Summary Table.

This register is a read-only and shows the current rail requestor whose request is being granted and the current value of the counter associated with this requestor.

Table 10-23. WKUP_PSC0_RAILSTAT Instances

Instance	Physical Address
WKUP_PSC0	4200 0100h

Figure 10-11. WKUP_PSC0_RAILSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			RAILNUM					RESERVED							
R-X			R-0h					R-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED								RAILCNT							
R-X								R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 10-24. WKUP_PSC0_RAILSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	X	
28-24	RAILNUM	R	0h	Indicates Current Rail Requestor being processed by GPSC
23-8	RESERVED	R	X	
7-0	RAILCNT	R	0h	Indicates the current rail counter value

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10.13 WKUP_PSC0_RAILCTL Register (Offset = 104h) [reset = X]

WKUP_PSC0_RAILCTL is shown in Figure 10-12 and described in Table 10-26.

Return to Summary Table.

This register is user programmable. It holds the counter values for rail counter. User can select one of the two counter values to be used for each power domain (see WKUP_PSC0_RAILSEL register).

Table 10-25. WKUP_PSC0_RAILCTL Instances

Instance	Physical Address
WKUP_PSC0	4200 0104h

Figure 10-12. WKUP_PSC0_RAILCTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RAILCTR1								RAILCTR0							
R/W-X																R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 10-26. WKUP_PSC0_RAILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	RAILCTR1	R/W	0h	Rail Counter Value 1
7-0	RAILCTR0	R/W	0h	Rail Counter Value 0

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10.14 WKUP_PSC0_RAILSEL Register (Offset = 108h) [reset = 0h]

WKUP_PSC0_RAILSEL is shown in Figure 10-13 and described in Table 10-28.

Return to Summary Table.

User can use this register to select the counter value (WKUP_PSC0_RAILCTL) for each power domain.

Table 10-27. WKUP_PSC0_RAILSEL Instances

Instance	Physical Address
WKUP_PSC0	4200 0108h

Figure 10-13. WKUP_PSC0_RAILSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 10-28. WKUP_PSC0_RAILSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	P	R/W	0h	Rail Counter Select for Power Domain

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10.15 WKUP_PSC0_PTCMD Register (Offset = 120h) [reset = 0h]

WKUP_PSC0_PTCMD is shown in Figure 10-14 and described in Table 10-30.

Return to Summary Table.

This is a pseudo-command register with no actual storage. Reads return 0. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-29. WKUP_PSC0_PTCMD Instances

Instance	Physical Address
WKUP_PSC0	4200 0120h

Figure 10-14. WKUP_PSC0_PTCMD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GO																															
W1S-0h																															

LEGEND: W1S = Write 1 to Set Bit; -*n* = value after reset

Table 10-30. WKUP_PSC0_PTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GO	W1S	0h	Power Domain n GO Transition 0h = Write of 0 has no effect 1h = Sets corresponding WKUP_PSC0_PTSTAT.GOSTAT field which causes PSC hardware to evaluate PDCTL.NEXT and MDCTL.NEXT for this domain.

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10.16 WKUP_PSC0_PTSTAT Register (Offset = 128h) [reset = 0h]

WKUP_PSC0_PTSTAT is shown in Figure 10-15 and described in Table 10-32.

Return to Summary Table.

This is a status register. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-31. WKUP_PSC0_PTSTAT Instances

Instance	Physical Address
WKUP_PSC0	4200 0128h

Figure 10-15. WKUP_PSC0_PTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GOSTAT																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 10-32. WKUP_PSC0_PTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GOSTAT	R	0h	Power Domain n Transition Command Status 0h = No transitions in progress in Power Domain 1h = Power Domain Transition in progress. Either the power domain is transitioning, or modules on this domain are transitioning.

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10.17 WKUP_PSC0_PDSTAT_y Register (Offset = 200h + formula) [reset = X]

WKUP_PSC0_PDSTAT_y is shown in Figure 10-16 and described in Table 10-34.

Return to Summary Table.

This is a status register. One register per power domain. Each register contains the status for the given power domain.

Offset = 200h + (y * 4h); where y = 0h to 1h

Table 10-33. WKUP_PSC0_PDSTAT_y Instances

Instance	Physical Address
WKUP_PSC0	4200 0200h + formula

Figure 10-16. WKUP_PSC0_PDSTAT_y Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED				EMUIHB	PWRBAD	PORDONE	PORZ
R-X				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED			STATE				
R-X			R-X				

LEGEND: R = Read Only; *-n* = value after reset

Table 10-34. WKUP_PSC0_PDSTAT_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	X	
11	EMUIHB	R	0h	Emulation Alters Domain State
10	PWRBAD	R	0h	Power Bad error
9	PORDONE	R	0h	POR Done Input Status
8	PORZ	R	0h	PORz output actual status
7-5	RESERVED	R	X	
4-0	STATE	R	X	Current Power Domain State **Note** NOTE: Reset values per WKUP_PSC0 Power Domain Features. 0h = Power domain is off 1h = Power domain is on

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10.18 WKUP_PSC0_PDCTL_y Register (Offset = 300h + formula) [reset = X]

WKUP_PSC0_PDCTL_y is shown in Figure 10-17 and described in Table 10-36.

Return to Summary Table.

This is a control register. One register per power domain.

Offset = 300h + (y * 4h); where y = 0h to 1h

Table 10-35. WKUP_PSC0_PDCTL_y Instances

Instance	Physical Address
WKUP_PSC0	4200 0300h + formula

Figure 10-17. WKUP_PSC0_PDCTL_y Register

31	30	29	28	27	26	25	24
FORCE	RESERVED	PWRSW	ISO	RESERVED			
R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-X			
23	22	21	20	19	18	17	16
WAKECNT							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	PDMODE			RESERVED		EMUIHBIE	EPCGOOD
R/W-X	R/W-0h			R/W-X		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED							NEXT
R/W-X							R/W-X

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 10-36. WKUP_PSC0_PDCTL_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	0h	Force Bit
30	RESERVED	R/W	X	
29	PWRSW	R/W	0h	Power shorting Switch Control
28	ISO	R/W	0h	Isolation Cell control
27-24	RESERVED	R/W	X	
23-16	WAKECNT	R/W	0h	RAM wake count delay value
15	RESERVED	R/W	X	
14-12	PDMODE	R/W	0h	Power Down mode 0h = Core Off, RAM Array Off, RAM Periphery Off 8h = Core Retention, RAM Array Off, RAM Periphery Off 9h = Core Retention, RAM Array Retention, RAM Periphery Off Ah = Core On, RAM Array Retention, RAM Periphery Off Bh = Core On, RAM Array Retention, RAM Periphery On Fh = Core On, RAM Array On, RAM Periphery On
11-10	RESERVED	R/W	X	

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Table 10-36. WKUP_PSC0_PDCTL_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EMUIHBIE	R/W	0h	Emulation alters domain state 0h = Not enabled 1h = Interrupt enabled
8	EPCGOOD	R/W	0h	External Power Control Power Good Indication
7-1	RESERVED	R/W	X	
0	NEXT	R/W	X	User_Desired Next Power Domain State **Note** NOTE: Reset values per WKUP_PSC0 Power Domain Features. 0h = Off 1h = On

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10.19 WKUP_PSC0_PDCFG_y Register (Offset = 400h + formula) [reset = X]

WKUP_PSC0_PDCFG_y is shown in Figure 10-18 and described in Table 10-38.

Return to Summary Table.

This is a status register. It shows PSC settings for easy debug.

Offset = 400h + (y * 4h); where y = 0h to 1h

Table 10-37. WKUP_PSC0_PDCFG_y Instances

Instance	Physical Address
WKUP_PSC0	4200 0400h + formula

Figure 10-18. WKUP_PSC0_PDCFG_y Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				ICEPICK	RESERVED	MEMSLPKWK	ALWAYSON
R-X				R-0h	R-X	R-0h	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 10-38. WKUP_PSC0_PDCFG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	ICEPICK	R	0h	Icepick support 0h = This domain does not have IcePick support 1h = This domain has IcePick support because one or more of its LPSCs have IcePick support
2	RESERVED	R	X	
1	MEMSLPKWK	R	0h	Memory sleep-wake domain
0	ALWAYSON	R	X	Always on power domain **Note** NOTE: Reset values per WKUP_PSC0 Power Domain Features. 0h = This domain is not an AlwaysON power domain 1h = This domain is an AlwaysON power domain

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10.20 WKUP_PSC0_MDCFG_y Register (Offset = 600h + formula) [reset = X]

WKUP_PSC0_MDCFG_y is shown in Figure 10-19 and described in Table 10-40.

Return to Summary Table.

This is a constant register showing some PSC settings for easy debug. This register is read only.

Offset = 600h + (y * 4h); where y = 0h to 15h

Table 10-39. WKUP_PSC0_MDCFG_y Instances

Instance	Physical Address
WKUP_PSC0	4200 0600h + formula

Figure 10-19. WKUP_PSC0_MDCFG_y Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED			PWRDOM				
R-X			R-0h				
15	14	13	12	11	10	9	8
AUTOONLY	RESETISO	NEXTLOCK	ASYNC	ICEPICK	PERMDIS	PLLHANDSHAKE	NUMSCRDISBALE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
NUMSCRDISBALE		NUMCLKEN			NUMCLK		
R-0h		R-0h			R-0h		

LEGEND: R = Read Only; *-n* = value after reset

Table 10-40. WKUP_PSC0_MDCFG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	X	
20-16	PWRDOM	R	0h	Indicates which power domain this module belongs to
15	AUTOONLY	R	0h	0: This LPSC supports all modes, 1: This LPSC supports Enable
14	RESETISO	R	0h	0: This LPSC does not support Reset Isolation, 1: This LPSC supports Reset Isolation
13	NEXTLOCK	R	0h	0: MDCTL.NEXT field is writable, 1: MDCTL.NEXT field is locked
12	ASYNC	R	0h	Async Lpsc
11	ICEPICK	R	0h	IcePick support
10	PERMDIS	R	0h	Permanently disable
9	PLLHANDSHAKE	R	0h	RTL parameter PLL_HANDSHAKE
8-6	NUMSCRDISBALE	R	0h	Number of PWR_SCR_DISABLE interfaces required on LPSC
5-3	NUMCLKEN	R	0h	Number of PWR_CLK_EN interfaces required on LPSC
2-0	NUMCLK	R	0h	Number of PWR_CLKSTOP interfaces required on LPSC

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10.21 WKUP_PSC0_MDSTAT_y Register (Offset = 800h + formula) [reset = X]

WKUP_PSC0_MDSTAT_y is shown in Figure 10-20 and described in Table 10-42.

Return to Summary Table.

This register shows the status of each module. Requires one register per module on the device.

Offset = 800h + (y * 4h); where y = 0h to 15h

Table 10-41. WKUP_PSC0_MDSTAT_y Instances

Instance	Physical Address
WKUP_PSC0	4200 0800h + formula

Figure 10-20. WKUP_PSC0_MDSTAT_y Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED						EMUIHB	EMURST
R-X						R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED			MCKOUT	MRSTDONE	MRSTZ	LRSTDONE	LRSTZ
R-X			R-X	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED		STATE					
R-X		R-X					

LEGEND: R = Read Only; *-n* = value after reset

Table 10-42. WKUP_PSC0_MDSTAT_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17	EMUIHB	R	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. 0h = No emulation altering user-desired module state 1h = Emulation alters user-desired module state
16	EMURST	R	0h	Emulation Alters Reset 0h = No emulation altering user-desired reset 1h = Emulation has altered module reset to be different from what user desires
15-13	RESERVED	R	X	
12	MCKOUT	R	X	Actual modclk output to module **Note** NOTE: Reset value per WKUP_PSC0 LPSC Features. 0h = modclk gated 1h = modclk on

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Table 10-42. WKUP_PSC0_MDSTAT_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	MRSTDONE	R	0h	Module reset initialization done status 0h = module reset initialization not done 1h = module reset initialization done
10	MRSTZ	R	0h	Module reset actual status 0h = module reset modrst_po* asserted 1h = module reset modrst_po* de-asserted
9	LRSTDONE	R	0h	Module local reset initialization done status 0h = local reset initialization not done 1h = local reset initialization done
8	LRSTZ	R	0h	Module local reset actual status 0h = local reset mod_lrst_po* asserted 1h = local reset mod_lrst_po* de-asserted
7-6	RESERVED	R	X	
5-0	STATE	R	X	These bits indicate the current module state **Note** NOTE: Reset value per WKUP_PSC0 LPSC Features. 0h = SwRstDisable 1h = SyncRst 2h = Disable 3h = Enable

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10.22 WKUP_PSC0_MDCTL_y Register (Offset = A00h + formula) [reset = X]

WKUP_PSC0_MDCTL_y is shown in Figure 10-21 and described in Table 10-44.

Return to Summary Table.

This register provides specific control for the individual module. One register per module on the device.

Offset = A00h + (y * 4h); where y = 0h to 15h

Table 10-43. WKUP_PSC0_MDCTL_y Instances

Instance	Physical Address
WKUP_PSC0	4200 0A00h + formula

Figure 10-21. WKUP_PSC0_MDCTL_y Register

31	30	29	28	27	26	25	24
FORCE	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			RESETISO	BLKCHIP1RST	EMUIHBIE	EMURSTIE	LRSTZ
R/W-X			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			NEXT				
R/W-X			R/W-X				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 10-44. WKUP_PSC0_MDCTL_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	0h	Force Bit 0h = No force 1h = Force
30-13	RESERVED	R/W	X	
12	RESETISO	R/W	0h	Reset Isolation 0h = No reset isolation 1h = Enable reset isolation
11	BLKCHIP1RST	R/W	0h	Block Chip_1_Reset
10	EMUIHBIE	R/W	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. 0h = Not enabled 1h = Interrupt enabled
9	EMURSTIE	R/W	0h	Emulation Alter Reset Interrupt Enable 0h = Not enabled 1h = Interrupt enabled

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Table 10-44. WKUP_PSC0_MDCTL_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	LRSTZ	R/W	0h	Module local reset control 0h = assert local reset 1h = de-assert local reset
7-5	RESERVED	R/W	X	
4-0	NEXT	R/W	X	Module Next State **Note** NOTE: Reset value per WKUP_PSC0 LPSC Features. 0h = SwRstDisable 1h = SyncRst 2h = Disable 3h = Enable

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10.23 PSC0 Registers

Table 10-46 lists the memory-mapped registers for the PSC0 registers. All register offset addresses not listed in Table 10-46 should be considered as reserved locations and the register contents should not be modified.

MMRs in region 0

Note

PSC functions are controlled via DMSC. For more information how to use DMSC, see TISCI API available at ti.com **(the TISCI API is under development)**.

Table 10-45. PSC0 Instances

Instance	Base Address
PSC0	0040 0000h

Table 10-46. PSC0 Registers

Offset	Acronym	Register Name	PSC0 Physical Address
0h	PSC0_PID	PSC0_PID register	0040 0000h
10h	PSC0_GBLCTL	Global Control Register	0040 0010h
14h	PSC0_GBLSTAT	Global Status Register	0040 0014h
18h	PSC0_INTEVAL	Interrupt Evaluation Register	0040 0018h
40h + formula	PSC0_MERRPR_y	Module Error Pending Register	0040 0040h + formula
50h + formula	PSC0_MERRCR_y	Module Error Clear Register	0040 0050h + formula
60h	PSC0_PERRPR	Power Error Pending Register	0040 0060h
68h	PSC0_PERRCR	Power Error Clear Register	0040 0068h
70h	PSC0_EPCPR	External Power Error Pending Register	0040 0070h
78h	PSC0_EPCCR	External Power Control Clear Register	0040 0078h
100h	PSC0_RAILSTAT	Power Rail Status Register	0040 0100h
104h	PSC0_RAILCTL	Power Rail Counter Control Register	0040 0104h
108h	PSC0_RAILSEL	Power Rail Counter Select Register	0040 0108h
120h	PSC0_PTCMD	Power Domain Transition Command Register	0040 0120h
128h	PSC0_PTSTAT	Power Domain Transition Status Register	0040 0128h
200h + formula	PSC0_PDSTAT_y	Power Domain Status Register	0040 0200h + formula
300h + formula	PSC0_PDCTL_y	Power Domain Control Register	0040 0300h + formula
400h + formula	PSC0_PDCFG_y	Power Domain Configuration Register	0040 0400h + formula
600h + formula	PSC0_MDCFG_y	Module Configuration Register	0040 0600h + formula
800h + formula	PSC0_MDSTAT_y	Module Status Register	0040 0800h + formula
A00h + formula	PSC0_MDCTL_y	Module Control Register	0040 0A00h + formula

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10.24 PSC0_PID Register (Offset = 0h) [reset = 44820200h]

PSC0_PID is shown in Figure 10-22 and described in Table 10-48.

Return to Summary Table.

The peripheral identification register is a constant register that contains the ID and ID revision number for that module. The PSC0_PID stores version information used to identify the module. All bits within this register are read-only (writes have no effect) meaning that the values within this register should be hard-coded with the appropriate values and must not change from their hard-coded values.

Table 10-47. PSC0_PID Instances

Instance	Physical Address
PSC0	0040 0000h

Figure 10-22. PSC0_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R-1h		R-0h		R-482h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-0h					R-2h			R-0h		R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 10-48. PSC0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PSC0_PID register scheme
29-28	BU	R	0h	Business Unit
27-16	FUNC	R	482h	Module ID
15-11	RTL	R	0h	RTL revision. Will vary depending on release
10-8	MAJOR	R	2h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

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10.25 PSC0_GBLCTL Register (Offset = 10h) [reset = X]

PSC0_GBLCTL is shown in Figure 10-23 and described in Table 10-50.

Return to Summary Table.

This register contains global control to PSC.

Table 10-49. PSC0_GBLCTL Instances

Instance	Physical Address
PSC0	0040 0010h

Figure 10-23. PSC0_GBLCTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-X															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IO_ANA_CTL								RESERVED							
R-0h								R-X							

LEGEND: R = Read Only; *-n* = value after reset

Table 10-50. PSC0_GBLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	X	
15-8	IO_ANA_CTL	R	0h	General purpose IO/Analog PowerDown control. Directly drives io_ana_pdctl_po [7:0] outputs.
7-0	RESERVED	R	X	

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10.26 PSC0_GBLSTAT Register (Offset = 14h) [reset = X]

PSC0_GBLSTAT is shown in Figure 10-24 and described in Table 10-52.

Return to Summary Table.

This register shows the PSC global status.

Table 10-51. PSC0_GBLSTAT Instances

Instance	Physical Address
PSC0	0040 0014h

Figure 10-24. PSC0_GBLSTAT Register

31	30	29	28	27	26	25	24
RESERVED				EF_SMRFLEX			
R-X				R-0h			
23	22	21	20	19	18	17	16
EF_SMRFLEX							
R-0h							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							OVRIDE
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 10-52. PSC0_GBLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R	X	
27-16	EF_SMRFLEX	R	0h	Smart reflex class0 bits
15-1	RESERVED	R	X	
0	OVRIDE	R	0h	PSC Override Status

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10.27 PSC0_INTEVAL Register (Offset = 18h) [reset = X]

PSC0_INTEVAL is shown in Figure 10-25 and described in Table 10-54.

Return to Summary Table.

This register has no storage. Read from this register returns 0.

Table 10-53. PSC0_INTEVAL Instances

Instance	Physical Address
PSC0	0040 0018h

Figure 10-25. PSC0_INTEVAL Register

31	30	29	28	27	26	25	24
RESERVED							
W-X							
23	22	21	20	19	18	17	16
RESERVED				GOSET	EPCSET	ERRSET	RESERVED
W-X				W-0h	W-0h	W-0h	W-X
15	14	13	12	11	10	9	8
RESERVED							
W-X							
7	6	5	4	3	2	1	0
RESERVED					EPCEV	ERREV	ALLEV
W-X					W-0h	W-0h	W-0h

LEGEND: W = Write Only; *-n* = value after reset

Table 10-54. PSC0_INTEVAL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	W	X	
19	GOSET	W	0h	GOSTAT Interrupt Set
18	EPCSET	W	0h	External Power Control Interrupt Set
17	ERRSET	W	0h	Combined Interrupt Set
16-3	RESERVED	W	X	
2	EPCEV	W	0h	External Power Control Interrupt Set
1	ERREV	W	0h	Re_evaluate Error Interrupt
0	ALLEV	W	0h	Re_evaluate combined PSC interrupt 0h = Write of 0 has no effect 1h = Re-evaluate the combined PSC interrupt PSC_ALLINT

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10.28 PSC0_MERRPR_y Register (Offset = 40h + formula) [reset = 0h]

PSC0_MERRPR_y is shown in Figure 10-26 and described in Table 10-56.

Return to Summary Table.

This register records pending error conditions for all modules. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Offset = 40h + (y * 4h); where y = 0h to 3h

Table 10-55. PSC0_MERRPR_y Instances

Instance	Physical Address
PSC0	0040 0040h + formula

Figure 10-26. PSC0_MERRPR_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 10-56. PSC0_MERRPR_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	M	R	0h	Records pending error conditions. Each bit n represents a module.

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10.29 PSC0_MERRCR_y Register (Offset = 50h + formula) [reset = 0h]

PSC0_MERRCR_y is shown in Figure 10-27 and described in Table 10-58.

Return to Summary Table.

This register has no storage. Read from this register returns 0. Each bit represents one module (index 0 for modules 0-31, index 1 for modules 32-63, etc.).

Offset = 50h + (y * 4h); where y = 0h to 3h

Table 10-57. PSC0_MERRCR_y Instances

Instance	Physical Address
PSC0	0040 0050h + formula

Figure 10-27. PSC0_MERRCR_y Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M																															
W1C-0h																															

LEGEND: W1C = Write 1 to Clear Bit; *-n* = value after reset

Table 10-58. PSC0_MERRCR_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	M	W1C	0h	Write of 1 clears the corresponding MERRPR bit.

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10.30 PSC0_PERRPR Register (Offset = 60h) [reset = 0h]

PSC0_PERRPR is shown in Figure 10-28 and described in Table 10-60.

Return to Summary Table.

This register records pending error conditions for each power domain. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-59. PSC0_PERRPR Instances

Instance	Physical Address
PSC0	0040 0060h

Figure 10-28. PSC0_PERRPR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 10-60. PSC0_PERRPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	P	R	0h	Power Domain n Error Condition. Each bit n represents a power domain.

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10.31 PSC0_PERRCR Register (Offset = 68h) [reset = 0h]

PSC0_PERRCR is shown in Figure 10-29 and described in Table 10-62.

Return to Summary Table.

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-61. PSC0_PERRCR Instances

Instance	Physical Address
PSC0	0040 0068h

Figure 10-29. PSC0_PERRCR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P																															
W1C-0h																															

LEGEND: W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 10-62. PSC0_PERRCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	P	W1C	0h	Write of 1 clears the corresponding PSC0_PERRPR bit.

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10.32 PSC0_EPCPR Register (Offset = 70h) [reset = 0h]

PSC0_EPCPR is shown in Figure 10-30 and described in Table 10-64.

Return to Summary Table.

This register records pending external power control conditions. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-63. PSC0_EPCPR Instances

Instance	Physical Address
PSC0	0040 0070h

Figure 10-30. PSC0_EPCPR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 10-64. PSC0_EPCPR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EPC	R	0h	External Power Control Intervention Request for Power Domain n

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10.33 PSC0_EPCCR Register (Offset = 78h) [reset = 0h]

PSC0_EPCCR is shown in Figure 10-31 and described in Table 10-66.

Return to Summary Table.

This register has no storage. Read from this register returns 0. Each bit represents one domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-65. PSC0_EPCCR Instances

Instance	Physical Address
PSC0	0040 0078h

Figure 10-31. PSC0_EPCCR Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC																															
W1C-0h																															

LEGEND: W1C = Write 1 to Clear Bit; -*n* = value after reset

Table 10-66. PSC0_EPCCR Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EPC	W1C	0h	Write of 1 clears the corresponding PSC0_EPCPR bit

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10.34 PSC0_RAILSTAT Register (Offset = 100h) [reset = X]

PSC0_RAILSTAT is shown in Figure 10-32 and described in Table 10-68.

Return to Summary Table.

This register is a read-only and shows the current rail requestor whose request is being granted and the current value of the counter associated with this requestor.

Table 10-67. PSC0_RAILSTAT Instances

Instance	Physical Address
PSC0	0040 0100h

Figure 10-32. PSC0_RAILSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED			RAILNUM					RESERVED							
R-X			R-0h					R-X							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RAILCNT							
R-X								R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 10-68. PSC0_RAILSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-29	RESERVED	R	X	
28-24	RAILNUM	R	0h	Indicates Current Rail Requestor being processed by GPSC
23-8	RESERVED	R	X	
7-0	RAILCNT	R	0h	Indicates the current rail counter value

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10.35 PSC0_RAILCTL Register (Offset = 104h) [reset = X]

PSC0_RAILCTL is shown in Figure 10-33 and described in Table 10-70.

Return to Summary Table.

This register is user programmable. It holds the counter values for rail counter. User can select one of the two counter values to be used for each power domain (see PSC0_RAILSEL register).

Table 10-69. PSC0_RAILCTL Instances

Instance	Physical Address
PSC0	0040 0104h

Figure 10-33. PSC0_RAILCTL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																RAILCTR1								RAILCTR0							
R/W-X																R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 10-70. PSC0_RAILCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	X	
15-8	RAILCTR1	R/W	0h	Rail Counter Value 1
7-0	RAILCTR0	R/W	0h	Rail Counter Value 0

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10.36 PSC0_RAILSEL Register (Offset = 108h) [reset = 0h]

PSC0_RAILSEL is shown in Figure 10-34 and described in Table 10-72.

Return to Summary Table.

User can use this register to select the counter value (PSC0_RAILCTL) for each power domain.

Table 10-71. PSC0_RAILSEL Instances

Instance	Physical Address
PSC0	0040 0108h

Figure 10-34. PSC0_RAILSEL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 10-72. PSC0_RAILSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	P	R/W	0h	Rail Counter Select for Power Domain

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10.37 PSC0_PTCMD Register (Offset = 120h) [reset = 0h]

PSC0_PTCMD is shown in Figure 10-35 and described in Table 10-74.

Return to Summary Table.

This is a pseudo-command register with no actual storage. Reads return 0. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-73. PSC0_PTCMD Instances

Instance	Physical Address
PSC0	0040 0120h

Figure 10-35. PSC0_PTCMD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GO																															
W1S-0h																															

LEGEND: W1S = Write 1 to Set Bit; *-n* = value after reset

Table 10-74. PSC0_PTCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GO	W1S	0h	Power Domain n GO Transition 0h = Write of 0 has no effect 1h = Sets corresponding PSC0_PTSTAT.GOSTAT field which causes PSC hardware to evaluate PDCTL.NEXT and MDCTL.NEXT for this domain.

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10.38 PSC0_PTSTAT Register (Offset = 128h) [reset = 0h]

PSC0_PTSTAT is shown in Figure 10-36 and described in Table 10-76.

Return to Summary Table.

This is a status register. One bit for each power domain (index 0 for domains 0-31, index 1 for domains 32-63, etc.).

Table 10-75. PSC0_PTSTAT Instances

Instance	Physical Address
PSC0	0040 0128h

Figure 10-36. PSC0_PTSTAT Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GOSTAT																															
R-0h																															

LEGEND: R = Read Only; *-n* = value after reset

Table 10-76. PSC0_PTSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	GOSTAT	R	0h	Power Domain n Transition Command Status 0h = No transitions in progress in Power Domain 1h = Power Domain Transition in progress. Either the power domain is transitioning, or modules on this domain are transitioning.

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10.39 PSC0_PDSTAT_y Register (Offset = 200h + formula) [reset = X]

PSC0_PDSTAT_y is shown in Figure 10-37 and described in Table 10-78.

Return to Summary Table.

This is a status register. One register per power domain. Each register contains the status for the given power domain.

Offset = 200h + (y * 4h); where y = 0h to 1Dh

Table 10-77. PSC0_PDSTAT_y Instances

Instance	Physical Address
PSC0	0040 0200h + formula

Figure 10-37. PSC0_PDSTAT_y Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED				EMUIHB	PWRBAD	PORDONE	PORZ
R-X				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED			STATE				
R-X			R-X				

LEGEND: R = Read Only; *-n* = value after reset

Table 10-78. PSC0_PDSTAT_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R	X	
11	EMUIHB	R	0h	Emulation Alters Domain State
10	PWRBAD	R	0h	Power Bad error
9	PORDONE	R	0h	POR Done Input Status
8	PORZ	R	0h	PORz output actual status
7-5	RESERVED	R	X	
4-0	STATE	R	X	Current Power Domain State **Note** NOTE: Reset value per PSC0 Power Domain Features. 0h = Power domain is off 1h = Power domain is on

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10.40 PSC0_PDCTL_y Register (Offset = 300h + formula) [reset = X]

PSC0_PDCTL_y is shown in Figure 10-38 and described in Table 10-80.

Return to Summary Table.

This is a control register. One register per power domain.

Offset = 300h + (y * 4h); where y = 0h to 1Dh

Table 10-79. PSC0_PDCTL_y Instances

Instance	Physical Address
PSC0	0040 0300h + formula

Figure 10-38. PSC0_PDCTL_y Register

31	30	29	28	27	26	25	24
FORCE	RESERVED	PWRSW	ISO	RESERVED			
R/W-0h	R/W-X	R/W-0h	R/W-0h	R/W-X			
23	22	21	20	19	18	17	16
WAKECNT							
R/W-0h							
15	14	13	12	11	10	9	8
RESERVED	PDMODE			RESERVED		EMUIHBIE	EPCGOOD
R/W-X	R/W-0h			R/W-X		R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED							NEXT
R/W-X							R/W-X

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 10-80. PSC0_PDCTL_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	0h	Force Bit
30	RESERVED	R/W	X	
29	PWRSW	R/W	0h	Power shorting Switch Control
28	ISO	R/W	0h	Isolation Cell control
27-24	RESERVED	R/W	X	
23-16	WAKECNT	R/W	0h	RAM wake count delay value
15	RESERVED	R/W	X	
14-12	PDMODE	R/W	0h	Power Down mode 0h = Core Off, RAM Array Off, RAM Periphery Off 8h = Core Retention, RAM Array Off, RAM Periphery Off 9h = Core Retention, RAM Array Retention, RAM Periphery Off Ah = Core On, RAM Array Retention, RAM Periphery Off Bh = Core On, RAM Array Retention, RAM Periphery On Fh = Core On, RAM Array On, RAM Periphery On
11-10	RESERVED	R/W	X	

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Table 10-80. PSC0_PDCTL_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	EMUIHBIE	R/W	0h	Emulation alters domain state 0h = Not enabled 1h = Interrupt enabled
8	EPCGOOD	R/W	0h	External Power Control Power Good Indication
7-1	RESERVED	R/W	X	
0	NEXT	R/W	X	User_Desired Next Power Domain State **Note** NOTE: Reset value per PSC0 Power Domain Features. 0h = Off 1h = On

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10.41 PSC0_PDCFG_y Register (Offset = 400h + formula) [reset = X]

PSC0_PDCFG_y is shown in Figure 10-39 and described in Table 10-82.

Return to Summary Table.

This is a status register. It shows PSC settings for easy debug.

Offset = 400h + (y * 4h); where y = 0h to 1Dh

Table 10-81. PSC0_PDCFG_y Instances

Instance	Physical Address
PSC0	0040 0400h + formula

Figure 10-39. PSC0_PDCFG_y Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED				ICEPICK	RESERVED	MEMSLPKWK	ALWAYSON
R-X				R-0h	R-X	R-0h	R-X

LEGEND: R = Read Only; *-n* = value after reset

Table 10-82. PSC0_PDCFG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	X	
3	ICEPICK	R	0h	Icepick support 0h = This domain does not have IcePick support 1h = This domain has IcePick support because one or more of its LPSCs have IcePick support
2	RESERVED	R	X	
1	MEMSLPKWK	R	0h	Memory sleep-wake domain
0	ALWAYSON	R	X	Always on power domain **Note** NOTE: Reset value per PSC0 Power Domain Features. 0h = This domain is not an AlwaysON power domain 1h = This domain is an AlwaysON power domain

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10.42 PSC0_MDCFG_y Register (Offset = 600h + formula) [reset = X]

PSC0_MDCFG_y is shown in Figure 10-40 and described in Table 10-84.

Return to Summary Table.

This is a constant register showing some PSC settings for easy debug. This register is read only.

Offset = 600h + (y * 4h); where y = 0h to 6Bh

Table 10-83. PSC0_MDCFG_y Instances

Instance	Physical Address
PSC0	0040 0600h + formula

Figure 10-40. PSC0_MDCFG_y Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED			PWRDOM				
R-X			R-0h				
15	14	13	12	11	10	9	8
AUTOONLY	RESETISO	NEXTLOCK	ASYNC	ICEPICK	PERMDIS	PLLHANDSHAKE	NUMSCRDISBALE
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
NUMSCRDISBALE		NUMCLKEN			NUMCLK		
R-0h		R-0h			R-0h		

LEGEND: R = Read Only; *-n* = value after reset

Table 10-84. PSC0_MDCFG_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	X	
20-16	PWRDOM	R	0h	Indicates which power domain this module belongs to
15	AUTOONLY	R	0h	0: This LPSC supports all modes, 1: This LPSC supports Enable
14	RESETISO	R	0h	0: This LPSC does not support Reset Isolation, 1: This LPSC supports Reset Isolation
13	NEXTLOCK	R	0h	0: MDCTL.NEXT field is writable, 1: MDCTL.NEXT field is locked
12	ASYNC	R	0h	Async Lpsc
11	ICEPICK	R	0h	IcePick support
10	PERMDIS	R	0h	Permanently disable
9	PLLHANDSHAKE	R	0h	RTL parameter PLL_HANDSHAKE
8-6	NUMSCRDISBALE	R	0h	Number of PWR_SCR_DISABLE interfaces required on LPSC
5-3	NUMCLKEN	R	0h	Number of PWR_CLK_EN interfaces required on LPSC
2-0	NUMCLK	R	0h	Number of PWR_CLKSTOP interfaces required on LPSC

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10.43 PSC0_MDSTAT_y Register (Offset = 800h + formula) [reset = X]

PSC0_MDSTAT_y is shown in Figure 10-41 and described in Table 10-86.

Return to Summary Table.

This register shows the status of each module. Requires one register per module on the device.

Offset = 800h + (y * 4h); where y = 0h to 6Bh

Table 10-85. PSC0_MDSTAT_y Instances

Instance	Physical Address
PSC0	0040 0800h + formula

Figure 10-41. PSC0_MDSTAT_y Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED						EMUIHB	EMURST
R-X						R-0h	R-0h
15	14	13	12	11	10	9	8
RESERVED			MCKOUT	MRSTDONE	MRSTZ	LRSTDONE	LRSTZ
R-X			R-X	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED		STATE					
R-X		R-X					

LEGEND: R = Read Only; *-n* = value after reset

Table 10-86. PSC0_MDSTAT_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31-18	RESERVED	R	X	
17	EMUIHB	R	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. 0h = No emulation altering user-desired module state 1h = Emulation alters user-desired module state
16	EMURST	R	0h	Emulation Alters Reset 0h = No emulation altering user-desired reset 1h = Emulation has altered module reset to be different from what user desires
15-13	RESERVED	R	X	
12	MCKOUT	R	X	Actual modclk output to module **Note** NOTE: Reset value per PSC0 LPSC Features. 0h = modclk gated 1h = modclk on

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Table 10-86. PSC0_MDSTAT_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	MRSTDONE	R	0h	Module reset initialization done status 0h = module reset initialization not done 1h = module reset initialization done
10	MRSTZ	R	0h	Module reset actual status 0h = module reset modrst_po* asserted 1h = module reset modrst_po* de-asserted
9	LRSTDONE	R	0h	Module local reset initialization done status 0h = local reset initialization not done 1h = local reset initialization done
8	LRSTZ	R	0h	Module local reset actual status 0h = local reset mod_lrst_po* asserted 1h = local reset mod_lrst_po* de-asserted
7-6	RESERVED	R	X	
5-0	STATE	R	X	These bits indicate the current module state **Note** NOTE: Reset value per PSC0 LPSC Features. 0h = SwRstDisable 1h = SyncRst 2h = Disable 3h = Enable

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10.44 PSC0_MDCTL_y Register (Offset = A00h + formula) [reset = X]

PSC0_MDCTL_y is shown in Figure 10-42 and described in Table 10-88.

Return to Summary Table.

This register provides specific control for the individual module. One register per module on the device.

Offset = A00h + (y * 4h); where y = 0h to 6Bh

Table 10-87. PSC0_MDCTL_y Instances

Instance	Physical Address
PSC0	0040 0A00h + formula

Figure 10-42. PSC0_MDCTL_y Register

31	30	29	28	27	26	25	24
FORCE	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED			RESETISO	BLKCHIP1RST	EMUIHBIE	EMURSTIE	LRSTZ
R/W-X			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
RESERVED			NEXT				
R/W-X			R/W-X				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 10-88. PSC0_MDCTL_y Register Field Descriptions

Bit	Field	Type	Reset	Description
31	FORCE	R/W	0h	Force Bit 0h = No force 1h = Force
30-13	RESERVED	R/W	X	
12	RESETISO	R/W	0h	Reset Isolation 0h = No reset isolation 1h = Enable reset isolation
11	BLKCHIP1RST	R/W	0h	Block Chip_1_Reset
10	EMUIHBIE	R/W	0h	Emulation Alters Module State. Inhibits Module Inactive or Force Module Active. 0h = Not enabled 1h = Interrupt enabled
9	EMURSTIE	R/W	0h	Emulation Alter Reset Interrupt Enable 0h = Not enabled 1h = Interrupt enabled

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Table 10-88. PSC0_MDCTL_y Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	LRSTZ	R/W	0h	Module local reset control 0h = assert local reset 1h = de-assert local reset
7-5	RESERVED	R/W	X	
4-0	NEXT	R/W	X	Module Next State **Note** NOTE: Reset value per PSC0 LPSC Features. 0h = SwRstDisable 1h = SyncRst 2h = Disable 3h = Enable

11 MCU_PLL0_CFG Registers

Table 11-2 lists the memory-mapped registers for the MCU_PLL0_CFG registers. All register offset addresses not listed in Table 11-2 should be considered as reserved locations and the register contents should not be modified.

Table 11-1. MCU_PLL0_CFG Instances

Instance	Base Address
MCU_PLL0_CFG	40D0 0000h

Table 11-2. MCU_PLL0_CFG Registers

Offset	Acronym	Register Name	MCU_PLL0_CFG Physical Address
0h	MCU_PLL0_PID	Peripheral Identification Register	40D0 0000h
8h	MCU_PLL0_CFG	PLL Configuration	40D0 0008h
10h	MCU_PLL0_LOCKKEY0	PLL0 Lock Key 0 Register	40D0 0010h
14h	MCU_PLL0_LOCKKEY1	PLL0 Lock Key 1 RegisterAddr	40D0 0014h
20h	MCU_PLL0_CTRL	PLL0 Control	40D0 0020h
24h	MCU_PLL0_STAT	PLL0 Status	40D0 0024h
30h	MCU_PLL0_FREQ_CTRL0	PLL0 Frequency Control 0 Register	40D0 0030h
34h	MCU_PLL0_FREQ_CTRL1	PLL0 Frequency Control 1 Register	40D0 0034h
38h	MCU_PLL0_DIV_CTRL	PLL0 Output Clock Divider Register	40D0 0038h
40h	MCU_PLL0_SS_CTRL	PLL_SS_CTRL register for pll0	40D0 0040h
44h	MCU_PLL0_SS_SPREAD	PLL_SS_SPREAD register for pll0	40D0 0044h
80h	MCU_PLL0_HSDIV_CTRL0	HSDIV_CTRL0 register for pll0	40D0 0080h
84h	MCU_PLL0_HSDIV_CTRL1	HSDIV_CTRL1 register for pll0	40D0 0084h
1000h	MCU_PLL1_PID	Peripheral Identification Register	40D0 1000h
1008h	MCU_PLL1_CFG	PLL Configuration	40D0 1008h
1010h	MCU_PLL1_LOCKKEY0	PLL1 Lock Key 0 Register	40D0 1010h
1014h	MCU_PLL1_LOCKKEY1	PLL1 Lock Key 1 RegisterAddr	40D0 1014h
1020h	MCU_PLL1_CTRL	PLL1 Control	40D0 1020h
1024h	MCU_PLL1_STAT	PLL1 Status	40D0 1024h
1030h	MCU_PLL1_FREQ_CTRL0	PLL1 Frequency Control 1 Register	40D0 1030h

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Table 11-2. MCU_PLL0_CFG Registers (continued)

Offset	Acronym	Register Name	MCU_PLL0_CFG Physical Address
1034h	MCU_PLL1_FREQ_CTRL1	PLL0 Frequency Control 1 Register	40D0 1034h
1038h	MCU_PLL1_DIV_CTRL	PLL1 Output Clock Divider Register	40D0 1038h
1040h	MCU_PLL1_SS_CTRL	PLL_SS_CTRL register for pll1	40D0 1040h
1044h	MCU_PLL1_SS_SPREAD	PLL_SS_SPREAD register for pll1	40D0 1044h
1080h	MCU_PLL1_HSDIV_CTRL0	HSDIV_CTRL0 register for pll1	40D0 1080h
1084h	MCU_PLL1_HSDIV_CTRL1	HSDIV_CTRL1 register for pll1	40D0 1084h
1088h	MCU_PLL1_HSDIV_CTRL2	HSDIV_CTRL2 register for pll1	40D0 1088h
108Ch	MCU_PLL1_HSDIV_CTRL3	HSDIV_CTRL3 register for pll1	40D0 108Ch
1090h	MCU_PLL1_HSDIV_CTRL4	HSDIV_CTRL4 register for pll1	40D0 1090h
2000h	MCU_PLL2_PID	Peripheral Identification Register	40D0 2000h
2008h	MCU_PLL2_CFG	PLL Configuration	40D0 2008h
2010h	MCU_PLL2_LOCKKEY0	PLL2 Lock Key 0 Register	40D0 2010h
2014h	MCU_PLL2_LOCKKEY1	PLL2 Lock Key 1 RegisterAddr	40D0 2014h
2020h	MCU_PLL2_CTRL	PLL2 Control	40D0 2020h
2024h	MCU_PLL2_STAT	PLL2 Status	40D0 2024h
2030h	MCU_PLL2_FREQ_CTRL0	PLL2 Frequency Control 2 Register	40D0 2030h
2034h	MCU_PLL2_FREQ_CTRL1	PLL0 Frequency Control 1 Register	40D0 2034h
2038h	MCU_PLL2_DIV_CTRL	PLL2 Output Clock Divider Register	40D0 2038h
2040h	MCU_PLL2_SS_CTRL	PLL_SS_CTRL register for pll2	40D0 2040h
2044h	MCU_PLL2_SS_SPREAD	PLL_SS_SPREAD register for pll2	40D0 2044h
2080h	MCU_PLL2_HSDIV_CTRL0	HSDIV_CTRL0 register for pll2	40D0 2080h
2084h	MCU_PLL2_HSDIV_CTRL1	HSDIV_CTRL1 register for pll2	40D0 2084h
2088h	MCU_PLL2_HSDIV_CTRL2	HSDIV_CTRL2 register for pll2	40D0 2088h
208Ch	MCU_PLL2_HSDIV_CTRL3	HSDIV_CTRL3 register for pll2	40D0 208Ch
2090h	MCU_PLL2_HSDIV_CTRL4	HSDIV_CTRL4 register for pll2	40D0 2090h

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11.1 MCU_PLL0_PID Register (Offset = 0h) [reset = 61801001h]

MCU_PLL0_PID is shown in Figure 11-1 and described in Table 11-4.

Return to Summary Table.

Peripheral Identification Register

Table 11-3. MCU_PLL0_PID Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0000h

Figure 11-1. MCU_PLL0_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 11-4. MCU_PLL0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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11.2 MCU_PLL0_CFG Register (Offset = 8h) [reset = X]

MCU_PLL0_CFG is shown in Figure 11-2 and described in Table 11-6.

Return to Summary Table.

PLL Configuration

Table 11-5. MCU_PLL0_CFG Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0008h

Figure 11-2. MCU_PLL0_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 11-6. MCU_PLL0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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11.3 MCU_PLL0_LOCKKEY0 Register (Offset = 10h) [reset = 0h]

MCU_PLL0_LOCKKEY0 is shown in Figure 11-3 and described in Table 11-8.

Return to Summary Table.

MCU_PLL0_LOCKKEY0 - PLL0 Lock Key 0 Register

Table 11-7. MCU_PLL0_LOCKKEY0 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0010h

Figure 11-3. MCU_PLL0_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 11-8. MCU_PLL0_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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11.4 MCU_PLL0_LOCKKEY1 Register (Offset = 14h) [reset = 0h]

MCU_PLL0_LOCKKEY1 is shown in Figure 11-4 and described in Table 11-10.

Return to Summary Table.

MCU_PLL0_LOCKKEY1 - PLL0 Lock Key 1 RegisterAddr

Table 11-9. MCU_PLL0_LOCKKEY1 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0014h

Figure 11-4. MCU_PLL0_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 11-10. MCU_PLL0_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers

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11.5 MCU_PLL0_CTRL Register (Offset = 20h) [reset = X]

MCU_PLL0_CTRL is shown in Figure 11-5 and described in Table 11-12.

Return to Summary Table.

MCU_PLL0_CTRL - PLL0 Control

Table 11-11. MCU_PLL0_CTRL Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0020h

Figure 11-5. MCU_PLL0_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h

7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-12. MCU_PLL0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 11-12. MCU_PLL0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-phase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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11.6 MCU_PLL0_STAT Register (Offset = 24h) [reset = X]

MCU_PLL0_STAT is shown in Figure 11-6 and described in Table 11-14.

Return to Summary Table.

MCU_PLL0_STAT - PLL0 Status

Table 11-13. MCU_PLL0_STAT Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0024h

Figure 11-6. MCU_PLL0_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 11-14. MCU_PLL0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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11.7 MCU_PLL0_FREQ_CTRL0 Register (Offset = 30h) [reset = X]

MCU_PLL0_FREQ_CTRL0 is shown in Figure 11-7 and described in Table 11-16.

Return to Summary Table.

MCU_PLL0_FREQ_CTRL0 - PLL0 Frequency Control 0 Register

Table 11-15. MCU_PLL0_FREQ_CTRL0 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0030h

Figure 11-7. MCU_PLL0_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 11-16. MCU_PLL0_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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11.8 MCU_PLL0_FREQ_CTRL1 Register (Offset = 34h) [reset = X]

MCU_PLL0_FREQ_CTRL1 is shown in Figure 11-8 and described in Table 11-18.

Return to Summary Table.

MCU_PLL0_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 11-17. MCU_PLL0_FREQ_CTRL1 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0034h

Figure 11-8. MCU_PLL0_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 11-18. MCU_PLL0_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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11.9 MCU_PLL0_DIV_CTRL Register (Offset = 38h) [reset = X]

MCU_PLL0_DIV_CTRL is shown in Figure 11-9 and described in Table 11-20.

Return to Summary Table.

MCU_PLL0_DIV_CTRL - PLL0 Output Clock Divider Register

Table 11-19. MCU_PLL0_DIV_CTRL Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0038h

Figure 11-9. MCU_PLL0_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-20. MCU_PLL0_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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11.10 MCU_PLL0_SS_CTRL Register (Offset = 40h) [reset = X]

MCU_PLL0_SS_CTRL is shown in Figure 11-10 and described in Table 11-22.

Return to Summary Table.

PLL_SS_CTRL register for pll0

Table 11-21. MCU_PLL0_SS_CTRL Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0040h

Figure 11-10. MCU_PLL0_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-22. MCU_PLL0_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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11.11 MCU_PLL0_SS_SPREAD Register (Offset = 44h) [reset = X]

MCU_PLL0_SS_SPREAD is shown in Figure 11-11 and described in Table 11-24.

Return to Summary Table.

PLL_SS_SPREAD register for PLL0

Table 11-23. MCU_PLL0_SS_SPREAD Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0044h

Figure 11-11. MCU_PLL0_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-24. MCU_PLL0_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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11.12 MCU_PLL0_HSDIV_CTRL0 Register (Offset = 80h) [reset = X]

MCU_PLL0_HSDIV_CTRL0 is shown in Figure 11-12 and described in Table 11-26.

Return to Summary Table.

HSDIV_CTRL0 register for pll0

Table 11-25. MCU_PLL0_HSDIV_CTRL0 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0080h

Figure 11-12. MCU_PLL0_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-26. MCU_PLL0_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.13 MCU_PLL0_HSDIV_CTRL1 Register (Offset = 84h) [reset = X]

MCU_PLL0_HSDIV_CTRL1 is shown in Figure 11-13 and described in Table 11-28.

Return to Summary Table.

HSDIV_CTRL1 register for pll0

Table 11-27. MCU_PLL0_HSDIV_CTRL1 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 0084h

Figure 11-13. MCU_PLL0_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-28. MCU_PLL0_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.14 MCU_PLL1_PID Register (Offset = 1000h) [reset = 61801001h]

MCU_PLL1_PID is shown in Figure 11-14 and described in Table 11-30.

Return to Summary Table.

Peripheral Identification Register

Table 11-29. MCU_PLL1_PID Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1000h

Figure 11-14. MCU_PLL1_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 11-30. MCU_PLL1_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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11.15 MCU_PLL1_CFG Register (Offset = 1008h) [reset = X]

MCU_PLL1_CFG is shown in Figure 11-15 and described in Table 11-32.

Return to Summary Table.

PLL Configuration

Table 11-31. MCU_PLL1_CFG Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1008h

Figure 11-15. MCU_PLL1_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1Fh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1Fh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 11-32. MCU_PLL1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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11.16 MCU_PLL1_LOCKKEY0 Register (Offset = 1010h) [reset = 0h]

MCU_PLL1_LOCKKEY0 is shown in Figure 11-16 and described in Table 11-34.

Return to Summary Table.

MCU_PLL1_LOCKKEY0 - PLL1 Lock Key 0 Register

Table 11-33. MCU_PLL1_LOCKKEY0 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1010h

Figure 11-16. MCU_PLL1_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 11-34. MCU_PLL1_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition1 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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11.17 MCU_PLL1_LOCKKEY1 Register (Offset = 1014h) [reset = 0h]

MCU_PLL1_LOCKKEY1 is shown in Figure 11-17 and described in Table 11-36.

Return to Summary Table.

MCU_PLL1_LOCKKEY1 - PLL1 Lock Key 1 RegisterAddr

Table 11-35. MCU_PLL1_LOCKKEY1 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1014h

Figure 11-17. MCU_PLL1_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 11-36. MCU_PLL1_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition1 registers

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11.18 MCU_PLL1_CTRL Register (Offset = 1020h) [reset = X]

MCU_PLL1_CTRL is shown in Figure 11-18 and described in Table 11-38.

Return to Summary Table.

MCU_PLL1_CTRL - PLL1 Control

Table 11-37. MCU_PLL1_CTRL Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1020h

Figure 11-18. MCU_PLL1_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h

7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-38. MCU_PLL1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 11-38. MCU_PLL1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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11.19 MCU_PLL1_STAT Register (Offset = 1024h) [reset = X]

MCU_PLL1_STAT is shown in Figure 11-19 and described in Table 11-40.

Return to Summary Table.

MCU_PLL1_STAT - PLL1 Status

Table 11-39. MCU_PLL1_STAT Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1024h

Figure 11-19. MCU_PLL1_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 11-40. MCU_PLL1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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11.20 MCU_PLL1_FREQ_CTRL0 Register (Offset = 1030h) [reset = X]

MCU_PLL1_FREQ_CTRL0 is shown in Figure 11-20 and described in Table 11-42.

Return to Summary Table.

MCU_PLL1_FREQ_CTRL0 - PLL1 Frequency Control 1 Register

Table 11-41. MCU_PLL1_FREQ_CTRL0 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1030h

Figure 11-20. MCU_PLL1_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 11-42. MCU_PLL1_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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11.21 MCU_PLL1_FREQ_CTRL1 Register (Offset = 1034h) [reset = X]

MCU_PLL1_FREQ_CTRL1 is shown in Figure 11-21 and described in Table 11-44.

Return to Summary Table.

MCU_PLL1_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 11-43. MCU_PLL1_FREQ_CTRL1 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1034h

Figure 11-21. MCU_PLL1_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 11-44. MCU_PLL1_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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11.22 MCU_PLL1_DIV_CTRL Register (Offset = 1038h) [reset = X]

MCU_PLL1_DIV_CTRL is shown in Figure 11-22 and described in Table 11-46.

Return to Summary Table.

MCU_PLL1_DIV_CTRL - PLL1 Output Clock Divider Register

Table 11-45. MCU_PLL1_DIV_CTRL Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1038h

Figure 11-22. MCU_PLL1_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-46. MCU_PLL1_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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11.23 MCU_PLL1_SS_CTRL Register (Offset = 1040h) [reset = X]

MCU_PLL1_SS_CTRL is shown in Figure 11-23 and described in Table 11-48.

Return to Summary Table.

PLL_SS_CTRL register for pll1

Table 11-47. MCU_PLL1_SS_CTRL Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1040h

Figure 11-23. MCU_PLL1_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-48. MCU_PLL1_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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11.24 MCU_PLL1_SS_SPREAD Register (Offset = 1044h) [reset = X]

MCU_PLL1_SS_SPREAD is shown in Figure 11-24 and described in Table 11-50.

Return to Summary Table.

PLL_SS_SPREAD register for pll1

Table 11-49. MCU_PLL1_SS_SPREAD Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1044h

Figure 11-24. MCU_PLL1_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-50. MCU_PLL1_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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11.25 MCU_PLL1_HSDIV_CTRL0 Register (Offset = 1080h) [reset = X]

MCU_PLL1_HSDIV_CTRL0 is shown in Figure 11-25 and described in Table 11-52.

Return to Summary Table.

HSDIV_CTRL0 register for pll1

Table 11-51. MCU_PLL1_HSDIV_CTRL0 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1080h

Figure 11-25. MCU_PLL1_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-52. MCU_PLL1_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.26 MCU_PLL1_HSDIV_CTRL1 Register (Offset = 1084h) [reset = X]

MCU_PLL1_HSDIV_CTRL1 is shown in Figure 11-26 and described in Table 11-54.

Return to Summary Table.

HSDIV_CTRL1 register for pll1

Table 11-53. MCU_PLL1_HSDIV_CTRL1 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1084h

Figure 11-26. MCU_PLL1_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-54. MCU_PLL1_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.27 MCU_PLL1_HSDIV_CTRL2 Register (Offset = 1088h) [reset = X]

MCU_PLL1_HSDIV_CTRL2 is shown in Figure 11-27 and described in Table 11-56.

Return to Summary Table.

HSDIV_CTRL2 register for pll1

Table 11-55. MCU_PLL1_HSDIV_CTRL2 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1088h

Figure 11-27. MCU_PLL1_HSDIV_CTRL2 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-56. MCU_PLL1_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.28 MCU_PLL1_HSDIV_CTRL3 Register (Offset = 108Ch) [reset = X]

MCU_PLL1_HSDIV_CTRL3 is shown in Figure 11-28 and described in Table 11-58.

Return to Summary Table.

HSDIV_CTRL3 register for pll1

Table 11-57. MCU_PLL1_HSDIV_CTRL3 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 108Ch

Figure 11-28. MCU_PLL1_HSDIV_CTRL3 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-58. MCU_PLL1_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.29 MCU_PLL1_HSDIV_CTRL4 Register (Offset = 1090h) [reset = X]

MCU_PLL1_HSDIV_CTRL4 is shown in Figure 11-29 and described in Table 11-60.

Return to Summary Table.

HSDIV_CTRL4 register for pll1

Table 11-59. MCU_PLL1_HSDIV_CTRL4 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 1090h

Figure 11-29. MCU_PLL1_HSDIV_CTRL4 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-60. MCU_PLL1_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.30 MCU_PLL2_PID Register (Offset = 2000h) [reset = 61801001h]

MCU_PLL2_PID is shown in Figure 11-30 and described in Table 11-62.

Return to Summary Table.

Peripheral Identification Register

Table 11-61. MCU_PLL2_PID Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2000h

Figure 11-30. MCU_PLL2_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 11-62. MCU_PLL2_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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11.31 MCU_PLL2_CFG Register (Offset = 2008h) [reset = X]

MCU_PLL2_CFG is shown in Figure 11-31 and described in Table 11-64.

Return to Summary Table.

PLL Configuration

Table 11-63. MCU_PLL2_CFG Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2008h

Figure 11-31. MCU_PLL2_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1Fh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1Fh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 11-64. MCU_PLL2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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11.32 MCU_PLL2_LOCKKEY0 Register (Offset = 2010h) [reset = 0h]

MCU_PLL2_LOCKKEY0 is shown in Figure 11-32 and described in Table 11-66.

Return to Summary Table.

MCU_PLL2_LOCKKEY0 - PLL2 Lock Key 0 Register

Table 11-65. MCU_PLL2_LOCKKEY0 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2010h

Figure 11-32. MCU_PLL2_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 11-66. MCU_PLL2_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition2 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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11.33 MCU_PLL2_LOCKKEY1 Register (Offset = 2014h) [reset = 0h]

MCU_PLL2_LOCKKEY1 is shown in Figure 11-33 and described in Table 11-68.

Return to Summary Table.

MCU_PLL2_LOCKKEY1 - PLL2 Lock Key 1 RegisterAddr

Table 11-67. MCU_PLL2_LOCKKEY1 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2014h

Figure 11-33. MCU_PLL2_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 11-68. MCU_PLL2_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition2 registers

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11.34 MCU_PLL2_CTRL Register (Offset = 2020h) [reset = X]

MCU_PLL2_CTRL is shown in Figure 11-34 and described in Table 11-70.

Return to Summary Table.

MCU_PLL2_CTRL - PLL2 Control

Table 11-69. MCU_PLL2_CTRL Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2020h

Figure 11-34. MCU_PLL2_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-70. MCU_PLL2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 11-70. MCU_PLL2_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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11.35 MCU_PLL2_STAT Register (Offset = 2024h) [reset = X]

MCU_PLL2_STAT is shown in Figure 11-35 and described in Table 11-72.

Return to Summary Table.

MCU_PLL2_STAT - PLL2 Status

Table 11-71. MCU_PLL2_STAT Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2024h

Figure 11-35. MCU_PLL2_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 11-72. MCU_PLL2_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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11.36 MCU_PLL2_FREQ_CTRL0 Register (Offset = 2030h) [reset = X]

MCU_PLL2_FREQ_CTRL0 is shown in Figure 11-36 and described in Table 11-74.

Return to Summary Table.

MCU_PLL2_FREQ_CTRL0 - PLL2 Frequency Control 2 Register

Table 11-73. MCU_PLL2_FREQ_CTRL0 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2030h

Figure 11-36. MCU_PLL2_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 11-74. MCU_PLL2_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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11.37 MCU_PLL2_FREQ_CTRL1 Register (Offset = 2034h) [reset = X]

MCU_PLL2_FREQ_CTRL1 is shown in Figure 11-37 and described in Table 11-76.

Return to Summary Table.

MCU_PLL2_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 11-75. MCU_PLL2_FREQ_CTRL1 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2034h

Figure 11-37. MCU_PLL2_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 11-76. MCU_PLL2_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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11.38 MCU_PLL2_DIV_CTRL Register (Offset = 2038h) [reset = X]

MCU_PLL2_DIV_CTRL is shown in Figure 11-38 and described in Table 11-78.

Return to Summary Table.

MCU_PLL2_DIV_CTRL - PLL2 Output Clock Divider Register

Table 11-77. MCU_PLL2_DIV_CTRL Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2038h

Figure 11-38. MCU_PLL2_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-78. MCU_PLL2_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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11.39 MCU_PLL2_SS_CTRL Register (Offset = 2040h) [reset = X]

MCU_PLL2_SS_CTRL is shown in Figure 11-39 and described in Table 11-80.

Return to Summary Table.

PLL_SS_CTRL register for pll2

Table 11-79. MCU_PLL2_SS_CTRL Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2040h

Figure 11-39. MCU_PLL2_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-80. MCU_PLL2_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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11.40 MCU_PLL2_SS_SPREAD Register (Offset = 2044h) [reset = X]

MCU_PLL2_SS_SPREAD is shown in Figure 11-40 and described in Table 11-82.

Return to Summary Table.

PLL_SS_SPREAD register for pll2

Table 11-81. MCU_PLL2_SS_SPREAD Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2044h

Figure 11-40. MCU_PLL2_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-82. MCU_PLL2_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% : 5'b10000 - 1.6% : 5'b11111 - 3.1%

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11.41 MCU_PLL2_HSDIV_CTRL0 Register (Offset = 2080h) [reset = X]

MCU_PLL2_HSDIV_CTRL0 is shown in Figure 11-41 and described in Table 11-84.

Return to Summary Table.

HSDIV_CTRL0 register for pll2

Table 11-83. MCU_PLL2_HSDIV_CTRL0 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2080h

Figure 11-41. MCU_PLL2_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-84. MCU_PLL2_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.42 MCU_PLL2_HSDIV_CTRL1 Register (Offset = 2084h) [reset = X]

MCU_PLL2_HSDIV_CTRL1 is shown in Figure 11-42 and described in Table 11-86.

Return to Summary Table.

HSDIV_CTRL1 register for pll2

Table 11-85. MCU_PLL2_HSDIV_CTRL1 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2084h

Figure 11-42. MCU_PLL2_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-86. MCU_PLL2_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.43 MCU_PLL2_HSDIV_CTRL2 Register (Offset = 2088h) [reset = X]

MCU_PLL2_HSDIV_CTRL2 is shown in Figure 11-43 and described in Table 11-88.

Return to Summary Table.

HSDIV_CTRL2 register for pll2

Table 11-87. MCU_PLL2_HSDIV_CTRL2 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2088h

Figure 11-43. MCU_PLL2_HSDIV_CTRL2 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-88. MCU_PLL2_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.44 MCU_PLL2_HSDIV_CTRL3 Register (Offset = 208Ch) [reset = X]

MCU_PLL2_HSDIV_CTRL3 is shown in Figure 11-44 and described in Table 11-90.

Return to Summary Table.

HSDIV_CTRL3 register for pll2

Table 11-89. MCU_PLL2_HSDIV_CTRL3 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 208Ch

Figure 11-44. MCU_PLL2_HSDIV_CTRL3 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-90. MCU_PLL2_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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11.45 MCU_PLL2_HSDIV_CTRL4 Register (Offset = 2090h) [reset = X]

MCU_PLL2_HSDIV_CTRL4 is shown in Figure 11-45 and described in Table 11-92.

Return to Summary Table.

HSDIV_CTRL4 register for pll2

Table 11-91. MCU_PLL2_HSDIV_CTRL4 Instances

Instance	Physical Address
MCU_PLL0_CFG	40D0 2090h

Figure 11-45. MCU_PLL2_HSDIV_CTRL4 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 11-92. MCU_PLL2_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12 PLL0_CFG Registers

Table 12-2 lists the memory-mapped registers for the cfg registers. All register offset addresses not listed in Table 12-2 should be considered as reserved locations and the register contents should not be modified.

Table 12-1. PLL0_CFG Instances

Instance	Base Address
PLL0_CFG	0068 0000h

Table 12-2. PLL0_CFG Registers

Offset	Acronym	Register Name	PLL0_CFG Physical Address
0h	PLL0_PID	Peripheral Identification Register	0068 0000h
8h	PLL0_CFG	PLL Configuration	0068 0008h
10h	PLL0_LOCKKEY0	PLL0 Lock Key 0 Register	0068 0010h
14h	PLL0_LOCKKEY1	PLL0 Lock Key 1 RegisterAddr	0068 0014h
20h	PLL0_CTRL	PLL0 Control	0068 0020h
24h	PLL0_STAT	PLL0 Status	0068 0024h
30h	PLL0_FREQ_CTRL0	PLL0 Frequency Control 0 Register	0068 0030h
34h	PLL0_FREQ_CTRL1	PLL0 Frequency Control 1 Register	0068 0034h
38h	PLL0_DIV_CTRL	PLL0 Output Clock Divider Register	0068 0038h
40h	PLL0_SS_CTRL	PLL_SS_CTRL register for pll0	0068 0040h
44h	PLL0_SS_SPREAD	PLL_SS_SPREAD register for pll0	0068 0044h
80h	PLL0_HSDIV_CTRL0	HSDIV_CTRL0 register for pll0	0068 0080h
84h	PLL0_HSDIV_CTRL1	HSDIV_CTRL1 register for pll0	0068 0084h
88h	PLL0_HSDIV_CTRL2	HSDIV_CTRL2 register for pll0	0068 0088h
8Ch	PLL0_HSDIV_CTRL3	HSDIV_CTRL3 register for pll0	0068 008Ch
90h	PLL0_HSDIV_CTRL4	HSDIV_CTRL4 register for pll0	0068 0090h
94h	PLL0_HSDIV_CTRL5	HSDIV_CTRL5 register for pll0	0068 0094h
98h	PLL0_HSDIV_CTRL6	HSDIV_CTRL6 register for pll0	0068 0098h
9Ch	PLL0_HSDIV_CTRL7	HSDIV_CTRL7 register for pll0	0068 009Ch
A0h	PLL0_HSDIV_CTRL8	HSDIV_CTRL8 register for pll0	0068 00A0h
1000h	PLL1_PID	Peripheral Identification Register	0068 1000h
1008h	PLL1_CFG	PLL Configuration	0068 1008h
1010h	PLL1_LOCKKEY0	PLL1 Lock Key 0 Register	0068 1010h
1014h	PLL1_LOCKKEY1	PLL1 Lock Key 1 RegisterAddr	0068 1014h
1020h	PLL1_CTRL	PLL1 Control	0068 1020h
1024h	PLL1_STAT	PLL1 Status	0068 1024h
1030h	PLL1_FREQ_CTRL0	PLL1 Frequency Control 1 Register	0068 1030h
1034h	PLL1_FREQ_CTRL1	PLL0 Frequency Control 1 Register	0068 1034h
1038h	PLL1_DIV_CTRL	PLL1 Output Clock Divider Register	0068 1038h
1040h	PLL1_SS_CTRL	PLL_SS_CTRL register for pll1	0068 1040h
1044h	PLL1_SS_SPREAD	PLL_SS_SPREAD register for pll1	0068 1044h
1080h	PLL1_HSDIV_CTRL0	HSDIV_CTRL0 register for pll1	0068 1080h
1084h	PLL1_HSDIV_CTRL1	HSDIV_CTRL1 register for pll1	0068 1084h
1088h	PLL1_HSDIV_CTRL2	HSDIV_CTRL2 register for pll1	0068 1088h
108Ch	PLL1_HSDIV_CTRL3	HSDIV_CTRL3 register for pll1	0068 108Ch
1090h	PLL1_HSDIV_CTRL4	HSDIV_CTRL4 register for pll1	0068 1090h
1094h	PLL1_HSDIV_CTRL5	HSDIV_CTRL5 register for pll1	0068 1094h
1098h	PLL1_HSDIV_CTRL6	HSDIV_CTRL6 register for pll1	0068 1098h

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Table 12-2. PLL0_CFG Registers (continued)

Offset	Acronym	Register Name	PLL0_CFG Physical Address
109Ch	PLL1_HSDIV_CTRL7	HSDIV_CTRL7 register for pll1	0068 109Ch
10A0h	PLL1_HSDIV_CTRL8	HSDIV_CTRL8 register for pll1	0068 10A0h
2000h	PLL2_PID	Peripheral Identification Register	0068 2000h
2008h	PLL2_CFG	PLL Configuration	0068 2008h
2010h	PLL2_LOCKKEY0	PLL2 Lock Key 0 Register	0068 2010h
2014h	PLL2_LOCKKEY1	PLL2 Lock Key 1 RegisterAddr	0068 2014h
2020h	PLL2_CTRL	PLL2 Control	0068 2020h
2024h	PLL2_STAT	PLL2 Status	0068 2024h
2030h	PLL2_FREQ_CTRL0	PLL2 Frequency Control 2 Register	0068 2030h
2034h	PLL2_FREQ_CTRL1	PLL2 Frequency Control 1 Register	0068 2034h
2038h	PLL2_DIV_CTRL	PLL2 Output Clock Divider Register	0068 2038h
2040h	PLL2_SS_CTRL	PLL_SS_CTRL register for pll2	0068 2040h
2044h	PLL2_SS_SPREAD	PLL_SS_SPREAD register for pll2	0068 2044h
2080h	PLL2_HSDIV_CTRL0	HSDIV_CTRL0 register for pll2	0068 2080h
2084h	PLL2_HSDIV_CTRL1	HSDIV_CTRL1 register for pll2	0068 2084h
2088h	PLL2_HSDIV_CTRL2	HSDIV_CTRL2 register for pll2	0068 2088h
208Ch	PLL2_HSDIV_CTRL3	HSDIV_CTRL3 register for pll2	0068 208Ch
2090h	PLL2_HSDIV_CTRL4	HSDIV_CTRL4 register for pll2	0068 2090h
2094h	PLL2_HSDIV_CTRL5	HSDIV_CTRL5 register for pll2	0068 2094h
2098h	PLL2_HSDIV_CTRL6	HSDIV_CTRL6 register for pll2	0068 2098h
209Ch	PLL2_HSDIV_CTRL7	HSDIV_CTRL7 register for pll2	0068 209Ch
3000h	PLL3_PID	Peripheral Identification Register	0068 3000h
3008h	PLL3_CFG	PLL Configuration	0068 3008h
3010h	PLL3_LOCKKEY0	PLL3 Lock Key 0 Register	0068 3010h
3014h	PLL3_LOCKKEY1	PLL3 Lock Key 1 RegisterAddr	0068 3014h
3020h	PLL3_CTRL	PLL3 Control	0068 3020h
3024h	PLL3_STAT	PLL3 Status	0068 3024h
3030h	PLL3_FREQ_CTRL0	PLL3 Frequency Control 2 Register	0068 3030h
3034h	PLL3_FREQ_CTRL1	PLL3 Frequency Control 1 Register	0068 3034h
3038h	PLL3_DIV_CTRL	PLL3 Output Clock Divider Register	0068 3038h
3040h	PLL3_SS_CTRL	PLL_SS_CTRL register for pll3	0068 3040h
3044h	PLL3_SS_SPREAD	PLL_SS_SPREAD register for pll3	0068 3044h
3080h	PLL3_HSDIV_CTRL0	HSDIV_CTRL0 register for pll3	0068 3080h
3084h	PLL3_HSDIV_CTRL1	HSDIV_CTRL1 register for pll3	0068 3084h
3088h	PLL3_HSDIV_CTRL2	HSDIV_CTRL2 register for pll3	0068 3088h
308Ch	PLL3_HSDIV_CTRL3	HSDIV_CTRL3 register for pll3	0068 308Ch
3090h	PLL3_HSDIV_CTRL4	HSDIV_CTRL4 register for pll3	0068 3090h
4000h	PLL4_PID	Peripheral Identification Register	0068 4000h
4008h	PLL4_CFG	PLL Configuration	0068 4008h
4010h	PLL4_LOCKKEY0	PLL4 Lock Key 0 Register	0068 4010h
4014h	PLL4_LOCKKEY1	PLL4 Lock Key 1 RegisterAddr	0068 4014h
4020h	PLL4_CTRL	PLL4 Control	0068 4020h
4024h	PLL4_STAT	PLL4 Status	0068 4024h
4030h	PLL4_FREQ_CTRL0	PLL4Frequency Control 2 Register	0068 4030h
4034h	PLL4_FREQ_CTRL1	PLL4 Frequency Control 1 Register	0068 4034h

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Table 12-2. PLL0_CFG Registers (continued)

Offset	Acronym	Register Name	PLL0_CFG Physical Address
4038h	PLL4_DIV_CTRL	PLL4 Output Clock Divider Register	0068 4038h
4040h	PLL4_SS_CTRL	PLL_SS_CTRL register for pll4	0068 4040h
4044h	PLL4_SS_SPREAD	PLL_SS_SPREAD register for pll4	0068 4044h
4080h	PLL4_HSDIV_CTRL0	HSDIV_CTRL0 register for pll4	0068 4080h
4084h	PLL4_HSDIV_CTRL1	HSDIV_CTRL1 register for pll4	0068 4084h
4088h	PLL4_HSDIV_CTRL2	HSDIV_CTRL2 register for pll4	0068 4088h
408Ch	PLL4_HSDIV_CTRL3	HSDIV_CTRL3 register for pll4	0068 408Ch
5000h	PLL5_PID	Peripheral Identification Register	0068 5000h
5008h	PLL5_CFG	PLL Configuration	0068 5008h
5010h	PLL5_LOCKKEY0	PLL5 Lock Key 0 Register	0068 5010h
5014h	PLL5_LOCKKEY1	PLL5 Lock Key 1 RegisterAddr	0068 5014h
5020h	PLL5_CTRL	PLL5 Control	0068 5020h
5024h	PLL5_STAT	PLL5 Status	0068 5024h
5030h	PLL5_FREQ_CTRL0	PLL5 Frequency Control 2 Register	0068 5030h
5034h	PLL5_FREQ_CTRL1	PLL5 Frequency Control 1 Register	0068 5034h
5038h	PLL5_DIV_CTRL	PLL5 Output Clock Divider Register	0068 5038h
5040h	PLL5_SS_CTRL	PLL_SS_CTRL register for pll5	0068 5040h
5044h	PLL5_SS_SPREAD	PLL_SS_SPREAD register for pll5	0068 5044h
5080h	PLL5_HSDIV_CTRL0	HSDIV_CTRL0 register for pll5	0068 5080h
5084h	PLL5_HSDIV_CTRL1	HSDIV_CTRL1 register for pll5	0068 5084h
5088h	PLL5_HSDIV_CTRL2	HSDIV_CTRL2 register for pll5	0068 5088h
508Ch	PLL5_HSDIV_CTRL3	HSDIV_CTRL3 register for pll5	0068 508Ch
6000h	PLL6_PID	Peripheral Identification Register	0068 6000h
6008h	PLL6_CFG	PLL Configuration	0068 6008h
6010h	PLL6_LOCKKEY0	PLL6 Lock Key 0 Register	0068 6010h
6014h	PLL6_LOCKKEY1	PLL6 Lock Key 1 RegisterAddr	0068 6014h
6020h	PLL6_CTRL	PLL6 Control	0068 6020h
6024h	PLL6_STAT	PLL6 Status	0068 6024h
6030h	PLL6_FREQ_CTRL0	PLL6 Frequency Control 2 Register	0068 6030h
6034h	PLL6_FREQ_CTRL1	PLL6 Frequency Control 1 Register	0068 6034h
6038h	PLL6_DIV_CTRL	PLL6 Output Clock Divider Register	0068 6038h
6040h	PLL6_SS_CTRL	PLL_SS_CTRL register for pll6	0068 6040h
6044h	PLL6_SS_SPREAD	PLL_SS_SPREAD register for pll6	0068 6044h
6080h	PLL6_HSDIV_CTRL0	HSDIV_CTRL0 register for pll6	0068 6080h
7000h	PLL7_PID	Peripheral Identification Register	0068 7000h
7008h	PLL7_CFG	PLL Configuration	0068 7008h
7010h	PLL7_LOCKKEY0	PLL7 Lock Key 0 Register	0068 7010h
7014h	PLL7_LOCKKEY1	PLL7 Lock Key 1 RegisterAddr	0068 7014h
7020h	PLL7_CTRL	PLL7 Control	0068 7020h
7024h	PLL7_STAT	PLL7 Status	0068 7024h
7030h	PLL7_FREQ_CTRL0	PLL7 Frequency Control 2 Register	0068 7030h
7034h	PLL7_FREQ_CTRL1	PLL7 Frequency Control 1 Register	0068 7034h
7038h	PLL7_DIV_CTRL	PLL7 Output Clock Divider Register	0068 7038h
7040h	PLL7_SS_CTRL	PLL_SS_CTRL register for pll7	0068 7040h
7044h	PLL7_SS_SPREAD	PLL_SS_SPREAD register for pll7	0068 7044h

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Table 12-2. PLL0_CFG Registers (continued)

Offset	Acronym	Register Name	PLL0_CFG Physical Address
7080h	PLL7_HSDIV_CTRL0	HSDIV_CTRL0 register for pll7	0068 7080h
8000h	PLL8_PID	Peripheral Identification Register	0068 8000h
8008h	PLL8_CFG	PLL Configuration	0068 8008h
8010h	PLL8_LOCKKEY0	PLL8 Lock Key 0 Register	0068 8010h
8014h	PLL8_LOCKKEY1	PLL8 Lock Key 1 RegisterAddr	0068 8014h
8020h	PLL8_CTRL	PLL8 Control	0068 8020h
8024h	PLL8_STAT	PLL8 Status	0068 8024h
8030h	PLL8_FREQ_CTRL0	PLL8 Frequency Control 2 Register	0068 8030h
8034h	PLL8_FREQ_CTRL1	PLL8 Frequency Control 1 Register	0068 8034h
8038h	PLL8_DIV_CTRL	PLL8 Output Clock Divider Register	0068 8038h
8040h	PLL8_SS_CTRL	PLL_SS_CTRL register for pll8	0068 8040h
8044h	PLL8_SS_SPREAD	PLL_SS_SPREAD register for pll8	0068 8044h
8080h	PLL8_HSDIV_CTRL0	HSDIV_CTRL0 register for pll8	0068 8080h
9000h	PLL9_PID	Peripheral Identification Register	0068 9000h
9008h	PLL9_CFG	PLL Configuration	0068 9008h
9010h	PLL9_LOCKKEY0	PLL9 Lock Key 0 Register	0068 9010h
9014h	PLL9_LOCKKEY1	PLL9 Lock Key 1 RegisterAddr	0068 9014h
9020h	PLL9_CTRL	PLL9 Control	0068 9020h
9024h	PLL9_STAT	PLL9 Status	0068 9024h
9030h	PLL9_FREQ_CTRL0	PLL9 Frequency Control 2 Register	0068 9030h
9034h	PLL9_FREQ_CTRL1	PLL9 Frequency Control 1 Register	0068 9034h
9038h	PLL9_DIV_CTRL	PLL9 Output Clock Divider Register	0068 9038h
9040h	PLL9_SS_CTRL	PLL_SS_CTRL register for pll9	0068 9040h
9044h	PLL9_SS_SPREAD	PLL_SS_SPREAD register for pll9	0068 9044h
9080h	PLL9_HSDIV_CTRL0	HSDIV_CTRL0 register for pll9	0068 9080h
C000h	PLL12_PID	Peripheral Identification Register	0068 C000h
C008h	PLL12_CFG	PLL Configuration	0068 C008h
C010h	PLL12_LOCKKEY0	PLL12 Lock Key 0 Register	0068 C010h
C014h	PLL12_LOCKKEY1	PLL12 Lock Key 1 RegisterAddr	0068 C014h
C020h	PLL12_CTRL	PLL12 Control	0068 C020h
C024h	PLL12_STAT	PLL12 Status	0068 C024h
C030h	PLL12_FREQ_CTRL0	PLL12 Frequency Control 2 Register	0068 C030h
C034h	PLL12_FREQ_CTRL1	PLL12 Frequency Control 1 Register	0068 C034h
C038h	PLL12_DIV_CTRL	PLL12 Output Clock Divider Register	0068 C038h
C040h	PLL12_SS_CTRL	PLL_SS_CTRL register for pll12	0068 C040h
C044h	PLL12_SS_SPREAD	PLL_SS_SPREAD register for pll12	0068 C044h
C060h	PLL12_CAL_CTRL	PLL12 Calibration Control Register	0068 C060h
C064h	PLL12_CAL_STAT	PLL12 Calibration Status Register	0068 C064h
C080h	PLL12_HSDIV_CTRL0	HSDIV_CTRL0 register for pll12	0068 C080h
D000h	PLL13_PID	Peripheral Identification Register	0068 D000h
D008h	PLL13_CFG	PLL Configuration	0068 D008h
D010h	PLL13_LOCKKEY0	PLL13 Lock Key 0 Register	0068 D010h
D014h	PLL13_LOCKKEY1	PLL13 Lock Key 1 RegisterAddr	0068 D014h
D020h	PLL13_CTRL	PLL13 Control	0068 D020h
D024h	PLL13_STAT	PLL13 Status	0068 D024h

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Table 12-2. PLL0_CFG Registers (continued)

Offset	Acronym	Register Name	PLL0_CFG Physical Address
D030h	PLL13_FREQ_CTRL0	PLL13 Frequency Control 2 Register	0068 D030h
D034h	PLL13_FREQ_CTRL1	PLL13 Frequency Control 1 Register	0068 D034h
D038h	PLL13_DIV_CTRL	PLL13 Output Clock Divider Register	0068 D038h
D040h	PLL13_SS_CTRL	PLL_SS_CTRL register for pll13	0068 D040h
D044h	PLL13_SS_SPREAD	PLL_SS_SPREAD register for pll13	0068 D044h
D080h	PLL13_HSDIV_CTRL0	HSDIV_CTRL0 register for pll13	0068 D080h
D084h	PLL13_HSDIV_CTRL1	HSDIV_CTRL1 register for pll13	0068 D084h
D088h	PLL13_HSDIV_CTRL2	HSDIV_CTRL2 register for pll13	0068 D088h
D08Ch	PLL13_HSDIV_CTRL3	HSDIV_CTRL3 register for pll13	0068 D08Ch
E000h	PLL14_PID	Peripheral Identification Register	0068 E000h
E008h	PLL14_CFG	PLL Configuration	0068 E008h
E010h	PLL14_LOCKKEY0	PLL14 Lock Key 0 Register	0068 E010h
E014h	PLL14_LOCKKEY1	PLL14 Lock Key 1 RegisterAddr	0068 E014h
E020h	PLL14_CTRL	PLL14 Control	0068 E020h
E024h	PLL14_STAT	PLL14 Status	0068 E024h
E030h	PLL14_FREQ_CTRL0	PLL14 Frequency Control 2 Register	0068 E030h
E034h	PLL14_FREQ_CTRL1	PLL14 Frequency Control 1 Register	0068 E034h
E038h	PLL14_DIV_CTRL	PLL14 Output Clock Divider Register	0068 E038h
E040h	PLL14_SS_CTRL	PLL_SS_CTRL register for pll14	0068 E040h
E044h	PLL14_SS_SPREAD	PLL_SS_SPREAD register for pll14	0068 E044h
E080h	PLL14_HSDIV_CTRL0	HSDIV_CTRL0 register for pll14	0068 E080h
E084h	PLL14_HSDIV_CTRL1	HSDIV_CTRL1 register for pll14	0068 E084h
F000h	PLL15_PID	Peripheral Identification Register	0068 F000h
F008h	PLL15_CFG	PLL Configuration	0068 F008h
F010h	PLL15_LOCKKEY0	PLL15 Lock Key 0 Register	0068 F010h
F014h	PLL15_LOCKKEY1	PLL15 Lock Key 1 RegisterAddr	0068 F014h
F020h	PLL15_CTRL	PLL15 Control	0068 F020h
F024h	PLL15_STAT	PLL15 Status	0068 F024h
F030h	PLL15_FREQ_CTRL0	PLL15 Frequency Control 2 Register	0068 F030h
F034h	PLL15_FREQ_CTRL1	PLL15 Frequency Control 1 Register	0068 F034h
F038h	PLL15_DIV_CTRL	PLL15 Output Clock Divider Register	0068 F038h
F040h	PLL15_SS_CTRL	PLL_SS_CTRL register for pll15	0068 F040h
F044h	PLL15_SS_SPREAD	PLL_SS_SPREAD register for pll15	0068 F044h
F080h	PLL15_HSDIV_CTRL0	HSDIV_CTRL0 register for pll15	0068 F080h
F084h	PLL15_HSDIV_CTRL1	HSDIV_CTRL1 register for pll15	0068 F084h
F088h	PLL15_HSDIV_CTRL2	HSDIV_CTRL2 register for pll15	0068 F088h
F08Ch	PLL15_HSDIV_CTRL3	HSDIV_CTRL3 register for pll15	0068 F08Ch
00010000h	PLL16_PID	Peripheral Identification Register	0069 0000h
00010008h	PLL16_CFG	PLL Configuration	0069 0008h
00010010h	PLL16_LOCKKEY0	PLL16 Lock Key 0 Register	0069 0010h
00010014h	PLL16_LOCKKEY1	PLL16 Lock Key 1 RegisterAddr	0069 0014h
00010020h	PLL16_CTRL	PLL16 Control	0069 0020h
00010024h	PLL16_STAT	PLL16 Status	0069 0024h
00010030h	PLL16_FREQ_CTRL0	PLL16 Frequency Control 2 Register	0069 0030h
00010034h	PLL16_FREQ_CTRL1	PLL16 Frequency Control 1 Register	0069 0034h

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Table 12-2. PLL0_CFG Registers (continued)

Offset	Acronym	Register Name	PLL0_CFG Physical Address
00010038h	PLL16_DIV_CTRL	PLL16 Output Clock Divider Register	0069 0038h
00010040h	PLL16_SS_CTRL	PLL_SS_CTRL register for pll16	0069 0040h
00010044h	PLL16_SS_SPREAD	PLL_SS_SPREAD register for pll16	0069 0044h
00010080h	PLL16_HSDIV_CTRL0	HSDIV_CTRL0 register for pll16	0069 0080h
00010084h	PLL16_HSDIV_CTRL1	HSDIV_CTRL1 register for pll16	0069 0084h
00011000h	PLL17_PID	Peripheral Identification Register	0069 1000h
00011008h	PLL17_CFG	PLL Configuration	0069 1008h
00011010h	PLL17_LOCKKEY0	PLL17 Lock Key 0 Register	0069 1010h
00011014h	PLL17_LOCKKEY1	PLL17 Lock Key 1 RegisterAddr	0069 1014h
00011020h	PLL17_CTRL	PLL17 Control	0069 1020h
00011024h	PLL17_STAT	PLL17 Status	0069 1024h
00011030h	PLL17_FREQ_CTRL0	PLL17 Frequency Control 2 Register	0069 1030h
00011034h	PLL17_FREQ_CTRL1	PLL17 Frequency Control 1 Register	0069 1034h
00011038h	PLL17_DIV_CTRL	PLL17 Output Clock Divider Register	0069 1038h
00011040h	PLL17_SS_CTRL	PLL_SS_CTRL register for pll17	0069 1040h
00011044h	PLL17_SS_SPREAD	PLL_SS_SPREAD register for pll17	0069 1044h
00011080h	PLL17_HSDIV_CTRL0	HSDIV_CTRL0 register for pll17	0069 1080h
00011084h	PLL17_HSDIV_CTRL1	HSDIV_CTRL1 register for pll17	0069 1084h
00012000h	PLL18_PID	Peripheral Identification Register	0069 2000h
00012008h	PLL18_CFG	PLL Configuration	0069 2008h
00012010h	PLL18_LOCKKEY0	PLL18 Lock Key 0 Register	0069 2010h
00012014h	PLL18_LOCKKEY1	PLL18 Lock Key 1 RegisterAddr	0069 2014h
00012020h	PLL18_CTRL	PLL18 Control	0069 2020h
00012024h	PLL18_STAT	PLL18 Status	0069 2024h
00012030h	PLL18_FREQ_CTRL0	PLL18 Frequency Control 2 Register	0069 2030h
00012034h	PLL18_FREQ_CTRL1	PLL18 Frequency Control 1 Register	0069 2034h
00012038h	PLL18_DIV_CTRL	PLL18 Output Clock Divider Register	0069 2038h
00012040h	PLL18_SS_CTRL	PLL_SS_CTRL register for pll18	0069 2040h
00012044h	PLL18_SS_SPREAD	PLL_SS_SPREAD register for pll18	0069 2044h
00012080h	PLL18_HSDIV_CTRL0	HSDIV_CTRL0 register for pll18	0069 2080h
00012084h	PLL18_HSDIV_CTRL1	HSDIV_CTRL1 register for pll18	0069 2084h
00013000h	PLL19_PID	Peripheral Identification Register	0069 3000h
00013008h	PLL19_CFG	PLL Configuration	0069 3008h
00013010h	PLL19_LOCKKEY0	PLL19 Lock Key 0 Register	0069 3010h
00013014h	PLL19_LOCKKEY1	PLL19 Lock Key 1 RegisterAddr	0069 3014h
00013020h	PLL19_CTRL	PLL19 Control	0069 3020h
00013024h	PLL19_STAT	PLL19 Status	0069 3024h
00013030h	PLL19_FREQ_CTRL0	PLL19 Frequency Control 2 Register	0069 3030h
00013034h	PLL19_FREQ_CTRL1	PLL19 Frequency Control 1 Register	0069 3034h
00013038h	PLL19_DIV_CTRL	PLL19 Output Clock Divider Register	0069 3038h
00013040h	PLL19_SS_CTRL	PLL_SS_CTRL register for pll19	0069 3040h
00013044h	PLL19_SS_SPREAD	PLL_SS_SPREAD register for pll19	0069 3044h
00013080h	PLL19_HSDIV_CTRL0	HSDIV_CTRL0 register for pll19	0069 3080h
00013084h	PLL19_HSDIV_CTRL1	HSDIV_CTRL1 register for pll19	0069 3084h
00014000h	PLL20_PID	Peripheral Identification Register	0069 4000h

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Table 12-2. PLL0_CFG Registers (continued)

Offset	Acronym	Register Name	PLL0_CFG Physical Address
00014008h	PLL20_CFG	PLL Configuration	0069 4008h
00014010h	PLL20_LOCKKEY0	PLL20 Lock Key 0 Register	0069 4010h
00014014h	PLL20_LOCKKEY1	PLL20 Lock Key 1 RegisterAddr	0069 4014h
00014020h	PLL20_CTRL	PLL20 Control	0069 4020h
00014024h	PLL20_STAT	PLL20 Status	0069 4024h
00014030h	PLL20_FREQ_CTRL0	PLL20 Frequency Control 2 Register	0069 4030h
00014034h	PLL20_FREQ_CTRL1	PLL20 Frequency Control 1 Register	0069 4034h
00014038h	PLL20_DIV_CTRL	PLL20 Output Clock Divider Register	0069 4038h
00014040h	PLL20_SS_CTRL	PLL_SS_CTRL register for pll20	0069 4040h
00014044h	PLL20_SS_SPREAD	PLL_SS_SPREAD register for pll20	0069 4044h
00014080h	PLL20_HSDIV_CTRL0	HSDIV_CTRL0 register for pll20	0069 4080h
00014084h	PLL20_HSDIV_CTRL1	HSDIV_CTRL1 register for pll20	0069 4084h
00015000h	PLL21_PID	Peripheral Identification Register	0069 5000h
00015008h	PLL21_CFG	PLL Configuration	0069 5008h
00015010h	PLL21_LOCKKEY0	PLL21 Lock Key 0 Register	0069 5010h
00015014h	PLL21_LOCKKEY1	PLL21 Lock Key 1 RegisterAddr	0069 5014h
00015020h	PLL21_CTRL	PLL21 Control	0069 5020h
00015024h	PLL21_STAT	PLL21 Status	0069 5024h
00015030h	PLL21_FREQ_CTRL0	PLL21 Frequency Control 2 Register	0069 5030h
00015034h	PLL21_FREQ_CTRL1	PLL21 Frequency Control 1 Register	0069 5034h
00015038h	PLL21_DIV_CTRL	PLL21 Output Clock Divider Register	0069 5038h
00015040h	PLL21_SS_CTRL	PLL_SS_CTRL register for pll21	0069 5040h
00015044h	PLL21_SS_SPREAD	PLL_SS_SPREAD register for pll21	0069 5044h
00015080h	PLL21_HSDIV_CTRL0	HSDIV_CTRL0 register for pll21	0069 5080h
00015084h	PLL21_HSDIV_CTRL1	HSDIV_CTRL1 register for pll21	0069 5084h
00016000h	PLL22_PID	Peripheral Identification Register	0069 6000h
00016008h	PLL22_CFG	PLL Configuration	0069 6008h
00016010h	PLL22_LOCKKEY0	PLL22 Lock Key 0 Register	0069 6010h
00016014h	PLL22_LOCKKEY1	PLL22 Lock Key 1 RegisterAddr	0069 6014h
00016020h	PLL22_CTRL	PLL22 Control	0069 6020h
00016024h	PLL22_STAT	PLL22 Status	0069 6024h
00016030h	PLL22_FREQ_CTRL0	PLL22 Frequency Control 2 Register	0069 6030h
00016034h	PLL22_FREQ_CTRL1	PLL22 Frequency Control 1 Register	0069 6034h
00016038h	PLL22_DIV_CTRL	PLL22 Output Clock Divider Register	0069 6038h
00016040h	PLL22_SS_CTRL	PLL_SS_CTRL register for pll22	0069 6040h
00016044h	PLL22_SS_SPREAD	PLL_SS_SPREAD register for pll22	0069 6044h
00016080h	PLL22_HSDIV_CTRL0	HSDIV_CTRL0 register for pll22	0069 6080h
00016084h	PLL22_HSDIV_CTRL1	HSDIV_CTRL1 register for pll22	0069 6084h
00017000h	PLL23_PID	Peripheral Identification Register	0069 7000h
00017008h	PLL23_CFG	PLL Configuration	0069 7008h
00017010h	PLL23_LOCKKEY0	PLL23 Lock Key 0 Register	0069 7010h
00017014h	PLL23_LOCKKEY1	PLL23 Lock Key 1 RegisterAddr	0069 7014h
00017020h	PLL23_CTRL	PLL23 Control	0069 7020h
00017024h	PLL23_STAT	PLL23 Status	0069 7024h
00017030h	PLL23_FREQ_CTRL0	PLL23 Frequency Control 2 Register	0069 7030h

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Table 12-2. PLL0_CFG Registers (continued)

Offset	Acronym	Register Name	PLL0_CFG Physical Address
00017034h	PLL23_FREQ_CTRL1	PLL23 Frequency Control 1 Register	0069 7034h
00017038h	PLL23_DIV_CTRL	PLL23 Output Clock Divider Register	0069 7038h
00017040h	PLL23_SS_CTRL	PLL_SS_CTRL register for pll23	0069 7040h
00017044h	PLL23_SS_SPREAD	PLL_SS_SPREAD register for pll23	0069 7044h
00017080h	PLL23_HSDIV_CTRL0	HSDIV_CTRL0 register for pll23	0069 7080h
00017084h	PLL23_HSDIV_CTRL1	HSDIV_CTRL1 register for pll23	0069 7084h
00018000h	PLL24_PID		0069 8000h
00018008h	PLL24_CFG	PLL Configuration	0069 8008h
00018010h	PLL24_LOCKKEY0	PLL24 Lock Key 0 Register	0069 8010h
00018014h	PLL24_LOCKKEY1	PLL24 Lock Kery 1 Register LOCKKEY1 component	0069 8014h
00018020h	PLL24_PLL_CTRL	PLL_CTRL register for pll24	0069 8020h
00018024h	PLL24_DSPLL_STAT	DSPLL_STAT register for pll24	0069 8024h
00018038h	PLL24_PLL_DIV_CTRL	PLL_DIV_CTRL register for pll24	0069 8038h
00018050h	PLL24_PLL_TEST_CTRL	PLL_TEST_CTRL register for pll24	0069 8050h
00018060h	PLL24_DSCAL_CTRL	DSCAL_CTRL register for pll24	0069 8060h
00018064h	PLL24_DSCAL_STAT	DSCAL_STAT register for pll24	0069 8064h
00018080h	PLL24_HSDIV_CTRL0	HSDIV_CTRL0 register for pll24	0069 8080h
00019000h	PLL25_PID	Peripheral Identification Register	0069 9000h
00019008h	PLL25_CFG	PLL Configuration	0069 9008h
00019010h	PLL25_LOCKKEY0	PLL25 Lock Key 0 Register	0069 9010h
00019014h	PLL25_LOCKKEY1	PLL25 Lock Key 1 RegisterAddr	0069 9014h
00019020h	PLL25_CTRL	PLL25 Control	0069 9020h
00019024h	PLL25_STAT	PLL25 Status	0069 9024h
00019030h	PLL25_FREQ_CTRL0	PLL25 Frequency Control 2 Register	0069 9030h
00019034h	PLL25_FREQ_CTRL1	PLL25 Frequency Control 1 Register	0069 9034h
00019038h	PLL25_DIV_CTRL	PLL25 Output Clock Divider Register	0069 9038h
00019040h	PLL25_SS_CTRL	PLL_SS_CTRL register for pll25	0069 9040h
00019044h	PLL25_SS_SPREAD	PLL_SS_SPREAD register for pll25	0069 9044h
00019080h	PLL25_HSDIV_CTRL0	HSDIV_CTRL0 register for pll25	0069 9080h
00019084h	PLL25_HSDIV_CTRL1	HSDIV_CTRL1 register for pll25	0069 9084h

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12.1 PLL0_PID Register (Offset = 0h) [reset = 61801001h]

PLL0_PID is shown in Figure 12-1 and described in Table 12-4.

Return to Summary Table.

Peripheral Identification Register

Table 12-3. PLL0_PID Instances

Instance	Physical Address
PLL0_CFG	0068 0000h

Figure 12-1. PLL0_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-4. PLL0_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.2 PLL0_CFG Register (Offset = 8h) [reset = X]

PLL0_CFG is shown in Figure 12-2 and described in Table 12-6.

Return to Summary Table.

PLL Configuration

Table 12-5. PLL0_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 0008h

Figure 12-2. PLL0_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1FFh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1FFh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-6. PLL0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1FFh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.3 PLL0_LOCKKEY0 Register (Offset = 10h) [reset = 0h]

PLL0_LOCKKEY0 is shown in Figure 12-3 and described in Table 12-8.

Return to Summary Table.

PLL0_LOCKKEY0 - PLL0 Lock Key 0 Register

Table 12-7. PLL0_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 0010h

Figure 12-3. PLL0_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-8. PLL0_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition0 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.4 PLL0_LOCKKEY1 Register (Offset = 14h) [reset = 0h]

PLL0_LOCKKEY1 is shown in Figure 12-4 and described in Table 12-10.

Return to Summary Table.

PLL0_LOCKKEY1 - PLL0 Lock Key 1 RegisterAddr

Table 12-9. PLL0_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 0014h

Figure 12-4. PLL0_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-10. PLL0_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition0 registers

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12.5 PLL0_CTRL Register (Offset = 20h) [reset = X]

PLL0_CTRL is shown in Figure 12-5 and described in Table 12-12.

Return to Summary Table.

PLL0_CTRL - PLL0 Control

Table 12-11. PLL0_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 0020h

Figure 12-5. PLL0_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						DSM_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-12. PLL0_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-12. PLL0_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.6 PLL0_STAT Register (Offset = 24h) [reset = X]

PLL0_STAT is shown in Figure 12-6 and described in Table 12-14.

Return to Summary Table.

PLL0_STAT - PLL0 Status

Table 12-13. PLL0_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 0024h

Figure 12-6. PLL0_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-14. PLL0_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.7 PLL0_FREQ_CTRL0 Register (Offset = 30h) [reset = X]

PLL0_FREQ_CTRL0 is shown in Figure 12-7 and described in Table 12-16.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL0 Frequency Control 0 Register

Table 12-15. PLL0_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 0030h

Figure 12-7. PLL0_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-16. PLL0_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.8 PLL0_FREQ_CTRL1 Register (Offset = 34h) [reset = X]

PLL0_FREQ_CTRL1 is shown in Figure 12-8 and described in Table 12-18.

Return to Summary Table.

PLL0_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-17. PLL0_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 0034h

Figure 12-8. PLL0_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-18. PLL0_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.9 PLL0_DIV_CTRL Register (Offset = 38h) [reset = X]

PLL0_DIV_CTRL is shown in Figure 12-9 and described in Table 12-20.

Return to Summary Table.

PLL0_DIV_CTRL - PLL0 Output Clock Divider Register

Table 12-19. PLL0_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 0038h

Figure 12-9. PLL0_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-20. PLL0_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.10 PLL0_SS_CTRL Register (Offset = 40h) [reset = X]

PLL0_SS_CTRL is shown in Figure 12-10 and described in Table 12-22.

Return to Summary Table.

PLL_SS_CTRL register for pll0

Table 12-21. PLL0_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 0040h

Figure 12-10. PLL0_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-22. PLL0_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.11 PLL0_SS_SPREAD Register (Offset = 44h) [reset = X]

PLL0_SS_SPREAD is shown in Figure 12-11 and described in Table 12-24.

Return to Summary Table.

PLL_SS_SPREAD register for pll0

Table 12-23. PLL0_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 0044h

Figure 12-11. PLL0_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-24. PLL0_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.12 PLL0_HSDIV_CTRL0 Register (Offset = 80h) [reset = X]

PLL0_HSDIV_CTRL0 is shown in Figure 12-12 and described in Table 12-26.

Return to Summary Table.

HSDIV_CTRL0 register for pll0

Table 12-25. PLL0_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 0080h

Figure 12-12. PLL0_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-26. PLL0_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.13 PLL0_HSDIV_CTRL1 Register (Offset = 84h) [reset = X]

PLL0_HSDIV_CTRL1 is shown in Figure 12-13 and described in Table 12-28.

Return to Summary Table.

HSDIV_CTRL1 register for pll0

Table 12-27. PLL0_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 0084h

Figure 12-13. PLL0_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-28. PLL0_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.14 PLL0_HSDIV_CTRL2 Register (Offset = 88h) [reset = X]

PLL0_HSDIV_CTRL2 is shown in Figure 12-14 and described in Table 12-30.

Return to Summary Table.

HSDIV_CTRL2 register for pll0

Table 12-29. PLL0_HSDIV_CTRL2 Instances

Instance	Physical Address
PLL0_CFG	0068 0088h

Figure 12-14. PLL0_HSDIV_CTRL2 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-30. PLL0_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.15 PLL0_HSDIV_CTRL3 Register (Offset = 8Ch) [reset = X]

PLL0_HSDIV_CTRL3 is shown in Figure 12-15 and described in Table 12-32.

Return to Summary Table.

HSDIV_CTRL3 register for pll0

Table 12-31. PLL0_HSDIV_CTRL3 Instances

Instance	Physical Address
PLL0_CFG	0068 008Ch

Figure 12-15. PLL0_HSDIV_CTRL3 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-32. PLL0_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.16 PLL0_HSDIV_CTRL4 Register (Offset = 90h) [reset = X]

PLL0_HSDIV_CTRL4 is shown in Figure 12-16 and described in Table 12-34.

Return to Summary Table.

HSDIV_CTRL4 register for pll0

Table 12-33. PLL0_HSDIV_CTRL4 Instances

Instance	Physical Address
PLL0_CFG	0068 0090h

Figure 12-16. PLL0_HSDIV_CTRL4 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-34. PLL0_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.17 PLL0_HSDIV_CTRL5 Register (Offset = 94h) [reset = X]

PLL0_HSDIV_CTRL5 is shown in Figure 12-17 and described in Table 12-36.

Return to Summary Table.

HSDIV_CTRL5 register for pll0

Table 12-35. PLL0_HSDIV_CTRL5 Instances

Instance	Physical Address
PLL0_CFG	0068 0094h

Figure 12-17. PLL0_HSDIV_CTRL5 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-36. PLL0_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.18 PLL0_HSDIV_CTRL6 Register (Offset = 98h) [reset = X]

PLL0_HSDIV_CTRL6 is shown in Figure 12-18 and described in Table 12-38.

Return to Summary Table.

HSDIV_CTRL6 register for pll0

Table 12-37. PLL0_HSDIV_CTRL6 Instances

Instance	Physical Address
PLL0_CFG	0068 0098h

Figure 12-18. PLL0_HSDIV_CTRL6 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-38. PLL0_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.19 PLL0_HSDIV_CTRL7 Register (Offset = 9Ch) [reset = X]

PLL0_HSDIV_CTRL7 is shown in Figure 12-19 and described in Table 12-40.

Return to Summary Table.

HSDIV_CTRL7 register for pll0

Table 12-39. PLL0_HSDIV_CTRL7 Instances

Instance	Physical Address
PLL0_CFG	0068 009Ch

Figure 12-19. PLL0_HSDIV_CTRL7 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-40. PLL0_HSDIV_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.20 PLL0_HSDIV_CTRL8 Register (Offset = A0h) [reset = X]

PLL0_HSDIV_CTRL8 is shown in Figure 12-20 and described in Table 12-42.

Return to Summary Table.

HSDIV_CTRL8 register for pll0

Table 12-41. PLL0_HSDIV_CTRL8 Instances

Instance	Physical Address
PLL0_CFG	0068 00A0h

Figure 12-20. PLL0_HSDIV_CTRL8 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-42. PLL0_HSDIV_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.21 PLL1_PID Register (Offset = 1000h) [reset = 61801001h]

PLL1_PID is shown in Figure 12-21 and described in Table 12-44.

Return to Summary Table.

Peripheral Identification Register

Table 12-43. PLL1_PID Instances

Instance	Physical Address
PLL0_CFG	0068 1000h

Figure 12-21. PLL1_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-44. PLL1_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.22 PLL1_CFG Register (Offset = 1008h) [reset = X]

PLL1_CFG is shown in Figure 12-22 and described in Table 12-46.

Return to Summary Table.

PLL Configuration

Table 12-45. PLL1_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 1008h

Figure 12-22. PLL1_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1FFh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1FFh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R/W-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-46. PLL1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1FFh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.23 PLL1_LOCKKEY0 Register (Offset = 1010h) [reset = 0h]

PLL1_LOCKKEY0 is shown in Figure 12-23 and described in Table 12-48.

Return to Summary Table.

PLL1_LOCKKEY0 - PLL1 Lock Key 0 Register

Table 12-47. PLL1_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 1010h

Figure 12-23. PLL1_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-48. PLL1_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition1 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.24 PLL1_LOCKKEY1 Register (Offset = 1014h) [reset = 0h]

PLL1_LOCKKEY1 is shown in Figure 12-24 and described in Table 12-50.

Return to Summary Table.

PLL1_LOCKKEY1 - PLL1 Lock Key 1 RegisterAddr

Table 12-49. PLL1_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 1014h

Figure 12-24. PLL1_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-50. PLL1_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition1 registers

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12.25 PLL1_CTRL Register (Offset = 1020h) [reset = X]

PLL1_CTRL is shown in Figure 12-25 and described in Table 12-52.

Return to Summary Table.

PLL1_CTRL - PLL1 Control

Table 12-51. PLL1_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 1020h

Figure 12-25. PLL1_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h

7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-52. PLL1_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-52. PLL1_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.26 PLL1_STAT Register (Offset = 1024h) [reset = X]

PLL1_STAT is shown in Figure 12-26 and described in Table 12-54.

Return to Summary Table.

PLL1_STAT - PLL1 Status

Table 12-53. PLL1_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 1024h

Figure 12-26. PLL1_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-54. PLL1_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.27 PLL1_FREQ_CTRL0 Register (Offset = 1030h) [reset = X]

PLL1_FREQ_CTRL0 is shown in Figure 12-27 and described in Table 12-56.

Return to Summary Table.

PLL1_FREQ_CTRL0 - PLL1 Frequency Control 1 Register

Table 12-55. PLL1_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 1030h

Figure 12-27. PLL1_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-56. PLL1_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.28 PLL1_FREQ_CTRL1 Register (Offset = 1034h) [reset = X]

PLL1_FREQ_CTRL1 is shown in Figure 12-28 and described in Table 12-58.

Return to Summary Table.

PLL1_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-57. PLL1_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 1034h

Figure 12-28. PLL1_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-58. PLL1_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.29 PLL1_DIV_CTRL Register (Offset = 1038h) [reset = X]

PLL1_DIV_CTRL is shown in Figure 12-29 and described in Table 12-60.

Return to Summary Table.

PLL1_DIV_CTRL - PLL1 Output Clock Divider Register

Table 12-59. PLL1_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 1038h

Figure 12-29. PLL1_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-60. PLL1_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.30 PLL1_SS_CTRL Register (Offset = 1040h) [reset = X]

PLL1_SS_CTRL is shown in Figure 12-30 and described in Table 12-62.

Return to Summary Table.

PLL_SS_CTRL register for pll1

Table 12-61. PLL1_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 1040h

Figure 12-30. PLL1_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-62. PLL1_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.31 PLL1_SS_SPREAD Register (Offset = 1044h) [reset = X]

PLL1_SS_SPREAD is shown in Figure 12-31 and described in Table 12-64.

Return to Summary Table.

PLL_SS_SPREAD register for pll1

Table 12-63. PLL1_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 1044h

Figure 12-31. PLL1_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-64. PLL1_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.32 PLL1_HSDIV_CTRL0 Register (Offset = 1080h) [reset = X]

PLL1_HSDIV_CTRL0 is shown in Figure 12-32 and described in Table 12-66.

Return to Summary Table.

HSDIV_CTRL0 register for pll1

Table 12-65. PLL1_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 1080h

Figure 12-32. PLL1_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-66. PLL1_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.33 PLL1_HSDIV_CTRL1 Register (Offset = 1084h) [reset = X]

PLL1_HSDIV_CTRL1 is shown in Figure 12-33 and described in Table 12-68.

Return to Summary Table.

HSDIV_CTRL1 register for pll1

Table 12-67. PLL1_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 1084h

Figure 12-33. PLL1_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-68. PLL1_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.34 PLL1_HSDIV_CTRL2 Register (Offset = 1088h) [reset = X]

PLL1_HSDIV_CTRL2 is shown in Figure 12-34 and described in Table 12-70.

Return to Summary Table.

HSDIV_CTRL2 register for pll1

Table 12-69. PLL1_HSDIV_CTRL2 Instances

Instance	Physical Address
PLL0_CFG	0068 1088h

Figure 12-34. PLL1_HSDIV_CTRL2 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-70. PLL1_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.35 PLL1_HSDIV_CTRL3 Register (Offset = 108Ch) [reset = X]

PLL1_HSDIV_CTRL3 is shown in Figure 12-35 and described in Table 12-72.

Return to Summary Table.

HSDIV_CTRL3 register for pll1

Table 12-71. PLL1_HSDIV_CTRL3 Instances

Instance	Physical Address
PLL0_CFG	0068 108Ch

Figure 12-35. PLL1_HSDIV_CTRL3 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-72. PLL1_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.36 PLL1_HSDIV_CTRL4 Register (Offset = 1090h) [reset = X]

PLL1_HSDIV_CTRL4 is shown in Figure 12-36 and described in Table 12-74.

Return to Summary Table.

HSDIV_CTRL4 register for pll1

Table 12-73. PLL1_HSDIV_CTRL4 Instances

Instance	Physical Address
PLL0_CFG	0068 1090h

Figure 12-36. PLL1_HSDIV_CTRL4 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-74. PLL1_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.37 PLL1_HSDIV_CTRL5 Register (Offset = 1094h) [reset = X]

PLL1_HSDIV_CTRL5 is shown in Figure 12-37 and described in Table 12-76.

Return to Summary Table.

HSDIV_CTRL5 register for pll1

Table 12-75. PLL1_HSDIV_CTRL5 Instances

Instance	Physical Address
PLL0_CFG	0068 1094h

Figure 12-37. PLL1_HSDIV_CTRL5 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-76. PLL1_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.38 PLL1_HSDIV_CTRL6 Register (Offset = 1098h) [reset = X]

PLL1_HSDIV_CTRL6 is shown in Figure 12-38 and described in Table 12-78.

Return to Summary Table.

HSDIV_CTRL6 register for pll1

Table 12-77. PLL1_HSDIV_CTRL6 Instances

Instance	Physical Address
PLL0_CFG	0068 1098h

Figure 12-38. PLL1_HSDIV_CTRL6 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-78. PLL1_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.39 PLL1_HSDIV_CTRL7 Register (Offset = 109Ch) [reset = X]

PLL1_HSDIV_CTRL7 is shown in Figure 12-39 and described in Table 12-80.

Return to Summary Table.

HSDIV_CTRL7 register for pll1

Table 12-79. PLL1_HSDIV_CTRL7 Instances

Instance	Physical Address
PLL0_CFG	0068 109Ch

Figure 12-39. PLL1_HSDIV_CTRL7 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-80. PLL1_HSDIV_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.40 PLL1_HSDIV_CTRL8 Register (Offset = 10A0h) [reset = X]

PLL1_HSDIV_CTRL8 is shown in Figure 12-40 and described in Table 12-82.

Return to Summary Table.

HSDIV_CTRL8 register for pll1

Table 12-81. PLL1_HSDIV_CTRL8 Instances

Instance	Physical Address
PLL0_CFG	0068 10A0h

Figure 12-40. PLL1_HSDIV_CTRL8 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-82. PLL1_HSDIV_CTRL8 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.41 PLL2_PID Register (Offset = 2000h) [reset = 61801001h]

PLL2_PID is shown in Figure 12-41 and described in Table 12-84.

Return to Summary Table.

Peripheral Identification Register

Table 12-83. PLL2_PID Instances

Instance	Physical Address
PLL0_CFG	0068 2000h

Figure 12-41. PLL2_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-84. PLL2_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.42 PLL2_CFG Register (Offset = 2008h) [reset = X]

PLL2_CFG is shown in Figure 12-42 and described in Table 12-86.

Return to Summary Table.

PLL Configuration

Table 12-85. PLL2_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 2008h

Figure 12-42. PLL2_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-FFh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-FFh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-86. PLL2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	FFh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.43 PLL2_LOCKKEY0 Register (Offset = 2010h) [reset = 0h]

PLL2_LOCKKEY0 is shown in Figure 12-43 and described in Table 12-88.

Return to Summary Table.

PLL2_LOCKKEY0 - PLL2 Lock Key 0 Register

Table 12-87. PLL2_LOCKKEY0 Instances

Instance	Physical Address
PLL2_CFG	0068 2010h

Figure 12-43. PLL2_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-88. PLL2_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition2 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.44 PLL2_LOCKKEY1 Register (Offset = 2014h) [reset = 0h]

PLL2_LOCKKEY1 is shown in Figure 12-44 and described in Table 12-90.

Return to Summary Table.

PLL2_LOCKKEY1 - PLL2 Lock Key 1 RegisterAddr

Table 12-89. PLL2_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 2014h

Figure 12-44. PLL2_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-90. PLL2_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition2 registers

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12.45 PLL2_CTRL Register (Offset = 2020h) [reset = X]

PLL2_CTRL is shown in Figure 12-45 and described in Table 12-92.

Return to Summary Table.

PLL2_CTRL - PLL2 Control

Table 12-91. PLL2_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 2020h

Figure 12-45. PLL2_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-92. PLL2_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-92. PLL2_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.46 PLL2_STAT Register (Offset = 2024h) [reset = X]

PLL2_STAT is shown in Figure 12-46 and described in Table 12-94.

Return to Summary Table.

PLL2_STAT - PLL2 Status

Table 12-93. PLL2_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 2024h

Figure 12-46. PLL2_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-94. PLL2_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.47 PLL2_FREQ_CTRL0 Register (Offset = 2030h) [reset = X]

PLL2_FREQ_CTRL0 is shown in Figure 12-47 and described in Table 12-96.

Return to Summary Table.

PLL2_FREQ_CTRL0 - PLL2 Frequency Control 2 Register

Table 12-95. PLL2_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 2030h

Figure 12-47. PLL2_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-96. PLL2_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.48 PLL2_FREQ_CTRL1 Register (Offset = 2034h) [reset = X]

PLL2_FREQ_CTRL1 is shown in Figure 12-48 and described in Table 12-98.

Return to Summary Table.

PLL2_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-97. PLL2_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 2034h

Figure 12-48. PLL2_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-98. PLL2_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.49 PLL2_DIV_CTRL Register (Offset = 2038h) [reset = X]

PLL2_DIV_CTRL is shown in Figure 12-49 and described in Table 12-100.

Return to Summary Table.

PLL2_DIV_CTRL - PLL2 Output Clock Divider Register

Table 12-99. PLL2_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 2038h

Figure 12-49. PLL2_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-100. PLL2_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.50 PLL2_SS_CTRL Register (Offset = 2040h) [reset = X]

PLL2_SS_CTRL is shown in Figure 12-50 and described in Table 12-102.

Return to Summary Table.

PLL_SS_CTRL register for pll2

Table 12-101. PLL2_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 2040h

Figure 12-50. PLL2_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-102. PLL2_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.51 PLL2_SS_SPREAD Register (Offset = 2044h) [reset = X]

PLL2_SS_SPREAD is shown in Figure 12-51 and described in Table 12-104.

Return to Summary Table.

PLL_SS_SPREAD register for pll2

Table 12-103. PLL2_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 2044h

Figure 12-51. PLL2_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-104. PLL2_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.52 PLL2_HSDIV_CTRL0 Register (Offset = 2080h) [reset = X]

PLL2_HSDIV_CTRL0 is shown in Figure 12-52 and described in Table 12-106.

Return to Summary Table.

HSDIV_CTRL0 register for pll2

Table 12-105. PLL2_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 2080h

Figure 12-52. PLL2_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-106. PLL2_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.53 PLL2_HSDIV_CTRL1 Register (Offset = 2084h) [reset = X]

PLL2_HSDIV_CTRL1 is shown in Figure 12-53 and described in Table 12-108.

Return to Summary Table.

HSDIV_CTRL1 register for pll2

Table 12-107. PLL2_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 2084h

Figure 12-53. PLL2_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-108. PLL2_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.54 PLL2_HSDIV_CTRL2 Register (Offset = 2088h) [reset = X]

PLL2_HSDIV_CTRL2 is shown in Figure 12-54 and described in Table 12-110.

Return to Summary Table.

HSDIV_CTRL2 register for pll2

Table 12-109. PLL2_HSDIV_CTRL2 Instances

Instance	Physical Address
PLL0_CFG	0068 2088h

Figure 12-54. PLL2_HSDIV_CTRL2 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-110. PLL2_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.55 PLL2_HSDIV_CTRL3 Register (Offset = 208Ch) [reset = X]

PLL2_HSDIV_CTRL3 is shown in Figure 12-55 and described in Table 12-112.

Return to Summary Table.

HSDIV_CTRL3 register for pll2

Table 12-111. PLL2_HSDIV_CTRL3 Instances

Instance	Physical Address
PLL0_CFG	0068 208Ch

Figure 12-55. PLL2_HSDIV_CTRL3 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-112. PLL2_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.56 PLL2_HSDIV_CTRL4 Register (Offset = 2090h) [reset = X]

PLL2_HSDIV_CTRL4 is shown in Figure 12-56 and described in Table 12-114.

Return to Summary Table.

HSDIV_CTRL4 register for pll2

Table 12-113. PLL2_HSDIV_CTRL4 Instances

Instance	Physical Address
PLL0_CFG	0068 2090h

Figure 12-56. PLL2_HSDIV_CTRL4 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-114. PLL2_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.57 PLL2_HSDIV_CTRL5 Register (Offset = 2094h) [reset = X]

PLL2_HSDIV_CTRL5 is shown in Figure 12-57 and described in Table 12-116.

Return to Summary Table.

HSDIV_CTRL5 register for pll2

Table 12-115. PLL2_HSDIV_CTRL5 Instances

Instance	Physical Address
PLL0_CFG	0068 2094h

Figure 12-57. PLL2_HSDIV_CTRL5 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-116. PLL2_HSDIV_CTRL5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.58 PLL2_HSDIV_CTRL6 Register (Offset = 2098h) [reset = X]

PLL2_HSDIV_CTRL6 is shown in Figure 12-58 and described in Table 12-118.

Return to Summary Table.

HSDIV_CTRL6 register for pll2

Table 12-117. PLL2_HSDIV_CTRL6 Instances

Instance	Physical Address
PLL0_CFG	0068 2098h

Figure 12-58. PLL2_HSDIV_CTRL6 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-118. PLL2_HSDIV_CTRL6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.59 PLL2_HSDIV_CTRL7 Register (Offset = 209Ch) [reset = X]

PLL2_HSDIV_CTRL7 is shown in Figure 12-59 and described in Table 12-120.

Return to Summary Table.

HSDIV_CTRL7 register for pll2

Table 12-119. PLL2_HSDIV_CTRL7 Instances

Instance	Physical Address
PLL0_CFG	0068 209Ch

Figure 12-59. PLL2_HSDIV_CTRL7 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-120. PLL2_HSDIV_CTRL7 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.60 PLL3_PID Register (Offset = 3000h) [reset = 61801001h]

PLL3_PID is shown in Figure 12-60 and described in Table 12-122.

Return to Summary Table.

Peripheral Identification Register

Table 12-121. PLL3_PID Instances

Instance	Physical Address
PLL0_CFG	0068 3000h

Figure 12-60. PLL3_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-122. PLL3_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.61 PLL3_CFG Register (Offset = 3008h) [reset = X]

PLL3_CFG is shown in Figure 12-61 and described in Table 12-124.

Return to Summary Table.

PLL Configuration

Table 12-123. PLL3_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 3008h

Figure 12-61. PLL3_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1Fh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1Fh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-124. PLL3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.62 PLL3_LOCKKEY0 Register (Offset = 3010h) [reset = 0h]

PLL3_LOCKKEY0 is shown in Figure 12-62 and described in Table 12-126.

Return to Summary Table.

PLL3_LOCKKEY0 - PLL3 Lock Key 0 Register

Table 12-125. PLL3_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 3010h

Figure 12-62. PLL3_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-126. PLL3_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition3 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.63 PLL3_LOCKKEY1 Register (Offset = 3014h) [reset = 0h]

PLL3_LOCKKEY1 is shown in Figure 12-63 and described in Table 12-128.

Return to Summary Table.

PLL3_LOCKKEY1 - PLL3 Lock Key 1 RegisterAddr

Table 12-127. PLL3_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 3014h

Figure 12-63. PLL3_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-128. PLL3_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition3 registers

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12.64 PLL3_CTRL Register (Offset = 3020h) [reset = X]

PLL3_CTRL is shown in Figure 12-64 and described in Table 12-130.

Return to Summary Table.

PLL3_CTRL - PLL3 Control

Table 12-129. PLL3_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 3020h

Figure 12-64. PLL3_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-130. PLL3_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-130. PLL3_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.65 PLL3_STAT Register (Offset = 3024h) [reset = X]

PLL3_STAT is shown in Figure 12-65 and described in Table 12-132.

Return to Summary Table.

PLL3_STAT - PLL3 Status

Table 12-131. PLL3_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 3024h

Figure 12-65. PLL3_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-132. PLL3_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.66 PLL3_FREQ_CTRL0 Register (Offset = 3030h) [reset = X]

PLL3_FREQ_CTRL0 is shown in Figure 12-66 and described in Table 12-134.

Return to Summary Table.

PLL3_FREQ_CTRL0 - PLL3 Frequency Control 3 Register

Table 12-133. PLL3_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 3030h

Figure 12-66. PLL3_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-134. PLL3_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.67 PLL3_FREQ_CTRL1 Register (Offset = 3034h) [reset = X]

PLL3_FREQ_CTRL1 is shown in Figure 12-67 and described in Table 12-136.

Return to Summary Table.

PLL3_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-135. PLL3_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 3034h

Figure 12-67. PLL3_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-136. PLL3_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.68 PLL3_DIV_CTRL Register (Offset = 3038h) [reset = X]

PLL3_DIV_CTRL is shown in Figure 12-68 and described in Table 12-138.

Return to Summary Table.

PLL3_DIV_CTRL - PLL3 Output Clock Divider Register

Table 12-137. PLL3_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 3038h

Figure 12-68. PLL3_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-138. PLL3_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.69 PLL3_SS_CTRL Register (Offset = 3040h) [reset = X]

PLL3_SS_CTRL is shown in Figure 12-69 and described in Table 12-140.

Return to Summary Table.

PLL_SS_CTRL register for pll3

Table 12-139. PLL3_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 3040h

Figure 12-69. PLL3_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-140. PLL3_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.70 PLL3_SS_SPREAD Register (Offset = 3044h) [reset = X]

PLL3_SS_SPREAD is shown in Figure 12-70 and described in Table 12-142.

Return to Summary Table.

PLL_SS_SPREAD register for pll3

Table 12-141. PLL3_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 3044h

Figure 12-70. PLL3_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-142. PLL3_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.71 PLL3_HSDIV_CTRL0 Register (Offset = 3080h) [reset = X]

PLL3_HSDIV_CTRL0 is shown in Figure 12-71 and described in Table 12-144.

Return to Summary Table.

HSDIV_CTRL0 register for pll3

Table 12-143. PLL3_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 3080h

Figure 12-71. PLL3_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-144. PLL3_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.72 PLL3_HSDIV_CTRL1 Register (Offset = 3084h) [reset = X]

PLL3_HSDIV_CTRL1 is shown in Figure 12-72 and described in Table 12-146.

Return to Summary Table.

HSDIV_CTRL1 register for pll3

Table 12-145. PLL3_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 3084h

Figure 12-72. PLL3_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-146. PLL3_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.73 PLL3_HSDIV_CTRL2 Register (Offset = 3088h) [reset = X]

PLL3_HSDIV_CTRL2 is shown in Figure 12-73 and described in Table 12-148.

Return to Summary Table.

HSDIV_CTRL2 register for pll3

Table 12-147. PLL3_HSDIV_CTRL2 Instances

Instance	Physical Address
PLL0_CFG	0068 3088h

Figure 12-73. PLL3_HSDIV_CTRL2 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-148. PLL3_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.74 PLL3_HSDIV_CTRL3 Register (Offset = 308Ch) [reset = X]

PLL3_HSDIV_CTRL3 is shown in Figure 12-74 and described in Table 12-150.

Return to Summary Table.

HSDIV_CTRL3 register for pll3

Table 12-149. PLL3_HSDIV_CTRL3 Instances

Instance	Physical Address
PLL0_CFG	0068 308Ch

Figure 12-74. PLL3_HSDIV_CTRL3 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-150. PLL3_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.75 PLL3_HSDIV_CTRL4 Register (Offset = 3090h) [reset = X]

PLL3_HSDIV_CTRL4 is shown in Figure 12-75 and described in Table 12-152.

Return to Summary Table.

HSDIV_CTRL4 register for pll3

Table 12-151. PLL3_HSDIV_CTRL4 Instances

Instance	Physical Address
PLL0_CFG	0068 3090h

Figure 12-75. PLL3_HSDIV_CTRL4 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-152. PLL3_HSDIV_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.76 PLL4_PID Register (Offset = 4000h) [reset = 61801001h]

PLL4_PID is shown in Figure 12-76 and described in Table 12-154.

Return to Summary Table.

Peripheral Identification Register

Table 12-153. PLL4_PID Instances

Instance	Physical Address
PLL0_CFG	0068 4000h

Figure 12-76. PLL4_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-154. PLL4_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.77 PLL4_CFG Register (Offset = 4008h) [reset = X]

PLL4_CFG is shown in Figure 12-77 and described in Table 12-156.

Return to Summary Table.

PLL Configuration

Table 12-155. PLL4_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 4008h

Figure 12-77. PLL4_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-Fh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-Fh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-156. PLL4_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.78 PLL4_LOCKKEY0 Register (Offset = 4010h) [reset = 0h]

PLL4_LOCKKEY0 is shown in Figure 12-78 and described in Table 12-158.

Return to Summary Table.

PLL4_LOCKKEY0 - PLL4 Lock Key 0 Register

Table 12-157. PLL4_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 4010h

Figure 12-78. PLL4_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-158. PLL4_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition4 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.79 PLL4_LOCKKEY1 Register (Offset = 4014h) [reset = 0h]

PLL4_LOCKKEY1 is shown in Figure 12-79 and described in Table 12-160.

Return to Summary Table.

PLL4_LOCKKEY1 - PLL4 Lock Key 1 RegisterAddr

Table 12-159. PLL4_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 4014h

Figure 12-79. PLL4_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-160. PLL4_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition4 registers

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12.80 PLL4_CTRL Register (Offset = 4020h) [reset = X]

PLL4_CTRL is shown in Figure 12-80 and described in Table 12-162.

Return to Summary Table.

PLL4_CTRL - PLL4 Control

Table 12-161. PLL4_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 4020h

Figure 12-80. PLL4_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h

7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-162. PLL4_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-162. PLL4_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.81 PLL4_STAT Register (Offset = 4024h) [reset = X]

PLL4_STAT is shown in Figure 12-81 and described in Table 12-164.

Return to Summary Table.

PLL4_STAT - PLL4 Status

Table 12-163. PLL4_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 4024h

Figure 12-81. PLL4_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-164. PLL4_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.82 PLL4_FREQ_CTRL0 Register (Offset = 4030h) [reset = X]

PLL4_FREQ_CTRL0 is shown in Figure 12-82 and described in Table 12-166.

Return to Summary Table.

PLL4_FREQ_CTRL0 - PLL4 Frequency Control 4 Register

Table 12-165. PLL4_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 4030h

Figure 12-82. PLL4_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-166. PLL4_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.83 PLL4_FREQ_CTRL1 Register (Offset = 4034h) [reset = X]

PLL4_FREQ_CTRL1 is shown in Figure 12-83 and described in Table 12-168.

Return to Summary Table.

PLL4_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-167. PLL4_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 4034h

Figure 12-83. PLL4_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-168. PLL4_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.84 PLL4_DIV_CTRL Register (Offset = 4038h) [reset = X]

PLL4_DIV_CTRL is shown in Figure 12-84 and described in Table 12-170.

Return to Summary Table.

PLL4_DIV_CTRL - PLL4 Output Clock Divider Register

Table 12-169. PLL4_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 4038h

Figure 12-84. PLL4_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-170. PLL4_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.85 PLL4_SS_CTRL Register (Offset = 4040h) [reset = X]

PLL4_SS_CTRL is shown in Figure 12-85 and described in Table 12-172.

Return to Summary Table.

PLL_SS_CTRL register for pll4

Table 12-171. PLL4_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 4040h

Figure 12-85. PLL4_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-172. PLL4_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.86 PLL4_SS_SPREAD Register (Offset = 4044h) [reset = X]

PLL4_SS_SPREAD is shown in Figure 12-86 and described in Table 12-174.

Return to Summary Table.

PLL_SS_SPREAD register for pll4

Table 12-173. PLL4_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 4044h

Figure 12-86. PLL4_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-174. PLL4_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.87 PLL4_HSDIV_CTRL0 Register (Offset = 4080h) [reset = X]

PLL4_HSDIV_CTRL0 is shown in Figure 12-87 and described in Table 12-176.

Return to Summary Table.

HSDIV_CTRL0 register for pll4

Table 12-175. PLL4_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 4080h

Figure 12-87. PLL4_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-176. PLL4_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.88 PLL4_HSDIV_CTRL1 Register (Offset = 4084h) [reset = X]

PLL4_HSDIV_CTRL1 is shown in Figure 12-88 and described in Table 12-178.

Return to Summary Table.

HSDIV_CTRL1 register for pll4

Table 12-177. PLL4_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 4084h

Figure 12-88. PLL4_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-178. PLL4_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.89 PLL4_HSDIV_CTRL2 Register (Offset = 4088h) [reset = X]

PLL4_HSDIV_CTRL2 is shown in Figure 12-89 and described in Table 12-180.

Return to Summary Table.

HSDIV_CTRL2 register for pll4

Table 12-179. PLL4_HSDIV_CTRL2 Instances

Instance	Physical Address
PLL0_CFG	0068 4088h

Figure 12-89. PLL4_HSDIV_CTRL2 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-180. PLL4_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.90 PLL4_HSDIV_CTRL3 Register (Offset = 408Ch) [reset = X]

PLL4_HSDIV_CTRL3 is shown in Figure 12-90 and described in Table 12-182.

Return to Summary Table.

HSDIV_CTRL3 register for pll4

Table 12-181. PLL4_HSDIV_CTRL3 Instances

Instance	Physical Address
PLL0_CFG	0068 408Ch

Figure 12-90. PLL4_HSDIV_CTRL3 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-182. PLL4_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.91 PLL5_PID Register (Offset = 5000h) [reset = 61801001h]

PLL5_PID is shown in Figure 12-91 and described in Table 12-184.

Return to Summary Table.

Peripheral Identification Register

Table 12-183. PLL5_PID Instances

Instance	Physical Address
PLL0_CFG	0068 5000h

Figure 12-91. PLL5_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-184. PLL5_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.92 PLL5_CFG Register (Offset = 5008h) [reset = X]

PLL5_CFG is shown in Figure 12-92 and described in Table 12-186.

Return to Summary Table.

PLL Configuration

Table 12-185. PLL5_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 5008h

Figure 12-92. PLL5_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-Fh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-Fh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-186. PLL5_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.93 PLL5_LOCKKEY0 Register (Offset = 5010h) [reset = 0h]

PLL5_LOCKKEY0 is shown in Figure 12-93 and described in Table 12-188.

Return to Summary Table.

PLL5_LOCKKEY0 - PLL5 Lock Key 0 Register

Table 12-187. PLL5_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 5010h

Figure 12-93. PLL5_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-188. PLL5_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition5 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.94 PLL5_LOCKKEY1 Register (Offset = 5014h) [reset = 0h]

PLL5_LOCKKEY1 is shown in Figure 12-94 and described in Table 12-190.

Return to Summary Table.

PLL5_LOCKKEY1 - PLL5 Lock Key 1 RegisterAddr

Table 12-189. PLL5_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 5014h

Figure 12-94. PLL5_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-190. PLL5_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition5 registers

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12.95 PLL5_CTRL Register (Offset = 5020h) [reset = X]

PLL5_CTRL is shown in Figure 12-95 and described in Table 12-192.

Return to Summary Table.

PLL5_CTRL - PLL5 Control

Table 12-191. PLL5_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 5020h

Figure 12-95. PLL5_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h

7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-192. PLL5_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-192. PLL5_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.96 PLL5_STAT Register (Offset = 5024h) [reset = X]

PLL5_STAT is shown in Figure 12-96 and described in Table 12-194.

Return to Summary Table.

PLL5_STAT - PLL5 Status

Table 12-193. PLL5_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 5024h

Figure 12-96. PLL5_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-194. PLL5_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.97 PLL5_FREQ_CTRL0 Register (Offset = 5030h) [reset = X]

PLL5_FREQ_CTRL0 is shown in Figure 12-97 and described in Table 12-196.

Return to Summary Table.

PLL5_FREQ_CTRL0 - PLL5 Frequency Control 5 Register

Table 12-195. PLL5_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 5030h

Figure 12-97. PLL5_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-196. PLL5_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.98 PLL5_FREQ_CTRL1 Register (Offset = 5034h) [reset = X]

PLL5_FREQ_CTRL1 is shown in Figure 12-98 and described in Table 12-198.

Return to Summary Table.

PLL5_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-197. PLL5_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 5034h

Figure 12-98. PLL5_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-198. PLL5_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.99 PLL5_DIV_CTRL Register (Offset = 5038h) [reset = X]

PLL5_DIV_CTRL is shown in Figure 12-99 and described in Table 12-200.

Return to Summary Table.

PLL5_DIV_CTRL - PLL5 Output Clock Divider Register

Table 12-199. PLL5_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 5038h

Figure 12-99. PLL5_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-200. PLL5_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.100 PLL5_SS_CTRL Register (Offset = 5040h) [reset = X]

PLL5_SS_CTRL is shown in Figure 12-100 and described in Table 12-202.

Return to Summary Table.

PLL_SS_CTRL register for pll5

Table 12-201. PLL5_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 5040h

Figure 12-100. PLL5_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-202. PLL5_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.101 PLL5_SS_SPREAD Register (Offset = 5044h) [reset = X]

PLL5_SS_SPREAD is shown in Figure 12-101 and described in Table 12-204.

Return to Summary Table.

PLL_SS_SPREAD register for pll5

Table 12-203. PLL5_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 5044h

Figure 12-101. PLL5_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-204. PLL5_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.102 PLL5_HSDIV_CTRL0 Register (Offset = 5080h) [reset = X]

PLL5_HSDIV_CTRL0 is shown in Figure 12-102 and described in Table 12-206.

Return to Summary Table.

HSDIV_CTRL0 register for pll5

Table 12-205. PLL5_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 5080h

Figure 12-102. PLL5_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-206. PLL5_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.103 PLL5_HSDIV_CTRL1 Register (Offset = 5084h) [reset = X]

PLL5_HSDIV_CTRL1 is shown in Figure 12-103 and described in Table 12-208.

Return to Summary Table.

HSDIV_CTRL1 register for pll5

Table 12-207. PLL5_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 5084h

Figure 12-103. PLL5_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-208. PLL5_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.104 PLL5_HSDIV_CTRL2 Register (Offset = 5088h) [reset = X]

PLL5_HSDIV_CTRL2 is shown in Figure 12-104 and described in Table 12-210.

Return to Summary Table.

HSDIV_CTRL2 register for pll5

Table 12-209. PLL5_HSDIV_CTRL2 Instances

Instance	Physical Address
PLL0_CFG	0068 5088h

Figure 12-104. PLL5_HSDIV_CTRL2 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-210. PLL5_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.105 PLL5_HSDIV_CTRL3 Register (Offset = 508Ch) [reset = X]

PLL5_HSDIV_CTRL3 is shown in Figure 12-105 and described in Table 12-212.

Return to Summary Table.

HSDIV_CTRL3 register for pll5

Table 12-211. PLL5_HSDIV_CTRL3 Instances

Instance	Physical Address
PLL0_CFG	0068 508Ch

Figure 12-105. PLL5_HSDIV_CTRL3 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-212. PLL5_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.106 PLL6_PID Register (Offset = 6000h) [reset = 61801001h]

PLL6_PID is shown in Figure 12-106 and described in Table 12-214.

Return to Summary Table.

Peripheral Identification Register

Table 12-213. PLL6_PID Instances

Instance	Physical Address
PLL0_CFG	0068 6000h

Figure 12-106. PLL6_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-214. PLL6_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.107 PLL6_CFG Register (Offset = 6008h) [reset = X]

PLL6_CFG is shown in Figure 12-107 and described in Table 12-216.

Return to Summary Table.

PLL Configuration

Table 12-215. PLL6_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 6008h

Figure 12-107. PLL6_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-216. PLL6_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.108 PLL6_LOCKKEY0 Register (Offset = 6010h) [reset = 0h]

PLL6_LOCKKEY0 is shown in Figure 12-108 and described in Table 12-218.

Return to Summary Table.

PLL6_LOCKKEY0 - PLL6 Lock Key 0 Register

Table 12-217. PLL6_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 6010h

Figure 12-108. PLL6_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-218. PLL6_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition6 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.109 PLL6_LOCKKEY1 Register (Offset = 6014h) [reset = 0h]

PLL6_LOCKKEY1 is shown in Figure 12-109 and described in Table 12-220.

Return to Summary Table.

PLL6_LOCKKEY1 - PLL6 Lock Key 1 RegisterAddr

Table 12-219. PLL6_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 6014h

Figure 12-109. PLL6_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-220. PLL6_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition6 registers

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12.110 PLL6_CTRL Register (Offset = 6020h) [reset = X]

PLL6_CTRL is shown in Figure 12-110 and described in Table 12-222.

Return to Summary Table.

PLL6_CTRL - PLL6 Control

Table 12-221. PLL6_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 6020h

Figure 12-110. PLL6_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h

7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-222. PLL6_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-222. PLL6_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.111 PLL6_STAT Register (Offset = 6024h) [reset = X]

PLL6_STAT is shown in Figure 12-111 and described in Table 12-224.

Return to Summary Table.

PLL6_STAT - PLL6 Status

Table 12-223. PLL6_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 6024h

Figure 12-111. PLL6_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-224. PLL6_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.112 PLL6_FREQ_CTRL0 Register (Offset = 6030h) [reset = X]

PLL6_FREQ_CTRL0 is shown in Figure 12-112 and described in Table 12-226.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL6 Frequency Control 6 Register

Table 12-225. PLL6_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 6030h

Figure 12-112. PLL6_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-226. PLL6_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.113 PLL6_FREQ_CTRL1 Register (Offset = 6034h) [reset = X]

PLL6_FREQ_CTRL1 is shown in Figure 12-113 and described in Table 12-228.

Return to Summary Table.

PLL6_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-227. PLL6_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 6034h

Figure 12-113. PLL6_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-228. PLL6_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.114 PLL6_DIV_CTRL Register (Offset = 6038h) [reset = X]

PLL6_DIV_CTRL is shown in Figure 12-114 and described in Table 12-230.

Return to Summary Table.

PLL6_DIV_CTRL - PLL6 Output Clock Divider Register

Table 12-229. PLL6_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 6038h

Figure 12-114. PLL6_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-230. PLL6_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.115 PLL6_SS_CTRL Register (Offset = 6040h) [reset = X]

PLL6_SS_CTRL is shown in Figure 12-115 and described in Table 12-232.

Return to Summary Table.

PLL_SS_CTRL register for pll6

Table 12-231. PLL6_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 6040h

Figure 12-115. PLL6_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-232. PLL6_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.116 PLL6_SS_SPREAD Register (Offset = 6044h) [reset = X]

PLL6_SS_SPREAD is shown in Figure 12-116 and described in Table 12-234.

Return to Summary Table.

PLL_SS_SPREAD register for pll6

Table 12-233. PLL6_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 6044h

Figure 12-116. PLL6_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-234. PLL6_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.117 PLL6_HSDIV_CTRL0 Register (Offset = 6080h) [reset = X]

PLL6_HSDIV_CTRL0 is shown in Figure 12-117 and described in Table 12-236.

Return to Summary Table.

HSDIV_CTRL0 register for pll6

Table 12-235. PLL6_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 6080h

Figure 12-117. PLL6_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-236. PLL6_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.118 PLL7_PID Register (Offset = 7000h) [reset = 61801001h]

PLL7_PID is shown in Figure 12-118 and described in Table 12-238.

Return to Summary Table.

Peripheral Identification Register

Table 12-237. PLL7_PID Instances

Instance	Physical Address
PLL0_CFG	0068 7000h

Figure 12-118. PLL7_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-238. PLL7_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.119 PLL7_CFG Register (Offset = 7008h) [reset = X]

PLL7_CFG is shown in Figure 12-119 and described in Table 12-240.

Return to Summary Table.

PLL Configuration

Table 12-239. PLL7_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 7008h

Figure 12-119. PLL7_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-240. PLL7_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.120 PLL7_LOCKKEY0 Register (Offset = 7010h) [reset = 0h]

PLL7_LOCKKEY0 is shown in Figure 12-120 and described in Table 12-242.

Return to Summary Table.

PLL7_LOCKKEY0 - PLL7 Lock Key 0 Register

Table 12-241. PLL7_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 7010h

Figure 12-120. PLL7_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-242. PLL7_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition7 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.121 PLL7_LOCKKEY1 Register (Offset = 7014h) [reset = 0h]

PLL7_LOCKKEY1 is shown in Figure 12-121 and described in Table 12-244.

Return to Summary Table.

PLL7_LOCKKEY1 - PLL7 Lock Key 1 RegisterAddr

Table 12-243. PLL7_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 7014h

Figure 12-121. PLL7_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-244. PLL7_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition7 registers

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12.122 PLL7_CTRL Register (Offset = 7020h) [reset = X]

PLL7_CTRL is shown in Figure 12-122 and described in Table 12-246.

Return to Summary Table.

PLL7_CTRL - PLL7 Control

Table 12-245. PLL7_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 7020h

Figure 12-122. PLL7_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-246. PLL7_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-246. PLL7_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.123 PLL7_STAT Register (Offset = 7024h) [reset = X]

PLL7_STAT is shown in Figure 12-123 and described in Table 12-248.

Return to Summary Table.

PLL7_STAT - PLL7 Status

Table 12-247. PLL7_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 7024h

Figure 12-123. PLL7_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-248. PLL7_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.124 PLL7_FREQ_CTRL0 Register (Offset = 7030h) [reset = X]

PLL7_FREQ_CTRL0 is shown in Figure 12-124 and described in Table 12-250.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL7 Frequency Control 7 Register

Table 12-249. PLL7_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 7030h

Figure 12-124. PLL7_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-250. PLL7_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.125 PLL7_FREQ_CTRL1 Register (Offset = 7034h) [reset = X]

PLL7_FREQ_CTRL1 is shown in Figure 12-125 and described in Table 12-252.

Return to Summary Table.

PLL7_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-251. PLL7_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 7034h

Figure 12-125. PLL7_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-252. PLL7_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.126 PLL7_DIV_CTRL Register (Offset = 7038h) [reset = X]

PLL7_DIV_CTRL is shown in Figure 12-126 and described in Table 12-254.

Return to Summary Table.

PLL7_DIV_CTRL - PLL7 Output Clock Divider Register

Table 12-253. PLL7_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 7038h

Figure 12-126. PLL7_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-254. PLL7_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.127 PLL7_SS_CTRL Register (Offset = 7040h) [reset = X]

PLL7_SS_CTRL is shown in Figure 12-127 and described in Table 12-256.

Return to Summary Table.

PLL_SS_CTRL register for pll7

Table 12-255. PLL7_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 7040h

Figure 12-127. PLL7_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-256. PLL7_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.128 PLL7_SS_SPREAD Register (Offset = 7044h) [reset = X]

PLL7_SS_SPREAD is shown in Figure 12-128 and described in Table 12-258.

Return to Summary Table.

PLL_SS_SPREAD register for pll7

Table 12-257. PLL7_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 7044h

Figure 12-128. PLL7_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-258. PLL7_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.129 PLL7_HSDIV_CTRL0 Register (Offset = 7080h) [reset = X]

PLL7_HSDIV_CTRL0 is shown in Figure 12-129 and described in Table 12-260.

Return to Summary Table.

HSDIV_CTRL0 register for pll7

Table 12-259. PLL7_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 7080h

Figure 12-129. PLL7_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-260. PLL7_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.130 PLL8_PID Register (Offset = 8000h) [reset = 61801001h]

PLL8_PID is shown in Figure 12-130 and described in Table 12-262.

Return to Summary Table.

Peripheral Identification Register

Table 12-261. PLL8_PID Instances

Instance	Physical Address
PLL0_CFG	0068 8000h

Figure 12-130. PLL8_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-262. PLL8_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.131 PLL8_CFG Register (Offset = 8008h) [reset = X]

PLL8_CFG is shown in Figure 12-131 and described in Table 12-264.

Return to Summary Table.

PLL Configuration

Table 12-263. PLL8_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 8008h

Figure 12-131. PLL8_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-264. PLL8_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.132 PLL8_LOCKKEY0 Register (Offset = 8010h) [reset = 0h]

PLL8_LOCKKEY0 is shown in Figure 12-132 and described in Table 12-266.

Return to Summary Table.

PLL8_LOCKKEY0 - PLL8 Lock Key 0 Register

Table 12-265. PLL8_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 8010h

Figure 12-132. PLL8_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-266. PLL8_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition8 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.133 PLL8_LOCKKEY1 Register (Offset = 8014h) [reset = 0h]

PLL8_LOCKKEY1 is shown in Figure 12-133 and described in Table 12-268.

Return to Summary Table.

PLL8_LOCKKEY1 - PLL8 Lock Key 1 RegisterAddr

Table 12-267. PLL8_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 8014h

Figure 12-133. PLL8_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-268. PLL8_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition8 registers

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12.134 PLL8_CTRL Register (Offset = 8020h) [reset = X]

PLL8_CTRL is shown in Figure 12-134 and described in Table 12-270.

Return to Summary Table.

PLL8_CTRL - PLL8 Control

Table 12-269. PLL8_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 8020h

Figure 12-134. PLL8_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-270. PLL8_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-270. PLL8_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.135 PLL8_STAT Register (Offset = 8024h) [reset = X]

PLL8_STAT is shown in Figure 12-135 and described in Table 12-272.

Return to Summary Table.

PLL8_STAT - PLL8 Status

Table 12-271. PLL8_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 8024h

Figure 12-135. PLL8_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-272. PLL8_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.136 PLL8_FREQ_CTRL0 Register (Offset = 8030h) [reset = X]

PLL8_FREQ_CTRL0 is shown in Figure 12-136 and described in Table 12-274.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL8 Frequency Control 8 Register

Table 12-273. PLL8_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 8030h

Figure 12-136. PLL8_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-274. PLL8_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.137 PLL8_FREQ_CTRL1 Register (Offset = 8034h) [reset = X]

PLL8_FREQ_CTRL1 is shown in Figure 12-137 and described in Table 12-276.

Return to Summary Table.

PLL8_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-275. PLL8_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 8034h

Figure 12-137. PLL8_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-276. PLL8_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.138 PLL8_DIV_CTRL Register (Offset = 8038h) [reset = X]

PLL8_DIV_CTRL is shown in Figure 12-138 and described in Table 12-278.

Return to Summary Table.

PLL8_DIV_CTRL - PLL8 Output Clock Divider Register

Table 12-277. PLL8_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 8038h

Figure 12-138. PLL8_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-278. PLL8_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.139 PLL8_SS_CTRL Register (Offset = 8040h) [reset = X]

PLL8_SS_CTRL is shown in Figure 12-139 and described in Table 12-280.

Return to Summary Table.

PLL_SS_CTRL register for pll8

Table 12-279. PLL8_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 8040h

Figure 12-139. PLL8_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-280. PLL8_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.140 PLL8_SS_SPREAD Register (Offset = 8044h) [reset = X]

PLL8_SS_SPREAD is shown in Figure 12-140 and described in Table 12-282.

Return to Summary Table.

PLL_SS_SPREAD register for pll8

Table 12-281. PLL8_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 8044h

Figure 12-140. PLL8_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-282. PLL8_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.141 PLL8_HSDIV_CTRL0 Register (Offset = 8080h) [reset = X]

PLL8_HSDIV_CTRL0 is shown in Figure 12-141 and described in Table 12-284.

Return to Summary Table.

HSDIV_CTRL0 register for pll8

Table 12-283. PLL8_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 8080h

Figure 12-141. PLL8_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-284. PLL8_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.142 PLL9_PID Register (Offset = 9000h) [reset = 61801001h]

PLL9_PID is shown in Figure 12-142 and described in Table 12-286.

Return to Summary Table.

Peripheral Identification Register

Table 12-285. PLL9_PID Instances

Instance	Physical Address
PLL0_CFG	0068 9000h

Figure 12-142. PLL9_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-286. PLL9_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.143 PLL9_CFG Register (Offset = 9008h) [reset = X]

PLL9_CFG is shown in Figure 12-143 and described in Table 12-288.

Return to Summary Table.

PLL Configuration

Table 12-287. PLL9_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 9008h

Figure 12-143. PLL9_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-288. PLL9_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.144 PLL9_LOCKKEY0 Register (Offset = 9010h) [reset = 0h]

PLL9_LOCKKEY0 is shown in Figure 12-144 and described in Table 12-290.

Return to Summary Table.

PLL9_LOCKKEY0 - PLL9 Lock Key 0 Register

Table 12-289. PLL9_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 9010h

Figure 12-144. PLL9_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-290. PLL9_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition9 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.145 PLL9_LOCKKEY1 Register (Offset = 9014h) [reset = 0h]

PLL9_LOCKKEY1 is shown in Figure 12-145 and described in Table 12-292.

Return to Summary Table.

PLL9_LOCKKEY1 - PLL9 Lock Key 1 RegisterAddr

Table 12-291. PLL9_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 9014h

Figure 12-145. PLL9_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-292. PLL9_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition9 registers

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12.146 PLL9_CTRL Register (Offset = 9020h) [reset = X]

PLL9_CTRL is shown in Figure 12-146 and described in Table 12-294.

Return to Summary Table.

PLL9_CTRL - PLL9 Control

Table 12-293. PLL9_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 9020h

Figure 12-146. PLL9_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-294. PLL9_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-294. PLL9_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.147 PLL9_STAT Register (Offset = 9024h) [reset = X]

PLL9_STAT is shown in Figure 12-147 and described in Table 12-296.

Return to Summary Table.

PLL9_STAT - PLL9 Status

Table 12-295. PLL9_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 9024h

Figure 12-147. PLL9_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-296. PLL9_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.148 PLL9_FREQ_CTRL0 Register (Offset = 9030h) [reset = X]

PLL9_FREQ_CTRL0 is shown in Figure 12-148 and described in Table 12-298.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL9 Frequency Control 9 Register

Table 12-297. PLL9_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 9030h

Figure 12-148. PLL9_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-298. PLL9_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.149 PLL9_FREQ_CTRL1 Register (Offset = 9034h) [reset = X]

PLL9_FREQ_CTRL1 is shown in Figure 12-149 and described in Table 12-300.

Return to Summary Table.

PLL9_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-299. PLL9_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 9034h

Figure 12-149. PLL9_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-300. PLL9_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.150 PLL9_DIV_CTRL Register (Offset = 9038h) [reset = X]

PLL9_DIV_CTRL is shown in Figure 12-150 and described in Table 12-302.

Return to Summary Table.

PLL9_DIV_CTRL - PLL9 Output Clock Divider Register

Table 12-301. PLL9_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 9038h

Figure 12-150. PLL9_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-302. PLL9_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 633

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12.151 PLL9_SS_CTRL Register (Offset = 9040h) [reset = X]

PLL9_SS_CTRL is shown in Figure 12-151 and described in Table 12-304.

Return to Summary Table.

PLL_SS_CTRL register for pll9

Table 12-303. PLL9_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 9040h

Figure 12-151. PLL9_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-304. PLL9_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.152 PLL9_SS_SPREAD Register (Offset = 9044h) [reset = X]

PLL9_SS_SPREAD is shown in Figure 12-152 and described in Table 12-306.

Return to Summary Table.

PLL_SS_SPREAD register for pll9

Table 12-305. PLL9_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 9044h

Figure 12-152. PLL9_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-306. PLL9_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.153 PLL9_HSDIV_CTRL0 Register (Offset = 9080h) [reset = X]

PLL9_HSDIV_CTRL0 is shown in Figure 12-153 and described in Table 12-308.

Return to Summary Table.

HSDIV_CTRL0 register for pll9

Table 12-307. PLL9_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 9080h

Figure 12-153. PLL9_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-308. PLL9_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.154 PLL12_PID Register (Offset = C000h) [reset = 61801001h]

PLL12_PID is shown in Figure 12-154 and described in Table 12-310.

Return to Summary Table.

Peripheral Identification Register

Table 12-309. PLL12_PID Instances

Instance	Physical Address
PLL0_CFG	0068 C000h

Figure 12-154. PLL12_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-310. PLL12_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.155 PLL12_CFG Register (Offset = C008h) [reset = X]

PLL12_CFG is shown in Figure 12-155 and described in Table 12-312.

Return to Summary Table.

PLL Configuration

Table 12-311. PLL12_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 C008h

Figure 12-155. PLL12_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-1h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-312. PLL12_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	1h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.156 PLL12_LOCKKEY0 Register (Offset = C010h) [reset = 0h]

PLL12_LOCKKEY0 is shown in Figure 12-156 and described in Table 12-314.

Return to Summary Table.

PLL12_LOCKKEY0 - PLL12 Lock Key 0 Register

Table 12-313. PLL12_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 C010h

Figure 12-156. PLL12_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-314. PLL12_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition12 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.157 PLL12_LOCKKEY1 Register (Offset = C014h) [reset = 0h]

PLL12_LOCKKEY1 is shown in Figure 12-157 and described in Table 12-316.

Return to Summary Table.

PLL12_LOCKKEY1 - PLL12 Lock Key 1 RegisterAddr

Table 12-315. PLL12_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 C014h

Figure 12-157. PLL12_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-316. PLL12_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition12 registers

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12.158 PLL12_CTRL Register (Offset = C020h) [reset = X]

PLL12_CTRL is shown in Figure 12-158 and described in Table 12-318.

Return to Summary Table.

PLL12_CTRL - PLL12 Control

Table 12-317. PLL12_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 C020h

Figure 12-158. PLL12_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-318. PLL12_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-318. PLL12_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.159 PLL12_STAT Register (Offset = C024h) [reset = X]

PLL12_STAT is shown in Figure 12-159 and described in Table 12-320.

Return to Summary Table.

PLL12_STAT - PLL12 Status

Table 12-319. PLL12_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 C024h

Figure 12-159. PLL12_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-320. PLL12_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.160 PLL12_FREQ_CTRL0 Register (Offset = C030h) [reset = X]

PLL12_FREQ_CTRL0 is shown in Figure 12-160 and described in Table 12-322.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL12 Frequency Control 12 Register

Table 12-321. PLL12_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 C030h

Figure 12-160. PLL12_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-322. PLL12_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.161 PLL12_FREQ_CTRL1 Register (Offset = C034h) [reset = X]

PLL12_FREQ_CTRL1 is shown in Figure 12-161 and described in Table 12-324.

Return to Summary Table.

PLL12_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-323. PLL12_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 C034h

Figure 12-161. PLL12_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-324. PLL12_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.162 PLL12_DIV_CTRL Register (Offset = C038h) [reset = X]

PLL12_DIV_CTRL is shown in Figure 12-162 and described in Table 12-326.

Return to Summary Table.

PLL12_DIV_CTRL - PLL12 Output Clock Divider Register

Table 12-325. PLL12_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 C038h

Figure 12-162. PLL12_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-326. PLL12_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.163 PLL12_SS_CTRL Register (Offset = C040h) [reset = X]

PLL12_SS_CTRL is shown in Figure 12-163 and described in Table 12-328.

Return to Summary Table.

PLL_SS_CTRL register for pll12

Table 12-327. PLL12_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 C040h

Figure 12-163. PLL12_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-328. PLL12_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.164 PLL12_SS_SPREAD Register (Offset = C044h) [reset = X]

PLL12_SS_SPREAD is shown in Figure 12-164 and described in Table 12-330.

Return to Summary Table.

PLL_SS_SPREAD register for pll12

Table 12-329. PLL12_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 C044h

Figure 12-164. PLL12_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-330. PLL12_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.165 PLL12_CAL_CTRL Register (Offset = C060h) [reset = X]

PLL12_CAL_CTRL is shown in Figure 12-165 and described in Table 12-332.

Return to Summary Table.

PLL12_CAL_CTRL - PLL12 Calibration Control Register

Table 12-331. PLL12_CAL_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 C060h

Figure 12-165. PLL12_CAL_CTRL Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
R/W-X			R/W-0h	R/W-X	R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CAL_BYP	RESERVED			CAL_IN			
R/W-0h	R/W-X			R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAL_IN							
R/W-0h							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-332. PLL12_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input
30-21	RESERVED	R/W	X	
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known
19	RESERVED	R/W	X	
18-16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction
14-12	RESERVED	R/W	X	
11-0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset.

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12.166 PLL12_CAL_STAT Register (Offset = C064h) [reset = X]

PLL12_CAL_STAT is shown in Figure 12-166 and described in Table 12-334.

Return to Summary Table.

PLL12_CAL_STAT - PLL12 Calibration Status Register

Table 12-333. PLL12_CAL_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 C064h

Figure 12-166. PLL12_CAL_STAT Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R-0h	R-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LOCK_CNT			
R-X				R-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				CAL_OUT			
R-X				R-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAL_OUT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 12-334. PLL12_CAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use
30-20	RESERVED	R	X	
19-16	LOCK_CNT	R	0h	Reserved for future use
15-12	RESERVED	R	X	
11-0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in [11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration

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12.167 PLL12_HSDIV_CTRL0 Register (Offset = C080h) [reset = X]

PLL12_HSDIV_CTRL0 is shown in Figure 12-167 and described in Table 12-336.

Return to Summary Table.

HSDIV_CTRL0 register for pll12

Table 12-335. PLL12_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 C080h

Figure 12-167. PLL12_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-336. PLL12_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.168 PLL13_PID Register (Offset = D000h) [reset = 61801001h]

PLL13_PID is shown in Figure 12-168 and described in Table 12-338.

Return to Summary Table.

Peripheral Identification Register

Table 12-337. PLL13_PID Instances

Instance	Physical Address
PLL0_CFG	0068 D000h

Figure 12-168. PLL13_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-338. PLL13_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.169 PLL13_CFG Register (Offset = D008h) [reset = X]

PLL13_CFG is shown in Figure 12-169 and described in Table 12-340.

Return to Summary Table.

PLL Configuration

Table 12-339. PLL13_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 D008h

Figure 12-169. PLL13_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-Fh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-Fh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-340. PLL13_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.170 PLL13_LOCKKEY0 Register (Offset = D010h) [reset = 0h]

PLL13_LOCKKEY0 is shown in Figure 12-170 and described in Table 12-342.

Return to Summary Table.

PLL13_LOCKKEY0 - PLL13 Lock Key 0 Register

Table 12-341. PLL13_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 D010h

Figure 12-170. PLL13_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-342. PLL13_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition13 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.171 PLL13_LOCKKEY1 Register (Offset = D014h) [reset = 0h]

PLL13_LOCKKEY1 is shown in Figure 12-171 and described in Table 12-344.

Return to Summary Table.

PLL13_LOCKKEY1 - PLL13 Lock Key 1 RegisterAddr

Table 12-343. PLL13_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 D014h

Figure 12-171. PLL13_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-344. PLL13_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition13 registers

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12.172 PLL13_CTRL Register (Offset = D020h) [reset = X]

PLL13_CTRL is shown in Figure 12-172 and described in Table 12-346.

Return to Summary Table.

PLL13_CTRL - PLL13 Control

Table 12-345. PLL13_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 D020h

Figure 12-172. PLL13_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-346. PLL13_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-346. PLL13_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.173 PLL13_STAT Register (Offset = D024h) [reset = X]

PLL13_STAT is shown in Figure 12-173 and described in Table 12-348.

Return to Summary Table.

PLL13_STAT - PLL13 Status

Table 12-347. PLL13_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 D024h

Figure 12-173. PLL13_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-348. PLL13_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.174 PLL13_FREQ_CTRL0 Register (Offset = D030h) [reset = X]

PLL13_FREQ_CTRL0 is shown in Figure 12-174 and described in Table 12-350.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL13 Frequency Control 13 Register

Table 12-349. PLL13_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 D030h

Figure 12-174. PLL13_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-350. PLL13_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.175 PLL13_FREQ_CTRL1 Register (Offset = D034h) [reset = X]

PLL13_FREQ_CTRL1 is shown in Figure 12-175 and described in Table 12-352.

Return to Summary Table.

PLL13_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-351. PLL13_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 D034h

Figure 12-175. PLL13_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-352. PLL13_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.176 PLL13_DIV_CTRL Register (Offset = D038h) [reset = X]

PLL13_DIV_CTRL is shown in Figure 12-176 and described in Table 12-354.

Return to Summary Table.

PLL13_DIV_CTRL - PLL13 Output Clock Divider Register

Table 12-353. PLL13_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 D038h

Figure 12-176. PLL13_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-354. PLL13_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.177 PLL13_SS_CTRL Register (Offset = D040h) [reset = X]

PLL13_SS_CTRL is shown in Figure 12-177 and described in Table 12-356.

Return to Summary Table.

PLL_SS_CTRL register for pll13

Table 12-355. PLL13_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 D040h

Figure 12-177. PLL13_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-356. PLL13_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.178 PLL13_SS_SPREAD Register (Offset = D044h) [reset = X]

PLL13_SS_SPREAD is shown in Figure 12-178 and described in Table 12-358.

Return to Summary Table.

PLL_SS_SPREAD register for pll13

Table 12-357. PLL13_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 D044h

Figure 12-178. PLL13_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-358. PLL13_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.179 PLL13_HSDIV_CTRL0 Register (Offset = D080h) [reset = X]

PLL13_HSDIV_CTRL0 is shown in Figure 12-179 and described in Table 12-360.

Return to Summary Table.

HSDIV_CTRL0 register for pll13

Table 12-359. PLL13_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 D080h

Figure 12-179. PLL13_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-360. PLL13_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.180 PLL13_HSDIV_CTRL1 Register (Offset = D084h) [reset = X]

PLL13_HSDIV_CTRL1 is shown in Figure 12-180 and described in Table 12-362.

Return to Summary Table.

HSDIV_CTRL1 register for pll13

Table 12-361. PLL13_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 D084h

Figure 12-180. PLL13_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-362. PLL13_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.181 PLL13_HSDIV_CTRL2 Register (Offset = D088h) [reset = X]

PLL13_HSDIV_CTRL2 is shown in Figure 12-181 and described in Table 12-364.

Return to Summary Table.

HSDIV_CTRL2 register for pll13

Table 12-363. PLL13_HSDIV_CTRL2 Instances

Instance	Physical Address
PLL0_CFG	0068 D088h

Figure 12-181. PLL13_HSDIV_CTRL2 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-364. PLL13_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.182 PLL13_HSDIV_CTRL3 Register (Offset = D08Ch) [reset = X]

PLL13_HSDIV_CTRL3 is shown in Figure 12-182 and described in Table 12-366.

Return to Summary Table.

HSDIV_CTRL3 register for pll13

Table 12-365. PLL13_HSDIV_CTRL3 Instances

Instance	Physical Address
PLL0_CFG	0068 D08Ch

Figure 12-182. PLL13_HSDIV_CTRL3 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-366. PLL13_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.183 PLL14_PID Register (Offset = E000h) [reset = 61801001h]

PLL14_PID is shown in Figure 12-183 and described in Table 12-368.

Return to Summary Table.

Peripheral Identification Register

Table 12-367. PLL14_PID Instances

Instance	Physical Address
PLL0_CFG	0068 E000h

Figure 12-183. PLL14_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-368. PLL14_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.184 PLL14_CFG Register (Offset = E008h) [reset = X]

PLL14_CFG is shown in Figure 12-184 and described in Table 12-370.

Return to Summary Table.

PLL Configuration

Table 12-369. PLL14_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 E008h

Figure 12-184. PLL14_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-370. PLL14_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.185 PLL14_LOCKKEY0 Register (Offset = E010h) [reset = 0h]

PLL14_LOCKKEY0 is shown in Figure 12-185 and described in Table 12-372.

Return to Summary Table.

PLL14_LOCKKEY0 - PLL14 Lock Key 0 Register

Table 12-371. PLL14_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 E010h

Figure 12-185. PLL14_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-372. PLL14_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition14 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.186 PLL14_LOCKKEY1 Register (Offset = E014h) [reset = 0h]

PLL14_LOCKKEY1 is shown in Figure 12-186 and described in Table 12-374.

Return to Summary Table.

PLL14_LOCKKEY1 - PLL14 Lock Key 1 RegisterAddr

Table 12-373. PLL14_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 E014h

Figure 12-186. PLL14_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-374. PLL14_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition14 registers

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12.187 PLL14_CTRL Register (Offset = E020h) [reset = X]

PLL14_CTRL is shown in Figure 12-187 and described in Table 12-376.

Return to Summary Table.

PLL14_CTRL - PLL14 Control

Table 12-375. PLL14_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 E020h

Figure 12-187. PLL14_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-376. PLL14_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-376. PLL14_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.188 PLL14_STAT Register (Offset = E024h) [reset = X]

PLL14_STAT is shown in Figure 12-188 and described in Table 12-378.

Return to Summary Table.

PLL14_STAT - PLL14 Status

Table 12-377. PLL14_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 E024h

Figure 12-188. PLL14_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-378. PLL14_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.189 PLL14_FREQ_CTRL0 Register (Offset = E030h) [reset = X]

PLL14_FREQ_CTRL0 is shown in Figure 12-189 and described in Table 12-380.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL14 Frequency Control 14 Register

Table 12-379. PLL14_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 E030h

Figure 12-189. PLL14_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-380. PLL14_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.190 PLL14_FREQ_CTRL1 Register (Offset = E034h) [reset = X]

PLL14_FREQ_CTRL1 is shown in Figure 12-190 and described in Table 12-382.

Return to Summary Table.

PLL14_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-381. PLL14_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 E034h

Figure 12-190. PLL14_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-382. PLL14_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.191 PLL14_DIV_CTRL Register (Offset = E038h) [reset = X]

PLL14_DIV_CTRL is shown in Figure 12-191 and described in Table 12-384.

Return to Summary Table.

PLL14_DIV_CTRL - PLL14 Output Clock Divider Register

Table 12-383. PLL14_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 E038h

Figure 12-191. PLL14_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-384. PLL14_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.192 PLL14_SS_CTRL Register (Offset = E040h) [reset = X]

PLL14_SS_CTRL is shown in Figure 12-192 and described in Table 12-386.

Return to Summary Table.

PLL_SS_CTRL register for pll14

Table 12-385. PLL14_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 E040h

Figure 12-192. PLL14_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-386. PLL14_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.193 PLL14_SS_SPREAD Register (Offset = E044h) [reset = X]

PLL14_SS_SPREAD is shown in Figure 12-193 and described in Table 12-388.

Return to Summary Table.

PLL_SS_SPREAD register for pll14

Table 12-387. PLL14_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 E044h

Figure 12-193. PLL14_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-388. PLL14_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.194 PLL14_HSDIV_CTRL0 Register (Offset = E080h) [reset = X]

PLL14_HSDIV_CTRL0 is shown in Figure 12-194 and described in Table 12-390.

Return to Summary Table.

HSDIV_CTRL0 register for pll14

Table 12-389. PLL14_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 E080h

Figure 12-194. PLL14_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-390. PLL14_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.195 PLL14_HSDIV_CTRL1 Register (Offset = E084h) [reset = X]

PLL14_HSDIV_CTRL1 is shown in Figure 12-195 and described in Table 12-392.

Return to Summary Table.

HSDIV_CTRL1 register for pll14

Table 12-391. PLL14_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 E084h

Figure 12-195. PLL14_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-392. PLL14_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.196 PLL15_PID Register (Offset = F000h) [reset = 61801001h]

PLL15_PID is shown in Figure 12-196 and described in Table 12-394.

Return to Summary Table.

Peripheral Identification Register

Table 12-393. PLL15_PID Instances

Instance	Physical Address
PLL0_CFG	0068 F000h

Figure 12-196. PLL15_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-394. PLL15_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.197 PLL15_CFG Register (Offset = F008h) [reset = X]

PLL15_CFG is shown in Figure 12-197 and described in Table 12-396.

Return to Summary Table.

PLL Configuration

Table 12-395. PLL15_CFG Instances

Instance	Physical Address
PLL0_CFG	0068 F008h

Figure 12-197. PLL15_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-Fh							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-Fh							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-396. PLL15_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	Fh	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.198 PLL15_LOCKKEY0 Register (Offset = F010h) [reset = 0h]

PLL15_LOCKKEY0 is shown in Figure 12-198 and described in Table 12-398.

Return to Summary Table.

PLL15_LOCKKEY0 - PLL15 Lock Key 0 Register

Table 12-397. PLL15_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0068 F010h

Figure 12-198. PLL15_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-398. PLL15_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition15 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.199 PLL15_LOCKKEY1 Register (Offset = F014h) [reset = 0h]

PLL15_LOCKKEY1 is shown in Figure 12-199 and described in Table 12-400.

Return to Summary Table.

PLL15_LOCKKEY1 - PLL15 Lock Key 1 RegisterAddr

Table 12-399. PLL15_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0068 F014h

Figure 12-199. PLL15_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-400. PLL15_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition15 registers

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12.200 PLL15_CTRL Register (Offset = F020h) [reset = X]

PLL15_CTRL is shown in Figure 12-200 and described in Table 12-402.

Return to Summary Table.

PLL15_CTRL - PLL15 Control

Table 12-401. PLL15_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 F020h

Figure 12-200. PLL15_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-402. PLL15_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-402. PLL15_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.201 PLL15_STAT Register (Offset = F024h) [reset = X]

PLL15_STAT is shown in Figure 12-201 and described in Table 12-404.

Return to Summary Table.

PLL15_STAT - PLL15 Status

Table 12-403. PLL15_STAT Instances

Instance	Physical Address
PLL0_CFG	0068 F024h

Figure 12-201. PLL15_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-404. PLL15_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.202 PLL15_FREQ_CTRL0 Register (Offset = F030h) [reset = X]

PLL15_FREQ_CTRL0 is shown in Figure 12-202 and described in Table 12-406.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL15 Frequency Control 15 Register

Table 12-405. PLL15_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 F030h

Figure 12-202. PLL15_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-406. PLL15_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.203 PLL15_FREQ_CTRL1 Register (Offset = F034h) [reset = X]

PLL15_FREQ_CTRL1 is shown in Figure 12-203 and described in Table 12-408.

Return to Summary Table.

PLL15_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-407. PLL15_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 F034h

Figure 12-203. PLL15_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-408. PLL15_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.204 PLL15_DIV_CTRL Register (Offset = F038h) [reset = X]

PLL15_DIV_CTRL is shown in Figure 12-204 and described in Table 12-410.

Return to Summary Table.

PLL15_DIV_CTRL - PLL15 Output Clock Divider Register

Table 12-409. PLL15_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 F038h

Figure 12-204. PLL15_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-410. PLL15_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.205 PLL15_SS_CTRL Register (Offset = F040h) [reset = X]

PLL15_SS_CTRL is shown in Figure 12-205 and described in Table 12-412.

Return to Summary Table.

PLL_SS_CTRL register for pll15

Table 12-411. PLL15_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0068 F040h

Figure 12-205. PLL15_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-412. PLL15_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.206 PLL15_SS_SPREAD Register (Offset = F044h) [reset = X]

PLL15_SS_SPREAD is shown in Figure 12-206 and described in Table 12-414.

Return to Summary Table.

PLL_SS_SPREAD register for pll15

Table 12-413. PLL15_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0068 F044h

Figure 12-206. PLL15_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-414. PLL15_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.207 PLL15_HSDIV_CTRL0 Register (Offset = F080h) [reset = X]

PLL15_HSDIV_CTRL0 is shown in Figure 12-207 and described in Table 12-416.

Return to Summary Table.

HSDIV_CTRL0 register for pll15

Table 12-415. PLL15_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0068 F080h

Figure 12-207. PLL15_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-416. PLL15_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.208 PLL15_HSDIV_CTRL1 Register (Offset = F084h) [reset = X]

PLL15_HSDIV_CTRL1 is shown in Figure 12-208 and described in Table 12-418.

Return to Summary Table.

HSDIV_CTRL1 register for pll15

Table 12-417. PLL15_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0068 F084h

Figure 12-208. PLL15_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-418. PLL15_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.209 PLL15_HSDIV_CTRL2 Register (Offset = F088h) [reset = X]

PLL15_HSDIV_CTRL2 is shown in Figure 12-209 and described in Table 12-420.

Return to Summary Table.

HSDIV_CTRL2 register for pll15

Table 12-419. PLL15_HSDIV_CTRL2 Instances

Instance	Physical Address
PLL0_CFG	0068 F088h

Figure 12-209. PLL15_HSDIV_CTRL2 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-420. PLL15_HSDIV_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.210 PLL15_HSDIV_CTRL3 Register (Offset = F08Ch) [reset = X]

PLL15_HSDIV_CTRL3 is shown in Figure 12-210 and described in Table 12-422.

Return to Summary Table.

HSDIV_CTRL3 register for pll15

Table 12-421. PLL15_HSDIV_CTRL3 Instances

Instance	Physical Address
PLL0_CFG	0068 F08Ch

Figure 12-210. PLL15_HSDIV_CTRL3 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-422. PLL15_HSDIV_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.211 PLL16_PID Register (Offset = 00010000h) [reset = 61801001h]

PLL16_PID is shown in Figure 12-211 and described in Table 12-424.

Return to Summary Table.

Peripheral Identification Register

Table 12-423. PLL16_PID Instances

Instance	Physical Address
PLL0_CFG	0069 0000h

Figure 12-211. PLL16_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-424. PLL16_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.212 PLL16_CFG Register (Offset = 00010008h) [reset = X]

PLL16_CFG is shown in Figure 12-212 and described in Table 12-426.

Return to Summary Table.

PLL Configuration

Table 12-425. PLL16_CFG Instances

Instance	Physical Address
PLL0_CFG	0069 0008h

Figure 12-212. PLL16_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-426. PLL16_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.213 PLL16_LOCKKEY0 Register (Offset = 00010010h) [reset = 0h]

PLL16_LOCKKEY0 is shown in Figure 12-213 and described in Table 12-428.

Return to Summary Table.

PLL16_LOCKKEY0 - PLL16 Lock Key 0 Register

Table 12-427. PLL16_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0069 0010h

Figure 12-213. PLL16_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-428. PLL16_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition16 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.214 PLL16_LOCKKEY1 Register (Offset = 00010014h) [reset = 0h]

PLL16_LOCKKEY1 is shown in Figure 12-214 and described in Table 12-430.

Return to Summary Table.

PLL16_LOCKKEY1 - PLL16 Lock Key 1 RegisterAddr

Table 12-429. PLL16_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0069 0014h

Figure 12-214. PLL16_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-430. PLL16_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition16 registers

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12.215 PLL16_CTRL Register (Offset = 00010020h) [reset = X]

PLL16_CTRL is shown in Figure 12-215 and described in Table 12-432.

Return to Summary Table.

PLL16_CTRL - PLL16 Control

Table 12-431. PLL16_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 0020h

Figure 12-215. PLL16_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h

7	6	5	4	3	2	1	0
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-432. PLL16_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-432. PLL16_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.216 PLL16_STAT Register (Offset = 00010024h) [reset = X]

PLL16_STAT is shown in Figure 12-216 and described in Table 12-434.

Return to Summary Table.

PLL16_STAT - PLL16 Status

Table 12-433. PLL16_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 0024h

Figure 12-216. PLL16_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-434. PLL16_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.217 PLL16_FREQ_CTRL0 Register (Offset = 00010030h) [reset = X]

PLL16_FREQ_CTRL0 is shown in Figure 12-217 and described in Table 12-436.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL16 Frequency Control 16 Register

Table 12-435. PLL16_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 0030h

Figure 12-217. PLL16_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-436. PLL16_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.218 PLL16_FREQ_CTRL1 Register (Offset = 00010034h) [reset = X]

PLL16_FREQ_CTRL1 is shown in Figure 12-218 and described in Table 12-438.

Return to Summary Table.

PLL16_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-437. PLL16_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 0034h

Figure 12-218. PLL16_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-438. PLL16_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.219 PLL16_DIV_CTRL Register (Offset = 00010038h) [reset = X]

PLL16_DIV_CTRL is shown in Figure 12-219 and described in Table 12-440.

Return to Summary Table.

PLL16_DIV_CTRL - PLL16 Output Clock Divider Register

Table 12-439. PLL16_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 0038h

Figure 12-219. PLL16_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-440. PLL16_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.220 PLL16_SS_CTRL Register (Offset = 00010040h) [reset = X]

PLL16_SS_CTRL is shown in Figure 12-220 and described in Table 12-442.

Return to Summary Table.

PLL_SS_CTRL register for pll16

Table 12-441. PLL16_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 0040h

Figure 12-220. PLL16_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-442. PLL16_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.221 PLL16_SS_SPREAD Register (Offset = 00010044h) [reset = X]

PLL16_SS_SPREAD is shown in Figure 12-221 and described in Table 12-444.

Return to Summary Table.

PLL_SS_SPREAD register for pll16

Table 12-443. PLL16_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0069 0044h

Figure 12-221. PLL16_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-444. PLL16_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.222 PLL16_HSDIV_CTRL0 Register (Offset = 00010080h) [reset = X]

PLL16_HSDIV_CTRL0 is shown in Figure 12-222 and described in Table 12-446.

Return to Summary Table.

HSDIV_CTRL0 register for pll16

Table 12-445. PLL16_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 0080h

Figure 12-222. PLL16_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-446. PLL16_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.223 PLL16_HSDIV_CTRL1 Register (Offset = 00010084h) [reset = X]

PLL16_HSDIV_CTRL1 is shown in Figure 12-223 and described in Table 12-448.

Return to Summary Table.

HSDIV_CTRL1 register for pll16

Table 12-447. PLL16_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 0084h

Figure 12-223. PLL16_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-448. PLL16_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.224 PLL17_PID Register (Offset = 00011000h) [reset = 61801001h]

PLL17_PID is shown in Figure 12-224 and described in Table 12-450.

Return to Summary Table.

Peripheral Identification Register

Table 12-449. PLL17_PID Instances

Instance	Physical Address
PLL0_CFG	0069 1000h

Figure 12-224. PLL17_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-450. PLL17_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.225 PLL17_CFG Register (Offset = 00011008h) [reset = X]

PLL17_CFG is shown in Figure 12-225 and described in Table 12-452.

Return to Summary Table.

PLL Configuration

Table 12-451. PLL17_CFG Instances

Instance	Physical Address
PLL0_CFG	0069 1008h

Figure 12-225. PLL17_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-452. PLL17_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.226 PLL17_LOCKKEY0 Register (Offset = 00011010h) [reset = 0h]

PLL17_LOCKKEY0 is shown in Figure 12-226 and described in Table 12-454.

Return to Summary Table.

PLL17_LOCKKEY0 - PLL17 Lock Key 0 Register

Table 12-453. PLL17_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0069 1010h

Figure 12-226. PLL17_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-454. PLL17_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition17 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.227 PLL17_LOCKKEY1 Register (Offset = 00011014h) [reset = 0h]

PLL17_LOCKKEY1 is shown in Figure 12-227 and described in Table 12-456.

Return to Summary Table.

PLL17_LOCKKEY1 - PLL17 Lock Key 1 RegisterAddr

Table 12-455. PLL17_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0069 1014h

Figure 12-227. PLL17_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-456. PLL17_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition17 registers

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12.228 PLL17_CTRL Register (Offset = 00011020h) [reset = X]

PLL17_CTRL is shown in Figure 12-228 and described in Table 12-458.

Return to Summary Table.

PLL17_CTRL - PLL17 Control

Table 12-457. PLL17_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 1020h

Figure 12-228. PLL17_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-458. PLL17_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-458. PLL17_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.229 PLL17_STAT Register (Offset = 00011024h) [reset = X]

PLL17_STAT is shown in Figure 12-229 and described in Table 12-460.

Return to Summary Table.

PLL17_STAT - PLL17 Status

Table 12-459. PLL17_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 1024h

Figure 12-229. PLL17_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-460. PLL17_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.230 PLL17_FREQ_CTRL0 Register (Offset = 00011030h) [reset = X]

PLL17_FREQ_CTRL0 is shown in Figure 12-230 and described in Table 12-462.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL17 Frequency Control 17 Register

Table 12-461. PLL17_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 1030h

Figure 12-230. PLL17_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-462. PLL17_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.231 PLL17_FREQ_CTRL1 Register (Offset = 00011034h) [reset = X]

PLL17_FREQ_CTRL1 is shown in Figure 12-231 and described in Table 12-464.

Return to Summary Table.

PLL17_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-463. PLL17_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 1034h

Figure 12-231. PLL17_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-464. PLL17_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.232 PLL17_DIV_CTRL Register (Offset = 00011038h) [reset = X]

PLL17_DIV_CTRL is shown in Figure 12-232 and described in Table 12-466.

Return to Summary Table.

PLL17_DIV_CTRL - PLL17 Output Clock Divider Register

Table 12-465. PLL17_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 1038h

Figure 12-232. PLL17_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-466. PLL17_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.233 PLL17_SS_CTRL Register (Offset = 00011040h) [reset = X]

PLL17_SS_CTRL is shown in Figure 12-233 and described in Table 12-468.

Return to Summary Table.

PLL_SS_CTRL register for pll17

Table 12-467. PLL17_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 1040h

Figure 12-233. PLL17_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-468. PLL17_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.234 PLL17_SS_SPREAD Register (Offset = 00011044h) [reset = X]

PLL17_SS_SPREAD is shown in Figure 12-234 and described in Table 12-470.

Return to Summary Table.

PLL_SS_SPREAD register for pll17

Table 12-469. PLL17_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0069 1044h

Figure 12-234. PLL17_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-470. PLL17_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.235 PLL17_HSDIV_CTRL0 Register (Offset = 00011080h) [reset = X]

PLL17_HSDIV_CTRL0 is shown in Figure 12-235 and described in Table 12-472.

Return to Summary Table.

HSDIV_CTRL0 register for pll17

Table 12-471. PLL17_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 1080h

Figure 12-235. PLL17_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-472. PLL17_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.236 PLL17_HSDIV_CTRL1 Register (Offset = 00011084h) [reset = X]

PLL17_HSDIV_CTRL1 is shown in Figure 12-236 and described in Table 12-474.

Return to Summary Table.

HSDIV_CTRL1 register for pll17

Table 12-473. PLL17_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 1084h

Figure 12-236. PLL17_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-474. PLL17_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.237 PLL18_PID Register (Offset = 00012000h) [reset = 61801001h]

PLL18_PID is shown in Figure 12-237 and described in Table 12-476.

Return to Summary Table.

Peripheral Identification Register

Table 12-475. PLL18_PID Instances

Instance	Physical Address
PLL0_CFG	0069 2000h

Figure 12-237. PLL18_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-476. PLL18_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.238 PLL18_CFG Register (Offset = 00012008h) [reset = X]

PLL18_CFG is shown in Figure 12-238 and described in Table 12-478.

Return to Summary Table.

PLL Configuration

Table 12-477. PLL18_CFG Instances

Instance	Physical Address
PLL0_CFG	0069 2008h

Figure 12-238. PLL18_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-478. PLL18_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.239 PLL18_LOCKKEY0 Register (Offset = 00012010h) [reset = 0h]

PLL18_LOCKKEY0 is shown in Figure 12-239 and described in Table 12-480.

Return to Summary Table.

PLL18_LOCKKEY0 - PLL18 Lock Key 0 Register

Table 12-479. PLL18_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0069 2010h

Figure 12-239. PLL18_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-480. PLL18_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition18 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.240 PLL18_LOCKKEY1 Register (Offset = 00012014h) [reset = 0h]

PLL18_LOCKKEY1 is shown in Figure 12-240 and described in Table 12-482.

Return to Summary Table.

PLL18_LOCKKEY1 - PLL18 Lock Key 1 RegisterAddr

Table 12-481. PLL18_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0069 2014h

Figure 12-240. PLL18_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-482. PLL18_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition18 registers

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12.241 PLL18_CTRL Register (Offset = 00012020h) [reset = X]

PLL18_CTRL is shown in Figure 12-241 and described in Table 12-484.

Return to Summary Table.

PLL18_CTRL - PLL18 Control

Table 12-483. PLL18_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 2020h

Figure 12-241. PLL18_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-484. PLL18_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-484. PLL18_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.242 PLL18_STAT Register (Offset = 00012024h) [reset = X]

PLL18_STAT is shown in Figure 12-242 and described in Table 12-486.

Return to Summary Table.

PLL18_STAT - PLL18 Status

Table 12-485. PLL18_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 2024h

Figure 12-242. PLL18_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-486. PLL18_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.243 PLL18_FREQ_CTRL0 Register (Offset = 00012030h) [reset = X]

PLL18_FREQ_CTRL0 is shown in Figure 12-243 and described in Table 12-488.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL18 Frequency Control 18 Register

Table 12-487. PLL18_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 2030h

Figure 12-243. PLL18_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-488. PLL18_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.244 PLL18_FREQ_CTRL1 Register (Offset = 00012034h) [reset = X]

PLL18_FREQ_CTRL1 is shown in Figure 12-244 and described in Table 12-490.

Return to Summary Table.

PLL18_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-489. PLL18_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 2034h

Figure 12-244. PLL18_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-490. PLL18_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.245 PLL18_DIV_CTRL Register (Offset = 00012038h) [reset = X]

PLL18_DIV_CTRL is shown in Figure 12-245 and described in Table 12-492.

Return to Summary Table.

PLL18_DIV_CTRL - PLL18 Output Clock Divider Register

Table 12-491. PLL18_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 2038h

Figure 12-245. PLL18_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-492. PLL18_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.246 PLL18_SS_CTRL Register (Offset = 00012040h) [reset = X]

PLL18_SS_CTRL is shown in Figure 12-246 and described in Table 12-494.

Return to Summary Table.

PLL_SS_CTRL register for pll18

Table 12-493. PLL18_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 2040h

Figure 12-246. PLL18_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-494. PLL18_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.247 PLL18_SS_SPREAD Register (Offset = 00012044h) [reset = X]

PLL18_SS_SPREAD is shown in Figure 12-247 and described in Table 12-496.

Return to Summary Table.

PLL_SS_SPREAD register for pll18

Table 12-495. PLL18_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0069 2044h

Figure 12-247. PLL18_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-496. PLL18_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.248 PLL18_HSDIV_CTRL0 Register (Offset = 00012080h) [reset = X]

PLL18_HSDIV_CTRL0 is shown in Figure 12-248 and described in Table 12-498.

Return to Summary Table.

HSDIV_CTRL0 register for pll18

Table 12-497. PLL18_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 2080h

Figure 12-248. PLL18_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-498. PLL18_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.249 PLL18_HSDIV_CTRL1 Register (Offset = 00012084h) [reset = X]

PLL18_HSDIV_CTRL1 is shown in Figure 12-249 and described in Table 12-500.

Return to Summary Table.

HSDIV_CTRL1 register for pll18

Table 12-499. PLL18_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 2084h

Figure 12-249. PLL18_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-500. PLL18_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.250 PLL19_PID Register (Offset = 00013000h) [reset = 61801001h]

PLL19_PID is shown in Figure 12-250 and described in Table 12-502.

Return to Summary Table.

Peripheral Identification Register

Table 12-501. PLL19_PID Instances

Instance	Physical Address
PLL0_CFG	0069 3000h

Figure 12-250. PLL19_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-502. PLL19_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.251 PLL19_CFG Register (Offset = 00013008h) [reset = X]

PLL19_CFG is shown in Figure 12-251 and described in Table 12-504.

Return to Summary Table.

PLL Configuration

Table 12-503. PLL19_CFG Instances

Instance	Physical Address
PLL0_CFG	0069 3008h

Figure 12-251. PLL19_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-504. PLL19_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.252 PLL19_LOCKKEY0 Register (Offset = 00013010h) [reset = 0h]

PLL19_LOCKKEY0 is shown in Figure 12-252 and described in Table 12-506.

Return to Summary Table.

PLL19_LOCKKEY0 - PLL19 Lock Key 0 Register

Table 12-505. PLL19_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0069 3010h

Figure 12-252. PLL19_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-506. PLL19_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition19 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.253 PLL19_LOCKKEY1 Register (Offset = 00013014h) [reset = 0h]

PLL19_LOCKKEY1 is shown in Figure 12-253 and described in Table 12-508.

Return to Summary Table.

PLL19_LOCKKEY1 - PLL19 Lock Key 1 RegisterAddr

Table 12-507. PLL19_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0069 3014h

Figure 12-253. PLL19_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-508. PLL19_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition19 registers

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12.254 PLL19_CTRL Register (Offset = 00013020h) [reset = X]

PLL19_CTRL is shown in Figure 12-254 and described in Table 12-510.

Return to Summary Table.

PLL19_CTRL - PLL19 Control

Table 12-509. PLL19_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 3020h

Figure 12-254. PLL19_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-510. PLL19_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-510. PLL19_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.255 PLL19_STAT Register (Offset = 00013024h) [reset = X]

PLL19_STAT is shown in Figure 12-255 and described in Table 12-512.

Return to Summary Table.

PLL19_STAT - PLL19 Status

Table 12-511. PLL19_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 3024h

Figure 12-255. PLL19_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-512. PLL19_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.256 PLL19_FREQ_CTRL0 Register (Offset = 00013030h) [reset = X]

PLL19_FREQ_CTRL0 is shown in Figure 12-256 and described in Table 12-514.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL19 Frequency Control 19 Register

Table 12-513. PLL19_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 3030h

Figure 12-256. PLL19_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-514. PLL19_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.257 PLL19_FREQ_CTRL1 Register (Offset = 00013034h) [reset = X]

PLL19_FREQ_CTRL1 is shown in Figure 12-257 and described in Table 12-516.

Return to Summary Table.

PLL19_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-515. PLL19_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 3034h

Figure 12-257. PLL19_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-516. PLL19_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.258 PLL19_DIV_CTRL Register (Offset = 00013038h) [reset = X]

PLL19_DIV_CTRL is shown in Figure 12-258 and described in Table 12-518.

Return to Summary Table.

PLL19_DIV_CTRL - PLL19 Output Clock Divider Register

Table 12-517. PLL19_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 3038h

Figure 12-258. PLL19_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-518. PLL19_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.259 PLL19_SS_CTRL Register (Offset = 00013040h) [reset = X]

PLL19_SS_CTRL is shown in Figure 12-259 and described in Table 12-520.

Return to Summary Table.

PLL_SS_CTRL register for pll19

Table 12-519. PLL19_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 3040h

Figure 12-259. PLL19_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-520. PLL19_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.260 PLL19_SS_SPREAD Register (Offset = 00013044h) [reset = X]

PLL19_SS_SPREAD is shown in Figure 12-260 and described in Table 12-522.

Return to Summary Table.

PLL_SS_SPREAD register for pll19

Table 12-521. PLL19_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0069 3044h

Figure 12-260. PLL19_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-522. PLL19_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.261 PLL19_HSDIV_CTRL0 Register (Offset = 00013080h) [reset = X]

PLL19_HSDIV_CTRL0 is shown in Figure 12-261 and described in Table 12-524.

Return to Summary Table.

HSDIV_CTRL0 register for pll19

Table 12-523. PLL19_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 3080h

Figure 12-261. PLL19_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-524. PLL19_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.262 PLL19_HSDIV_CTRL1 Register (Offset = 00013084h) [reset = X]

PLL19_HSDIV_CTRL1 is shown in Figure 12-262 and described in Table 12-526.

Return to Summary Table.

HSDIV_CTRL1 register for pll19

Table 12-525. PLL19_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 3084h

Figure 12-262. PLL19_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-526. PLL19_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.263 PLL20_PID Register (Offset = 00014000h) [reset = 61801001h]

PLL20_PID is shown in Figure 12-263 and described in Table 12-528.

Return to Summary Table.

Peripheral Identification Register

Table 12-527. PLL20_PID Instances

Instance	Physical Address
PLL0_CFG	0069 4000h

Figure 12-263. PLL20_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-528. PLL20_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.264 PLL20_CFG Register (Offset = 00014008h) [reset = X]

PLL20_CFG is shown in Figure 12-264 and described in Table 12-530.

Return to Summary Table.

PLL Configuration

Table 12-529. PLL20_CFG Instances

Instance	Physical Address
PLL0_CFG	0069 4008h

Figure 12-264. PLL20_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-530. PLL20_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.265 PLL20_LOCKKEY0 Register (Offset = 00014010h) [reset = 0h]

PLL20_LOCKKEY0 is shown in Figure 12-265 and described in Table 12-532.

Return to Summary Table.

PLL20_LOCKKEY0 - PLL20 Lock Key 0 Register

Table 12-531. PLL20_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0069 4010h

Figure 12-265. PLL20_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-532. PLL20_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition20 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.266 PLL20_LOCKKEY1 Register (Offset = 00014014h) [reset = 0h]

PLL20_LOCKKEY1 is shown in Figure 12-266 and described in Table 12-534.

Return to Summary Table.

PLL20_LOCKKEY1 - PLL20 Lock Key 1 RegisterAddr

Table 12-533. PLL20_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0069 4014h

Figure 12-266. PLL20_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-534. PLL20_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition20 registers

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12.267 PLL20_CTRL Register (Offset = 00014020h) [reset = X]

PLL20_CTRL is shown in Figure 12-267 and described in Table 12-536.

Return to Summary Table.

PLL20_CTRL - PLL20 Control

Table 12-535. PLL20_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 4020h

Figure 12-267. PLL20_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-536. PLL20_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-536. PLL20_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.268 PLL20_STAT Register (Offset = 00014024h) [reset = X]

PLL20_STAT is shown in Figure 12-268 and described in Table 12-538.

Return to Summary Table.

PLL20_STAT - PLL20 Status

Table 12-537. PLL20_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 4024h

Figure 12-268. PLL20_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-538. PLL20_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.269 PLL20_FREQ_CTRL0 Register (Offset = 00014030h) [reset = X]

PLL20_FREQ_CTRL0 is shown in Figure 12-269 and described in Table 12-540.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL20 Frequency Control 20 Register

Table 12-539. PLL20_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 4030h

Figure 12-269. PLL20_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-540. PLL20_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.270 PLL20_FREQ_CTRL1 Register (Offset = 00014034h) [reset = X]

PLL20_FREQ_CTRL1 is shown in Figure 12-270 and described in Table 12-542.

Return to Summary Table.

PLL20_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-541. PLL20_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 4034h

Figure 12-270. PLL20_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-542. PLL20_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.271 PLL20_DIV_CTRL Register (Offset = 00014038h) [reset = X]

PLL20_DIV_CTRL is shown in Figure 12-271 and described in Table 12-544.

Return to Summary Table.

PLL20_DIV_CTRL - PLL20 Output Clock Divider Register

Table 12-543. PLL20_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 4038h

Figure 12-271. PLL20_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-544. PLL20_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.272 PLL20_SS_CTRL Register (Offset = 00014040h) [reset = X]

PLL20_SS_CTRL is shown in Figure 12-272 and described in Table 12-546.

Return to Summary Table.

PLL_SS_CTRL register for pll20

Table 12-545. PLL20_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 4040h

Figure 12-272. PLL20_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-546. PLL20_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.273 PLL20_SS_SPREAD Register (Offset = 00014044h) [reset = X]

PLL20_SS_SPREAD is shown in Figure 12-273 and described in Table 12-548.

Return to Summary Table.

PLL_SS_SPREAD register for pll20

Table 12-547. PLL20_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0069 4044h

Figure 12-273. PLL20_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-548. PLL20_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.274 PLL20_HSDIV_CTRL0 Register (Offset = 00014080h) [reset = X]

PLL20_HSDIV_CTRL0 is shown in Figure 12-274 and described in Table 12-550.

Return to Summary Table.

HSDIV_CTRL0 register for pll20

Table 12-549. PLL20_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 4080h

Figure 12-274. PLL20_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-550. PLL20_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.275 PLL20_HSDIV_CTRL1 Register (Offset = 00014084h) [reset = X]

PLL20_HSDIV_CTRL1 is shown in Figure 12-275 and described in Table 12-552.

Return to Summary Table.

HSDIV_CTRL1 register for pll20

Table 12-551. PLL20_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 4084h

Figure 12-275. PLL20_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-552. PLL20_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.276 PLL21_PID Register (Offset = 00015000h) [reset = 61801001h]

PLL21_PID is shown in Figure 12-276 and described in Table 12-554.

Return to Summary Table.

Peripheral Identification Register

Table 12-553. PLL21_PID Instances

Instance	Physical Address
PLL0_CFG	0069 5000h

Figure 12-276. PLL21_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-554. PLL21_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.277 PLL21_CFG Register (Offset = 00015008h) [reset = X]

PLL21_CFG is shown in Figure 12-277 and described in Table 12-556.

Return to Summary Table.

PLL Configuration

Table 12-555. PLL21_CFG Instances

Instance	Physical Address
PLL0_CFG	0069 5008h

Figure 12-277. PLL21_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-556. PLL21_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.278 PLL21_LOCKKEY0 Register (Offset = 00015010h) [reset = 0h]

PLL21_LOCKKEY0 is shown in Figure 12-278 and described in Table 12-558.

Return to Summary Table.

PLL21_LOCKKEY0 - PLL21 Lock Key 0 Register

Table 12-557. PLL21_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0069 5010h

Figure 12-278. PLL21_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-558. PLL21_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition21 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.279 PLL21_LOCKKEY1 Register (Offset = 00015014h) [reset = 0h]

PLL21_LOCKKEY1 is shown in Figure 12-279 and described in Table 12-560.

Return to Summary Table.

PLL21_LOCKKEY1 - PLL21 Lock Key 1 RegisterAddr

Table 12-559. PLL21_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0069 5014h

Figure 12-279. PLL21_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-560. PLL21_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition21 registers

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12.280 PLL21_CTRL Register (Offset = 00015020h) [reset = X]

PLL21_CTRL is shown in Figure 12-280 and described in Table 12-562.

Return to Summary Table.

PLL21_CTRL - PLL21 Control

Table 12-561. PLL21_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 5020h

Figure 12-280. PLL21_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-562. PLL21_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-562. PLL21_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.281 PLL21_STAT Register (Offset = 00015024h) [reset = X]

PLL21_STAT is shown in Figure 12-281 and described in Table 12-564.

Return to Summary Table.

PLL21_STAT - PLL21 Status

Table 12-563. PLL21_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 5024h

Figure 12-281. PLL21_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-564. PLL21_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.282 PLL21_FREQ_CTRL0 Register (Offset = 00015030h) [reset = X]

PLL21_FREQ_CTRL0 is shown in Figure 12-282 and described in Table 12-566.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL21 Frequency Control 21 Register

Table 12-565. PLL21_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 5030h

Figure 12-282. PLL21_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-566. PLL21_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.283 PLL21_FREQ_CTRL1 Register (Offset = 00015034h) [reset = X]

PLL21_FREQ_CTRL1 is shown in Figure 12-283 and described in Table 12-568.

Return to Summary Table.

PLL21_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-567. PLL21_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 5034h

Figure 12-283. PLL21_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-568. PLL21_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.284 PLL21_DIV_CTRL Register (Offset = 00015038h) [reset = X]

PLL21_DIV_CTRL is shown in Figure 12-284 and described in Table 12-570.

Return to Summary Table.

PLL21_DIV_CTRL - PLL21 Output Clock Divider Register

Table 12-569. PLL21_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 5038h

Figure 12-284. PLL21_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-570. PLL21_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.285 PLL21_SS_CTRL Register (Offset = 00015040h) [reset = X]

PLL21_SS_CTRL is shown in Figure 12-285 and described in Table 12-572.

Return to Summary Table.

PLL_SS_CTRL register for pll21

Table 12-571. PLL21_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 5040h

Figure 12-285. PLL21_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-572. PLL21_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.286 PLL21_SS_SPREAD Register (Offset = 00015044h) [reset = X]

PLL21_SS_SPREAD is shown in Figure 12-286 and described in Table 12-574.

Return to Summary Table.

PLL_SS_SPREAD register for pll21

Table 12-573. PLL21_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0069 5044h

Figure 12-286. PLL21_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-574. PLL21_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.287 PLL21_HSDIV_CTRL0 Register (Offset = 00015080h) [reset = X]

PLL21_HSDIV_CTRL0 is shown in Figure 12-287 and described in Table 12-576.

Return to Summary Table.

HSDIV_CTRL0 register for pll21

Table 12-575. PLL21_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 5080h

Figure 12-287. PLL21_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-576. PLL21_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.288 PLL21_HSDIV_CTRL1 Register (Offset = 00015084h) [reset = X]

PLL21_HSDIV_CTRL1 is shown in Figure 12-288 and described in Table 12-578.

Return to Summary Table.

HSDIV_CTRL1 register for pll21

Table 12-577. PLL21_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 5084h

Figure 12-288. PLL21_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							
R/W-X							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-578. PLL21_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.289 PLL22_PID Register (Offset = 00016000h) [reset = 61801001h]

PLL22_PID is shown in Figure 12-289 and described in Table 12-580.

Return to Summary Table.

Peripheral Identification Register

Table 12-579. PLL22_PID Instances

Instance	Physical Address
PLL0_CFG	0069 6000h

Figure 12-289. PLL22_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-580. PLL22_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.290 PLL22_CFG Register (Offset = 00016008h) [reset = X]

PLL22_CFG is shown in Figure 12-290 and described in Table 12-582.

Return to Summary Table.

PLL Configuration

Table 12-581. PLL22_CFG Instances

Instance	Physical Address
PLL0_CFG	0069 6008h

Figure 12-290. PLL22_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-582. PLL22_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.291 PLL22_LOCKKEY0 Register (Offset = 00016010h) [reset = 0h]

PLL22_LOCKKEY0 is shown in Figure 12-291 and described in Table 12-584.

Return to Summary Table.

PLL22_LOCKKEY0 - PLL22 Lock Key 0 Register

Table 12-583. PLL22_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0069 6010h

Figure 12-291. PLL22_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-584. PLL22_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition22 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.292 PLL22_LOCKKEY1 Register (Offset = 00016014h) [reset = 0h]

PLL22_LOCKKEY1 is shown in Figure 12-292 and described in Table 12-586.

Return to Summary Table.

PLL22_LOCKKEY1 - PLL22 Lock Key 1 RegisterAddr

Table 12-585. PLL22_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0069 6014h

Figure 12-292. PLL22_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-586. PLL22_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition22 registers

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12.293 PLL22_CTRL Register (Offset = 00016020h) [reset = X]

PLL22_CTRL is shown in Figure 12-293 and described in Table 12-588.

Return to Summary Table.

PLL22_CTRL - PLL22 Control

Table 12-587. PLL22_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 6020h

Figure 12-293. PLL22_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-588. PLL22_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-588. PLL22_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.294 PLL22_STAT Register (Offset = 00016024h) [reset = X]

PLL22_STAT is shown in Figure 12-294 and described in Table 12-590.

Return to Summary Table.

PLL22_STAT - PLL22 Status

Table 12-589. PLL22_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 6024h

Figure 12-294. PLL22_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-590. PLL22_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.295 PLL22_FREQ_CTRL0 Register (Offset = 00016030h) [reset = X]

PLL22_FREQ_CTRL0 is shown in Figure 12-295 and described in Table 12-592.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL22 Frequency Control 22 Register

Table 12-591. PLL22_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 6030h

Figure 12-295. PLL22_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-592. PLL22_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.296 PLL22_FREQ_CTRL1 Register (Offset = 00016034h) [reset = X]

PLL22_FREQ_CTRL1 is shown in Figure 12-296 and described in Table 12-594.

Return to Summary Table.

PLL22_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-593. PLL22_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 6034h

Figure 12-296. PLL22_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-594. PLL22_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.297 PLL22_DIV_CTRL Register (Offset = 00016038h) [reset = X]

PLL22_DIV_CTRL is shown in Figure 12-297 and described in Table 12-596.

Return to Summary Table.

PLL22_DIV_CTRL - PLL22 Output Clock Divider Register

Table 12-595. PLL22_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 6038h

Figure 12-297. PLL22_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-596. PLL22_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.298 PLL22_SS_CTRL Register (Offset = 00016040h) [reset = X]

PLL22_SS_CTRL is shown in Figure 12-298 and described in Table 12-598.

Return to Summary Table.

PLL_SS_CTRL register for pll22

Table 12-597. PLL22_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 6040h

Figure 12-298. PLL22_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-598. PLL22_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.299 PLL22_SS_SPREAD Register (Offset = 00016044h) [reset = X]

PLL22_SS_SPREAD is shown in Figure 12-299 and described in Table 12-600.

Return to Summary Table.

PLL_SS_SPREAD register for pll22

Table 12-599. PLL22_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0069 6044h

Figure 12-299. PLL22_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-600. PLL22_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.300 PLL22_HSDIV_CTRL0 Register (Offset = 00016080h) [reset = X]

PLL22_HSDIV_CTRL0 is shown in Figure 12-300 and described in Table 12-602.

Return to Summary Table.

HSDIV_CTRL0 register for pll22

Table 12-601. PLL22_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 6080h

Figure 12-300. PLL22_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-602. PLL22_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.301 PLL22_HSDIV_CTRL1 Register (Offset = 00016084h) [reset = X]

PLL22_HSDIV_CTRL1 is shown in Figure 12-301 and described in Table 12-604.

Return to Summary Table.

HSDIV_CTRL1 register for pll22

Table 12-603. PLL22_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 6084h

Figure 12-301. PLL22_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-604. PLL22_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.302 PLL23_PID Register (Offset = 00017000h) [reset = 61801001h]

PLL23_PID is shown in Figure 12-302 and described in Table 12-606.

Return to Summary Table.

Peripheral Identification Register

Table 12-605. PLL23_PID Instances

Instance	Physical Address
PLL0_CFG	0069 7000h

Figure 12-302. PLL23_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-606. PLL23_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.303 PLL23_CFG Register (Offset = 00017008h) [reset = X]

PLL23_CFG is shown in Figure 12-303 and described in Table 12-608.

Return to Summary Table.

PLL Configuration

Table 12-607. PLL23_CFG Instances

Instance	Physical Address
PLL0_CFG	0069 7008h

Figure 12-303. PLL23_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-608. PLL23_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.304 PLL23_LOCKKEY0 Register (Offset = 00017010h) [reset = 0h]

PLL23_LOCKKEY0 is shown in Figure 12-304 and described in Table 12-610.

Return to Summary Table.

PLL23_LOCKKEY0 - PLL23 Lock Key 0 Register

Table 12-609. PLL23_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0069 7010h

Figure 12-304. PLL23_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-610. PLL23_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition23 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.305 PLL23_LOCKKEY1 Register (Offset = 00017014h) [reset = 0h]

PLL23_LOCKKEY1 is shown in Figure 12-305 and described in Table 12-612.

Return to Summary Table.

PLL23_LOCKKEY1 - PLL23 Lock Key 1 RegisterAddr

Table 12-611. PLL23_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0069 7014h

Figure 12-305. PLL23_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-612. PLL23_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition23 registers

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12.306 PLL23_CTRL Register (Offset = 00017020h) [reset = X]

PLL23_CTRL is shown in Figure 12-306 and described in Table 12-614.

Return to Summary Table.

PLL23_CTRL - PLL23 Control

Table 12-613. PLL23_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 7020h

Figure 12-306. PLL23_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-614. PLL23_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-614. PLL23_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.307 PLL23_STAT Register (Offset = 00017024h) [reset = X]

PLL23_STAT is shown in Figure 12-307 and described in Table 12-616.

Return to Summary Table.

PLL23_STAT - PLL23 Status

Table 12-615. PLL23_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 7024h

Figure 12-307. PLL23_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-616. PLL23_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.308 PLL23_FREQ_CTRL0 Register (Offset = 00017030h) [reset = X]

PLL23_FREQ_CTRL0 is shown in Figure 12-308 and described in Table 12-618.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL23 Frequency Control 23 Register

Table 12-617. PLL23_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 7030h

Figure 12-308. PLL23_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-618. PLL23_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.309 PLL23_FREQ_CTRL1 Register (Offset = 00017034h) [reset = X]

PLL23_FREQ_CTRL1 is shown in Figure 12-309 and described in Table 12-620.

Return to Summary Table.

PLL23_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-619. PLL23_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 7034h

Figure 12-309. PLL23_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-620. PLL23_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.310 PLL23_DIV_CTRL Register (Offset = 00017038h) [reset = X]

PLL23_DIV_CTRL is shown in Figure 12-310 and described in Table 12-622.

Return to Summary Table.

PLL23_DIV_CTRL - PLL23 Output Clock Divider Register

Table 12-621. PLL23_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 7038h

Figure 12-310. PLL23_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-622. PLL23_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.311 PLL23_SS_CTRL Register (Offset = 00017040h) [reset = X]

PLL23_SS_CTRL is shown in Figure 12-311 and described in Table 12-624.

Return to Summary Table.

PLL_SS_CTRL register for pll23

Table 12-623. PLL23_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 7040h

Figure 12-311. PLL23_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-624. PLL23_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.312 PLL23_SS_SPREAD Register (Offset = 00017044h) [reset = X]

PLL23_SS_SPREAD is shown in Figure 12-312 and described in Table 12-626.

Return to Summary Table.

PLL_SS_SPREAD register for pll23

Table 12-625. PLL23_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0069 7044h

Figure 12-312. PLL23_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-626. PLL23_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.313 PLL23_HSDIV_CTRL0 Register (Offset = 00017080h) [reset = X]

PLL23_HSDIV_CTRL0 is shown in Figure 12-313 and described in Table 12-628.

Return to Summary Table.

HSDIV_CTRL0 register for pll23

Table 12-627. PLL23_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 7080h

Figure 12-313. PLL23_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-628. PLL23_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.314 PLL23_HSDIV_CTRL1 Register (Offset = 00017084h) [reset = X]

PLL23_HSDIV_CTRL1 is shown in Figure 12-314 and described in Table 12-630.

Return to Summary Table.

HSDIV_CTRL1 register for pll23

Table 12-629. PLL23_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 7084h

Figure 12-314. PLL23_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-630. PLL23_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.315 PLL24_PID Register (Offset = 00018000h) [reset = 61801001h]

PLL24_PID is shown in Figure 12-315 and described in Table 12-632.

Return to Summary Table.

Table 12-631. PLL24_PID Instances

Instance	Physical Address
PLL0_CFG	0069 8000h

Figure 12-315. PLL24_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-632. PLL24_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.316 PLL24_CFG Register (Offset = 00018008h) [reset = X]

PLL24_CFG is shown in Figure 12-316 and described in Table 12-634.

Return to Summary Table.

PLL Configuration

Table 12-633. PLL24_CFG Instances

Instance	Physical Address
PLL0_CFG	0069 8008h

Figure 12-316. PLL24_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-1h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-1h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-0h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-2h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-634. PLL24_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	1h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	0h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	2h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.317 PLL24_LOCKKEY0 Register (Offset = 00018010h) [reset = 0h]

PLL24_LOCKKEY0 is shown in Figure 12-317 and described in Table 12-636.

Return to Summary Table.

PLL24_LOCKKEY0 - PLL24 Lock Key 0 Register

Table 12-635. PLL24_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0069 8010h

Figure 12-317. PLL24_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-636. PLL24_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition24 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.318 PLL24_LOCKKEY1 Register (Offset = 00018014h) [reset = 0h]

PLL24_LOCKKEY1 is shown in Figure 12-318 and described in Table 12-638.

Return to Summary Table.

LOCK register - LOCKKEY1 component

Table 12-637. PLL24_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0069 8014h

Figure 12-318. PLL24_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-638. PLL24_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition24 registers

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12.319 PLL24_PLL_CTRL Register (Offset = 00018020h) [reset = X]

PLL24_PLL_CTRL is shown in Figure 12-319 and described in Table 12-640.

Return to Summary Table.

PLL_CTRL register for pll24

Table 12-639. PLL24_PLL_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 8020h

Figure 12-319. PLL24_PLL_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED							INTL_BYP_EN
R/W-X							R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			PD_EN	RESERVED			VCO_SEL
R/W-X			R/W-1h	R/W-X			R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-640. PLL24_PLL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL clock outputs 1'b1 - Synchronously select the reference clock for all PLL cock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-5	RESERVED	R/W	X	
4	PD_EN	R/W	1h	Power down. When set to 1, deskew PLL is powered down
3-1	RESERVED	R/W	X	

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Table 12-640. PLL24_PLL_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	VCO_SEL	R/W	1h	Select clock source for post divider 1'b0 - Use VCOCLK /2 **NOTE: VCO_SEL bit does not affect FOUT1X output used in this family of devices.**

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12.320 PLL24_DSPLL_STAT Register (Offset = 00018024h) [reset = X]

PLL24_DSPLL_STAT is shown in Figure 12-320 and described in Table 12-642.

Return to Summary Table.

DSPLL_STAT register for pll24

Table 12-641. PLL24_DSPLL_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 8024h

Figure 12-320. PLL24_DSPLL_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-642. PLL24_DSPLL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.321 PLL24_PLL_DIV_CTRL Register (Offset = 00018038h) [reset = X]

PLL24_PLL_DIV_CTRL is shown in Figure 12-321 and described in Table 12-644.

Return to Summary Table.

PLL_DIV_CTRL register for pll24

Table 12-643. PLL24_PLL_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 8038h

Figure 12-321. PLL24_PLL_DIV_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED		FB_DIV		RESERVED	POST_DIV		
R/W-X		R/W-2h		R/W-X	R/W-0h		
7	6	5	4	3	2	1	0
RESERVED						REF_DIV	
R/W-X						R/W-2h	

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-644. PLL24_PLL_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-14	RESERVED	R/W	X	
13-12	FB_DIV	R/W	2h	Feedback divide value: 2'b00 – Divide by 4 2'b01 – Divide by 2 2'b10 – Divide by 1 2'b11 – Divide by 1
11	RESERVED	R/W	X	
10-8	POST_DIV	R/W	0h	Post divide value: 3'b000 – Divided by 1 3'b001 – Divided by 2 3'b010 – Divided by 4 3'b011– Divided by 8 3'b100 – Divided by 16 3'b101 – Divided by 32 3'b110 – Divided by 64 3'b111 – Divided by 128
7-2	RESERVED	R/W	X	
1-0	REF_DIV	R/W	2h	Reference divide value: 2'b00 – Divide by 4 2'b01 – Divide by 2 2'b10 – Divide by 1 2'b11 – Divide by 1

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12.322 PLL24_PLL_TEST_CTRL Register (Offset = 00018050h) [reset = X]

PLL24_PLL_TEST_CTRL is shown in Figure 12-322 and described in Table 12-646.

Return to Summary Table.

PLL_TEST_CTRL register for pll24

Table 12-645. PLL24_PLL_TEST_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 8050h

Figure 12-322. PLL24_PLL_TEST_CTRL Register

31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
TEST_EN	RESERVED		PD_CAL	RESERVED			TEST_SEL
R/W-0h	R/W-X		R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-646. PLL24_PLL_TEST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R/W	X	
7	TEST_EN	R/W	0h	Enable test mux output 1'b0 - TESTOUT is held low 1'b1 - TESTOUT is CKFB or FREF based on test_sel bit
6-5	RESERVED	R/W	X	
4	PD_CAL	R/W	0h	Skew calibration power down. This bit is for test purposes only. 1'b0 - Skew calibration is not powered down 1'b1 - Skew calibration is powered down
3-1	RESERVED	R/W	X	
0	TEST_SEL	R/W	0h	Selects TESTOUT clock source 1'b0 - CKFB 1'b1 - FREF

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12.323 PLL24_DSCAL_CTRL Register (Offset = 00018060h) [reset = X]

PLL24_DSCAL_CTRL is shown in Figure 12-323 and described in Table 12-648.

Return to Summary Table.

DSCAL_CTRL register for pll24

Table 12-647. PLL24_DSCAL_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 8060h

Figure 12-323. PLL24_DSCAL_CTRL Register

31	30	29	28	27	26	25	24
CAL_EN	RESERVED			SPO_CAL_EN	RESERVED		
R/W-0h	R/W-X			R/W-0h	R/W-X		
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED			FAST_CAL	RESERVED	CAL_CNT		
R/W-X			R/W-0h	R/W-X	R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CAL_BYP	RESERVED			CAL_IN			
R/W-0h	R/W-X			R/W-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAL_IN							
R/W-0h							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-648. PLL24_DSCAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_EN	R/W	0h	Calibration enable to actively adjust for input skew 1'b0 - Disabled. Static phase offset determined by analog matching only 1'b1 - Enabled. Static phase offset adjusted by phase sensing at input
30-28	RESERVED	R/W	X	
27	SPO_CAL_EN	R/W	0h	Enable the SPO_CAL_CLKOUT when set
26-21	RESERVED	R/W	X	
20	FAST_CAL	R/W	0h	Fast calibration enabled 1'b0 - Normal operation 1'b1 - Used for initial calibration if initial value is not already known
19	RESERVED	R/W	X	
18-16	CAL_CNT	R/W	2h	Calibration loop programmable counter. Selects the number of PFD edges to wait after each calibration step defined by 2**cal_cnt
15	CAL_BYP	R/W	0h	Calibration bypass 1'b0 - Use the calibration output to set the phase correction 1'b1 - Use the cal_in input value to set the phase correction
14-12	RESERVED	R/W	X	
11-0	CAL_IN	R/W	0h	Calibration input When cal_byp is 1'b0, this represents the initial condition for calibration. When cal_byp is 1'b1, this is the override value for calibration. Value is a signed integer with positive values delaying the faster path reset and negative values delaying the slower path reset.

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12.324 PLL24_DSCAL_STAT Register (Offset = 00018064h) [reset = X]

PLL24_DSCAL_STAT is shown in Figure 12-324 and described in Table 12-650.

Return to Summary Table.

DSCAL_STAT register for pll24

Table 12-649. PLL24_DSCAL_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 8064h

Figure 12-324. PLL24_DSCAL_STAT Register

31	30	29	28	27	26	25	24
CAL_LOCK	RESERVED						
R-0h	R-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED				LOCK_CNT			
R-X				R-0h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESERVED				CAL_OUT			
R-X				R-0h			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CAL_OUT							
R-0h							

LEGEND: R = Read Only; *-n* = value after reset

Table 12-650. PLL24_DSCAL_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CAL_LOCK	R	0h	Reserved for future use
30-20	RESERVED	R	X	
19-16	LOCK_CNT	R	0h	Reserved for future use
15-12	RESERVED	R	X	
11-0	CAL_OUT	R	0h	Output of the calibration block if cal_byp = 1'b0. If cal_byp = 1'b1 it is a buffer version of cal_in [11:0]. Can be used to read the phase calibration state to for later use as an override value to bypass skew calibration.

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12.325 PLL24_HSDIV_CTRL0 Register (Offset = 00018080h) [reset = X]

PLL24_HSDIV_CTRL0 is shown in Figure 12-325 and described in Table 12-652.

Return to Summary Table.

HSDIV_CTRL0 register for pll24

Table 12-651. PLL24_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 8080h

Figure 12-325. PLL24_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-652. PLL24_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.326 PLL25_PID Register (Offset = 00019000h) [reset = 61801001h]

PLL25_PID is shown in Figure 12-326 and described in Table 12-654.

Return to Summary Table.

Peripheral Identification Register

Table 12-653. PLL25_PID Instances

Instance	Physical Address
PLL0_CFG	0069 9000h

Figure 12-326. PLL25_PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		MODULE											
R-1h		R-2h		R-180h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISC					MAJOR			CUSTOM		MINOR					
R-2h					R-0h			R-0h		R-1h					

LEGEND: R = Read Only; *-n* = value after reset

Table 12-654. PLL25_PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID follows new scheme
29-28	BU	R	2h	Business Unit - Processors
27-16	MODULE	R	180h	Module functional identifier
15-11	MISC	R	2h	Misc revision number
10-8	MAJOR	R	0h	Major revision number
7-6	CUSTOM	R	0h	custom revision number
5-0	MINOR	R	1h	Minor revision number

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12.327 PLL25_CFG Register (Offset = 00019008h) [reset = X]

PLL25_CFG is shown in Figure 12-327 and described in Table 12-656.

Return to Summary Table.

PLL Configuration

Table 12-655. PLL25_CFG Instances

Instance	Physical Address
PLL0_CFG	0069 9008h

Figure 12-327. PLL25_CFG Register

31	30	29	28	27	26	25	24
HSDIV_PRSNT							
R-3h							
23	22	21	20	19	18	17	16
HSDIV_PRSNT							
R-3h							
15	14	13	12	11	10	9	8
RESERVED			SSM_TYPE		RESERVED		SSM_WVTBL
R-X			R-1h		R-X		R/W-0h
7	6	5	4	3	2	1	0
RESERVED						PLL_TYPE	
R-X						R-0h	

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-656. PLL25_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	HSDIV_PRSNT	R	3h	High Speed Divider Presence Each bit Indicates the presence of High Speed dividers 0-15. By definition HSDIV [4:0] are connected the PLL FOUTVCO output clock and HSDIV [15:5] are connected to the PLL FOUTPOSTDIV output clock
15-13	RESERVED	R	X	
12-11	SSM_TYPE	R	1h	Spread spectrum module presence Field values (Others are reserved): 2'b00 - SSM is not present 2'b01 - SSM is present 2'b10 - Reserved 2'b11 - Reserved
10-9	RESERVED	R	X	
8	SSM_WVTBL	R/W	0h	Spread spectrum wave table presence 1'b0 - SSM Wave table is not present 1'b1 - SSM Wave table is present
7-2	RESERVED	R	X	
1-0	PLL_TYPE	R	0h	Indicates PLL type Field values (Others are reserved): 2'b00 - Fractional PLL 2'b01 - FractionalF PLL 2'b10 - De-Skew PLL

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12.328 PLL25_LOCKKEY0 Register (Offset = 00019010h) [reset = 0h]

PLL25_LOCKKEY0 is shown in Figure 12-328 and described in Table 12-658.

Return to Summary Table.

PLL25_LOCKKEY0 - PLL25 Lock Key 0 Register

Table 12-657. PLL25_LOCKKEY0 Instances

Instance	Physical Address
PLL0_CFG	0069 9010h

Figure 12-328. PLL25_LOCKKEY0 Register

31	30	29	28	27	26	25	24
KEY							
R/W-0h							
23	22	21	20	19	18	17	16
KEY							
R/W-0h							
15	14	13	12	11	10	9	8
KEY							
R/W-0h							
7	6	5	4	3	2	1	0
KEY							UNLOCKED
R/W-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 12-658. PLL25_LOCKKEY0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	KEY	R/W	0h	Write the kick0 unlock value followed by the kick1 unlock value to unlock the write-protected Partition25 registers
0	UNLOCKED	R	0h	Unlock status. When set, indicates that the proper unlock sequence has been performed and the partition is unlocked for writing.

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12.329 PLL25_LOCKKEY1 Register (Offset = 00019014h) [reset = 0h]

PLL25_LOCKKEY1 is shown in Figure 12-329 and described in Table 12-660.

Return to Summary Table.

PLL25_LOCKKEY1 - PLL25 Lock Key 1 RegisterAddr

Table 12-659. PLL25_LOCKKEY1 Instances

Instance	Physical Address
PLL0_CFG	0069 9014h

Figure 12-329. PLL25_LOCKKEY1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKKEY1_VAL																															
R/W-0h																															

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-660. PLL25_LOCKKEY1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	LOCKKEY1_VAL	R/W	0h	Write the kick1 unlock value after the kick0 unlock value to unlock the write-protected Partition25 registers

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12.330 PLL25_CTRL Register (Offset = 00019020h) [reset = X]

PLL25_CTRL is shown in Figure 12-330 and described in Table 12-662.

Return to Summary Table.

PLL25_CTRL - PLL25 Control

Table 12-661. PLL25_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 9020h

Figure 12-330. PLL25_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED						
R/W-1h	R/W-X						
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESERVED							BYP_ON_LOCKLOSS
R/W-X							R/W-1h
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLL_EN	RESERVED						INTL_BYP_EN
R/W-0h	R/W-X						R/W-0h
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		CLK_4PH_EN	CLK_POSTDIV_EN	RESERVED		DSM_EN	DAC_EN
R/W-X		R/W-0h	R/W-1h	R/W-X		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-662. PLL25_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass enable. This controls the glitch-free bypass mux. The BYPASS_EN bit should be set prior to making any changes to the PLL settings. 1'b0 - Synchronously select PLL and associated HSDIV clock outputs 1'b1 - Synchronously select the reference clock for all PLL and HSDIV clock outputs
30-17	RESERVED	R/W	X	
16	BYP_ON_LOCKLOSS	R/W	1h	Bypass on loss of PLL lock. This bit controls the PLL bypass mux to automatically switch the clock source to the reference clock when the PLL losses lock. 1'b0 - Do not automatically switch to ref clock source on PLL lock loss 1'b1 - Switch to ref clock source when PLL losses lock
15	PLL_EN	R/W	0h	PLL enable 1'b0 - PLL is disabled 1'b1 - PLL is enabled
14-9	RESERVED	R/W	X	
8	INTL_BYP_EN	R/W	0h	PLL internal bypass enable. This is an asynchronous mux which can produce glitches on the output clocks during switching. NOTE: Always program this bit field to 0. 1'b0 - Output clocks are derived from the VCO clock 1'b1 - Output clocks are derived from the FREF reference clock
7-6	RESERVED	R/W	X	

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Table 12-662. PLL25_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	CLK_4PH_EN	R/W	0h	Enable 4-phase clock generator. NOTE: Always program this bit to 0. This bit is ignored if CLK_POSTDIV_EN = 0 1'b0 - 4-phase dividers disabled. FOUT1PHx and FOUTn clocks are held low. 1'b1 - 4-phase dividers enabled. FOUT1PH0/90/180/270 and FOUT2, FOUT3, FOUT4 clocks are enabled.
4	CLK_POSTDIV_EN	R/W	1h	Post divide CLK enable 1'b0 - Post divide powered down. FOUTPOSTDIV and all auxiliary PLL clocks (4-ohase and synchronous divided clocks) are held low 1'b1 - Post divide enabled. FOUTPOSTDIV, 4-phase and synchronous clocks are enabled.
3-2	RESERVED	R/W	X	
1	DSM_EN	R/W	0h	Delta-Sigma modulator enable 1'b0 - Delta-Sigma modulator is disabled 1'b1 - Delta-Sigma modulator is enabled
0	DAC_EN	R/W	1h	Enable fractional noise canceling DAC This bit has no function when DSM_EN = 0 1'b0 - Fractional NC DAC is disabled 1'b1 - Fractional NC DAC is enabled

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12.331 PLL25_STAT Register (Offset = 00019024h) [reset = X]

PLL25_STAT is shown in Figure 12-331 and described in Table 12-664.

Return to Summary Table.

PLL25_STAT - PLL25 Status

Table 12-663. PLL25_STAT Instances

Instance	Physical Address
PLL0_CFG	0069 9024h

Figure 12-331. PLL25_STAT Register

31	30	29	28	27	26	25	24
RESERVED							
R-X							
23	22	21	20	19	18	17	16
RESERVED							
R-X							
15	14	13	12	11	10	9	8
RESERVED							
R-X							
7	6	5	4	3	2	1	0
RESERVED							LOCK
R-X							R-0h

LEGEND: R = Read Only; *-n* = value after reset

Table 12-664. PLL25_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-1	RESERVED	R	X	
0	LOCK	R	0h	PLL lock status. Software should wait for lock to be asserted before clearing the PLL_CTRL[31] BYPASS_EN bit 1'b0 - PLL is not locked 1'b1 - PLL is locked

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12.332 PLL25_FREQ_CTRL0 Register (Offset = 00019030h) [reset = X]

PLL25_FREQ_CTRL0 is shown in Figure 12-332 and described in Table 12-666.

Return to Summary Table.

PLL0_FREQ_CTRL0 - PLL25 Frequency Control 25 Register

Table 12-665. PLL25_FREQ_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 9030h

Figure 12-332. PLL25_FREQ_CTRL0 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																				FB_DIV_INT											
R/W-X																				R/W-10h											

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 12-666. PLL25_FREQ_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-12	RESERVED	R/W	X	
11-0	FB_DIV_INT	R/W	10h	PLL multiplier (integer portion) In Integer mode values of 16 - 3200 (dec) are supported. In Fractional mode values of 20 to 320 are supported. 12'h000 - 12'h00F - Not supported 12'h010 - Divide by 16 12'h011 - Divide by 17 ... 12'h140 - Divide by 320 ... 12'hC80 - Divide by 3200 12'hC81 - 12'hFFF - Not supported

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12.333 PLL25_FREQ_CTRL1 Register (Offset = 00019034h) [reset = X]

PLL25_FREQ_CTRL1 is shown in Figure 12-333 and described in Table 12-668.

Return to Summary Table.

PLL25_FREQ_CTRL1 - PLL0 Frequency Control 1 Register

Table 12-667. PLL25_FREQ_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 9034h

Figure 12-333. PLL25_FREQ_CTRL1 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FB_DIV_FRAC																							
R/W-X								R/W-0h																							

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-668. PLL25_FREQ_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R/W	X	
23-0	FB_DIV_FRAC	R/W	0h	PLL multiplier (fractional portion). Supports values of 0 to 0.999999940395. The total feedback divide value is (FB_DIV_INT + FB_DIV_FRAC / (2^{24})) 24'h000000 - 0 24'h000001 - .000000059605 (1/(2^{24})) 24'h000002 - .000000119209 (2/(2^{24})) ... 24'h800000 - .500000000000 ... 24'hFFFFFF - .999999940395 (1677215/(2^{24}))

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12.334 PLL25_DIV_CTRL Register (Offset = 00019038h) [reset = X]

PLL25_DIV_CTRL is shown in Figure 12-334 and described in Table 12-670.

Return to Summary Table.

PLL25_DIV_CTRL - PLL25 Output Clock Divider Register

Table 12-669. PLL25_DIV_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 9038h

Figure 12-334. PLL25_DIV_CTRL Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED					POST_DIV2			RESERVED					POST_DIV1		
R/W-X					R/W-1h			R/W-X					R/W-2h		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED										REF_DIV					
R/W-X										R/W-1h					

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-670. PLL25_DIV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	X	
26-24	POST_DIV2	R/W	1h	Secondary post divider. Supports values of 1-7.
23-19	RESERVED	R/W	X	
18-16	POST_DIV1	R/W	2h	Primary post divider. To ensure correct operation, POST_DIV1 must always be programmed to a value equal to or greater that POST_DIV2. Supports values of Supports values of 1-7 (Others are reserved): 3'b000 - Reserved 3'b001 - Divide by 1 3'b010 - Divide by 2 3'b011 - Divide by 3 3'b100 - Divide by 4 3'b101 - Divide by 5 3'b110 - Divide by 6 3'b111 - Divide by 7
15-6	RESERVED	R/W	X	
5-0	REF_DIV	R/W	1h	Reference clock pre-divider. Supports values of 1-63 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63

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12.335 PLL25_SS_CTRL Register (Offset = 00019040h) [reset = X]

PLL25_SS_CTRL is shown in Figure 12-335 and described in Table 12-672.

Return to Summary Table.

PLL_SS_CTRL register for pll25

Table 12-671. PLL25_SS_CTRL Instances

Instance	Physical Address
PLL0_CFG	0069 9040h

Figure 12-335. PLL25_SS_CTRL Register

31	30	29	28	27	26	25	24
BYPASS_EN	RESERVED					WV_TBLE_MAXADDR	
R/W-1h	R/W-X					R/W-0h	
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
WV_TBLE_MAXADDR						RESERVED	
R/W-0h						R/W-X	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RESET	RESERVED						
R/W-0h	R/W-X						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			DOWNSPREAD_EN	RESERVED			WAVE_SEL
R/W-X			R/W-0h	R/W-X			R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-672. PLL25_SS_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31	BYPASS_EN	R/W	1h	Bypass the SS modulator. 1'b0 - Spread spectrum modulation is enabled 1'b1 - SSMOD is bypassed. No modulation of PLL frequency
30-26	RESERVED	R/W	X	
25-18	WV_TBLE_MAXADDR	R/W	0h	Wave table max address. Indicates the maximum number of address bits used to access the external wave table. These bits are not used if PLLn_CFG[8] SSM_WVTBL = 0
17-16	RESERVED	R/W	X	
15	RESET	R/W	0h	HSDIV reset. When set to 1 the SSM modulator is in reset
14-5	RESERVED	R/W	X	
4	DOWNSPREAD_EN	R/W	0h	Selects center spread or down spread clock variance 1'b0 - Center spread 1'b1 - Down spread
3-1	RESERVED	R/W	X	
0	WAVE_SEL	R/W	0h	Wave pattern select External wave table should only be selected if PLLn_CFG[8] SSM_WVTBL = 1 Field values (Others are reserved): 1'b0 - Use 128 point triangle wave table 1'b1 - Use external wave table

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12.336 PLL25_SS_SPREAD Register (Offset = 00019044h) [reset = X]

PLL25_SS_SPREAD is shown in Figure 12-336 and described in Table 12-674.

Return to Summary Table.

PLL_SS_SPREAD register for pll25

Table 12-673. PLL25_SS_SPREAD Instances

Instance	Physical Address
PLL0_CFG	0069 9044h

Figure 12-336. PLL25_SS_SPREAD Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED												MOD_DIV			
R/W-X												R/W-1h			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED											SPREAD				
R/W-X											R/W-1h				

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-674. PLL25_SS_SPREAD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-20	RESERVED	R/W	X	
19-16	MOD_DIV	R/W	1h	Input clock divider. This divider sets the modulation frequency. Supports divide values of 1-63: 6'b000000 - Reserved 6'b000001 - Divide by 1 6'b000010 - Divide by 2 ... 6'b111111 - Divide by 63
15-5	RESERVED	R/W	X	
4-0	SPREAD	R/W	1h	Sets the spread modulation depth. The depth is spread*0.1% 5'b00000 - Reserved (don't use) 5'b00001 - 0.1% 5'b00010 - 0.2% ... 5'b10000 - 1.6% ... 5'b11111 - 3.1%

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12.337 PLL25_HSDIV_CTRL0 Register (Offset = 00019080h) [reset = X]

PLL25_HSDIV_CTRL0 is shown in Figure 12-337 and described in Table 12-676.

Return to Summary Table.

HSDIV_CTRL0 register for pll25

Table 12-675. PLL25_HSDIV_CTRL0 Instances

Instance	Physical Address
PLL0_CFG	0069 9080h

Figure 12-337. PLL25_HSDIV_CTRL0 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-676. PLL25_HSDIV_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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12.338 PLL25_HSDIV_CTRL1 Register (Offset = 00019084h) [reset = X]

PLL25_HSDIV_CTRL1 is shown in Figure 12-338 and described in Table 12-678.

Return to Summary Table.

HSDIV_CTRL1 register for pll25

Table 12-677. PLL25_HSDIV_CTRL1 Instances

Instance	Physical Address
PLL0_CFG	0069 9084h

Figure 12-338. PLL25_HSDIV_CTRL1 Register

31	30	29	28	27	26	25	24
RESET	RESERVED						
R/W-0h	R/W-X						
23	22	21	20	19	18	17	16
RESERVED							
R/W-X							
15	14	13	12	11	10	9	8
CLKOUT_EN	RESERVED						SYNC_DIS
R/W-0h	R/W-X						R/W-0h
7	6	5	4	3	2	1	0
RESERVED	HSDIV						
R/W-X	R/W-0h						

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 12-678. PLL25_HSDIV_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESET	R/W	0h	HSDIV reset. When set to 1 HSDIV is in reset
30-16	RESERVED	R/W	X	
15	CLKOUT_EN	R/W	0h	CLKOUT1 enable 1'b0 - Synchronously disable CLKOUT1 1'b1 - Synchronously enable CLKOUT1
14-9	RESERVED	R/W	X	
8	SYNC_DIS	R/W	0h	Disable divider synchronization logic 1'b0 - Changes to DIV value synchronized to prevent glitches 1'b1 - Changes are asynchronous
7	RESERVED	R/W	X	
6-0	HSDIV	R/W	0h	CLKOUT0 divider value (HSDIV1+1) Allowed values are 0-127

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13 PLLCTRL Registers

Table 13-2 lists the memory-mapped registers for the PLLCTRL registers. All register offset addresses not listed in Table 13-2 should be considered as reserved locations and the register contents should not be modified.

Table 13-1. PLLCTRL Instances

Instance	Base Address
PLLCTRL0	0041 0000h
WKUP_PLLCTRL0	4201 0000h

Table 13-2. PLLCTRL Registers

Offset	Acronym	Register Name	PLLCTRL0 Physical Address	WKUP_PLLCTRL0 Physical Address
0h	PID	PID register	0041 0000h	4201 0000h
100h	PLLCTL	PLL control register	0041 0100h	4201 0100h
118h	PLLDIV1	PLL controller divider1 control register	0041 0118h	4201 0118h
11Ch	PLLDIV2	PLL controller divider2 control register	0041 011Ch	4201 011Ch
138h	PLLCMD	PLL Controller command register	0041 0138h	4201 0138h
13Ch	PLLSTAT	PLL Controller status register	0041 013Ch	4201 013Ch
140h	ALNCTL	PLL Controller clock align control register	0041 0140h	4201 0140h
144h	DCHANGE	PLLDIV ratio change register	0041 0144h	4201 0144h

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13.1 PID Register (Offset = 0h) [reset = 44815C00h]

PID is shown in Figure 13-1 and described in Table 13-4.

Return to Summary Table.

PID register

Table 13-3. PID Instances

Instance	Physical Address
PLLCTRL0	0041 0000h
WKUP_PLLCTRL0	4201 0000h

Figure 13-1. PID Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCHEME		BU		FUNC											
R-1h		R-0h		R-481h											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTL					MAJOR			CUSTOM		MINOR					
R-Bh					R-4h			R-0h		R-0h					

LEGEND: R = Read Only; *-n* = value after reset

Table 13-4. PID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	SCHEME	R	1h	PID register scheme
29-28	BU	R	0h	Business Unit
27-16	FUNC	R	481h	Module ID
15-11	RTL	R	Bh	RTL revision. Will vary depending on release
10-8	MAJOR	R	4h	Major revision
7-6	CUSTOM	R	0h	Custom
5-0	MINOR	R	0h	Minor revision

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13.2 PLLCTL Register (Offset = 100h) [reset = X]

PLLCTL is shown in Figure 13-2 and described in Table 13-6.

Return to Summary Table.

PLL control register

Table 13-5. PLLCTL Instances

Instance	Physical Address
PLLCTRL0	0041 0100h
WKUP_PLLCTRL0	4201 0100h

Figure 13-2. PLLCTL Register

31	30	29	28	27	26	25	24
RSVD2							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD2							
R/W-0h							
15	14	13	12	11	10	9	8
RSVD2						EXCLKSRC	CLKMODE
R/W-0h						R/W-0h	R/W-X
7	6	5	4	3	2	1	0
PLLSELB	RSVD1	PLLENSRC	PLLDIS	PLLRST	RSVD	PLLPWRDN	PLLEN
R/W-0h	R/W-0h	R/W-1h	R/W-X	R/W-X	R/W-0h	R/W-1h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 13-6. PLLCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-10	RSVD2	R/W	0h	Reserved
9	EXCLKSRC	R/W	0h	Selects between using bypass clock or an external clock source. 0=bypass clock 1=external clock source
8	CLKMODE	R/W	X	Reference Clock Selection. 1 = CLKIN_PI is the reference clock 0 = OSCIN_PI is the reference clock This bit is only applicable when D_CLKMODESRC_PI = 1. It is otherwise don't care.
7	PLLSELB	R/W	0h	Selects PLL A versus PLL B. 1 = PLL B is selected. PLL A is put in power down (PLL_A_PWRDN_PO = 1) 0 = PLL A is selected. PLL B is put in power down. (PLL_B_PWRDN_PO = 1)
6	RSVD1	R/W	0h	Reserved
5	PLLENSRC	R/W	1h	PLLEN Mux Control Source 1 = PLLEN Mux is controlled by input PLLEN_PI. PLLCTL[0] PLLEN is don't care 0 = PLLEN Mux is controlled by PLLCTL[0] PLLEN. pllen_pi is don't care

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Table 13-6. PLLCTL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	PLLDIS	R/W	X	Asserts DISABLE to PLL if Supported 1 = PLL Controller output PLL_DISABLE_PO = 1. 0 = PLL Controller output PLL_DISABLE_PO = 0. Chip team must pay attention to the disable signal polarity of the PLL they use. Some PLLs may require PLLDIS=1 to disable PLL, some PLLs require PLLDIS=0 to disable PLL. Note that PLL Controller only supports one PLL_DISABLE_PO output for both PLLA and PLLB. This is possible because the non-selected PLL is already placed in power down mode.
3	PLLRST	R/W	X	Asserts RESET to PLL if Supported. Controls output PLL_RESET_PO. 1= PLL Controller output PLL_RESET_PO = 1. 0= PLL Controller output PLL_RESET_PO=0. Chip team must pay attention to the reset signal polarity of the PLL they use. Some PLLs require PLLRST=1 to reset the PLL. Some PLLs require PLLRST=0 to reset the PLL. Note that PLL Controller only supports one pll_reset_po output for both PLLA and PLLB. This is possible because the non-selected PLL is already placed in power down mode.
2	RSVD	R/W	0h	Reserved
1	PLLPWRDN	R/W	1h	Selects PLL Power Down for the PLL selected by PLLSELB. The PLL not selected by PLLSELB is NOT controlled by PLLPWRDN bit. The not-selected PLL will stay in power down regardless of PLLPWRDN value. 0 = Selected PLL Operational. If PLLSELB=0 (PLLA selected), PLL controller output pll_a_pwrdn_po is deasserted low. If PLLSELB=1 (PLLB selected), PLL controller output pll_b_pwrdn_po is deasserted low. 1 = Selected PLL Placed In Power Down State. If PLLSELB=0 (PLLA selected), PLL controller outputs pll_a_pwrdn_po is asserted high. If PLLSELB=1 (PLLB selected), pll_b_pwrdn_po is asserted
0	PLLEN	R/W	0h	PLL Mode Enable This bit controls the multiplexer before the SYSCLK dividers D1 to Dn. 0 = Bypass Mode PreDiv, PLL, and PostDiv are bypassed. SYSCLK divided down directly from input reference clock refclk. 1 = PLL Mode PLL is used. SYSCLK divided down from PostDiv output

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13.3 PLLDIV1 Register (Offset = 118h) [reset = X]

PLLDIV1 is shown in Figure 13-3 and described in Table 13-8.

Return to Summary Table.

PLL controller divider1 control register

Table 13-7. PLLDIV1 Instances

Instance	Physical Address
PLLCTRL0	0041 0118h
WKUP_PLLCTRL0	4201 0118h

Figure 13-3. PLLDIV1 Register

31	30	29	28	27	26	25	24
RSVD1							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD1							
R/W-0h							
15	14	13	12	11	10	9	8
DN_EN	HALF_RATIO	RSVD					
R-X	R/W-0h	R/W-0h					
7	6	5	4	3	2	1	0
RATIO							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 13-8. PLLDIV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD1	R/W	0h	Reserved
15	DN	R	1h	Divider Dn Enable 0 = Divider n Disabled. SYSCLKn is also gated before and after divider Dn. 1 = Divider n Enabled

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Table 13-8. PLLDIV1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	HALF_RATIO	R/W	0h	Ratio is in half steps. For example 1: if RATIO = 00000 and HALFRATIO=1 the divider will be /1.5. Example 2: RATIO=10111 and HALFRATIO=1 divider will be /24.5. example 3: if RATIO=00011 and HALFRATIO=0 divider will be /4. THE HALF RATIO DIVIDER IS NOT A 50% DUTY CYCLE. It is a single 1x high clock pulse followed by low time until ratio is met. * To enable half step ratio dividers you must also set the associated bit in the PLLHDIVEN register PRIOR to writing the PLLDIVn register. If PLLHDIVEN register is not enabled then HALF_RATIO will not be writable. Changing the PLLHDIVEN register, set or clear, will not set or clear the HALF_RATIO bit in PLLDIVn register. This is to protect and enable backward compatible software in the chance it accidently wrote this bit field.
13-8	RSVD	R/W	0h	Reserved

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Table 13-8. PLLDIV1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	RATIO	R/W	X	Divider Dn Ratio (SYSCLKn divider) 00000=/1 00001=/2 00010=/3 00011=/4 00100=/5 00101=/6 00110=/7 00111=/8 01000=/9 01001=/10 01010=/11 01011=/12 01100=/13 01101=/14 01110=/15 01111=/16 10000=/17 10001=/18 10010=/19 10011=/20 10100=/21 10101=/22 10110=/23 10111=/24 11000=/25 11001=/26 11010=/27 11011=/28 11100=/29 11101=/30 11110=/31 11111=/32 Note that the actual PLLDIVx divide ratio will not be modified when this field is written to. User must also set the GOSET bit so that the SYSCLKs selected in ALNCTL can change their RATIOs to the new values and remain phase-aligned. Note: see HALF_RATIO bit.

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13.4 PLLDIV2 Register (Offset = 11Ch) [reset = X]

PLLDIV2 is shown in Figure 13-4 and described in Table 13-10.

Return to Summary Table.

PLL controller divider2 control register

Table 13-9. PLLDIV2 Instances

Instance	Physical Address
PLLCTRL0	0041 011Ch
WKUP_PLLCTRL0	4201 011Ch

Figure 13-4. PLLDIV2 Register

31	30	29	28	27	26	25	24
RSVD1							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD1							
R/W-0h							
15	14	13	12	11	10	9	8
DN_EN	HALF_RATIO	RSVD					
R-X	R/W-0h	R/W-0h					
7	6	5	4	3	2	1	0
RATIO							
R/W-X							

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 13-10. PLLDIV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD1	R/W	0h	Reserved
15	DN	R	1h	Divider Dn Enable 0 = Divider n Disabled. SYSCLKn is also gated before and after divider Dn. 1 = Divider n Enabled

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Table 13-10. PLLDIV2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	HALF_RATIO	R/W	0h	Ratio is in half steps. For example 1: if RATIO = 00000 and HALFRATIO=1 the divider will be /1.5. Example 2: RATIO=10111 and HALFRATIO=1 divider will be /24.5. example 3: if RATIO=00011 and HALFRATIO=0 divider will be /4. THE HALF RATIO DIVIDER IS NOT A 50% DUTY CYCLE. It is a single 1x high clock pulse followed by low time until ratio is met. * To enable half step ratio dividers you must also set the associated bit in the PLLHDIVEN register PRIOR to writing the PLLDIVn register. If PLLHDIVEN register is not enabled then HALF_RATIO will not be writable. Changing the PLLHDIVEN register, set or clear, will not set or clear the HALF_RATIO bit in PLLDIVn register. This is to protect and enable backward compatible software in the chance it accidently wrote this bit field.
13-8	RSVD	R/W	0h	Reserved

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Table 13-10. PLLDIV2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-0	RATIO	R/W	X	Divider Dn Ratio (SYSCLKn divider) 00000=/1 00001=/2 00010=/3 00011=/4 00100=/5 00101=/6 00110=/7 00111=/8 01000=/9 01001=/10 01010=/11 01011=/12 01100=/13 01101=/14 01110=/15 01111=/16 10000=/17 10001=/18 10010=/19 10011=/20 10100=/21 10101=/22 10110=/23 10111=/24 11000=/25 11001=/26 11010=/27 11011=/28 11100=/29 11101=/30 11110=/31 11111=/32 Note that the actual PLLDIVx divide ratio will not be modified when this field is written to. User must also set the GOSET bit so that the SYSCLKs selected in ALNCTL can change their RATIOs to the new values and remain phase-aligned. Note: see HALF_RATIO bit.

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13.5 PLLCMD Register (Offset = 138h) [reset = 0h]

PLLCMD is shown in Figure 13-5 and described in Table 13-12.

Return to Summary Table.

PLL Controller command register

Table 13-11. PLLCMD Instances

Instance	Physical Address
PLLCTRL0	0041 0138h
WKUP_PLLCTRL0	4201 0138h

Figure 13-5. PLLCMD Register

31	30	29	28	27	26	25	24
RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
RSVD							
R/W-0h							
7	6	5	4	3	2	1	0
RSVD						OSCPWRDN	GOSET
R/W-0h						R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 13-12. PLLCMD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-2	RSVD	R/W	0h	Reserved
1	OSCPWRDN	R/W	0h	iOscillator Power Down Command 1: A write of 1 (doesn't need to be a transition from 0 to 1) to this bit initiates oscillator power down command. 0: A write of 0 to this bit clears the bit to zero but causes no effect. Read from this field returns the value previously written. Once written a 1, the bit remains a 1 unless if user writes a 0 to it. Do not read this bit for status of oscillator power down. In the case when CLKMODE = 1 (CLKIN mode), write to OSCPWRDN bit still occurs, but no oscillator power down command is actually sent because osc is already in power down. Read from this bit returns the value written.

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Table 13-12. PLLCMD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GOSET	R/W	0h	GO bit for SYSCLKx phase alignment. GOSET = 1: A write of 1 to this bit signifies that the new divide ratios in PLLDIV [1:n] are taken into account at the nearest possible rising edge to phase align the clocks. The actual SYSCLKx to be aligned are selected in register ALNCTL. When divide-ratio change and clock alignment are completed, GOSET remains 1. Subsequent write of 1 to this register (even though the field was already a 1) causes the command for divide-ratio change and clock alignment. GOSET = 0: A write of 0 to this bit clears the bit to zero but causes no effect. Read from this field returns the value previously written. When writing consecutively to this field, the user must poll the GOSTAT between accesses to see if previous command for clock alignment and divide-ratio change has completed. Otherwise operation is undefined. Do not read GOSET in this command register for status.

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13.6 PLLSTAT Register (Offset = 13Ch) [reset = X]

PLLSTAT is shown in Figure 13-6 and described in Table 13-14.

Return to Summary Table.

PLL Controller status register

Table 13-13. PLLSTAT Instances

Instance	Physical Address
PLLCTRL0	0041 013Ch
WKUP_PLLCTRL0	4201 013Ch

Figure 13-6. PLLSTAT Register

31	30	29	28	27	26	25	24
RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
RSVD							
R/W-0h							
7	6	5	4	3	2	1	0
RSVD					STABLE	LOCK	GOSTAT
R/W-0h					R-X	R-0h	R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 13-14. PLLSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-3	RSVD	R/W	0h	Reserved
2	STABLE	R	X	OSCIN Stable This bit shows the status of the rstclk_cnt_done_po signal. It indicates if the rstclk counter has finished counting, implying that the OSCIN/CLKIN is stable. The d_rstclk_cnt_pi must be set properly to allow rstclk counter to count sufficient amount of time for clock sources to become stable. 0 = rstclk counter not done counting, implying OSCIN/CLKIN input may not yet be stable. 1 = OSCIN/CLKIN is assumed to be stable. This bit is set to 1 if any one of the three cases is true: - rstclk counter has finished counting d_rstclk_cnt_pi number of rstclk cycles. - rstclk counter is paramterized out and does not exist, in which case OSCIN/CLKIN is assumed to be stable when por_pi_n is de-asserted.

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Table 13-14. PLLSTAT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	LOCK	R	0h	PLL Core STATUS This bit returns the lock status of the selected PLL core (if supported by PLL core). For example, if PLLSELB=0 (PLLA selected), it reflects the status of pll_a_lock_i. If PLLSELB-1 (PLLB selected), it reflects the status of pll_b_lock_i. 0 = PLL core not locked. The corresponding PLL Controller output pll_[x]_lock_out=0. (where [x] is a or b depending on PLLSELB). 1 = PLL core locked. The corresponding PLL Controller output pll_[x]_lock_out=1. (where [x] is a or b depending on PLLSELB). Note that not all PLL Core supports the lock signal. Check the PLL used to see if it has a functional lock output. Therefore this bit may not need to be documented to users.
0	GOSTAT	R	0h	Reflects the status of GO transition. Read from this register returns the status of the GO operation. Writes to the register are ignored. GOSTAT = 1: This bit goes to 1 as soon as GOSET in PLLCMD is written to. It remains a 1 when GO operation (divide-ratio change and clock alignment) is in progress. This bit automatically clears to 0 when GO operation is completed. GOSTAT = 0: No GO operation in progress. Software note: Users must not initiate another GOSET operation in PLLCMD until GOSTAT is cleared to 0.

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13.7 ALNCTL Register (Offset = 140h) [reset = 3h]

ALNCTL is shown in Figure 13-7 and described in Table 13-16.

Return to Summary Table.

PLL Controller clock align control register

Table 13-15. ALNCTL Instances

Instance	Physical Address
PLLCTRL0	0041 0140h
WKUP_PLLCTRL0	4201 0140h

Figure 13-7. ALNCTL Register

31	30	29	28	27	26	25	24
RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
ALN							
R/W-1h							
7	6	5	4	3	2	1	0
ALN							ALN1
R/W-1h							R/W-1h

LEGEND: R/W = Read/Write; *-n* = value after reset

Table 13-16. ALNCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD	R/W	0h	Reserved
15-1	ALN	R/W	1h	SYSCLKx needs to be aligned with other clocks selected in this register. ALNx = 0: Do not need to align SYSCLKx to other clocks. SYSCLKx is left free-running. ALNx = 1: Align SYSCLKx to other clocks selected in this register Software note: This bit should only be modified when GOSTAT is 0. Software note: In the case when a divider is disabled (DxEN=0) but the respective ALNx=1, GO operation should ignore ALNx=1. DxEN takes priority. Existence of ALN[8:3] are determined by RTL parameter SYSCLK. If the corresponding SYSCLK does not exist, the ALNx bit will be read-only and default to 0.
0	ALN1	R/W	1h	SYSCLK1 needs to be aligned with other clocks selected in this register. ALN1 = 0: Do not need to align SYSCLK1 to other clocks. SYSCLK1 is left free-running. ALN1 = 1: Align SYSCLK1 to other clocks selected in this register Software note: This bit should only be modified when GOSTAT is 0. Software note: in the case when a divider is disabled (D1EN=0) but ALN1=1, GO operation should ignore ALN1=1. D1EN takes priority.

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13.8 DCHANGE Register (Offset = 144h) [reset = 0h]

DCHANGE is shown in Figure 13-8 and described in Table 13-18.

Return to Summary Table.

PLLDIV ratio change register

Table 13-17. DCHANGE Instances

Instance	Physical Address
PLLCTRL0	0041 0144h
WKUP_PLLCTRL0	4201 0144h

Figure 13-8. DCHANGE Register

31	30	29	28	27	26	25	24
RSVD							
R/W-0h							
23	22	21	20	19	18	17	16
RSVD							
R/W-0h							
15	14	13	12	11	10	9	8
SYS							
R-0h							
7	6	5	4	3	2	1	0
SYS							SYS1
R-0h							R-0h

LEGEND: R = Read Only; R/W = Read/Write; *-n* = value after reset

Table 13-18. DCHANGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RSVD	R/W	0h	Reserved
15-1	SYS	R	0h	SYSCLKx divide ratio has been modified. SYSCLKx ratio will be changed during GO operation. SYSx = 0: SYSCLKx ratio has not been modified. When GOSET is set, SYSCLKx will not be affected. SYSx = 1: SYSCLKx ratio has been modified. When GOSET is set, SYSCLKx will change to the new ratio.
0	SYS1	R	0h	SYSCLK1 divide ratio has been modified. SYSCLK1 ratio will be changed during GO operation. SYS1 = 0: SYSCLK1 ratio has not been modified. When GOSET is set, SYSCLK1 will not be affected. SYS1 = 1: SYSCLK1 ratio has been modified. When GOSET is set, SYSCLK1 will change to the new ratio.

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