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Ray Simar of Texas Instruments

REVVING UP REAL TIME

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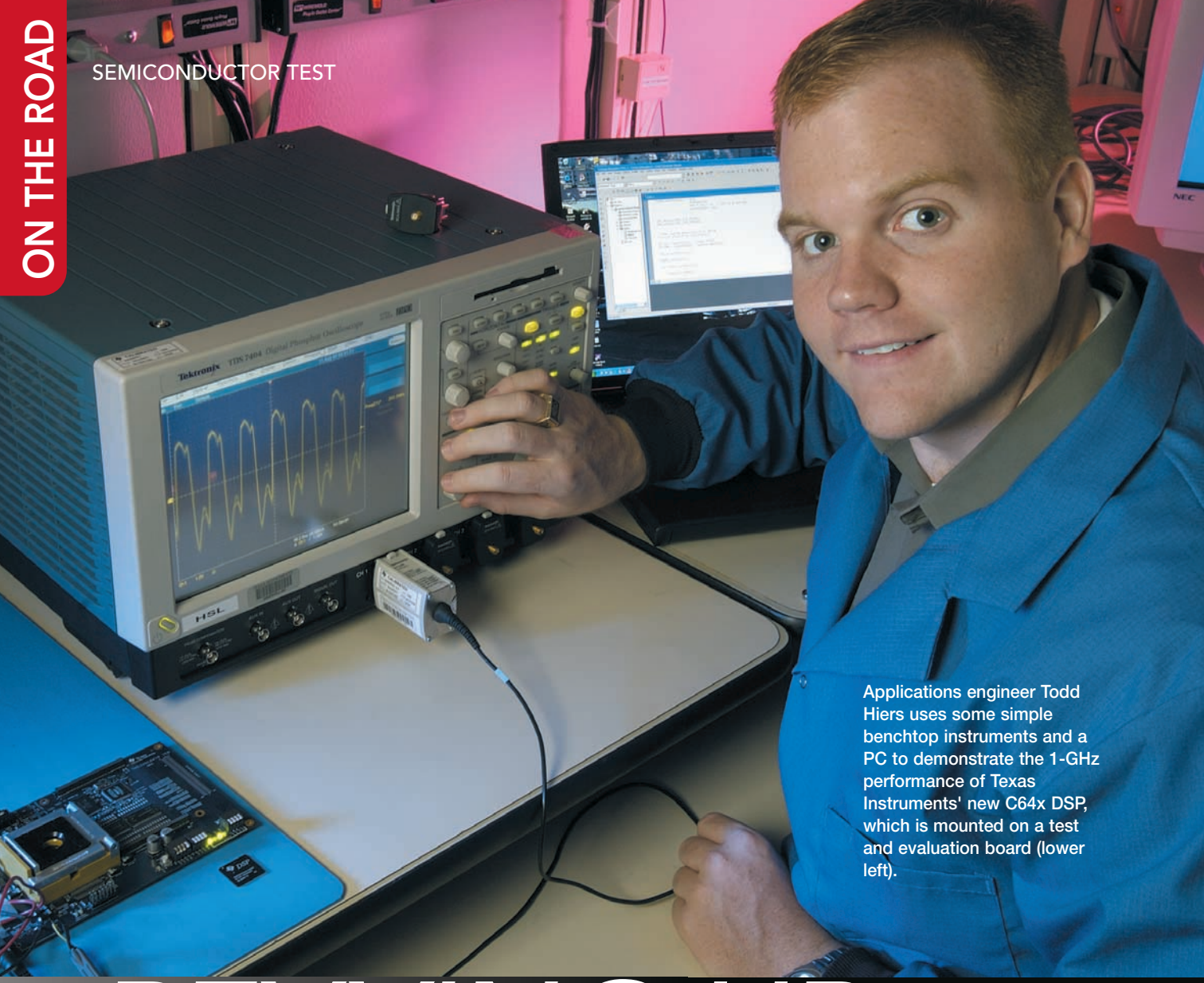

Applications engineer Todd Hiers uses some simple benchtop instruments and a PC to demonstrate the 1-GHz performance of Texas Instruments' new C64x DSP, which is mounted on a test and evaluation board (lower left).

REVVING UP REAL TIME

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RICK NELSON, EXECUTIVE EDITOR

Stafford, TX—Digital signal processors (DSPs) are opening the door to a broad range of real-time applications. At one end of this range are traditional communications applications, which are now expanding from voice processing to streaming media. At the other end are applications that can be described as "visionary": Researchers at the University of Southern California (USC), for instance, are developing artificial vision systems based on retinal implants that attempt to restore sight to the blind.

Digital signal processing's ability to serve such applications got a boost in May, when Texas Instruments demonstrated a 1-GHz version of its TMS320C64x fixed-point DSP, which represents a significant performance improvement over the 720-MHz version introduced just weeks earlier. A 1-GHz DSP, the USC researchers report, should provide the computational horsepower needed to deliver 1000-pixel real-time images to the vision impaired.

Of course, to economically produce the DSPs at the heart of such applications, TI engineers need exemplary vision into DSP performance and into the manufacturing process used to produce the devices. *Test & Measurement World* visited TI's DSP operation in this Houston suburb to learn what the implications are for testing these high-performance devices.

The drastic speed increases might seem to put a strain on test equipment, but TI engineers haven't found that to be the case. Flexibility, they suggest, is more important than raw speed in test equipment, and whether on the bench or on the production floor, engineering finesse seems more important than instrument brute force.

Applications engineer Todd Hiers hints at this approach: "You can use the chip to test itself. Feed it some input, and you know what output you should expect to get back."

That's the basis of Hiers' elegant demonstration, which shows that the new C64x does indeed operate at 1 GHz. In his test setup, he feeds a fractional clock signal into the device under test mounted on a low-cost test and evaluation board (TEB). That clock signal gets multiplied up to the 1-GHz CPU rate on chip.

Hiers then measures a clock-divided-by-four output on a garden-variety Tektronix scope, with the resulting 250-MHz measured signal demonstrating that the core CPU is running at a 1-GHz rate. (His setup includes a Hewlett-Packard programmable power supply, which slightly overdrives the 130-nm engineering prototype of the 1-GHz parts. The 90-nm production versions, available early next year, will operate at nominal voltage.)

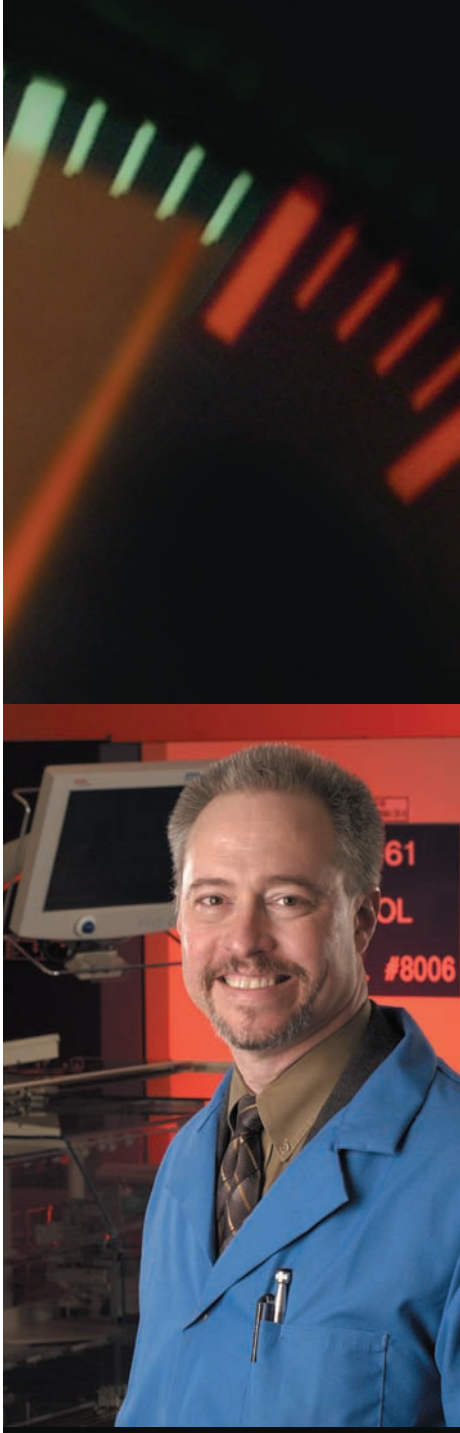
The proof of true 1-GHz performance comes in the form of Hiers' equally simple and elegant software test. Using a host PC, he programs the DSP to execute a half-second's worth of 512-point, 16-bit fast Fourier transforms, which require 3206 clock cycles each to complete. Finding that the DSP computes in excess of 156,000 such operations in a half second proves that the CPU is operating at a minimum of 1 GHz.

SOC-like test needs

Of course, a successful demonstration on an engineering prototype doesn't guarantee success in the marketplace, which demands the economical high-volume production of high-quality parts. Ray Simar, advanced architecture manager and a TI Fellow, says, "We have a big focus on ramp-to-volume. It's not enough just to [successfully] tape out a design. Several years ago, we focused on 'taping it out' and getting the first ones to wiggle. Now, the key is how quickly we can ramp to volume."

Simar likens DSP test requirements to those of SOCs more than to those of standard microprocessors. "A lot of systems will have a core CPU but with different memory sizes and peripheral mixes, which will determine how you test [the CPU]."

With respect to memory, Glenn Lorig, DSP product-engineering manager, says that in contrast to a general-purpose processor, which may have a limited amount of SRAM



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SCOTT F. KOHN PHOTOGRAPHY

cache, "Our devices have a significant amount of SRAM supporting both cache- and data-space needs, and we have to develop and execute a memory-specific test strategy for these areas of our designs."

Roberto Rivera, product engineering manager for the 1-GHz DSP devices, elaborates: "Our DSPs are general-purpose." To adapt to specific customer needs, the DSPs "have a wide variety of peripherals," and he cited a bewildering list. In addition to the common 32-bit/33-MHz PCI ports and 64-channel DMA interfaces, for example, TI DSPs support McBSP, McASP, HPI, UTOPIA, and EMIF interfaces plus Viterbi and turbo coprocessors (see "DSP peripheral functions" in the online version of this article at www.tmworld.com).

The many possible memory and peripheral combinations make for myriad unique processor configurations, Rivera says, and "we need ATE with enough features to test all of them." The key is flexibility: 1-GHz DSPs don't present 1-GHz signals at their output pins and therefore don't demand testers that support gigahertz-rate data streams.

Each peripheral function can have its own clock domain, though, and the multiple clock domains of today's DSPs present significant test challenges, says Hiers. Users choose a peripheral mix under software control, and this mix determines what function gets assigned to a particular device pin. A DSP might have a video port, a McBSP, and a McASP sharing the same pins, and an ATE system must be able to exercise all the functions to which one group of pins might be assigned.

Because of this complexity, says Lorig, "We ensure that our product and test

Glenn Lorig, DSP product-engineering manager, examines some of the systems on TI's tester roadmap, which includes commercial ATE as well as systems built in-house.

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DSP applications

Digital signal processors are designed to perform the high-speed calculations necessary to process image, voice, and other signals that are key to a multitude of products, from consumer cell phones to industrial robots. Specifically, DSPs are designed to efficiently execute multiply-accumulate operations of this form:

$$y = \sum_{i=1}^{N} a_i x_i$$

Fast execution of these operations is important for evaluating compression, digital-filter, and other algorithms.

DSPs typically employ pipelining and parallelism to simultaneously perform multiple operations. TI's 1-GHz C64x can execute eight operations in parallel, or 8 billion operations/s. TI cites several applications that can benefit from such processing power:

• **Digital cinematography.** Dalsa (Toronto, ON, Canada; www.dalsa.com) develops digital cameras for the motion-picture industry and employs DSP technology to combine the benefits of 35-mm film with those of digital cinematography. Dalsa, which can achieve standard 35-mm frame rates with 720-MHz DSPs, will use 1-GHz versions to extend frame rates and add real-time processing.

EVS Broadcast Equipment (Ougrée, Belgium; www.evs.tv) is also taking aim at digital cinematography. The manufacturer of servers and software for television stations, broadcasters, and production companies focuses on slow-motion replay and highlights-editing for sports, but the emergence of higher-speed DSPs will enable EVS to build high-definition servers for digital cinema theaters.

• **Control-room visualization.** Barco (Kortrijk, Belgium; www.barco.com) makes visualization systems for the control rooms found in network-operation centers, power plants, traffic-management centers, and broadcast studios. Currently, the company's systems can decode and display four video streams simultaneously; higher-speed DSPs will enable the addition of audio channels and will permit image analysis as well as display.

• **Wavelet-based image compression.** Aware (Boston, MA; www.aware.com) develops products built around two wavelet-based image-compression standards, WSQ and JPEG2000. The company's JPEG2000 software serves in medical- and geospatial-imaging applications, digital libraries, and digital archives. Aware has ported the Aware Motion JPEG2000 to TI DSPs to support the faster frame rates required for video surveillance. Each frame is compressed as a video image, which provides for quick access to high-resolution images that can serve as evidence in court cases, for instance.

• **Video conferencing.** Radvision (Glen Rock, NJ; www.radvision.com) plans to use the 1-GHz DSPs for its videoconferencing-infrastructure equipment. In a video presentation, Peter Benedict, Radvision director of global communications, says the company is unique in using a programmable DSP for such equipment; competitors' approaches are "locked in silicon," he adds. Programmability enables the company to upgrade its equipment (to add new features, accommodate new protocols, or implement new compression algorithms) with software-only upgrades.

engineers have a strong knowledge of the product from the inside out so that they can develop a viable and comprehensive test strategy."

All in the family

Lorig says TI performs all manufacturing and testing (at both wafer and package levels) internally and has no plans to use external test houses. He says that because TI owns the design, manufacturing, and test processes, engineers can rapidly adjust their designs as manufacturing and test information becomes available. He adds, "We also pair our production and test engineers with a design team before a product is released to our fab so that the production and test group may better learn the product and be ready for validation when first wafers are received."

Roberto Rivera, product engineering manager for TI's 1-GHz DSP devices, explains that DSPs support memory and peripheral combinations that make for myriad processor configurations.

Rivera points out that TI's DSP operation has no "test-engineering" group *per se*. Lorig adds, "We make our engineers not only responsible for testing but for overall manufacturing."

Lorig says many of TI's production and test engineers have experience in programming DSPs. "The depth of their [programming] knowledge is not as deep as our applications staff's, but it does enable them to write code for manufacturing requirements. We have a strong co-op program, which we've found to be an asset to our staffing needs. It can take one to two years for engineers to hit their stride. Within five years, they are contributing at a very strong level."

Rivera adds that in addition to programming experience, production and test engineers also need to understand the assembly and packaging operation: "Packaging plays a big role in performance." Hiers adds that even personnel who are primarily software engineers need a good amount of EE training.

From prototype to production

TI's 1-GHz DSP is now at the engineering-sample stage. I asked how the group gains confidence that yields will be sufficiently high for gigahertz-rate parts when they reach production early in 2004. Rivera attributes such confidence to the "very extensive characterization of our wafer process" that occurs before the team embarks on a new product.

Adds Lorig, "TI does process development and wafer manufacturing internally, and we have the opportunity to work very closely with the engineers responsible for those areas. We take advantage of this and work with them on a daily basis to establish a tight loop between wafer processing and product yield and performance."

Hiers notes that "if you don't own the process end to end, it is tough to see where the disconnects are. Fabless companies will have to stay 'middle of the road'. They have to stick with what they know is going to work, because they have fewer knobs to turn" to attempt to fix problems.

Simar says that within TI, "There are many groups that talk to each other," and such communication would be tough if these groups were spread across many companies, as is the case for fabless firms. "The fabless companies," adds Simar, "have always tended to lag 50% on features like clock rate. There are hooks we have to put in place to test these things. We are hitting on these issues way ahead of them. Now, as we are pushing our chips to higher speeds, power will be important, and we have to put the hooks in place for our testing. Some fabless companies may be doing this, but we are in a position to understand the problems much better."

Design and test

When embarking on the 1-GHz DSP development project, TI engineers didn't have to start from scratch. Simar points out that TI has been implementing scan test techniques since the mid-1980s. The design and design-for-test tools they use—from companies including Synopsys, Mentor Graphics, and Cadence—were already in place. "We use the best tools available for the job. We are not tied to one specific company," says Rivera.

Similarly, the team relied on TI's overall tester roadmap, which includes LTX Fusion systems as well as test systems built in-house. Says Lorig, "When we start a project, we've already determined which test equipment to utilize." Rivera says that a key requirement is that the tester be capable of clock synchronization at very high speeds.

Lorig says that a key to his team's success is a 360° view of design, fab, packaging, and test. "We can align design features to the test equipment we utilize. For example, we can influence design IP so that it communicates to the test equipment in the friendliest manner possible. The more self-testable we make our designs, the easier it is to move to the next level of coverage that we want to apply to the device."

Lorig adds, "Because TI is structured the way it is, you can really get everyone on the same page: The initial architect, product designer, product and test engineer, applications team, wafer and fabrication team, the development folks, and the assembly and test group." Says Simar, "One of the nice things is that Houston is a microcosm of that. All those groups are represented here in one building."

For the future, Lorig says, "EDA tools will have to get more manufacturing-centric. We can work with vendors" to help bring that about. Adds Rivera, "TI is a member of many external organizations and is always looking for new innovative techniques both internally and externally. The cost of test is a significant portion of the cost of manufacturing high-performance DSPs. We are always looking into all the techniques available to make the test more cost effective." T&MW

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