Application Note

Understanding ADC Input Leakage and Sampling Behavior in TIC12400-Q1

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ABSTRACT

This application note explains the input leakage and sampling behavior observed on the INx pins of the TIC12400-Q1 Multiple Switch Detection Interface (MSDI) when configured in 0mA wetting current mode. The underlying mechanism is analyzed in relation to the internal ADC front-end architecture, and practical system-level design guidelines are provided to achieve predictable, accurate ADC measurements.

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1 Introduction

TI's TIC12400-Q1 is a highly integrated Multiple Switch Detection Interface (MSDI) widely used in automotive Body Control Modules (BCM) and Zonal Control Modules (ZCM). It monitors switches and sensors through a combination of programmable wetting current sources, on-chip comparators, and a 10-bit ADC. Its polling-based architecture allows the host MCU to remain in a low-power sleep state between switch-scanning cycles, which is a key system-level benefit in power-sensitive automotive designs.

The on-chip ADC is primarily intended for use with resistor-coded analog switches, where the programmable wetting current flows through an external resistor network and generates a proportional voltage at the INx pin. In some applications, however, system constraints require the INx voltage to be provided directly by a passive resistor divider, a slide rheostat, or a similar high-impedance source, with the TIC12400-Q1 wetting current configured to 0mA. In these configurations, engineers have observed the following behavior:

- ADC conversion results that read higher than the expected steady-state input voltage
- Narrow voltage spikes on the INx pin that are synchronized with each sampling cycle
- Increased sensitivity to external RC filter components connected to the INx pin

This application note explains the root cause of these observations in the context of the TIC12400-Q1 internal ADC front-end architecture, provides a quantitative model for estimating the resulting measurement error, and describes practical mitigation approaches that allow the device to be used reliably in such configurations.

2 On-Chip ADC Front-End Architecture Overview

A fundamental understanding of the internal signal chain is necessary to correctly interpret the behavior observed at the INx pins. Figure 2-1 shows the functional block diagram of the TIC12400-Q1, highlighting the ADC front-end path.

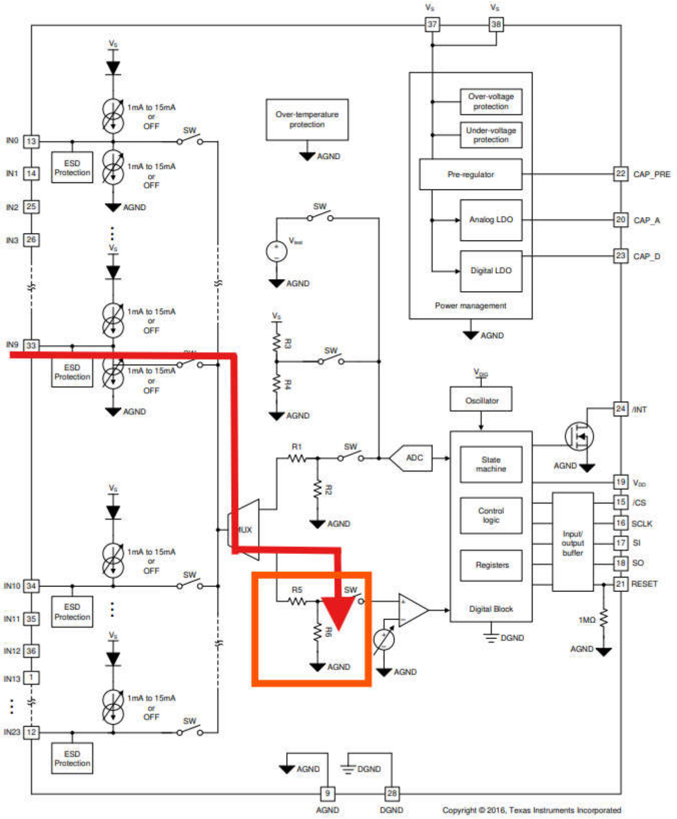

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Figure 2-1. TIC12400-Q1 Functional Block Diagram (ADC Front-End Signal Path Highlighted)

Each INx input pin is routed to either the ADC or the comparator through an internal multiplexer (MUX). On the ADC signal path, an internal resistive voltage divider scales the external input voltage down to a level compatible

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with the ADC input range before conversion. Several important architectural characteristics follow from this structure:

- The internal voltage divider is permanently present whenever an INx channel is assigned to the ADC. It always forms a load on the INx pin during the active MUX window, regardless of the wetting current setting.
- The ADC is factory-calibrated to report the voltage at the INx pin, not the voltage at the internal divided node. This means the full-scale range of 6V corresponds to ADC code 1023 as measured at the INx pin, consistent with the conversion formula in the TIC12400-Q1 datasheet.
- Only one INx channel is connected to the ADC or comparator at any given time, for the duration of the configured sampling window (T_{ADC} for ADC mode, T_{comp} for comparator mode). All other channels remain disconnected from the ADC or comparator during that interval.

3 Understanding the I_{LKG} Specification in the Datasheet

The TIC12400-Q1 datasheet specifies an input leakage current (I_{LKG}) of up to ±110µA at the INx pin when the wetting current is configured to 0mA. This specification is frequently misinterpreted as a steady-state DC leakage current that is continuously present on the INx pin. Understanding what this specification actually represents is critical to correctly designing the external interface circuitry.

3.1 Interpretation of the ±110 µA Specification

The ±110µA I_{LKG} specification is a worst-case bound that covers the full range of operating conditions, supply voltages, temperatures, and internal device states across all production units. The ± sign indicates that the current can flow in either direction—into or out of the INx pin—depending on the internal node voltages at the time the MUX connects the channel. This value is intended to bound the maximum transient current that the external source can be required to supply or absorb and should not be interpreted as a typical or continuous operating current.

3.2 The Leakage Current Is MUX-Activated and Time-Limited

Bench measurements demonstrate that the I_{LKG} current is not continuously present on the INx pin. Instead, it is injected only when the internal MUX actively connects a specific INx channel to the ADC or comparator circuitry. This transient lasts for the duration of the configured sampling window—approximately T_{adc} when the channel is assigned to ADC mode, or approximately T_{comp} when assigned to comparator mode. Outside of these windows, the INx pin is electrically isolated from the internal ADC front-end.

Figure 3-1 and Figure 3-2 show oscilloscope captures of the INx pin voltage during the sampling window in ADC mode and comparator mode, respectively. In both cases, the wetting current is set to 0 mA, and the voltage excursion at the INx pin is caused entirely by the transient MUX-connection current charging the external and parasitic capacitance on the INx node. Critically, switching between ADC and comparator configuration changes only the pulse width of the observed voltage spike, not its amplitude, which confirms that this phenomenon is associated with the MUX and internal ADC circuitry rather than with any external wetting current source.

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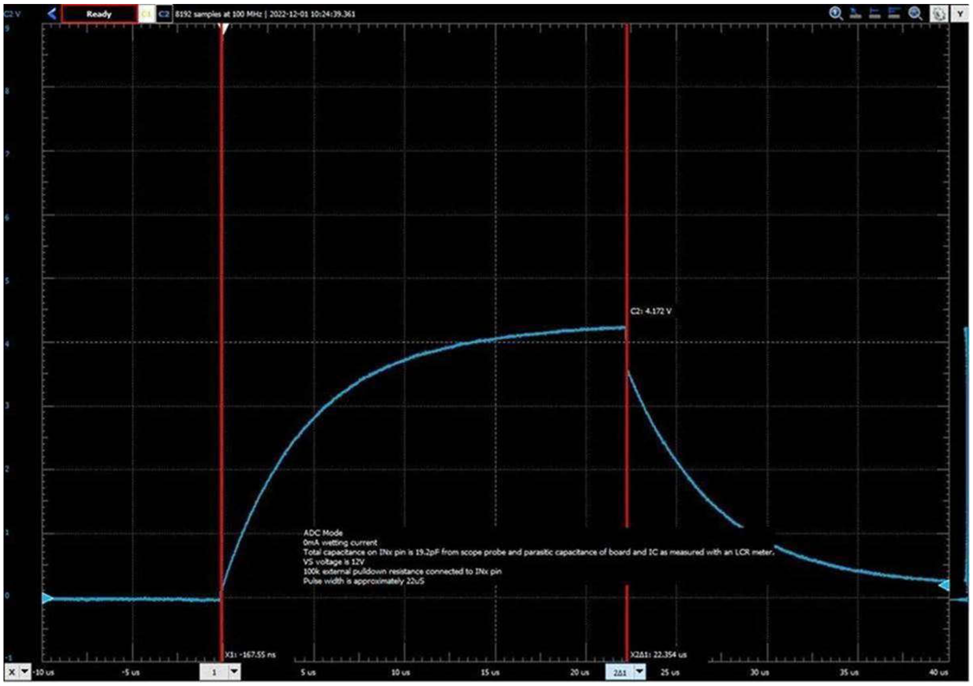
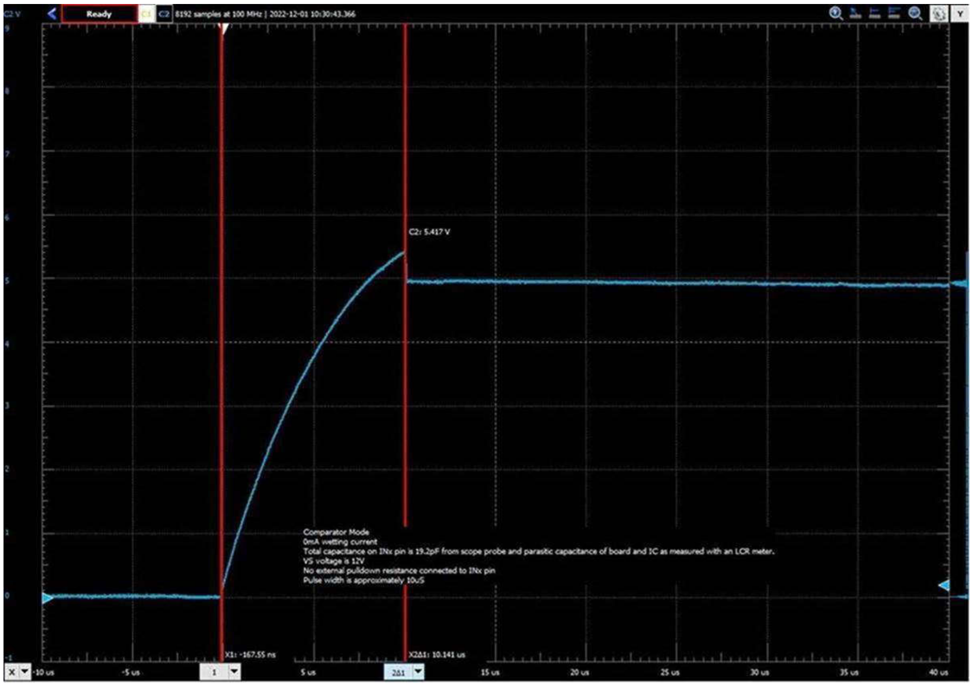


ADC Mode
0mA wetting current
Total capacitance on INx pin is 19.2pF from scope probe and parasitic capacitance of board and IC as measured with an LCR meter.
VS voltage is 12V
100k external pulldown resistance connected to INx pin
Pulse width is approximately 22uS

Figure 3-1. INx Pin Voltage During Sampling Window: ADC Mode



Comparator Mode
0mA wetting current
Total capacitance on INx pin is 19.2pF from scope probe and parasitic capacitance of board and IC as measured with an LCR meter.
VS voltage is 12V
No external pulldown resistance connected to INx pin
Pulse width is approximately 10uS

Figure 3-2. INx Pin Voltage During Sampling Window: Comparator Mode

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4 Design Considerations with Weak Voltage Sources

4.1 Definition of a Weak Voltage Source

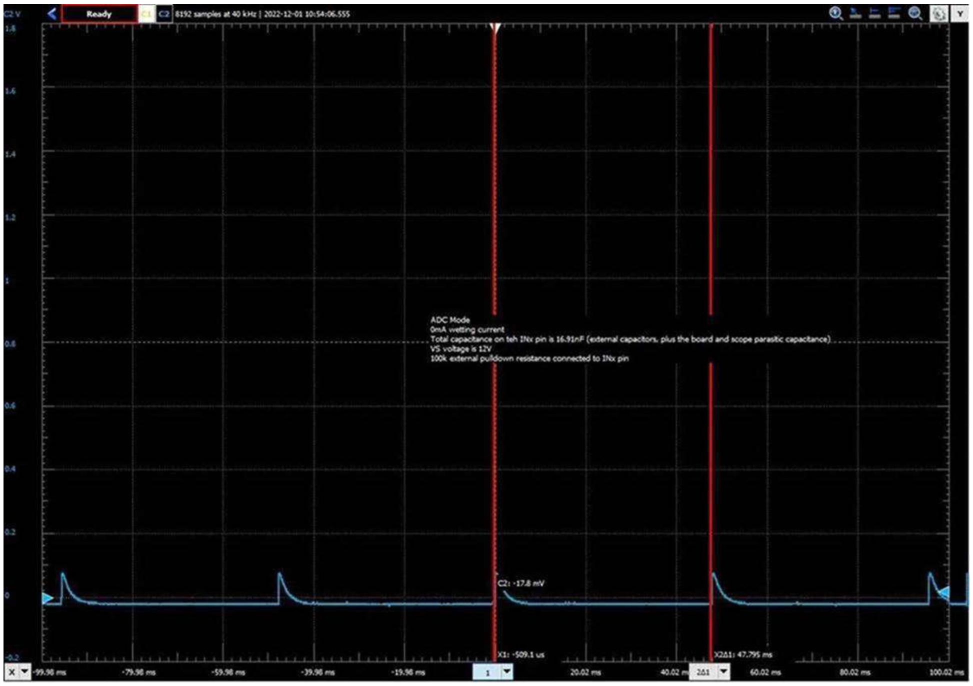
In the context of the TIC12400-Q1 ADC input, a weak voltage source is defined as an external source that can accurately establish a DC voltage level but has limited ability to rapidly supply or absorb transient currents. Common examples in automotive BCM and ZCM applications include:

- Passive resistor divider networks (for example, voltage references derived from a resistor ladder)
- Slide rheostats used as position sensors
- High-impedance sensor or transducer outputs that are not actively buffered

These sources can establish DC voltage accurately, but they cannot rapidly absorb or supply transient currents. When the source impedance is low (as in an actively driven output), the transient caused by the MUX-connection current is rapidly absorbed and has a negligible effect on the ADC reading. When the source impedance is high, however, the voltage deviation persists for a duration that can overlap with the ADC conversion window, introducing a systematic offset into the measurement result.

4.2 Mechanism of the Sampling Spike

When an INx channel is selected by the internal MUX, the internal voltage divider and ADC front-end circuitry are suddenly connected to the INx pin. During the sampling window (T_{adc} or T_{comp}), a leakage current up to the I_{LKG} bound is injected into the total capacitance present at the INx node. This total capacitance (C_{IN}) includes the parasitic capacitance of the PCB trace and the TIC12400-Q1 pin, as well as any external filter capacitor intentionally added to the node. At the end of the sampling window, the MUX disconnects the internal front-end, and the stored charge discharges through the external source impedance (R_{EXT}) back toward the steady-state voltage defined by the external network. Figure 4 shows the resulting narrow voltage spikes measured at the INx pin across multiple polling cycles.



ADC Mode
0mA wetting current
Total capacitance on teh INx pin is 16.91nF (external capacitors, plus the board and scope parasitic capacitance)
VS voltage is 12V
100k external pulldown resistance connected to INx pin

Figure 4-1. Repeating INx Voltage Spikes Across Polling Cycles — ADC Mode

Because the leakage current injection occurs consistently at each polling event and the $R_{EXT} \times C_{IN}$ discharge time constant can be long relative to the polling interval, the INx node may not fully recover to its steady-state voltage before the next sampling event. This leads to a quasi-static DC offset superimposed on the true input voltage.

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5 Quantitative Model and Error Estimation

The voltage deviation introduced by the MUX-connection transient can be estimated analytically using basic RC charge principles. While the model makes simplifying assumptions, it provides a useful first-order estimate for system design margin analysis.

5.1 Voltage Step During the Sampling Window

During the sampling window, the leakage current I_{LKG} charges the total capacitance C_{IN} at the INx pin. The resulting voltage step is approximated by:

$$\Delta V \approx \frac{I_{LKG} \cdot T_{sample}}{C_{IN}} (1) \tag{1}$$

where I_{LKG} is the leakage current (up to ±110 μA), T_{sample} is T_{adc} or T_{comp} as configured, and C_{IN} is the total capacitance at the INx node. Equation 1 shows that increasing C_{IN} directly reduces ΔV for a given leakage current and sampling duration.

5.2 Steady-State Offset with High-Impedance Sources

If the $R_{EXT} \times C_{IN}$ discharge time constant is long relative to the polling period T_{POLL}, the INx node does not fully discharge between consecutive sampling events. Each successive sampling event adds charge to the node before the previous charge has fully dissipated, causing the node voltage to accumulate toward a quasi-static offset above the true source voltage. Because the leakage current magnitude and the sampling timing are both deterministic and repeatable, this offset is systematic—it is constant across measurement cycles and can therefore be characterized and compensated. The steady-state DC offset can be estimated by considering the charge balance between the injection per sample and the discharge per polling period.

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6 Design Mitigation Methods

Three complementary approaches are available to manage the effect of MUX-connection transient leakage in 0mA wetting current applications. The choice among them depends on system cost constraints, allowable PCB area, and the required measurement accuracy.

6.1 Method 1: Strengthen the Voltage Source

The most direct approach is to reduce the Thévenin source impedance seen at the INx pin, so that the transient current injected during the sampling window cannot produce a significant voltage excursion. A low-impedance buffer amplifier placed between the passive network and the INx pin provides an actively driven, low-impedance source that can supply or absorb the I_{LKG} transient current without any measurable deviation at the INx node. This approach completely eliminates the sampling spike and the associated offset, and no additional calibration is required. The trade-off is increased BOM cost, additional PCB area, and the need to power the buffer in all operating modes including low-power sleep states where the TIC12400-Q1 polling is active.

6.2 Method 2: External RC Compensation (Recommended)

A more cost-effective approach is to add external capacitance directly at the INx pin. From Equation 1, increasing C_{IN} reduces the voltage step ΔV proportionally. Bench measurements confirm that capacitors of 15 nF or larger significantly attenuate the spike amplitude, and that further increasing capacitance continues to reduce the effect. A parallel pull-down resistor can be included to control the node discharge behavior and prevent charge accumulation between polling cycles, if needed based on the $R_{EXT} \times C_{IN}$ time constant relative to T_{POLL}. The designer must verify that the RC time constant formed by R_{EXT} and C_{IN} does not slow the signal settling to a level that impairs switch-state detection speed, and that the capacitor leakage current is negligible relative to the signal being measured.

6.3 Method 3: Static Offset Calibration

In applications where the residual offset after RC compensation is still above the required accuracy threshold, the systematic nature of the offset makes it amenable to factory or in-field calibration. Because the leakage current and timing are deterministic, the resulting offset ΔV_{offset} is constant and repeatable across measurement cycles. A corrected ADC result can therefore be obtained by:

$$V_{corrected} = V_{ADC} - \Delta V_{offset} \quad (2)$$

Bench measurements and simulation correlation show that when ΔV_{offset} is characterized at the system level under representative operating conditions, the total remaining error can be reduced to below 1% across the full operating voltage range. This method requires no additional hardware components beyond what is already present in the passive signal network, making it attractive in cost-sensitive designs where buffer amplifiers cannot be added.

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7 Summary

The input leakage current (I_{LKG}) of up to ±110µA specified in the TIC12400-Q1 datasheet for 0mA wetting current mode is a worst-case bound that covers all operating conditions, supply voltages, temperatures, and internal device states. It is not a continuous DC current present at the INx pin. Bench evaluation confirms that this leakage current is injected only during the brief MUX-active sampling window associated with each ADC or comparator measurement, and that its duration is directly determined by the configured sampling time (T_{adc} or T_{comp}).

When the external voltage applied to the INx pin is derived from a high-impedance source, such as a passive resistor divider or a slide rheostat—this transient leakage current charges the capacitance on the INx node and produces narrow voltage spikes synchronized with each polling event. If the RC discharge time constant is long relative to the polling period, a quasi-static offset can accumulate on the INx node, causing the ADC to report a value higher than the true steady-state input voltage. Because this behavior is entirely deterministic and repeatable, it can be effectively managed through one or more of the following system-level approaches: strengthening the external voltage source with a low-impedance buffer; adding appropriate external capacitance to reduce the transient voltage step per Equation 1; or characterizing the residual offset as a static, calibratable error. With these design considerations properly addressed, the TIC12400-Q1 can reliably perform analog voltage sensing using passive signal sources across a wide range of automotive BCM and ZCM applications.

8 References

1. Texas Instruments, *TIC12400-Q1 24-Input Multiple Switch Detection Interface (MSDI) With Integrated ADC and Adjustable Wetting Current for Automotive Systems*, datasheet.
2. Texas Instruments, *Steps to Configure TIC12400-Q1 Multiple Switch Detection Interface (MSDI)*, application note.
3. Texas Instruments, *Body Control Module Resources to Make Your Design More Efficient and Reliable*, technical article.

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Last updated 10/2025