Application Note

Optimizing IFF Transponder Turnaround Time Using Ultra-Low Latency ADCs

Jash Kothari, Srinivas Murthy

ABSTRACT

This application note details the use of the ADC366x family to minimize turnaround time in *Identification Friend or Foe (IFF)* transponders.

The ADC3668 and ADC3669 are dual-channel, 16-bit *non-interleaved* analog-to-digital converters (ADCs) supporting sampling rates of 250MSPS and 500MSPS, respectively. These devices are engineered to achieve high SNR while providing the benefits of Direct RF Sampling in the L-band. The power-efficient architecture consumes only 300mW/channel at 500MSPS and features power scaling for lower sampling rates (250mW/channel at 250MSPS) without compromising total latency. By leveraging the device's specialized 9-clock cycle *Low Latency Mode*, Designers can achieve the sub-microsecond processing speeds essential for compliance with *DoD AIMS 17-1000 (Mark XIIB), NATO STANAG 4193, RTCA DO-181E, and ICAO Annex 10* requirements.

Table of Contents

Trademarks

1 Introduction

Identification Friend or Foe (IFF) systems are used to distinguish between friendly assets and potential threats in both in the civilian as well as the defense sector.

The typical system utilizes a two-way interaction: *a primary interrogator and a secondary transponder*. The interrogator initiates the exchange by transmitting an encoded pulse sequence at a standardized frequency of 1030MHz. Upon reception using the transponder and successful decryption of this coded signal, the target's transponder emits an automated, encoded reply at 1090MHz, providing identification and telemetry data, such as altitude and GPS position.

To verify accurate range calculation, the transponder turnaround time is fixed by international standards. The interrogator calculates range by measuring the total time from *shout* to *echo* and then subtracting the internal processing constant – typically *3.0 microseconds ± 0.5 microseconds*. Any deviation in this, causes the aircraft's reported position to shift significantly from the actual location.

In military modes, the transponder does not just reply, it must decrypt the question and encrypt the answer. If the hardware is too slow, then the latency can exceed the interrogator's expected window, therefore causing it to mark a friendly aircraft as *unknown* or *hostile*. Moreover, after a transponder sends a reply, it enters a dead time (generally up to 125µs) where it cannot respond to other interrogations. In busy airspace, managing this latency is critical to prevent the aircraft from *disappearing* from other radars.

2 ADC366x Internal Rx Architecture

2.1 1.4GHz Wideband, High Performance and Low Power Direct RF Sampling

- The ADC3669 features a high-performance analog input bandwidth of 1.4GHz allowing for Direct RF Sampling of the 1030MHz and 1090MHz interrogation signal.
- This can help designers to eliminate analog down-conversion stages including mixers, Local Oscillators & IF filters. Eliminating these analog components, which inherently add delay, helps save on the total turn-around time.
- Further, the 16-bit core of ADC provides a very high value of SNR and SFDR which helps the systems distinguish weak, distant interrogation from the high-power interferences. (example, busy civilian airports or tactical combat zones.
- By operating at a highly efficient 300mW per channel at 500MSPS, the ADC3669 stands as one of the most power-efficient ADCs in this class, directly addressing the critical SWaP optimization constraints required for modern airborne systems.

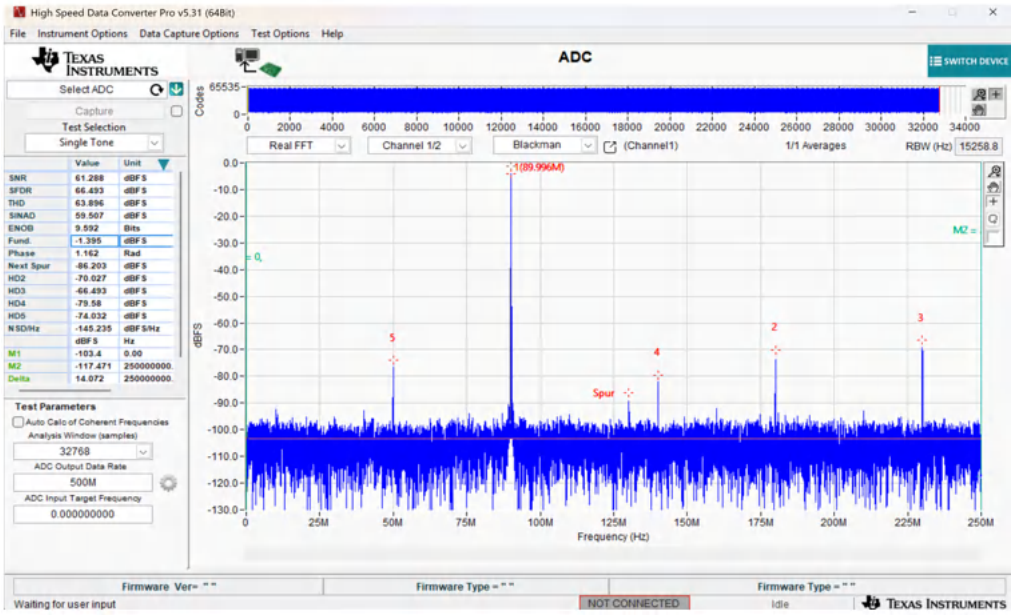

Figure 2-1. FFT Output of ADC3669 at Fin = 1090MHz

2.2 Integrated Digital Downconverter (DDC) and 32-Bit NCO

The ADC366x provides up to four Digital Downconverters (DDC) paired with 32-bit Numerically Controlled Oscillators (NCO).

Unlike analog systems which are susceptible to thermal drifts, the digital NCO allows to digitally shift the 1030MHz signal down to baseband within the ADC itself while, maintaining excellent stability across temperature. This ensures that the internal pulse-detection algorithms receive a consistent signal, preventing ***timing walk*** or ***jitter*** which helps maintain better range accuracy.

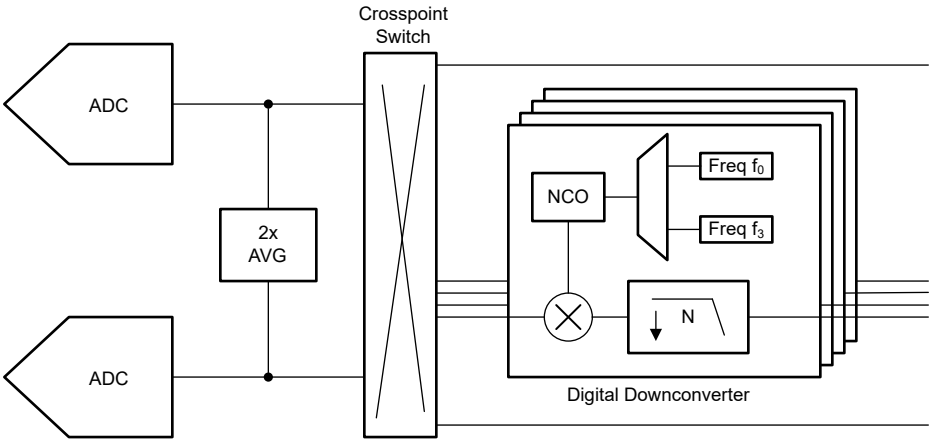

Figure 2-2. Internal Rx Architecture of ADC3668/ADC3669

As illustrated in Figure 2-3, leveraging the ADC366x's internal NCO and decimation blocks optimizes frequency planning by eliminating alias images at the hardware level. Performing decimation-by-4 natively within the ADC provides an expected 6dB processing gain by filtering out-of-band quantization noise. Offloading this digital down-conversion task from the FPGA to the converter helps minimize the power consumption by saving FPGA logic resources and reducing interface bandwidth.

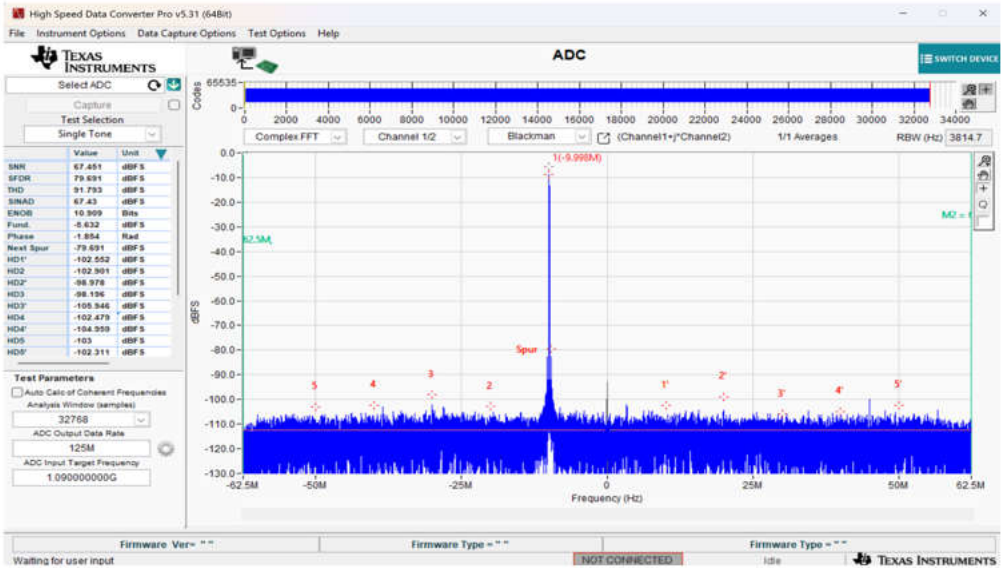

Figure 2-3. Complex FFT output with internal DDC + NCO and Decimation-by-4

3 ADC366x Low Latency Mode

The **ADC366x** series is specifically architected to minimize aggregate path latency (Propagation Latency + ADC sampling Latency + Digital Latency) to meet the stringent real-time requirements of high-precision applications like IFF systems.

It also provides a *low latency mode* of operation, bypassing the Digital Error Correction and all other digital features such as the decimation filter, test pattern or SDR LVDS to get a latency of just 9 clock cycles and which is ideal for applications such as low latency control loops.

Note that, since the Digital Error Correction block is bypassed, there can be some degradation in SFDR in this mode. However, in applications like IFF which rely more on the pulse timing where noise floor (NSD) or SNR is most critical, a degraded SFDR is typically not concerning.

The Low Latency Mode can be enabled in the <LOW LATENCY EN> register (0x165).

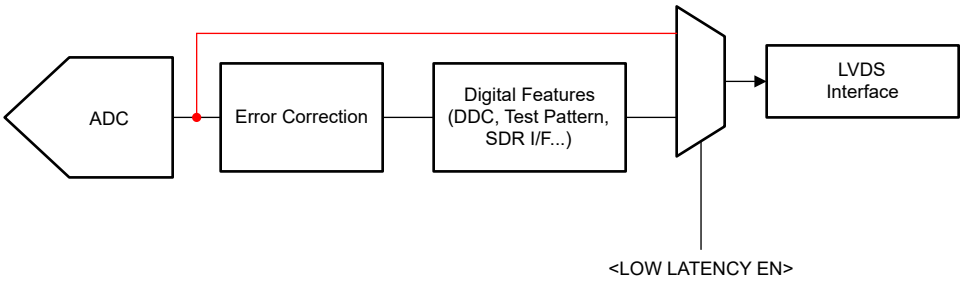

Figure 3-1. Low Latency Mode for ADC3668/ADC3669

Assuming a sampling rate (Fs) of 500MSPS, the major contributors to total latency are listed below. Using low-latency mode can reduce latency to less than 10ns.

Latencies	Conditions	Delays	Values
t_{PD} - Propagation delay		1.7 + Ts/4 nS	2.2nS
t_{ADC} - ADC Latency	DDR LVDS, normal mode	38 ADC clocks	76nS
	DDR LVDS, Low Latency mode	**4 ADC clocks**	**8nS**
tDIG - Digital delay	DDC bypass	5 ADC clocks	10nS
	DDC by 2	24 ADC clocks	48nS
	DDC by 16…32768	50 ADC clocks	100nS

4 IFF Pulse Processing Performance

To verify the linearity and sensitivity of ADC3669, input power was swept across a 50dB dynamic range from -10dBFS pulse down to a highly attenuated -60dBFS threshold, utilizing a RF pulse train having a pulse width of 2µs and a pulse repetition interval of 5µs.

4.1 ADC3669 Performance in Presence of a High-Power Signal Pulse

When processing a -10dBFS signal, the ADC3669 demonstrates high linearity across the full 16-bit operational dynamic range.

Time-domain analysis indicates the sampled signal spans from approximately **2,400 to 63,300 raw ADC codes, yielding a peak-to-peak distribution of ≈ 60,900 codes without any ADC saturation or clipping**. It can also be seen that the signal settles promptly to the **mid-scale baseline ≈ 32,750 codes** in between multiple pulses.

The time domain as well as the frequency domain performance of the above can be seen in the Figure 4-1 and Figure 4-2 below.

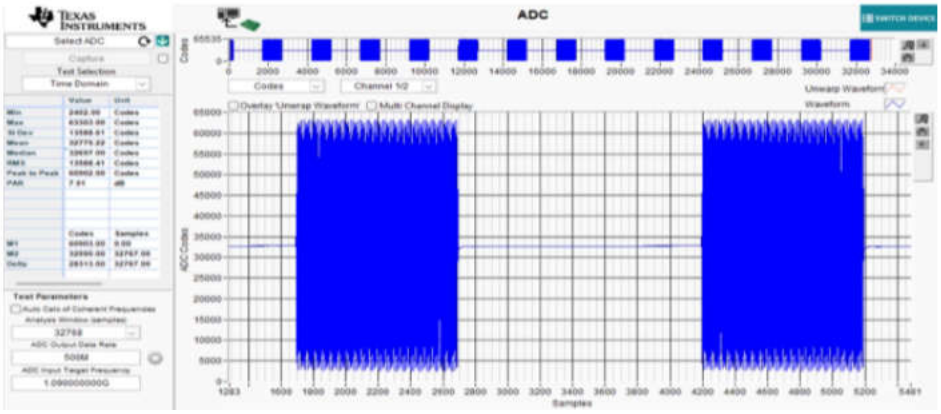

Figure 4-1. Time-Domain Capture of a 2µS Pulse at 1090MHz at -10dBFS

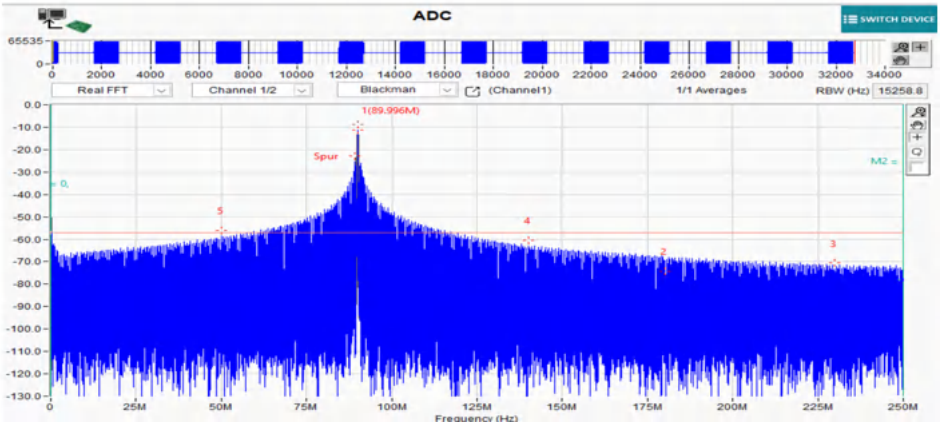

Figure 4-2. Frequency Domain Capture of a 2µS Pulse at 1090MHz at -10dBFS

4.2 ADC3669 Performance in Presence of a Weak Signal Pulse

When a weak -60dBFS input signal is introduced, the raw time-domain peak-to-peak code spread expands from an idle baseline of approximately 110 codes up to 175 codes. This 175-code envelope represents the summation of the approximately 110 codes of thermal noise present within the 250MHz Nyquist bandwidth and the 65-code peak-to-peak amplitude of the weak input pulse.

As illustrated in Figure 4-3, the time-domain capture of the 2µS pulse at -60dBFS tracks at this steady 175-code peak-to-peak window highlighting very good linear performance of the ADC3669, proving its ability to resolve waveforms even at extremely small signal strengths.

Because the pulse envelope is currently embedded within the wideband noise floor at the full 500 MSPS sample rate, the internal Digital Downconverters (DDCs) can be engaged to filter out out-of-band quantization noise, thus tightening the baseline and rendering the actual pulse shape clearly visible for downstream timing logic.

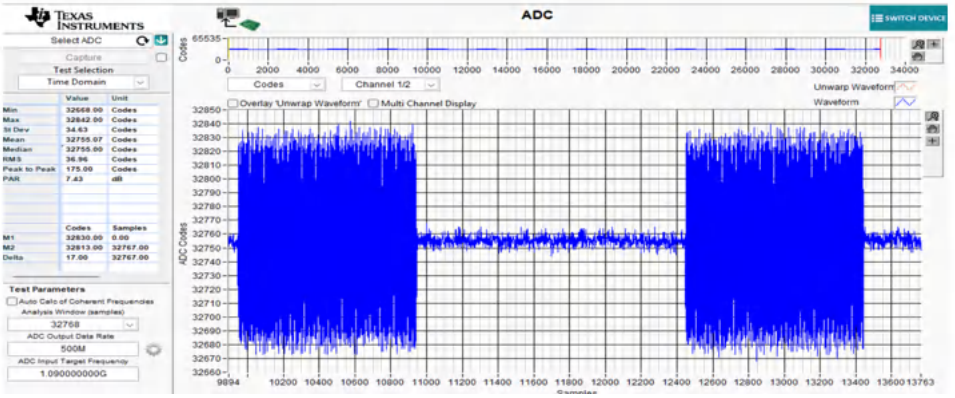

Figure 4-3. Time-Domain Capture of a 2µS Pulse at 1090MHz at -60dBFS

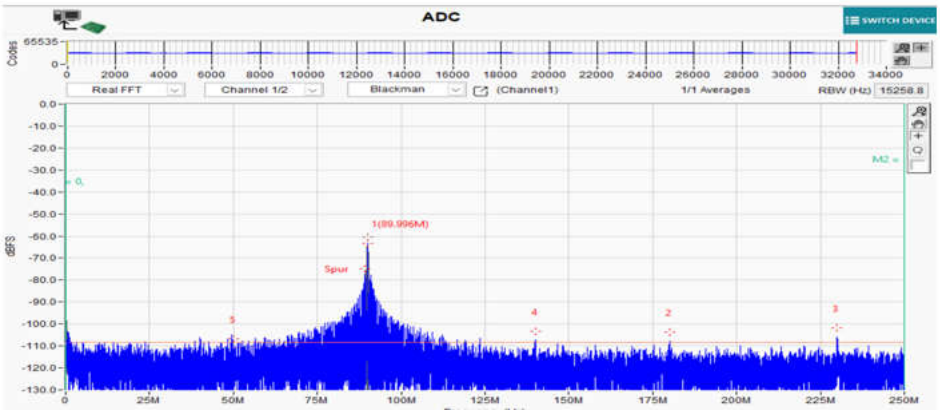

Figure 4-4. Frequency Domain Capture of a 2µS Pulse at 1090MHz at -60dBFS

5 Summary - *Buying Back* Time

Modern IFF, specifically Mode 5, requires advanced cryptographic techniques that utilize the majority of the 3.0µs turnaround window. By using the ADC366x, designers can effectively "buy back" over 200+ nanoseconds of processing time compared to standard ADCs in the systems. This extra margin allows them to implement more robust cryptographic encryption algorithms to prevent spoofing. In addition, the excellent small-signal linearity of the device and integrated digital features help offload a lot of filtering needs and power consumption from the FPGA.

6 References

- Texas Instruments, *ADC3668, ADC3669 Dual-Channel, 16-Bit 250MSPS and 500MSPS Analog-to-Digital Converter (ADC)*, data sheet.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025