TEXAS INSTRUMENTS

GS30 0.15-μm CMOS Standard Cell/Gate Array

Version 1.0

February, 2001

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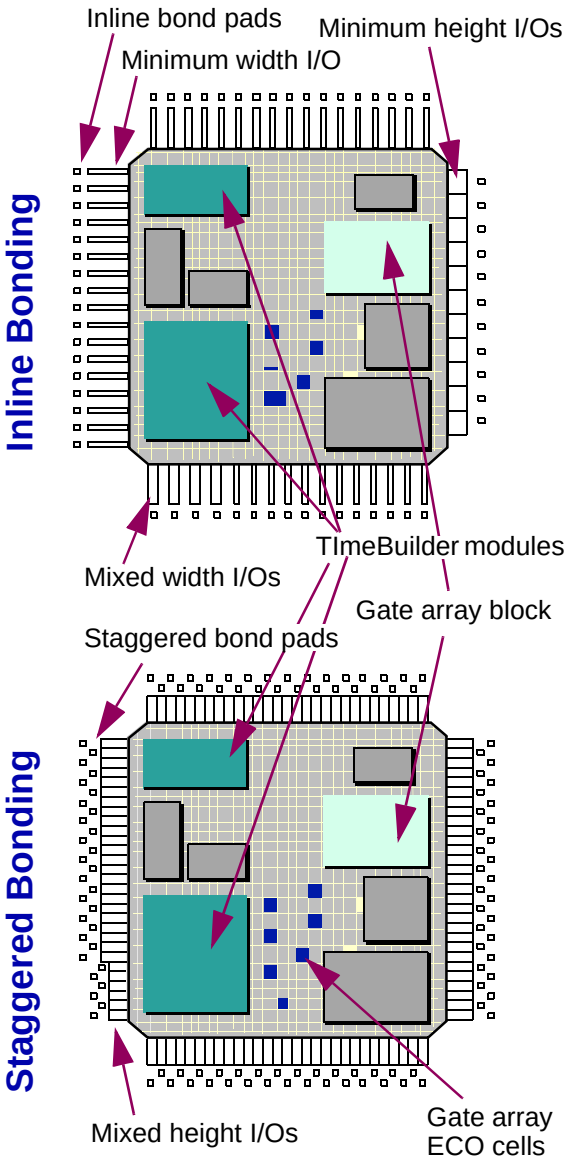
Literature number: SRST145

GS30 0.15-µm CMOS Standard Cell/Gate Array

High-Value ASIC

- **0.15-µm Leff process** (0.18-µm drawn) with Shallow Trench Isolation (STI)
- **4 and 5 levels of metal**
- **Density:** 75,000 gates/mm^2 at 50K gates
- **6 million random logic gates** plus 6 million equivalent gates in TImeBuilder™ modules and memory
- **Power supply:** 1.1/1.4/1.8 V cores I/Os: 1.8/2.5/2.75/3.3 V (selected combinations), 5 V-tolerant, failsafe
- **Power dissipation:** 0.018 µW/MHz/gate for 1.8 V core
- **Over 250 peripheral macros,** including LVCMOS, differential, level-shifting I/Os, ATA, CML, DPECL, GaAs, LVDS, SSTL, TTL, TLV, oscillators
- **More than 400 core cells**
- **Multi-gigabit** serial link transceiver technology
- **Extensive module selection**, including TMS 320 digital signal processors (DSPs), ARM™ 32-bit RISC microcontrollers, MIPS® JADE embedded processor, and analog functions
- **Memory compilers** including single-port, two-port, dual-port, three-port, ROM, CAM, and register file, synthesizable memories
- **TI ExSRAM** extremely high-density SRAM (>3 Mb of memory on a die)
- **Electrically-readable die ID**
- **Spare gate-array cells and gate-array blocks** for fast metal-level ECO
- **Packages:** TQFP, MicroStar™ BGA, plastic BGA, Generic BGA, PowerPad



Features and Benefits

GS30 uses Texas Instruments TImeCell™ Architecture, which combines on the same silicon the cost-efficiency of standard cells with the fast time-to-market of gate arrays. TI provides a full range of product options to address the challenges of producing ultra-dense, low-power devices that take advantage of system integration.

The GS30 product family is positioned to take advantage of TI's world leadership in areas key to system-level integration and systems-on-a-chip design:

- World's leading supplier of embedded ARM™ and MIPS™ cores, including the ARM 7 and ARM 9 families of RISC processors, and MIPS Jade™ and Opal™ processors
- World's leading Digital Signal Processor (DSP) supplier
- Easy integration of DSP, ARM and MIPS cores with standard cell, gate-array logic and memories
- World's leading supplier of analog and data transmission solutions, including the IEEE 1394 link core, the Universal Serial Bus (USB) function controller, and the Universal Asynchronous Receiver/Transmitter (UART), 622 Mb/s Serdes transceiver core
- Proven design methodology with integrated hardware/software coverification
- Advanced 0.15-micron L_{eff} process technology
- Superior design support and manufacturing— "no excuses" ramp to production

GS30 offers higher density and reduced die size, power and cost, or opportunity for more integration. Some key characteristics are shown in the table below.

Nominal core voltage	I/O voltage	Typical gate delay NA210, FO = 2	Typical design power dissipation
1.8 V	1.8, 2.5, 2.75, 3.3, 5.0	67 ps	0.018 µW/MHz/gate
1.4 V	1.8, 2.5, 2.75, 3.3	100 ps	0.011 µW/MHz/gate
1.1 V	1.8, 2.5, 2.75, 3.3	150 ps	0.005 µW/MHz/gate

Advanced Technology

- **4-level metal** or **5-level metal** for signal routing, with full Chemical Mechanical Polishing (CMP) planarization and fully stacked Tungsten vias.

Extensive Library for Density, Low Power, Value and Integration

- **Over 400 core macros**, including cells designed especially to meet high-performance requirements
- **A full range of inputs/outputs** (I/Os) in many specifications and voltages for speed and power trade-offs, including LVDS, HSTL, CML, 5-V I/Os and SSTL
- **TImeBuilder module library and methodology and analog cells** for easy system-level integration
- **Memory compilers**, including synthesizable RAMs for more area efficiency in small RAM configurations
- **Fully characterized libraries** for accurate modeling
- **Sprinkled gate array cells** and gate array blocks for fast metal-level design changes late in the design cycle

Proven Methodology

- **TImePilot™ design system**, which offers a multi-EDA-vendor strategy based on industry standards. This system, combined with enhancements in the design flow, simplifies and speeds the design process to help you achieve timing closure. An easy-to-use Design Sequencer steps you through the floorplanning process (built around a vendor-supplied floorplanner) and all of its associated design steps. See Table 8 on page 17 for a list of supported CAD tools.
- **Clock tree synthesis (CTS)** design flow that provides automatic synthesis of clock trees in physical design to meet designers' skew and insertion delay goals. The TI CTS flow supports more than 200 clock domains and clock gating for low power, and consistently achieves less than 50 ps clock skew.
- **Complete STA signoff methodology** enables comprehensive verification and minimizes gate-level simulation efforts at design hand-off. The Synopsys PrimeTime™-based signoff flow is supported with delay fault test generation capability using Sunrise™ tools.
- **SubChip™** design capabilities that support hierarchical design
- **VHDL, Verilog™, QuickSim II™ signoff flows** for reduced cycle time and improved accuracy
- **Synopsys Power Compiler™ support** for power reduction

Packaging for Value, Density and Performance

- **Package options** include thin quad flat pack (TQFP), MicroStar™ BGA, Plastic BGA, PowerPad, and Generic BGA. For more details, see Table 7 on page 13.

Core and I/O Macro Summary

This summary of core and I/O macros lists the selections available from the library.

Performance Equations

Every timing path through each GS30 family core and I/O macro is characterized at multiple voltage, temperature, process, input slew, and output load points. No global derating with respect to voltage, temperature, or process is used with the GS30 family. The characterized data coupled with nonlinear delay modeling allows SPICE-like accuracy for a large range of operating conditions.

Library Description

The GS30 family macro library has been optimized for use with synthesis and power optimization tools. Data from over 200 synthesized designs was analyzed to determine high-usage macros. In addition, a team of TI engineers worked closely with leading synthesis vendors to determine an optimal cell set. As a result, the GS30 family library features:

- A rich set of Boolean functions
- A wide variety of gates with inverting inputs
- Multiple-drive-strength gates
- Compact flip-flops and latches with Q only or QZ only
- Low-power combinational cells
- Minimized internal transistors in multistage macros
- Ultra-high-performance flip-flop and core macros
- Negative-edge flip-flops

A summary of core functions is shown in Table 1 on page 5.

Table 1: GS30 Family Core Macro Library Summary

Function	Number of macros
Datapath	13
AND/NAND/OR/NOR	87
Exclusive-OR/Exclusive-NOR	6
Inverters	12
Buffers	16
Boolean functions	61
Multiplexers	19
D-type flip-flops	58
Latches	23
Scan flip-flops/latches	94
PMT functions and JTAG	5
Clock generators	8
Clock-tree synthesis buffers	20
Analog functions	16
Special functions/miscellaneous	20
Total	**458**

Analog functions include an 8-bit analog-to-digital converter (pipeline), a 10-bit successive approximation register (SAR), an analog clock squarer, a 10-bit digital-to-analog converter, and a low frequency analog differential receiver/comparator. The special function macros include two electrically-readable die ID fuse array macros.

Gate Array Macros

The GS30 macro library also includes gate array cells for ECO as shown in Table 2 and gate array block cells as shown in Table 3.

Table 2: Gate-Array Cells for ECO

Function	Number of macros
AND	2
Buffers	8
D-type flip-flops	2
Exclusive-OR	1
Exclusive-NOR	2
Inverters	4
Latches	2
Multiplexers	2
NANDs	8
NORs	8
ORs	1
Scan flip-flops	2
Special functions/miscellaneous	3
Total	**45**

Table 3: Gate Array Block Cells

Function	Number of macros
AND	2
OR	1
Buffers	8
D-type flip-flops	2
Exclusive-OR	1
Exclusive-NOR	2
Inverters	4
Latches	2
Multiplexers	2
NANDs	8
NORs	8
Scan flip-flops	2
Clock-tree synthesis	15
Special functions/miscellaneous	3
Total	**60**

High-Performance Macros

High-speed applications, such as synchronous digital hierarchy (SDH) and asynchronous transfer mode (ATM), require correct alignment between the data and clock signals. To ensure this data synchronization, the GS30 family provides a set of macros to build systems capable of phase alignment and digital clock recovery. These high-performance macros include:

- DLP52 bit-phase aligner
- CK814A clock generator with integrated PLL (750 MHz)
- S8P20 serial-to-parallel converter
- DLP53 digital clock recovery

Key product features include operating range exceeding 750 MHz, tolerance to input jitter and pulse distortion up to 30 percent, data out retime to system clock, and high test coverage.

The phase alignment function (DLP52, clock macro, and serial-to-parallel converter) resynchronizes off-chip data to an on-chip clock when the relationship between the two is unknown or changing over time. The phase alignment function tracks this variation and maintains data integrity in the receiving function.

Other high-performance macros include:

- CML - up to 750 MHz
- GaAs - up to 750 MHz
- LVDS - up to 750 MHz

I/O Macros

GS30 provides 1.8, 2.5, 2.75, 3.3, and 5-V-tolerant I/Os. Low-voltage CMOS (LVCMOS), PCI, and differential buffers are available. Most output buffers are available in two noise performance options: low noise and ultra-low noise. To minimize system noise and power pins, select the lowest noise output that the application allows. Ultra-low-noise I/Os typically require only one-fifth the number of power pins that high-performance I/Os require.

The user creates a bidirectional macro by selecting inputs and outputs and combining the functions in the netlist. You can add pullup and pulldown macros to I/Os in the same manner. I/O macros include:

- LVCMOS, TTL, ATA
- CML, GaAs, TLV, LVDS, HSTL, SSTL, PCML, DPECL, SCSI
- Low noise, ultra-low noise, ultra-low power, failsafe, and 5 V-tolerant options
- 1/1mA - 12/24mA output drivers

Table 4: I/O Specifications

Type	Maximum Frequency	Signal Swing	Signal Type
TTL	200 MHz	3.3 V	single
LVCMOS	200 MHz	varies by V_{DDS}	single
CML	800 MHz	400 - 800 mV	differential
GaAs	800 MHz	600 - 800 mV	differential
TLV	250 MHz	800 mV	single & differential
LVDS	800 MHz	250 - 600 mV	differential
HSTL	400 MHz	1.5 V	single & differential
SSTL	125 MHz	2.5 V	single
PCI	66 MHz	3 V	single
PCML	400 MHz	400 mV	single & differential
DPECL	800 MHz	600 - 800 mV	differential
ATA-100	100 MHz	3.3 V	single
SCSI	20 MHz	2.85 V	single
SCSI	40MHz	400 mV	differential

Memories

GS30 supports synchronous single-port, two-port, dual-port, and three-port memory compilers and ROM, CAM and asynchronous two-port compilers. These dense memories let you specify the exact word and bit counts for each memory to meet the application's need. All memories can have synchronous operation, zero dc power and zero hold times.

Table 5: Memories Summary

Name	Description	Max Bits	Min Bits	Max Words	Max Bits/ Word
EY	2-port SRAM (1W/1R), asynchronous	32K	4	512K	256
MZ/MV	1-port Clocked RAM, density optimized, word write (MZ)/bit write (MV)	1Mbit	2K	32K	128
BW/BX	1-port CROM, via2, fast (BW)/dense (BX)	1Mbit	32	64K	64
BG	Dual-port CRAM, bit write (BG)	128K	64	4K	128
BT	1-port ROM, speed optimized, asynchrounous	1Mbit	64	64K	128
MR/BA	1-port CRAM, speed optimized, bit write (BA), word write (MR)	1Mbit	4K	64K	144
BR	1-port CRAM, multistrobe, page mode, low power, bit write	128K	1K	4K	64
MS/BS	2-port CRAM (1W/1R), small, word write (MS)/ bit write (BS)	9K	4	512	72
MG/BY	2-port register file (1W/1R), bit write (BY), synchronous write, asynchronous read	32K	2	512	256
MW/BL	1-port CRAM, area optimized, word write (MW)/bit write (BL)	128K	32	2K	128
BV/BU	1-port CROM, moat program, fast (BV)/dense (BU)	1Mbit	32	64K	64
MT/MU	3-port CRAM (1W/2R - MT, 2W/1R - MU)	144K	32	4K	128
BC	CAM compiler	128K	512	1K	128
MP	2-port CRAM (1W/1R), large, WE pin	128K	256	8K	128
MN	Dual-port CRAM	128K	64	4K	128
DA	Dual-port RAM, large bit count, very fast, bit write	256K	64	8K	32
DB	Dual-port RAM, simultaneous access capability, redundancy	128K	64	4K	32

Single-Port Clocked SRAM Compiler

The single-port clocked SRAM compiler creates speed-optimized RAM blocks based on user specifications. It creates data sheets, logic and layout models for simulation, testing, and layout based on the required number of words, number of bits per word, and the column multiplex factor. Contact the TI Customer Design Center for complete details.

Single-Port Clocked SRAM Compiler With Word-Write, Bit-Write and Multistrobe

In addition to the single-port clocked SRAM, TI also offers single-port memories with both word-write and bit-write capability. The bit-write capability enables you to update individual bits in the single port without changing the rest of the word. Multistrobe allows data to be read and/or written on up to three strobes.

Dual-Port Clocked SRAM Compiler

The dual-port clocked SRAM compiler creates area- and speed-optimized RAM based on user specifications. It creates data sheets, logic and layout models for simulation, testing, and layout based on the required number of words, number of bits per word, and the column multiplex factor.

Synthesizable Memories

For maximum flexibility, GS30 offers a number of memory options for use as “soft,” or synthesizable, memories. This compiler generates RTL (based on your specifications) as well as constraints for synthesis. Synopsys Design Compiler™ is then used to synthesize these memories to either flip-flop or latch-based implementation with support for multiple test methodologies. The compiler options are:

- 1-port CRAM area optimized
- 1-port CRAM speed optimized
- 2-port asynchronous RAM
- 2-port CRAM
- Dual-port RAM

TImeBuilder Modules

Texas Instruments has more than a decade of experience with complex integration and reuse for a wide variety of application-oriented markets. This experience gives TI a practical understanding of the challenges of integration; leadership in key integration areas gives TI the ability to offer unique solutions. TI is the world leader in digital signal processor (DSP) solutions, the world-leading supplier of data transmission peripherals, the world-leader in analog, and the world-leading supplier of ARM RISC processors (and also offers MIPS and NEC processors).

GS30 supports a wide variety of TImeBuilder modules for integrating complex functionality onto a single die. TImeBuilder gives you access to DSP technology from the company who invented it, and the ability to easily integrate it with a wide selection of core modules, including the ARM and MIPS Jade. Our DSPs, USB controller, DMA controller and bus bridges all contain logic to support easy access to the ARM Processor Interface (API).

Table 6: TImeBuilder Modules

Processors and Peripherals	
TMS320C54X Digital Signal Processor	ARM interrupt controller
ARM9TDMI	Multi-channel DMA controller
ARM7TDMI	Watchdog timer
MIPS Jade 32- and 64-bit	16-bit timer
NECv850	Clock manager
System bus controller	Configurable memory controller
System bus arbiter	Serial port— SPI/uWire
Multi-master arbiter	Peripheral bus controller
Communications	
UART	Reed Solomon encoder/decoder
Single-channel HDLC	1GHz low-jitter digital clock recovery
Multiple-channel HDLC	650 MHz bit-phase aligner
10/100 Ethernet MAC	622 Mb/s Serdes transceiver core
8-port 10/100 MAC with buffer memory	
Mixed Signal	
Analog-to-digital converters	1.25 GHz PLL
Digital-to-analog converters	
Interface	
GPIO	IEEE 1394 link core
I^2C master/slave	IrDA
IEEE 1284 host controller	PCI core
IEEE 1284 peripheral	USB generic function controller
	USB hub

Analog Cells

Analog cells include:

- Clock squarer with low power mode (dual gate only)
- Analog regulators
- Analog phase-locked loop, 50 - 500 MHz, zero-pin implementation
- Analog input and output switches

Packaging

GS30 supports the package types shown below.

Table 7: Supported Packages

Package	Pins	TI Suffix Code	Body Size (mm)	Lead Spacing (mm)
Thin Quad Flatpack	32	VF	7x 7x1.4	0.80
(TQFP)	48	PFB	7x 7x1.0	0.50
	52	PAH	10x10x1.0	0.65
	64	PAG	10x10x1.0	0.50
	80	PET	10x10x1.0	0.40
	80	PFC	12x12x1.0	0.50
	100	PZT	14x14x1.0	0.50
	128	PDT	14x14x1.0	0.40
	144	PGE	20x20x1.4	0.50
	176	PBL	20x20x1.4	0.40
	176	PGF	24x24x1.4	0.50
	208	PDV	24x24x1.4	0.50
	216	PDQ	24x24x1.4	0.40
	256	PEF	28x28x1.4	0.40
MicroStar Ball Grid	64	GGV	8x 8x0.9	0.80
Array (BGA)	80	GGM	10x10x0.9	0.80
	100	GGM	10x10x0.9	0.80
	100	GGT	11x11x0.9	0.80
	128	GGB	12x12x0.9	0.80
	144	GGU	12x12x0.9	0.80
	151	GHZ	10x10x0.9	0.50
	176	GGW	15x15x0.9	0.80
	196	GHC	15x15x0.9	1.00
	208	GGW	15x15x0.9	0.80
	240	GGW	15x15x0.9	0.80
	257	GHK	16x16x0.9	0.80
Plastic BGA	352	GFT	35x35x1.7	1.27
(PBGA)	388	GFW	35x35x1.7	1.27

Package	Pins	TI Suffix Code	Body Size (mm)	Lead Spacing (mm)
PowerPAD	64	PAP	10x10x1.0	0.50
	80	PFP	12x12x1.0	0.50
	100	PZP	14x14x1.0	0.50
	208	PYP	28x28x1.4	0.50
	216	RBP	24x24x1.4	0.40
	256	PFK	28x28x1.4	0.40
Generic BGA	352	GKN	27x27x1.7	1.00
Cavity Down	352	GLM	35x35x1.7	1.27
(GBGA_CD)	352	GPD	35x35x2.0	1.27
	432	GHQ	40x40x1.2	1.27
	432	GNP	40x40x1.9	1.27
	480	GNH	35x35x1.7	1.00
	520	GNP	40x40x1.9	1.27
	600	GNP	40x40x1.9	1.27
	672	GKP	40x40x1.6	1.27
	792	GKQ	40x40x1.4	1.00
	896	GKQ	40x40x1.4	1.00

Note: Body size is (length X widthX height) measured in millimeters. Body height is nominal thickness and does not include leads or balls. For overall package height, see individual package drawings.

TImePilot Design Flow and CAD Tools

Fully characterized libraries account for the effects of voltage, temperature, process, load, and input rise and fall times. Hierarchical design viewing and editing, floorplanning, and timing analysis allow the designer to achieve the accurate representation of silicon through forward annotation of timing to the layout software. This design approach, shown in Figure 1 on page 16, gives designers full advantage of the high-performance characteristics that submicron CMOS technology offers.

The TI approach to open CAD enables easy interaction with other systems. Signoff quality libraries for all supported simulators, test vector verification software, and design-rule-checking software enable the customer to verify the design completely before handoff to TI, significantly shortening design cycle time and eliminating correlation issues. Cadence Leapfrog, Synopsys VSS, and Model Technology ModelSim™ simulation libraries conform to IEEE Std. 1076.4-1995–VITAL 95. Tools and libraries in the TImePilot design environment are supported on both Sun™ and HP™ workstations.

TImePilot uses the Avant! Planet™ floorplanner. TI has added several features to the floorplanning flow, including a sequencer that steps users through all floorplanning-related tasks. Many traditional place-and-route features are now available in the floorplanner to help achieve first-pass timing convergence. Other features include:

- Gate-level floorplanning
- SubChips for reuse (see “Design Reuse” on page 18)
- Clock tree synthesis, a flexible, low power strategy for clock distribution (see “Clock Tree Synthesis (CTS)” on page 19
- Team design
- Path timing-driven placement
- Rules-driven placement
- Floorplan checks
- Wide-wire support for power management
- ECO

The primary aim of the design flow is to offer state-of-the art design tools and a highly productive environment to enable designers to achieve error-free designs in the shortest time that meets timing goals. The flow is also designed to comprehend the effects of deep submicron technology by accurately estimating interconnection lengths and resistance-capacitance (RC) effects, and by providing close correlation between floorplanning and synthesis and pre- to postlayout delays.

Figure 1: Design Flow Overview

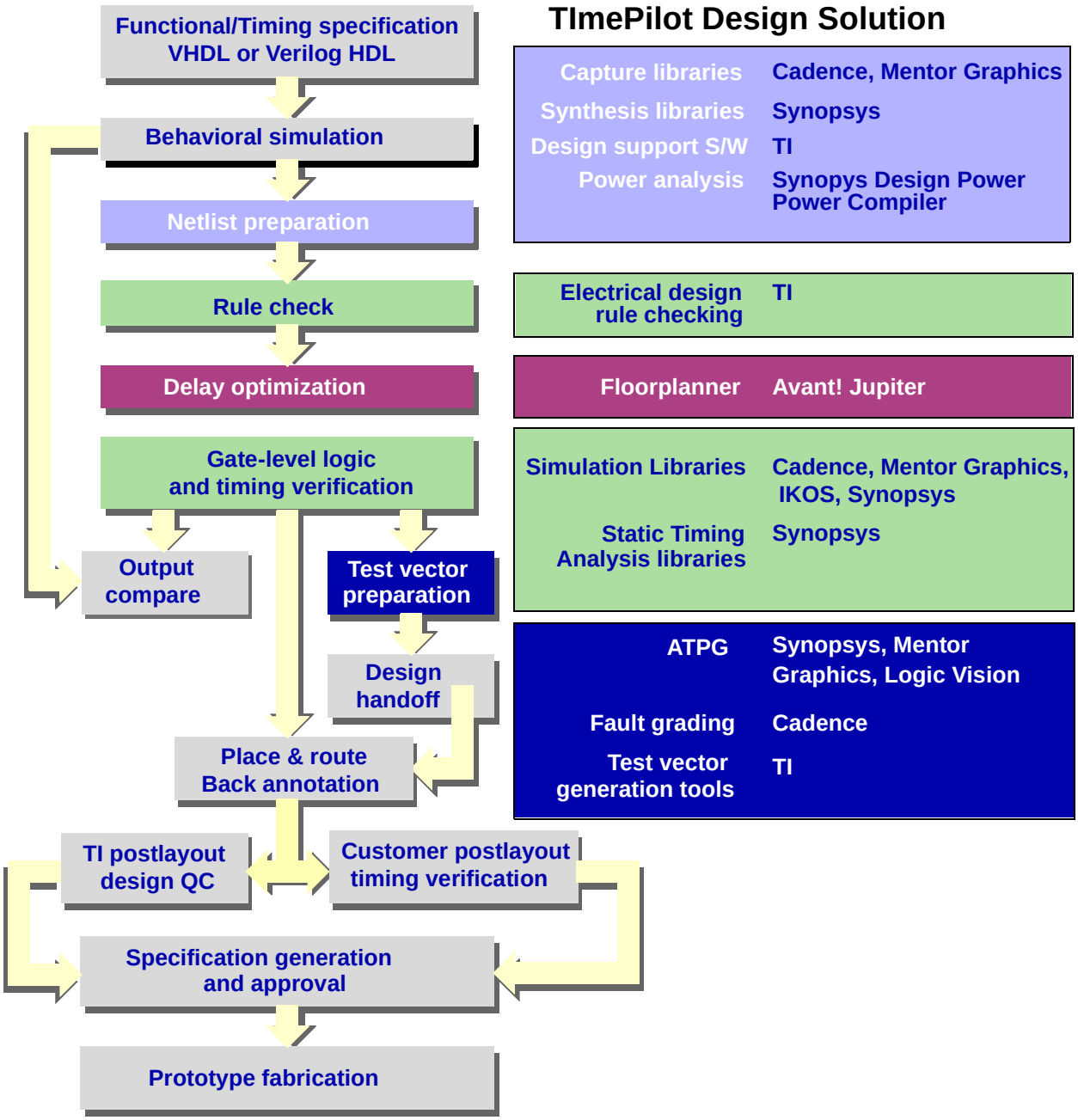


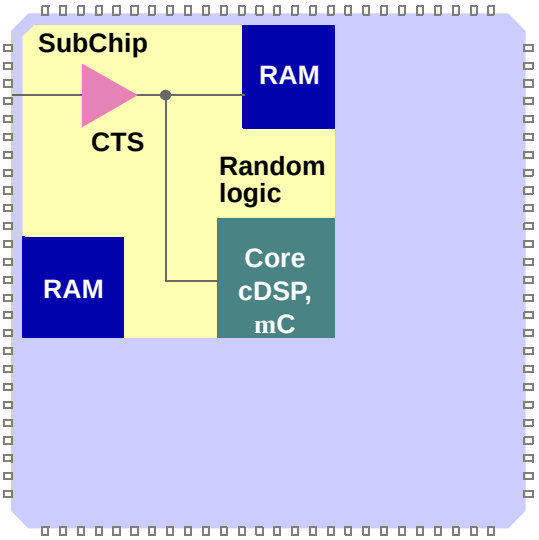
Table 8: TImePilot CAD Tool Support

Platform/Tool	Options
Hardware platforms and operating systems	Sun ULTRAsparc™ platforms (Solaris 7, 64-bit) HP9000 (HP-UX™ 11, 10.20)
Architectural synthesis	Synopsys Behavioral Compiler
Limited synthesis	Synopsys ECO Compiler
Logic synthesis	Synopsys DC Professional/Expert
Formal verification	Chrysalis Design VERIFYer™, Synopsys Formality™
RAM compilation	Web-based ACE toolkit
Floorplanning	Avant! Jupiter™
Simulation	Mentor Graphics ModelSim™, Cadence Verilog-XL™, Cadence NC-Verilog, NC-VHDL, IKOS Voyager NSIM CS/CSX, FS™
Datapath	Synopsys DesignWare™
Static Timing Analysis (STA) signoff	Synopsys Primetime™
Logic design rule checking	Detector™
Test vector verification	SimOut™
Test vector generation	TDLGEN™
Test vector rule checking	TDLCHKR™
Automatic place and route	Avant! Apollo™
Test synthesis and ATPG	Synopsys TetraMAX™, Mentor Graphics FastScan™, FlexText™, DFT Advisor™, LogicVision MEMBIST II
Fault grading	Cadence Verifault™
Evaluation	Paragon™
Power	Synopsys DesignPower™, Power Compiler™

Design Reuse

A SubChip is a design module that undergoes placement and routing as a discrete block that can be reused as a component of a larger design, as illustrated in Figure 9. When reused, the placement and routing of the SubChip stay the same so that its previous functionality and timing are preserved. This capability allows for independent optimization of design modules and provides increased designer productivity through module reuse. SubChips can be used on multiple designs.

Figure 2: SubChip Components



A SubChip can include:

- TImeBuilder modules
- Clock tree synthesis (CTS)
- Random logic
- Cores
- Analog cells
- Other SubChips

Some benefits of SubChips include:

- They are user- or TI-defined functions with known postlayout timing, area, and power that can be used in prelayout chip designs and simulations.
- Multiple instances can be placed in a design and will have identical timing.
- SubChips can be used by multiple designs.
- Complex designs can be implemented and/or easily modified by the designer without the difficult modeling or characterization associated with a complex hard macro design.

Clock Tree Synthesis (CTS)

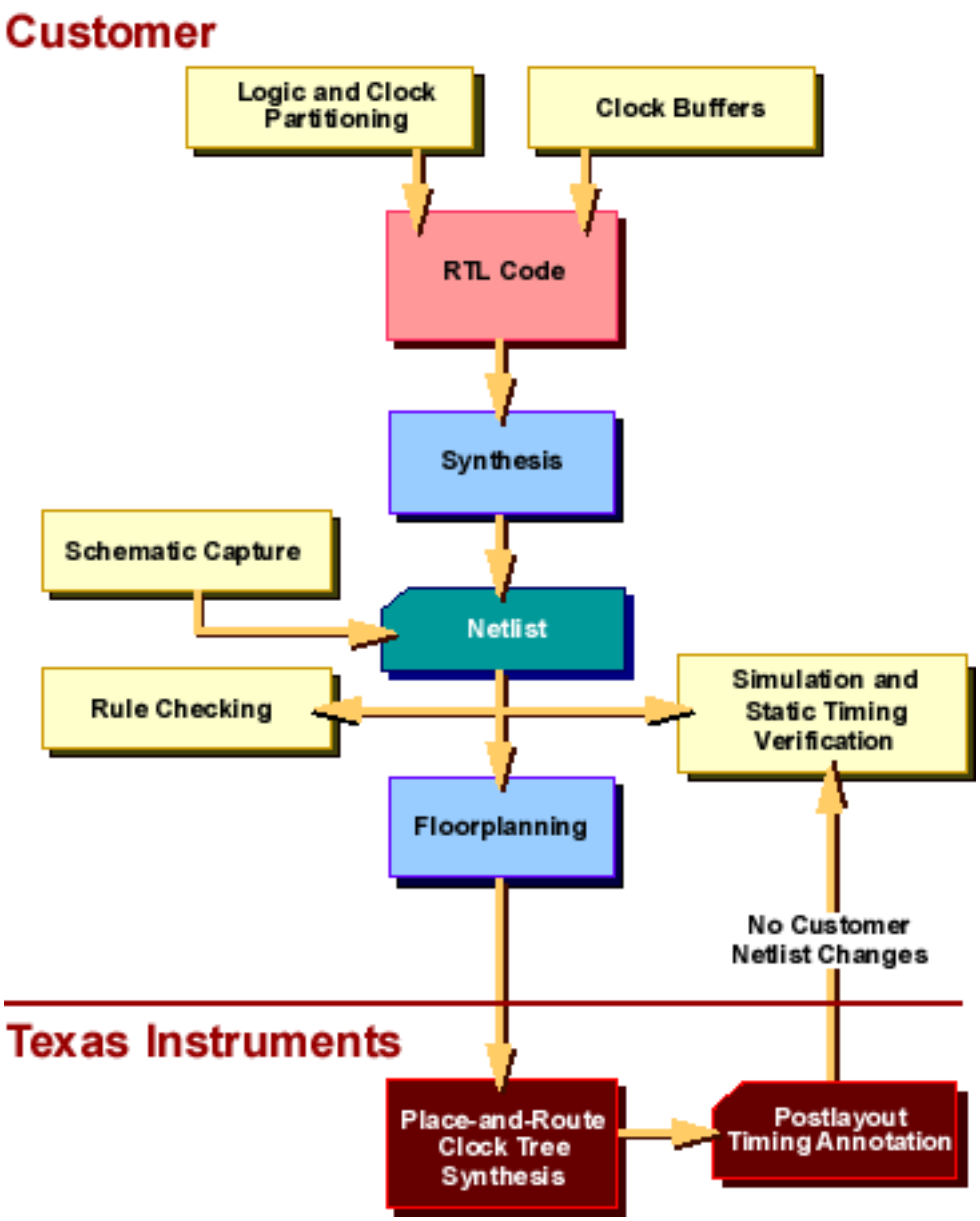
Clock tree synthesis (CTS), shown in Figure 3 on page 20, is the primary method of clock distribution for GS30 family standard cell designs. The key capabilities of the CTS flow are:

- Insertion delay, skew, and power management
- Capability to handle more than 200 clocks
- Gated clock support for lower power
- Ability to balance multiple clocks together
- Easy to use in design flow
- Good prelayout to postlayout correlation
- Layout-centered approach for lowest skew and delay
- No customer netlist modifications
- Balancing into a SubChip
- One CTS macro
- Automatic clock buffer selection

With clock tree synthesis, the customer instantiates a single CTS buffer per clock tree. The CTS buffer is expanded at layout into a multistage clock tree. The configuration of the clock tree is optimized for size, delay, and power in accordance with the requirements of the application, and the clock tree is placed according to the location of its loads.

The postlayout timing of the clock tree is back annotated to the customer's original netlist. The insertion delay is annotated as CTS buffer gate delay, and the clock skew is annotated to the input pin of the individual loads. Clock tree balancing and tuning are accomplished automatically by insertion of tuning buffers and loads at the root of the clock tree.

Figure 3: Clock Tree Synthesis Flow



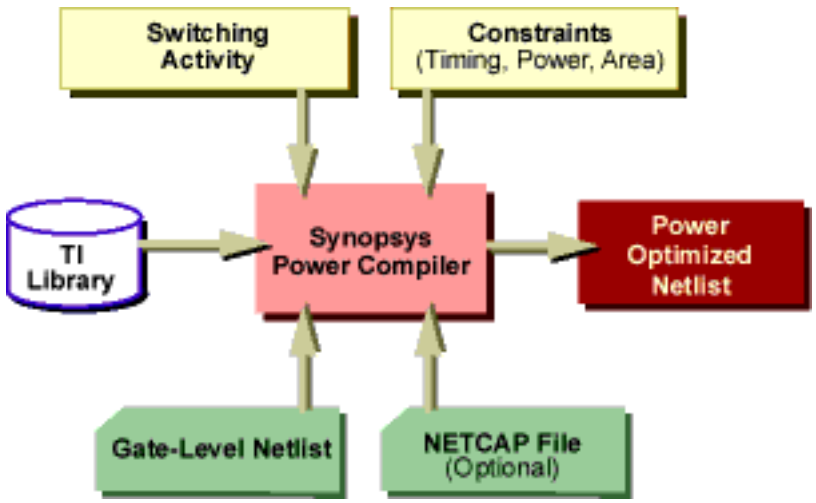
Power Analysis and Optimization

To achieve a low system power, the GS30 family provides:

- Support for Synopsys Power Compiler and DesignPower
- 1.1-V, 1.4-V, and 1.8-V libraries
- Core macros optimized for low power
- Optimized library for efficient synthesis, lowering net count and gate count to reduce power
- Full support for gated clock methodologies, which reduce switching activity through clock tree synthesis and clock balancing capabilities.
- Low-power and ultra-low-power I/Os
- TImeBuilder modules that draw zero dc current

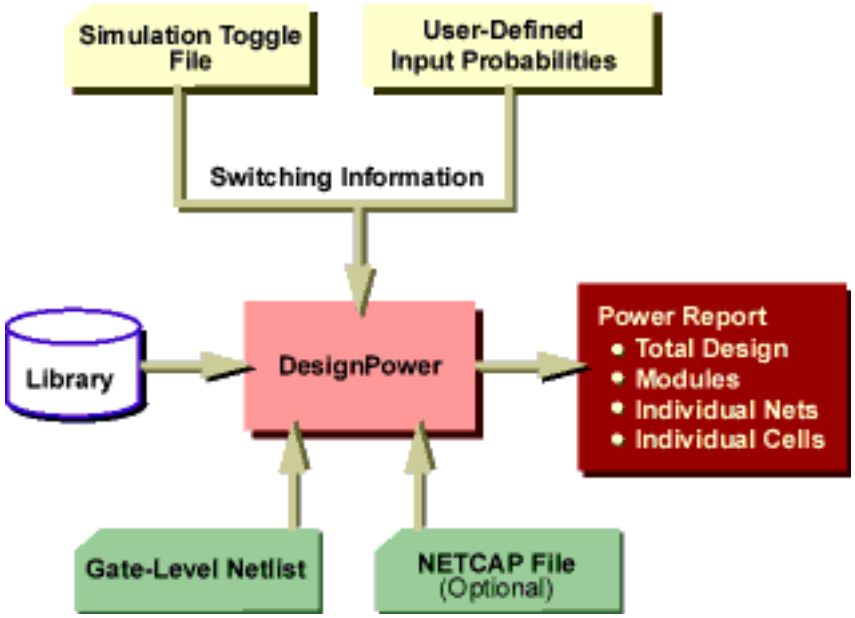
To optimize gate-level power, the GS30 family fully supports the Synopsys power optimization tool, Power Compiler. A design flow using Power Compiler is shown in Figure 3.

Figure 4: Design Flow Using Power Compiler



To analyze how much power is actually dissipated in a specific netlist, the GS30 family supports the Synopsys power analysis tool, DesignPower. A design flow using DesignPower is shown in Figure 4.

Figure 5: Power Estimation Using Synopsys DesignPower



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