High VOLT Interactive

Where power supply design meets collaboration

PCB layout for SMPS

Created by: Colin Gillmor
Presented by: Brian King

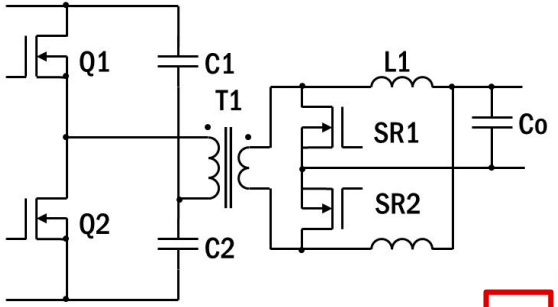
What will I get out of this session?

- The purpose of this session is to introduce the concepts needed to successfully layout a PCB for a switched mode power supply
- This presentation is relevant to all SMPS PCB layouts, from 1W to 10kW

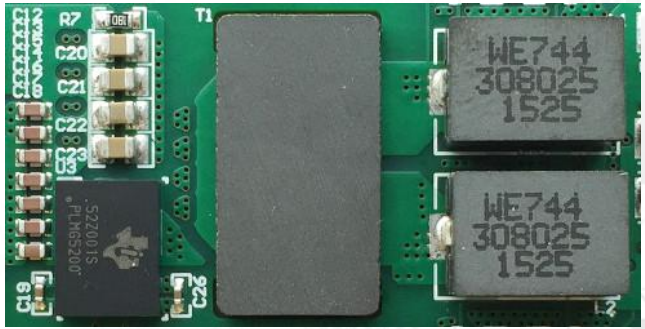
- Part numbers mentioned:
  - UCC28180
  - UCC28950
  - UCC28742
  - UCC28710
  - UCC24612
  - UCC24610
- Reference designs mentioned:
  - TIDA- 00443

Why is layout important?

- The best controller in the world cannot work well if embedded in a poor layout
- PCB layout for SMPS is extremely complicated!
- Same principles govern low and high power layouts
  - The difficulty is how to apply the principles in practice
- The PCB is often the most complex component in a design



How to translate a schematic into working hardware

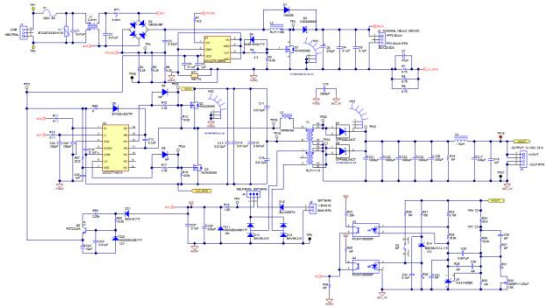


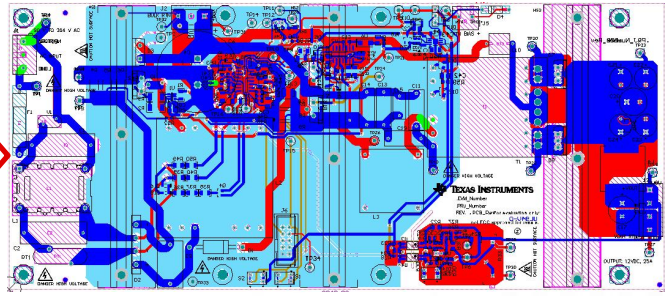
What are concerns for a power supply PCB layout?

- Safety
- EMI
- Parasitic inductance
- Parasitic capacitance
- Parasitic resistance
- Thermal performance
- High dv/dt
- High di/dt
- Grounding
- Noise

Agenda

- The schematic
- Parasitics
  - Resistance
  - Inductance
  - Capacitance
- EMI & safety
- Grounding & signal routing
- Thermal management
- PCB layout example
- Summary





Question #1: How involved are you in the design of the PCB for a SMPS?

A) I do the entire layout myself.

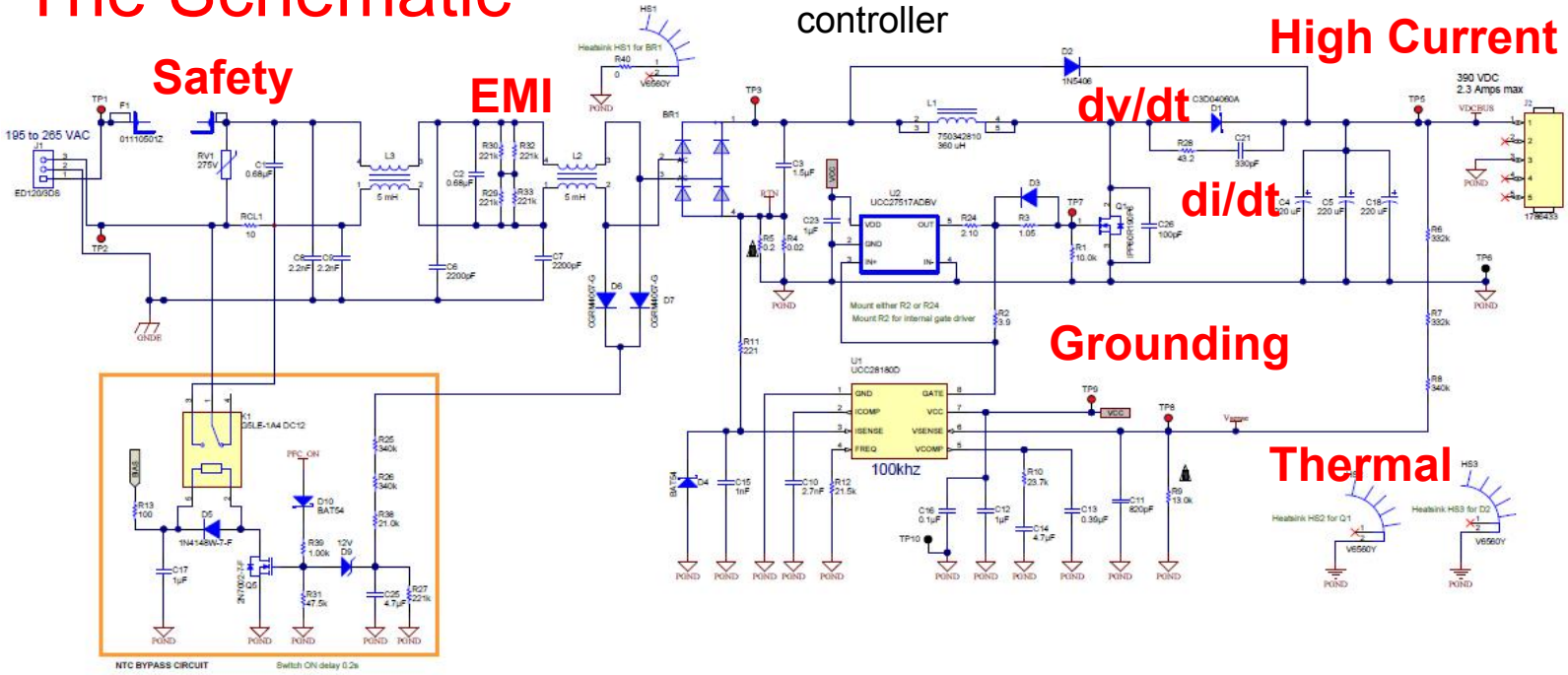
B) I work closely with a layout technician to make sure the layout is done correctly.

C) I create the schematic and let somebody else worry about the layout.

D) It’s not a key part of my job.

The Schematic

TIDA-00443 using UCC28180 PFC controller



Understand the circuit, including the parasitic components!

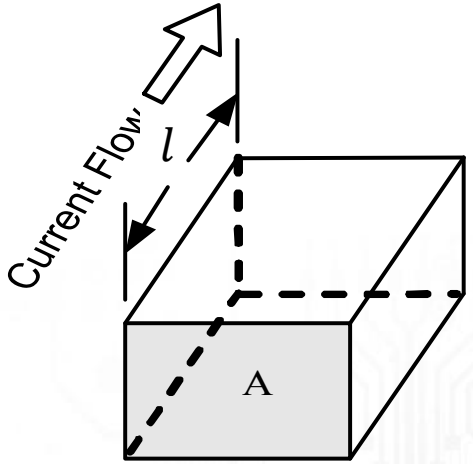
Parasitic resistance

You mean copper is not a perfect conductor?

Material	mW-cm	mW-in
Copper	1.70	0.67
Gold	2.2	0.87
Lead	22.0	8.66
Silver	1.5	0.59
Silver (plated)	1.8	0.71
Tin -lead	15	5.91
Tin (plated)	11	4.33

$$R = \frac{\rho \cdot l}{A}$$

$\rho = resistivity$



ρ(Cu) = 0.67 mΩ-in at 25°C

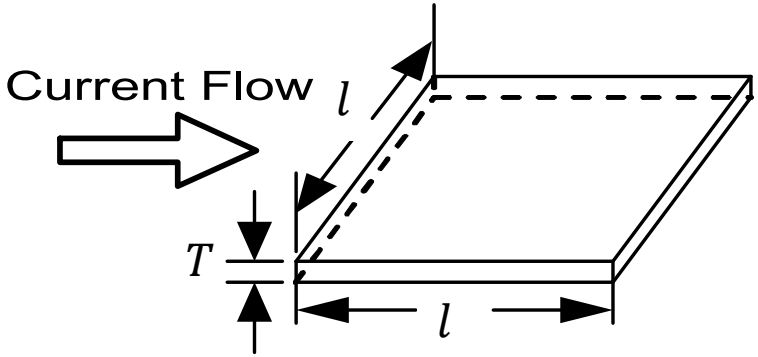
$TCR_{Cu} \approx 4000\ ^{ppm}/_{°C}$ (+40% for 100°C $rise$)

Impacts:

- **Regulation**
- **Efficiency**
- **Temperature rise**

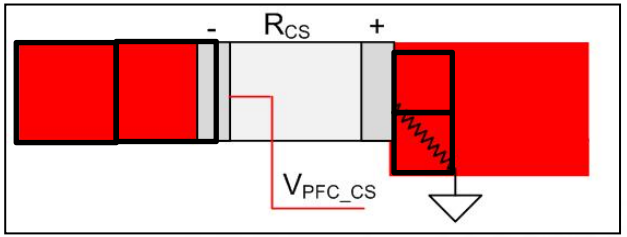
Parasitic resistance

Counting squares



$$R = \frac{\rho \cdot l}{T \cdot l} = \frac{\rho}{T}$$

Assume 1 oz. Cu



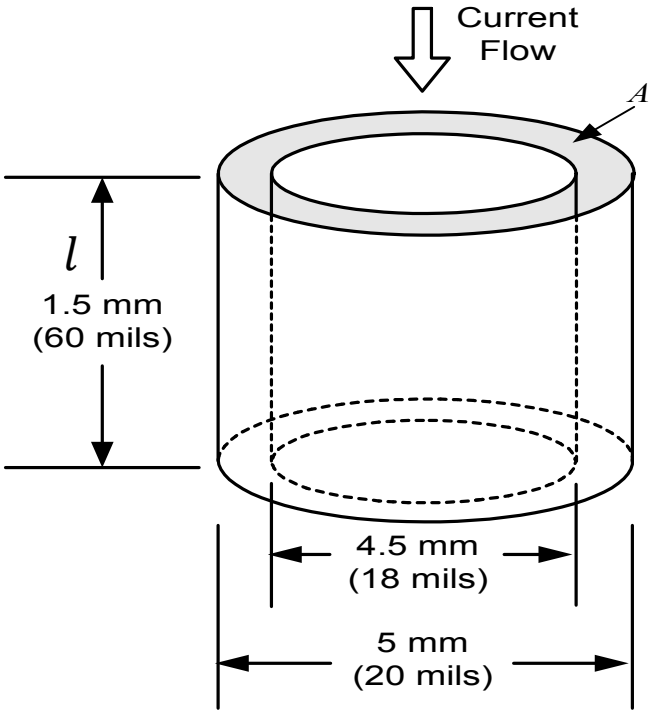
$2\ series\ squares\ = \sim 1.0\ m\Omega$

$2\ parallel\ squares\ = \sim 0.25\ m\Omega$

Copper Weight (Oz.)	Thickness (µm/mils)	mΩ per square (25°C)	mΩ per square (125°C)
1/2	17.5/0.7	1	1.4
1	35/1.4	0.5	0.7
2	70/2.8	0.25	0.35

Parasitic resistance

Vias have resistance too



Typical rule of thumb is 1 A to 3 A per via

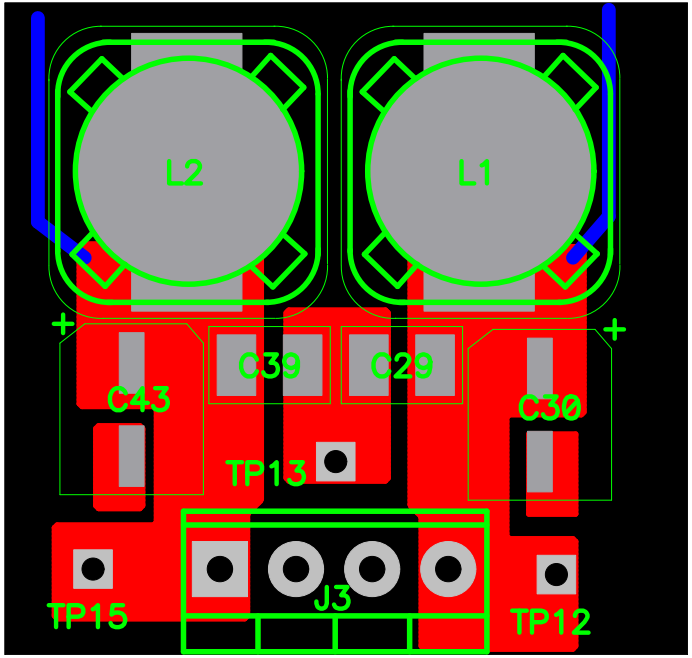
$$R = \frac{\rho \cdot l}{A}$$

$$R = \frac{\rho \cdot l}{\pi \cdot ({r_o}^2 - {r_i}^2)}$$

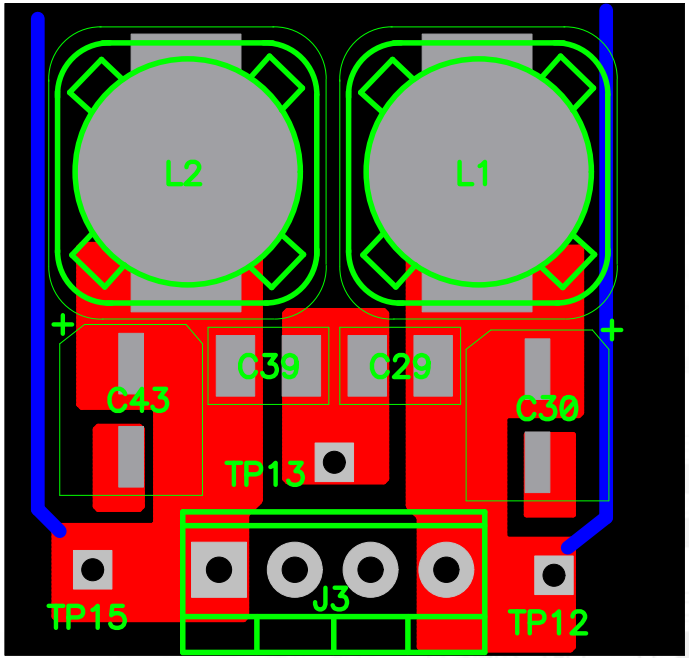
$$R = \frac{(0.67\ \mu\Omega \cdot in) \cdot (0.06\ in)}{\pi \cdot [(0.01\ in)^2 - (0.009\ in)^2]} = 0.67\ \text{m}\Omega$$

Parasitic resistance

Poor sense location



Sensing at output connector



How many mΩ between L2 and J3?

Identifying high di/dt

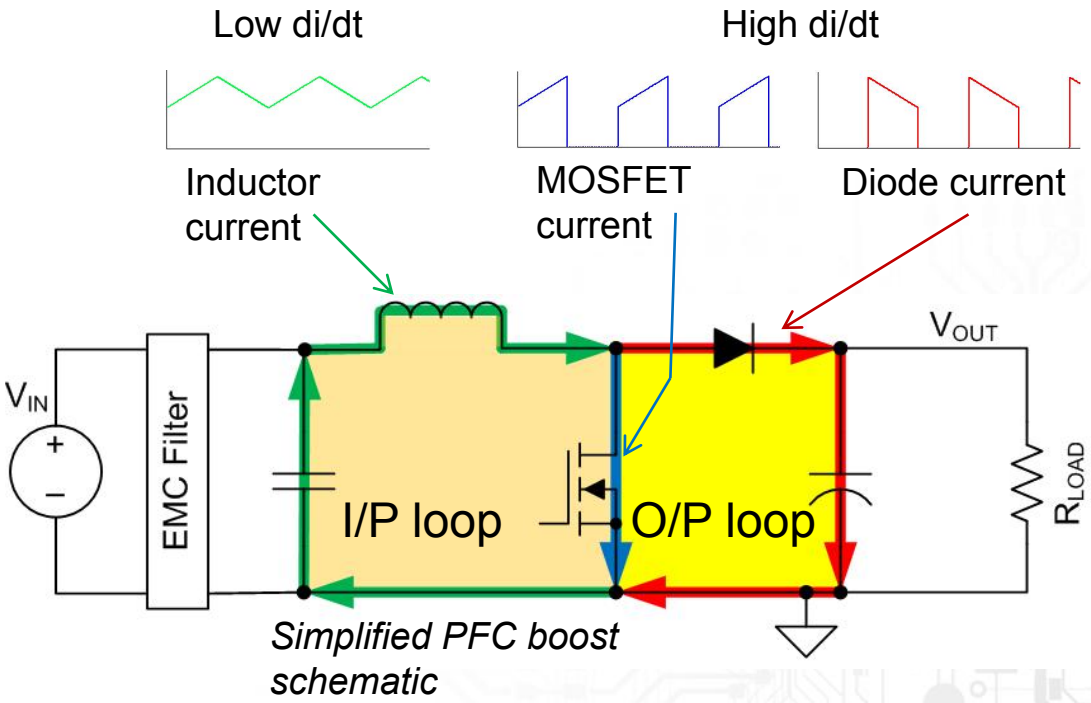
Switched current loops

O/P loop (**blue**/**red**)

- Inductor current alternates between MOSFET and diode paths
- Pulsating currents
- Stray inductance will cause voltage spikes

I/P loop (**green**)

- di/dt rates much lower
- Stray inductance is less critical
- C_{IN} provides local low impedance source



Simplified PFC boost schematic

Identifying high di/dt

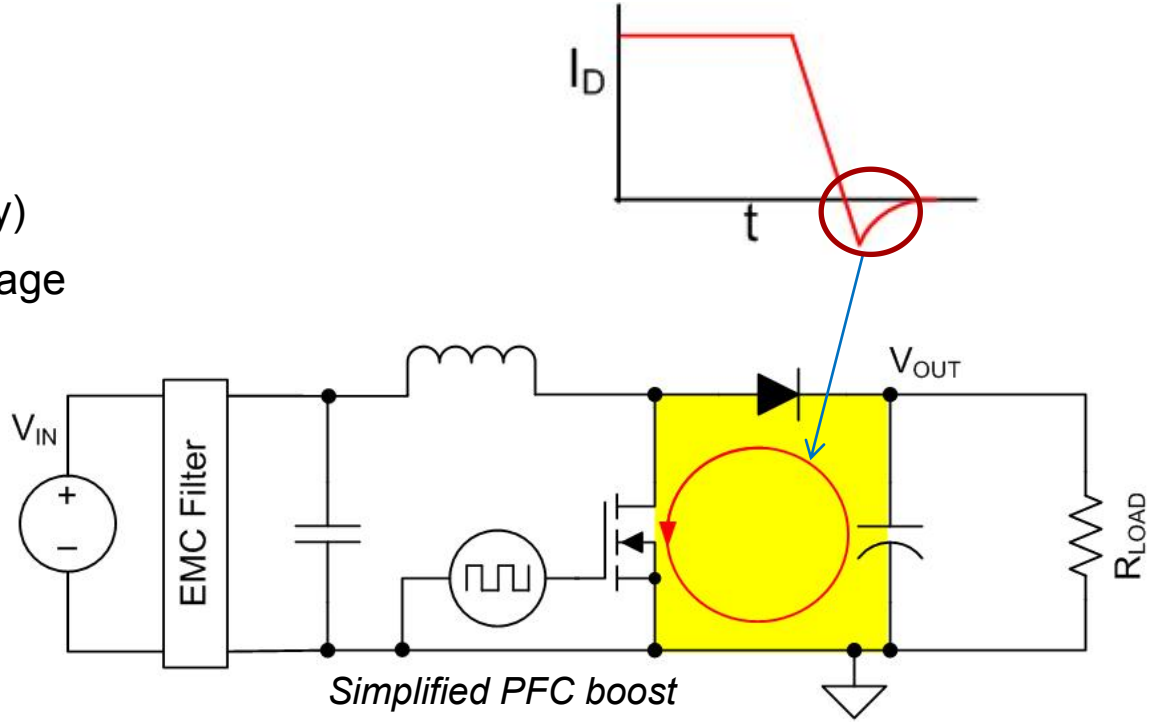
Reverse recovery

Occurs when:

- MOSFET turns ON during CCM operation (nearly every topology)
- Stray inductance will cause voltage spikes

Mitigation:

- Minimize loop inductance
- Use low Q_{RR} rectifiers –
  - SiC for high V_{OUT}
  - Schottky or ultra-fast diodes
  - Sync rectifiers with low Q_{RR}



Simplified PFC boost schematic

Identifying high di/dt

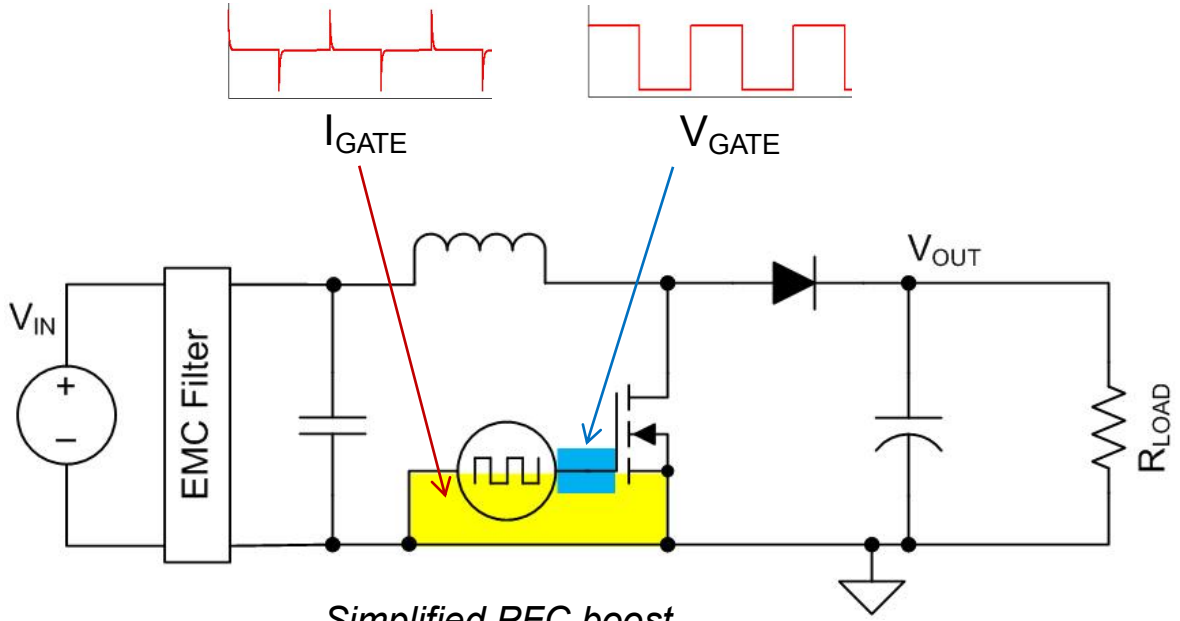
Gate drives

High di/dt in loop (**yellow**)

- Stray inductance:
  - Limits drive current
  - Can cause ringing
- Minimize loop inductance

High dv/dt on gate (**blue**)

- Can couple to noise-sensitive nodes
- Minimize capacitance

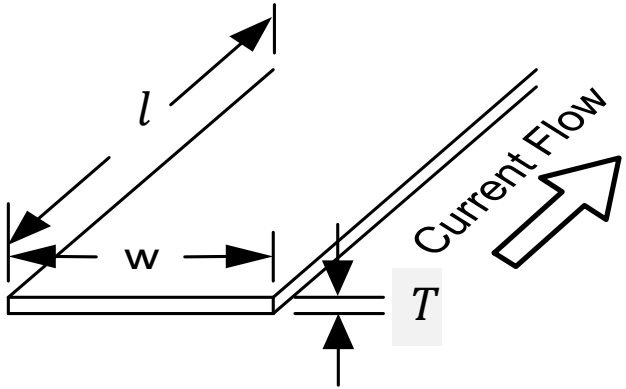


Simplified PFC boost schematic

Parasitic inductance

Self inductance of PWB traces

- Due to the natural logarithmic relationship, large changes in conductor width have minimal impact on inductance



$$L = 2 \cdot l \cdot \left(ln\left(\frac{l}{T+W}\right) + \frac{1}{2} \right) nH/_{cm}$$

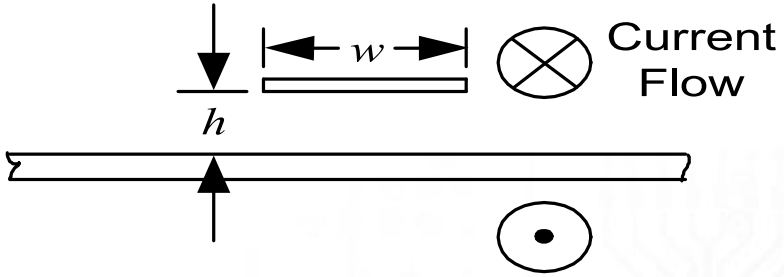
$$L = 5 \cdot l \cdot \left(ln\left(\frac{l}{T+W}\right) + \frac{1}{2} \right) nH/_{in}$$

W (mm/in)	T(mm/in)	Inductance (nH/cm or nH/in)
0.25/0.01	0.07/0.0028	10/24
2.5/0.1	0.07/0.0028	6/14
12.5/0.5	0.07/0.0028	2/6

Parasitic inductance

PWB traces over ground planes

- Substantial inductance reduction
- Inductance inversely proportional to width

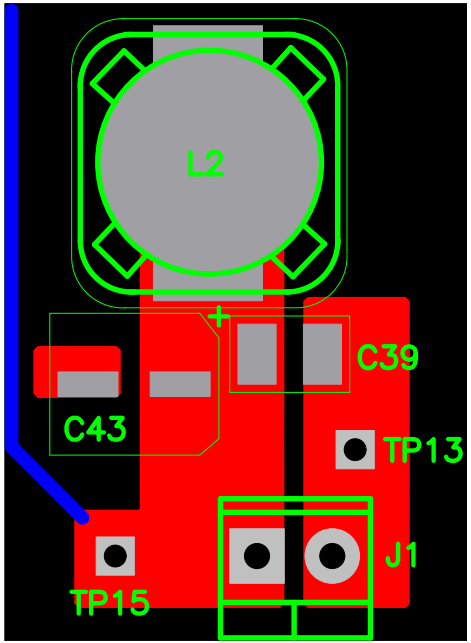


$$L = \frac{2 \cdot h \cdot l}{w} nH/cm \qquad L = \frac{5 \cdot h \cdot l}{w} nH/in$$

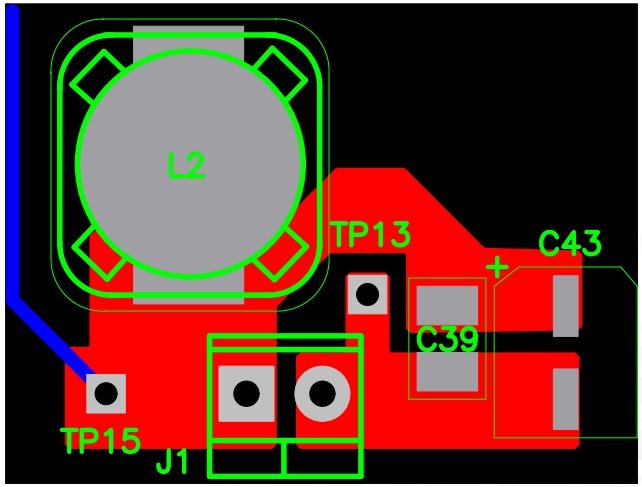
Metric			English		
h (cm)	w (cm)	Inductance (nH/cm)	h (in)	w (in)	Inductance (nH/in)
0.25	2.5	0.2	0.01	0.1	0.5
1.5	2.5	1.2	0.06	0.1	3.0

Parasitic inductance

Low series inductance



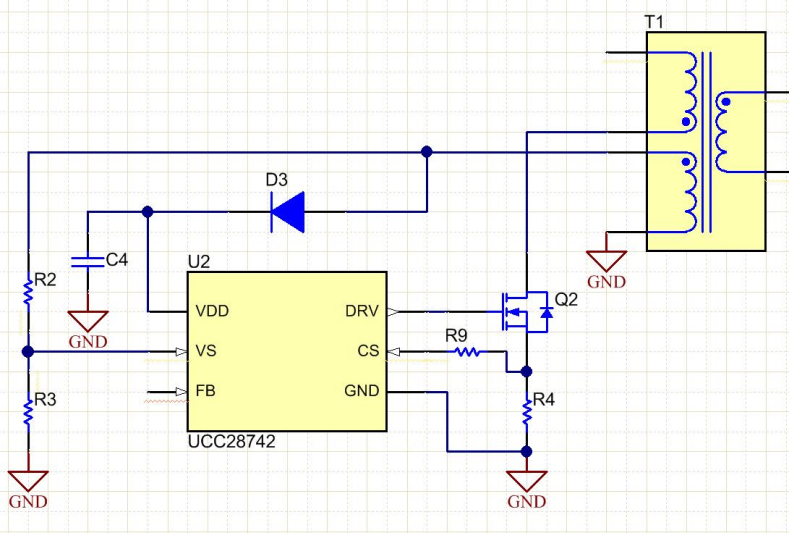
High series inductance

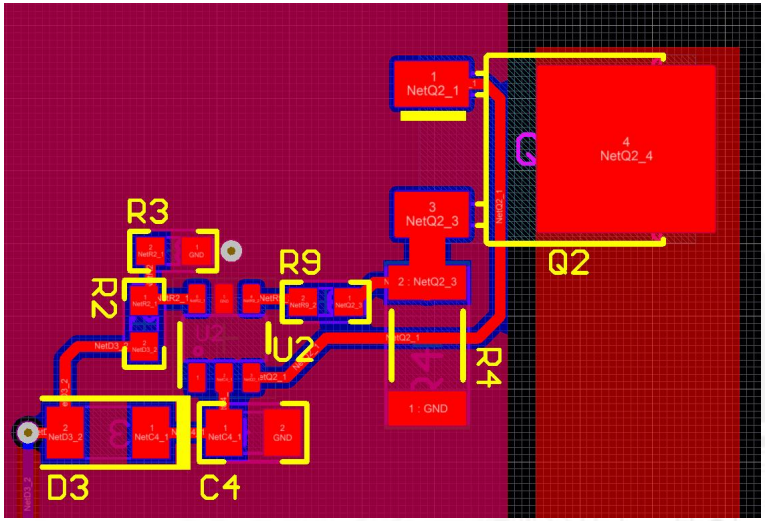


How much inductance in series with C39? (length ~ 1 in)

Parasitic inductance

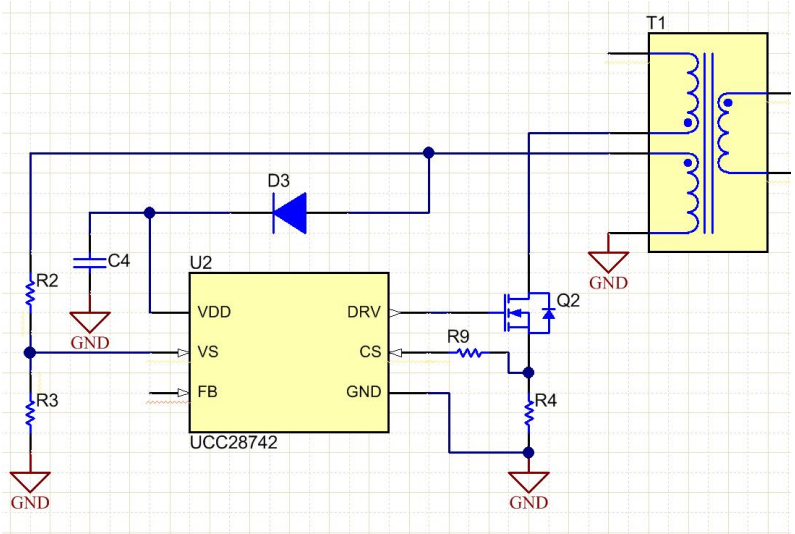
How to improve the gate drive path?

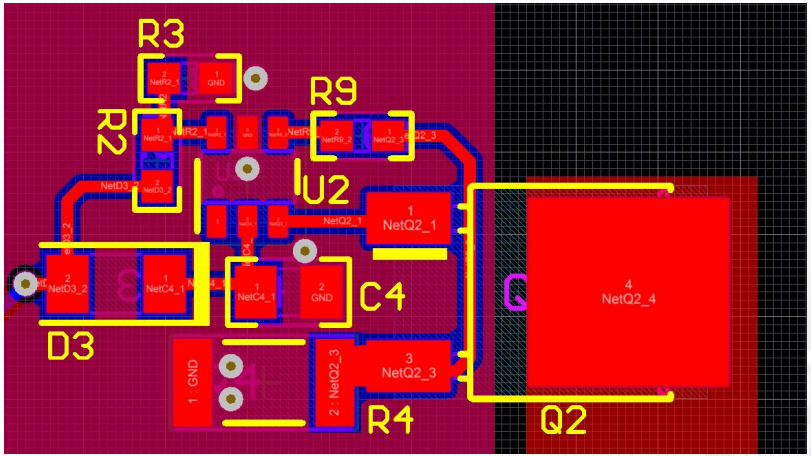




Parasitic inductance

Improved gate drive layout





Identifying high dv/dt

Switched nodes

High dv/dt at switched node (blue):

- Switched between 0V and V_{OUT}
- Stray capacitance can cause:
  - EMI problems
  - Noise injected to internal circuits
  - Reduced efficiency

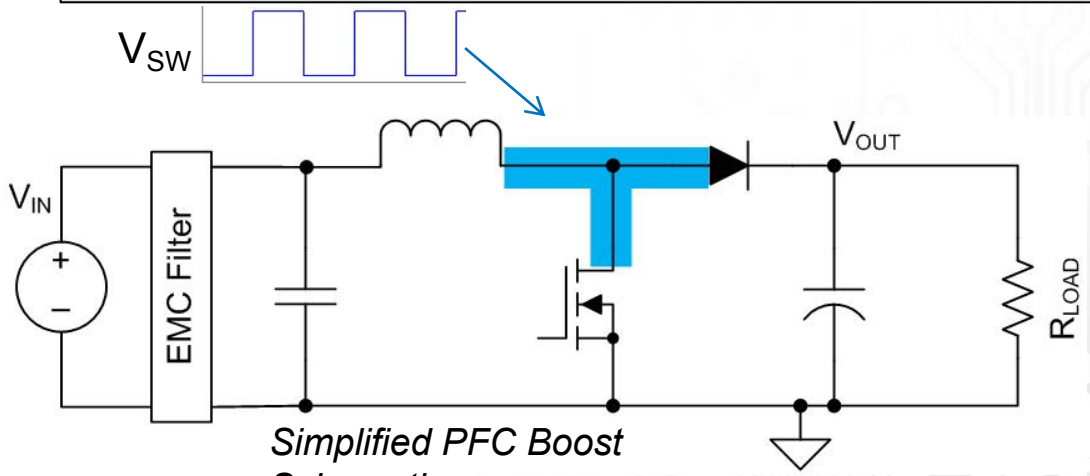
Mitigation:

- Minimize V_{SW} surface area
- Keep sensitive etch and components away from V_{SW}
- Ground the heatsink!

The switched node paradox

Increased surface area → Lower resistance, Lower inductance, Better cooling

Decreased surface area → Lower capacitance

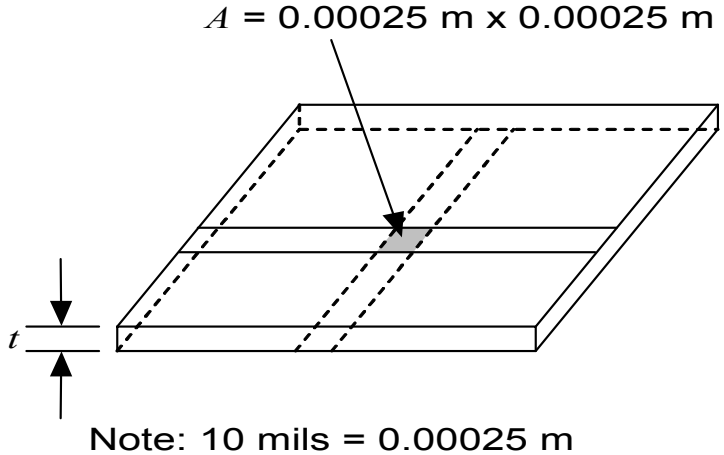


Simplified PFC Boost Schematic

Parasitic capacitance

Sample capacitance calculation

Consider two 10 mil traces crossing with 10 mil PWB thickness



Note: 10 mils = 0.00025 m

$$C = \frac{\varepsilon_r \cdot \varepsilon_0 \cdot A}{t}$$

$$C = \frac{5 \cdot \left(8.85 \times 10^{-12}\ {}^{F}/_{m}\right) \cdot (0.25\ mm)^2}{2.5\ mm}$$

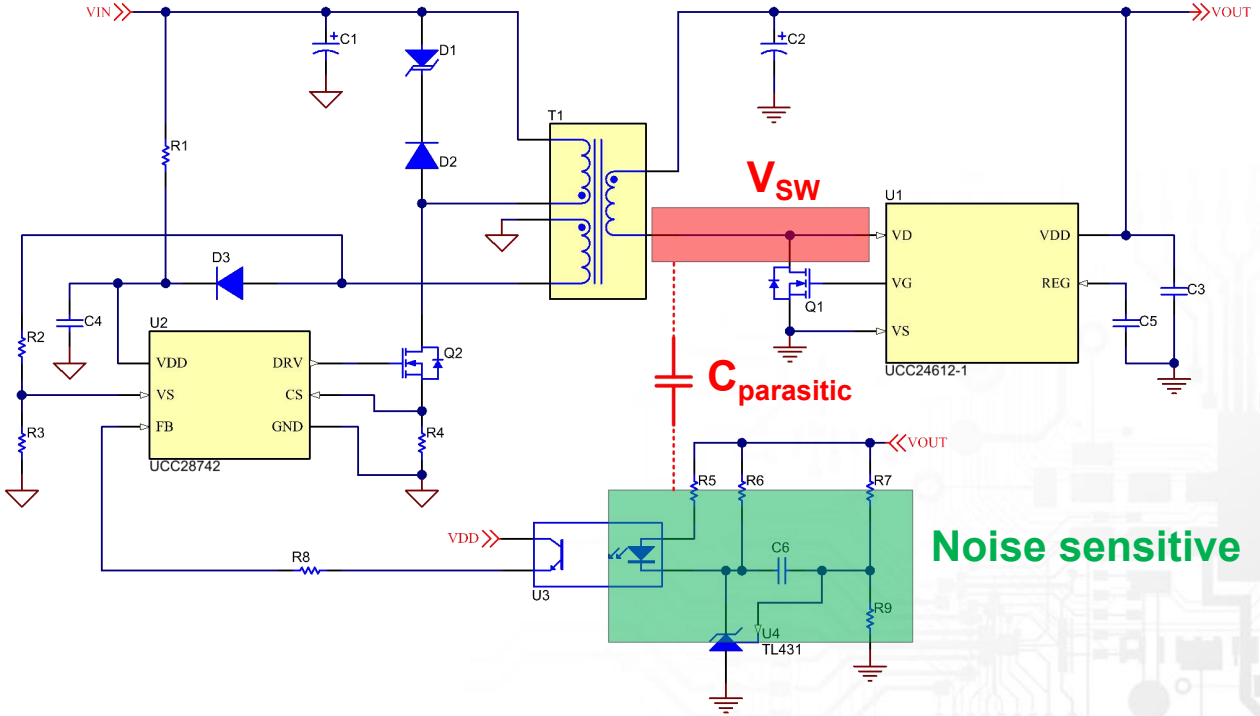
$$C = 0.01\ pF$$

Not much capacitance but consider the area of all components connected to the summing node

Parasitic capacitance

Chaos created by noise injection

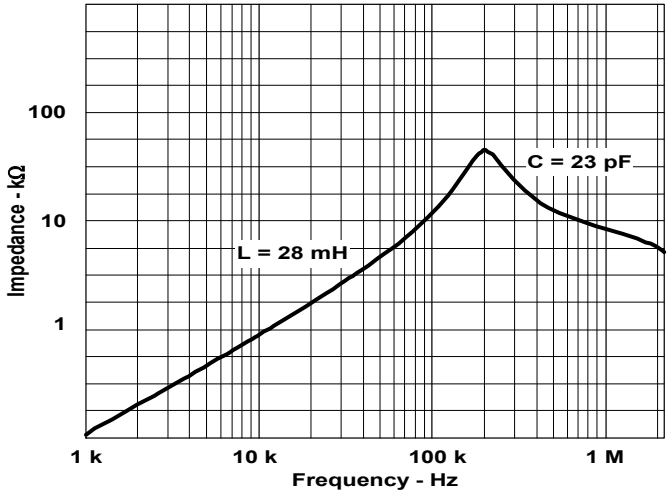
Ten 0.05 x 0.02 in² pads can increase parasitic capacitance to 2 pF

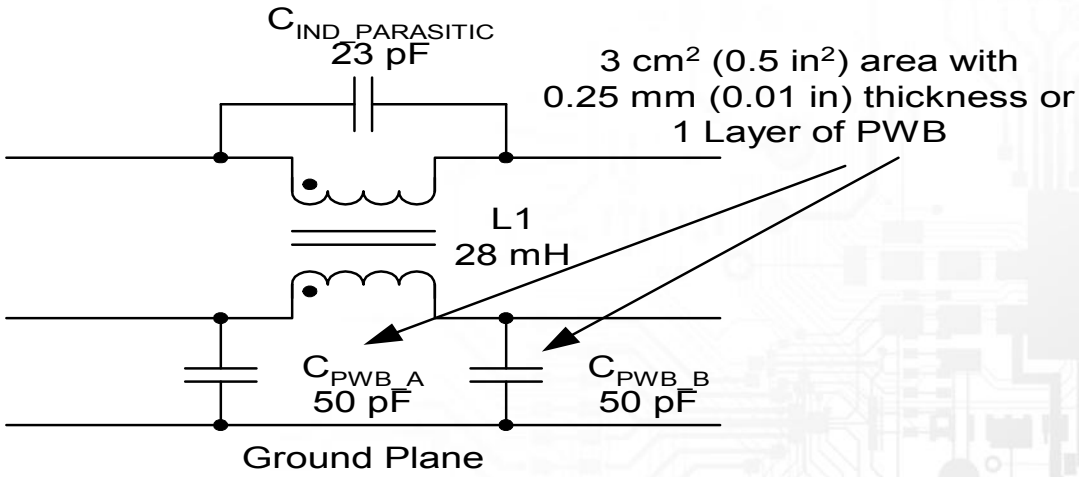


Parasitic capacitance

At high frequency inductors turn into capacitors

Don’t route planes under common mode inductors!

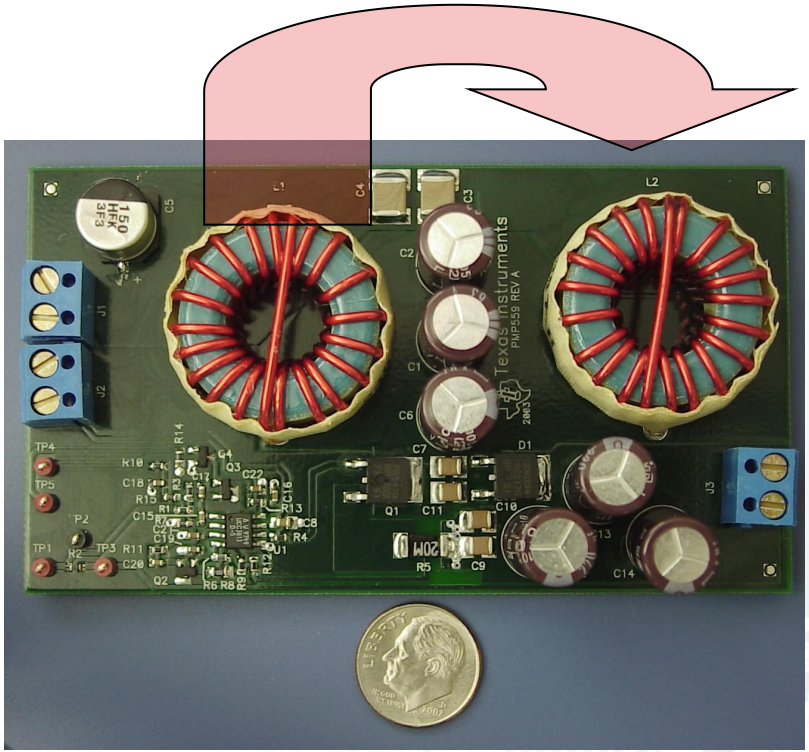




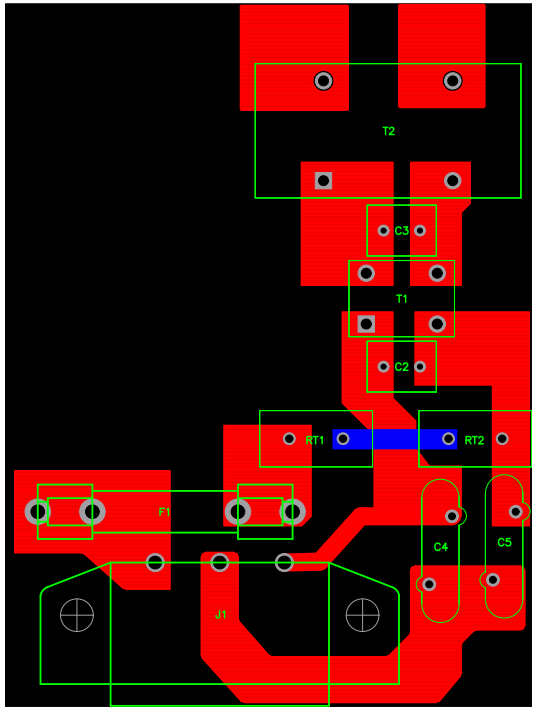
EMI considerations

Magnetic coupling

- External fields couple between inductors
- Can cause EMI issues
- Consider alternate orientation of second inductor to minimize coupling
- Use core shapes that provide better shielding



EMI considerations



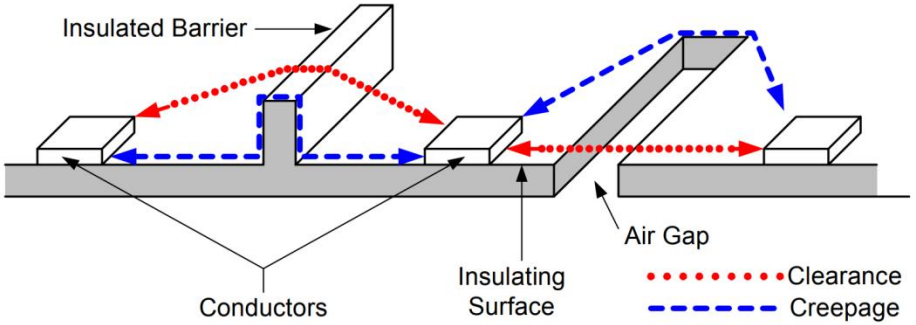
Input filter layout

- Place components away from noise sources
- Common mode inductor T2 input pins do not cross output pins
- No GND plane under EMI filter
- Wide, short etch used to minimize losses
- Wide spacing between etches meets HV requirements and minimizes coupling capacitance

Safety

Separate hazardous voltages from user accessible points

- Consult your safety expert!
- Create a very clear channel between primary and secondary
- Spacing depends on:
  - Type of insulation
  - Pollution degree
  - AC mains voltage
  - Working voltage
- Types of insulation:
  - Functional
  - Basic/supplementary
  - Reinforced



Working Voltage		AC Mains < 150 V (Transient to 1500 V) Pollution levels 1 and 2			AC Mains < 300 V (Transient to 2500 V) (Pollution levels 1 and 2)		
Peak dc V	rms V	F	B/S	R	F	B/S	R
71	50	0.4	1.0	2.0	1.0	2.0	4.0
210	150	0.5	1.0	2.0	1.4	2.0	4.0
420	300	1.5	2.0	4.0	1.5	2.0	4.0
840	600	3.0	3.2	6.4	3.0	3.2	6.4

Partial Clearance Dimensions (mm) from UL60950-1, Section 2.10.3, Table 2H

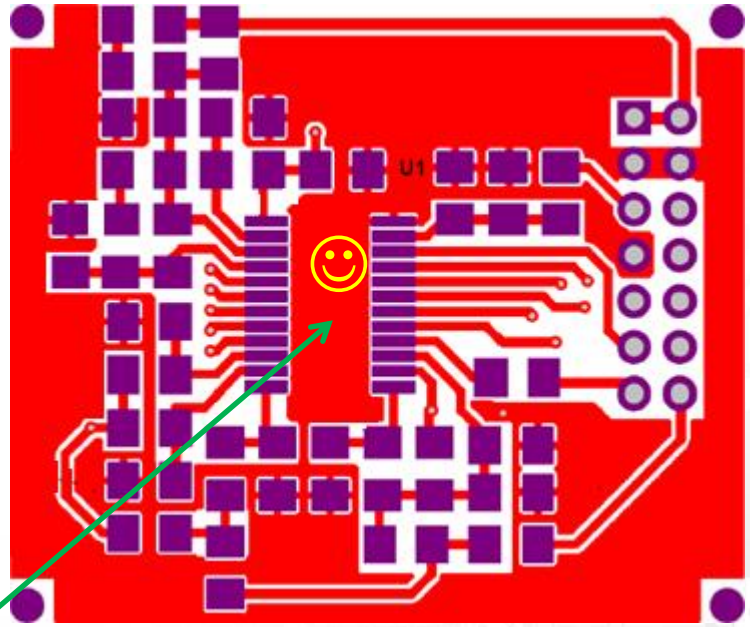
Ground planes

Ground planes provide:

- Low resistance return paths
- Low inductance return paths
- Lateral heat spreading across board

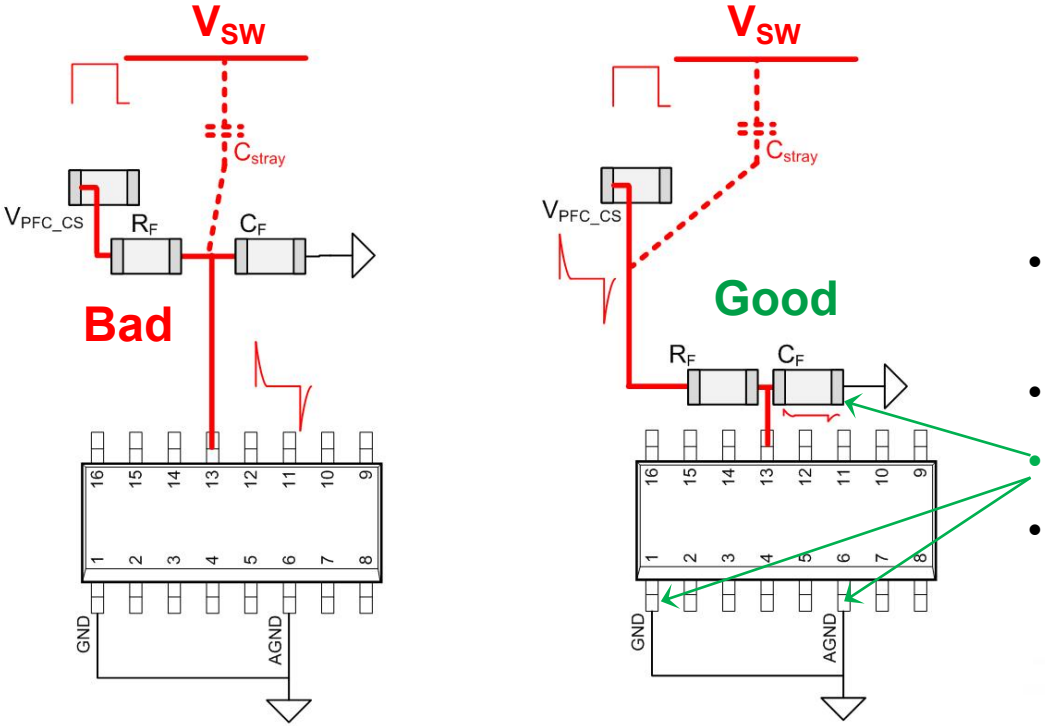
General ground plane tips:

- Consider flooding empty areas with ground
- Avoid putting slots in GND planes
- Use jumpers on single layer boards to improve GND planes
- Place as much GND under the IC as possible



Signal routing/placement

Avoid coupling noise to sensitive nodes



- Maximize the separation
  - Move the source, reduce C_{stray}
- Place capacitors and resistors near pins
- Place GND vias near caps, resistors, and IC
- Minimize the unfiltered track length

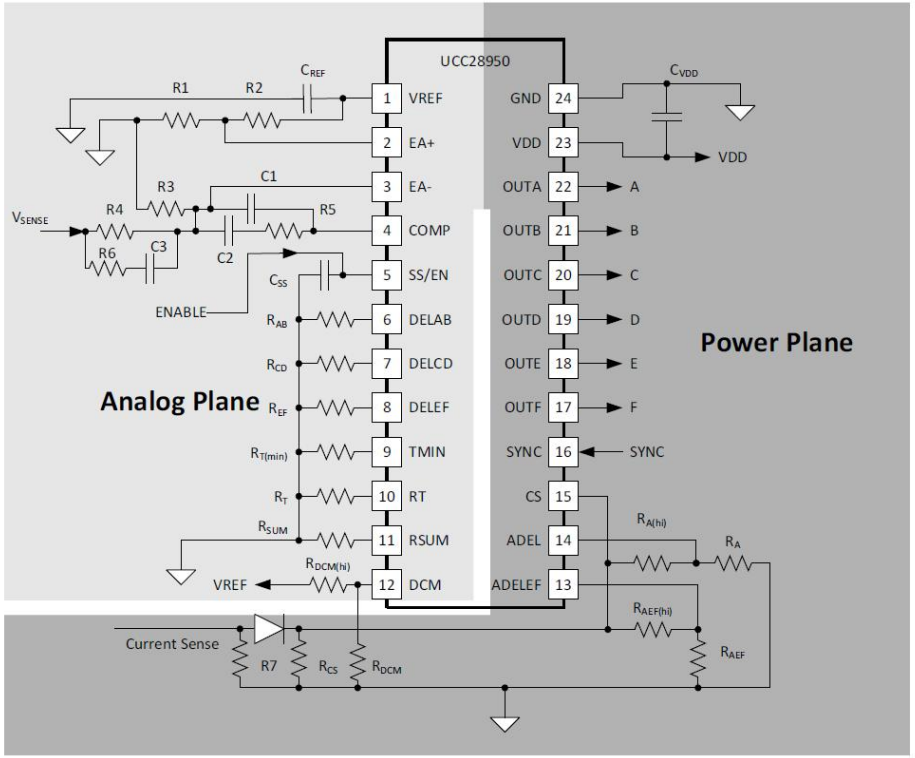
Signal routing/placement

Data sheets normally contain
PCB layout guidelines

10.1 Layout Guidelines

In order to increase the reliability and robustness of the design, TI recommends the following layout guidelines.

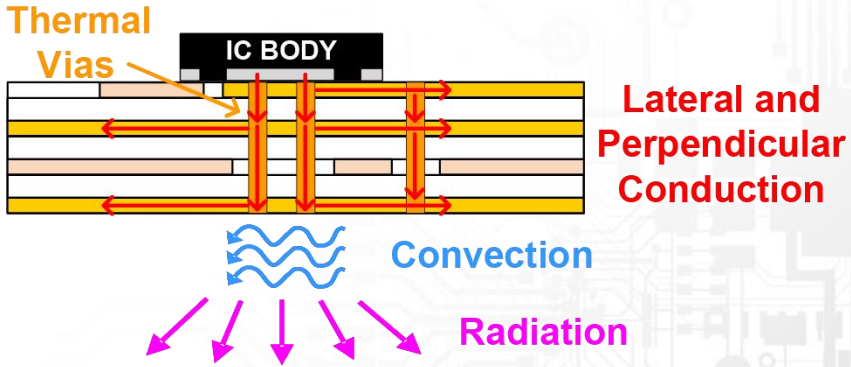
- VREF pin. Decouple this pin to GND with a good quality ceramic capacitor. A 1-uF, X7R, 25V capacitor is recommended. Keep VREF PCB tracks as far away as possible from sources of switching noise.
- EA+ pin. This is the non-inverting input to the error amplifier. It is a high impedance pin and is susceptible to noise pickup. Keep tracks from this pin as short as possible.
- EA– pin. This is the inverting input to the error amplifier. It is a high impedance pin and is susceptible to noise pickup. Keep tracks from this pin as short as possible.
- COMP pin. The error amplifier compensation network is normally connected to this pin. Keep tracks from this pin as short as possible.
- SS/EN pin. Keep tracks from this pin as short as possible. If the Enable signal is coming from a remote source then avoid running it close to any source of high dv/dt (MOSFET Drain connections for example) and add a simple RC filter at the SS/EN pin.
- DELAB, DELCD, DELEF, TMIN, RT, R_{SUM}, DCM, ADELEF and ADEL pins. The components connected to these pins are used to set important operating parameters. Keep these components close to the IC and provide short, low impedance return connections to the GND pin.
- CS pin. This connection is arguably the most important single connection in the entire PSU system. Avoid running the CS signal traces near to sources of high dv/dt. Provide a simple RC filter as close to the pin as possible to help filter out leading edge noise spikes which will occur at the beginning of each switching cycle.
- SYNC pin. This pin is essentially a digital I/O port. If it is unused, then it may be left open circuit or tied to ground via a 1-kΩ resistor. If Synchronisation is used, then route the incoming Synchronisation signal as far away from noise sensitive input pins as possible.
- OUTA, OUTB, OUTC, OUTD, OUTE and OUTF pins. These are the gate drive output pins and will have a high dv/dt rate associated with their rising and falling edges. Keep the tracks from these pins as far away from noise sensitive input pins as possible. Ensure that the return currents from these outputs do not cause voltage changes in the analog ground connections to noise sensitive input pins. Follow the layout recommendation for Analog and Power ground Planes in Figure 45.
- VDD pin. This pin must be decoupled to GND using ceramic capacitors as detailed in the 'Power Supply Recommendations' section. Keep this capacitor as close to the VDD and GND pins as possible.
- GND pin. This pin provides the ground reference to the controller. Use a Ground Plane to minimize the impedance of the ground connection and to reduce noise pickup.



Thermal management

PWB cooling strategy

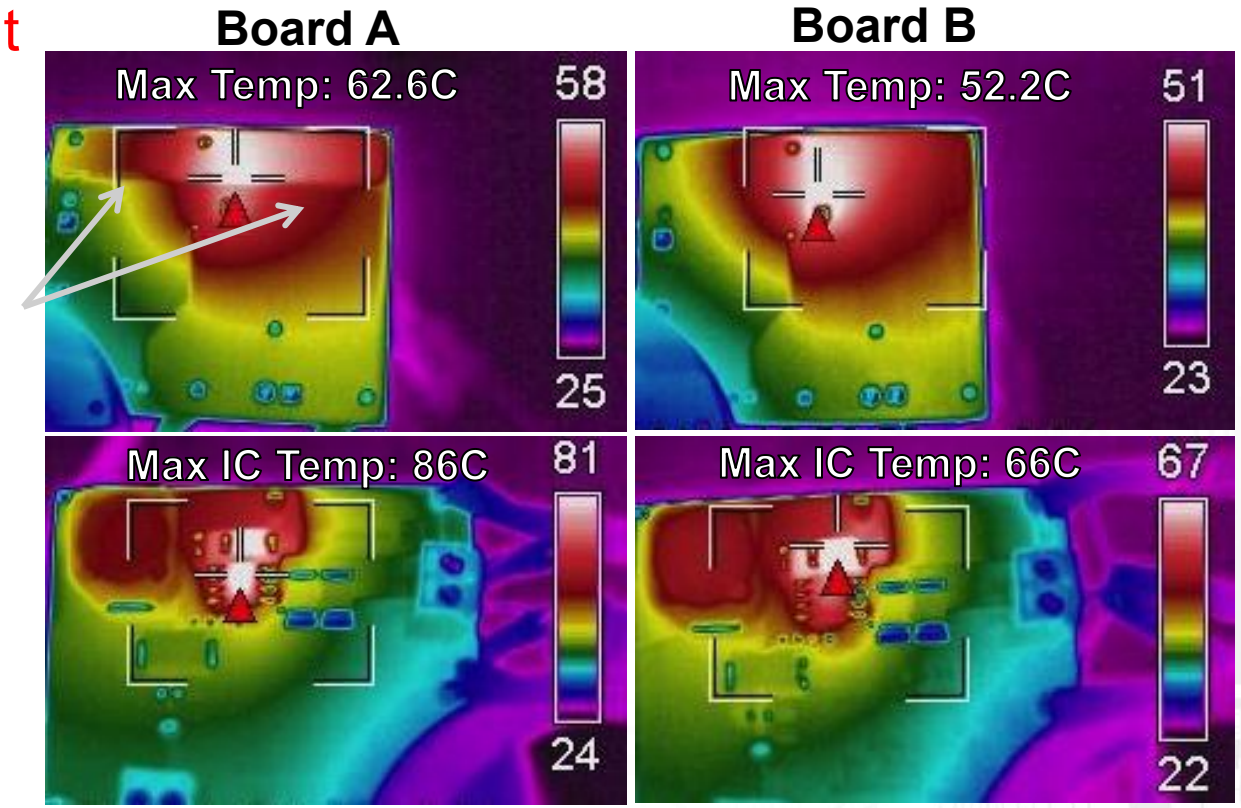
- Have **solid ground planes** to better spread heat across the layer
- **Avoid breaks in planes** as they substantially degrade lateral heat flow
- Use **thermal vias** to spread heat to other layers
- **Thermal pads** help to get the heat out of the IC into the PCB
- Use both sides of the board to cool
- Maximize the thermal paths with partial pours wherever practical
- DO NOT use switched node for cooling



Thermal management

Why Is board A 10°C hotter than B?

- Traces on the bottom layer **prevent heat from spreading** effectively
- **Removing horizontal trace** for a more solid bottom layer reduces IC temp on board B
- Hottest component on B is the catch diode



PCB layout example

Gather information and place large components

Useful information:

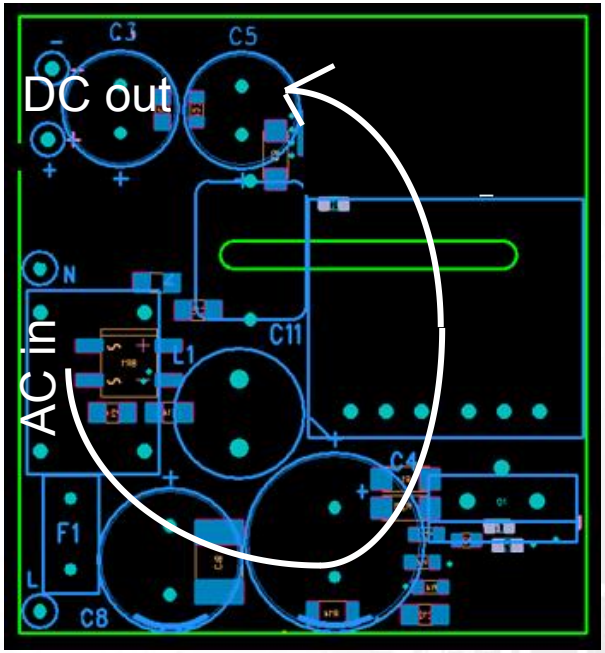
- PCB size and (layers, layer spacing, material)
- Position of inlet and outlet connections
- Mechanical restraints (keep outs and height restrictions)
- Manufacturing process constraints
- Know the creepage and clearance requirements

Understand the circuit:

- High current paths
- High di/dt paths
- High dv/dt nodes
- Hot parts

Imagine a general ‘flow’

- Trunk packing algorithm



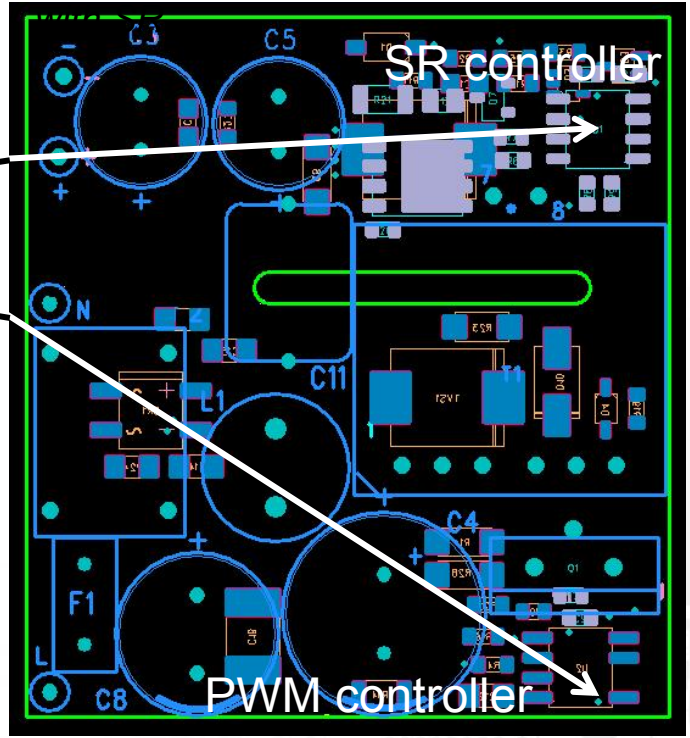
UCC28710/UCC24610 PSR flyback with SR

PCB layout example

Place remaining components

- Place the large parts in the power path first
- Reserve a ‘quiet’ location for the controller
  - NOT under transformer or node with high dv/dt
  - Place its associated parts nearby
- Reserve an area for the input filter
  - Keep filter input away from output
  - Rotate, reposition, reassign pins, repeat

UCC28710/UCC24610 PSR flyback



PCB layout example

Route power and signal etch

Two layers:

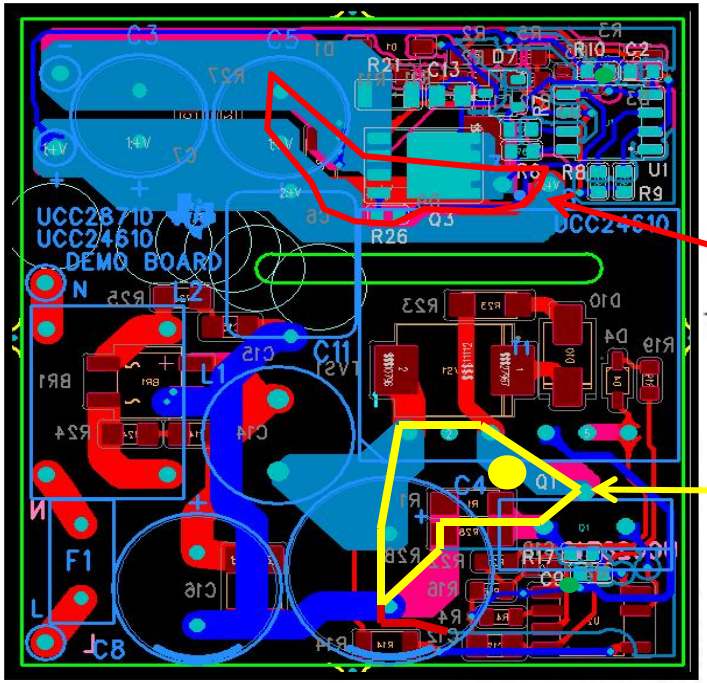
- Bottom layer (**red**)
- Top layer (**blue**)

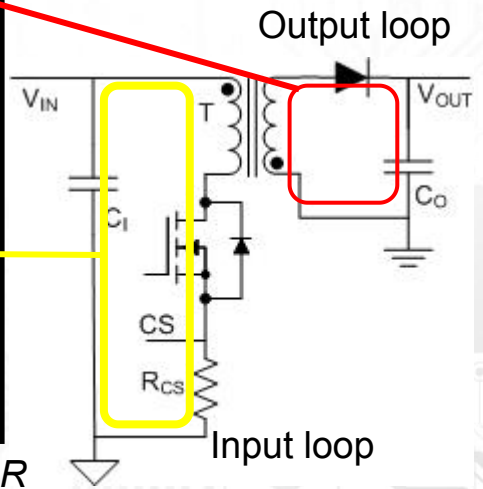
Route power path first

- Use wide etch and polygon pours
- Minimize high di/dt loop area
- Minimize high dv/dt surface area

Route signal etch last

- Keep away from high dv/dt nodes
- Keep noise sensitive etch short
- Shorten return paths



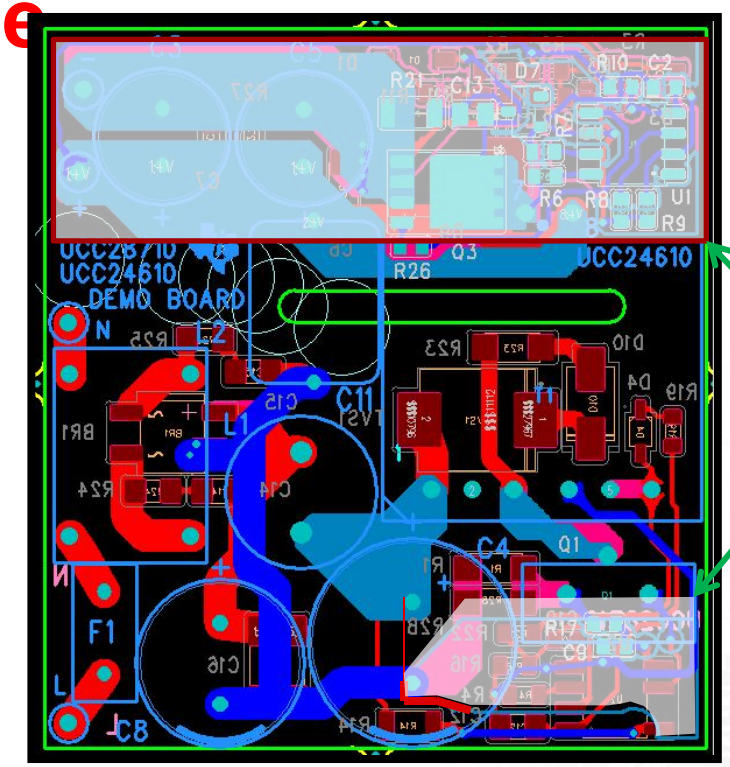


UCC28710/UCC24610 PSR flyback with SR

PCB layout example

Pour ground planes

- Flood empty areas:
  - Primary GND
  - Secondary GND
- Use vias to connect to GND planes
  - Near caps/resistors
  - Near GND pins of ICs
- Check for blocked GND connections
  - Move parts/etch as necessary
  - Be mindful of parasitic resistance and inductance



UCC28710/UCC24610 PSR flyback with SR

Summary: keys to a successful SMPS layout

- Understand your circuit: **high current and di/dt paths, high dv/dt nodes**
- Understand how **parasitic resistance, inductance, and capacitance** are manifested
- Understand how layout can significantly affect **EMI**
- Understand the **safety requirements** for your product
- Understand **how heat is transferred** through the PCB
- Follow a logical procedure:
  - Place large parts, place small parts, power routing, signal routing, pour planes
- Have someone review your layout!

Summary: references

- ***Constructing Your Power Supply - Layout Considerations***; R. Kollman; 2004 TI Power Supply Design Seminar; www.ti.com/seclit/ml/slup230/slup230.pdf
- ***Safety Considerations in Power Supply Design***; B. Mammano and L. Bahra; 2004 TI Power Supply Design Seminar; www.ti.com/seclit/ml/slup227/slup227.pdf
- ***Common Mistakes in DC/DC Converters and How to Fix Them***; P. Shenoy and A. Fagnani; 2018 TI Power Supply Design Seminar; www.ti.com/seclit/ml/slup384/slup384.pdf
- ***Grounding in Mixed-Signal Systems Demystified, Part 1 & Part 2***; S. Pithadia and S. More; 1Q 2013, TI Analog Applications Journal; www.ti.com/lit/an/slyt499/slyt499.pdf; www.ti.com/lit/an/slyt512/slyt512.pdf
- ***Why Should You Count Squares***; Brigitte; 2016 TI Power House Blog; http://e2e.ti.com/blogs_/b/powerhouse/archive/2016/10/03/why-should-i-count-squares

Thank you

SMPS characteristics

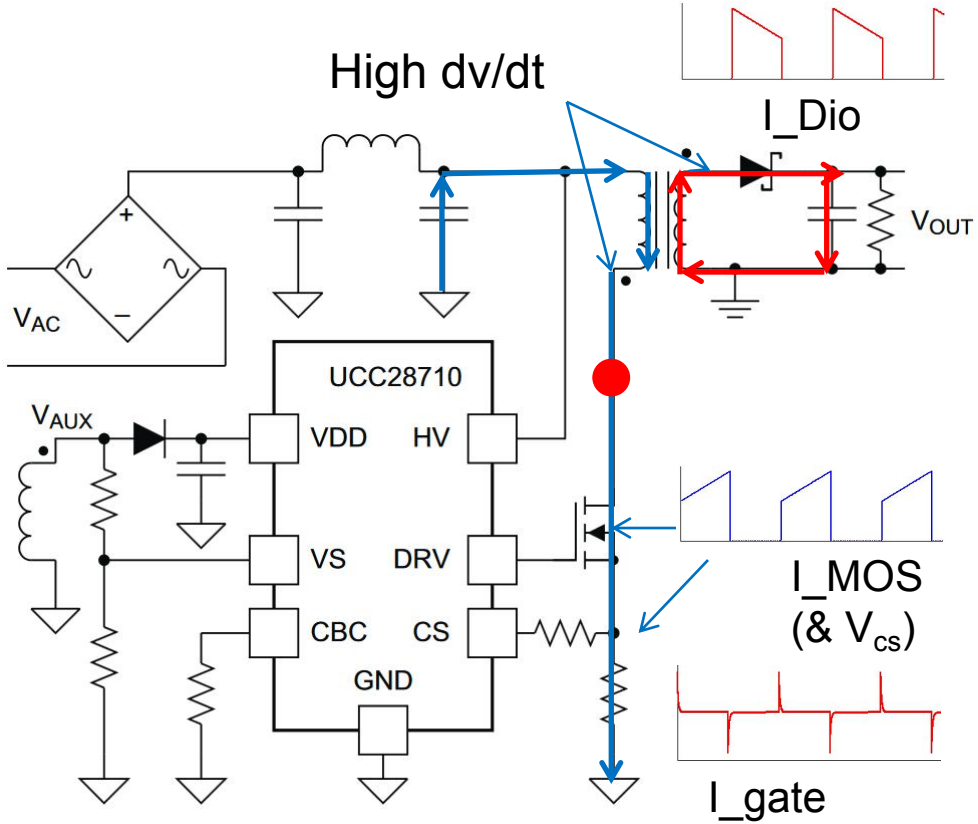
PCB layout: flyback

Low power but often used in off line applications where V_{in} is high

Input and output currents are pulsating

Gate drive currents as before

High dv/dt rates at the MOSFET drain – red dot



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265