

How to Select a Power-efficient Narrowband Receiver for Active Antenna-array Systems



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** This is the 10th post in an Analog Wire [RF-sampling blog series](#). **

In my previous [blog post](#), I discussed the advantages of radio-frequency (RF) sampling architectures for wide-bandwidth systems, but some systems operate with moderate bandwidth requirements or have other key considerations. Active antenna arrays use multiple antennas specifically distributed to create a more focused radiation pattern than what's possible with a single element. This focused pattern increases the antenna gain to the intended target or user while simultaneously providing interference rejection to areas outside the beam pattern, and thus does not require excessive signal bandwidth.

Radar array is one example of an active antenna system used to pinpoint the location of a target in space. The radar-array system depicted in [Figure 1](#) illustrates a simple three-by-three array capable of steering the beam in two dimensions to track a target.

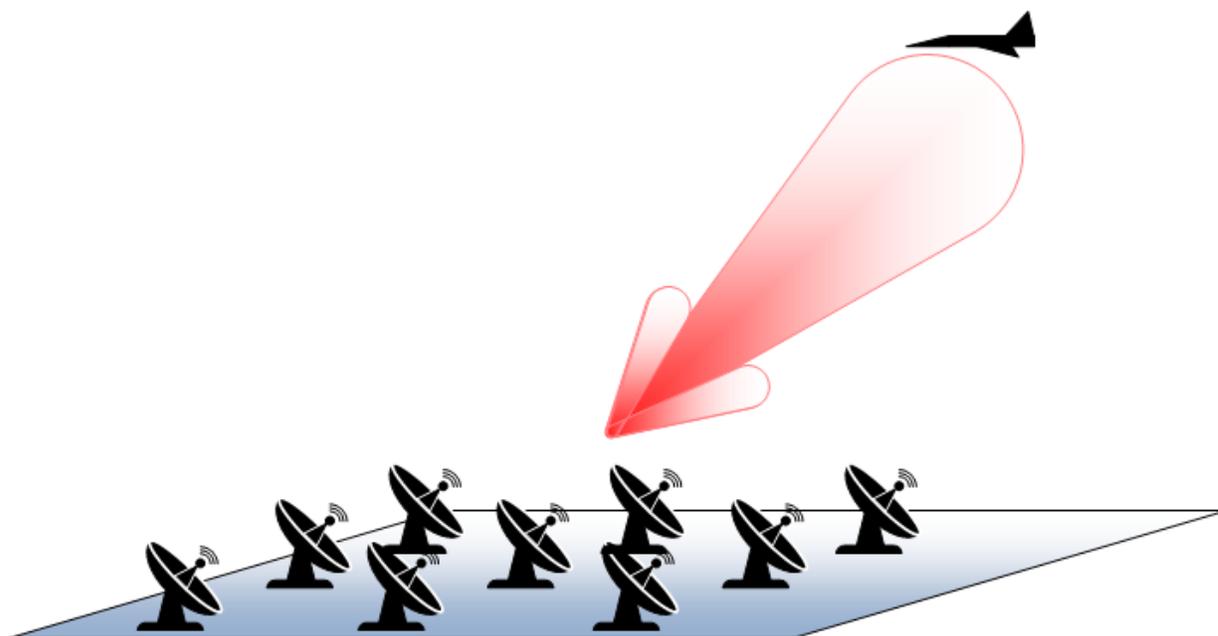


Figure 1. Three-by-three Radar-antenna Array

Each antenna element requires its own receiver. Smaller arrays may use eight elements; very large arrays use thousands of elements. With so many receivers required for these systems, it is imperative that each receiver be low cost and power-efficient; however, these systems still require high dynamic-range capabilities to discern the target from the background noise and interference.

The TI Designs 700-2700MHz Dual-Channel Receiver with 16-Bit ADC and 100MHz IF Bandwidth Reference Design (TIDA-00360) showcases the [TSW16DX370](#) evaluation module (EVM) which is a super-heterodyne receiver applicable for active antenna-array systems. [Figure 2](#) shows the block diagram. This reference design uses the TRF37B32 dual mixer to convert input RF signals to an intermediate frequency (IF). The mixer has excellent gain, noise figure and input-linearity performance for any high-end communication system. The

TRF37B32 achieves its performance at one of the lowest power-dissipation levels of similar devices. This is critical when the system must employ dozens to hundreds of receivers.

In normal operation, the device consumes about 1W per channel (at 1,950MHz). Current consumption is dependent on local oscillator (LO) frequency. If you need further power reduction, the TRF37B32 offers a low-power mode that drops the nominal dissipation to 0.6W per channel at 1,950MHz. There is also an option to independently power down each branch if you need only a single channel or power down both channels for time-division duplexing (TDD) operation.

The TSW16DX370EVM includes an IF band-pass filter centered around 250MHz with a 1dB bandwidth of 100MHz. The EVM incorporates the ADC16DX370 analog-to-digital converter (ADC), which provides 16-bit resolution and operates at 370MSPS. It offers the signal-to-noise performance required for discerning small signals from background noise and uses the JESD204B standard for serializing digital data. The ADC16DX370 uses as few as two lanes to transfer all of the data from two converters to a centralized processor. When dealing with many receivers, it is advantageous to condense the digital interface to minimize routing.

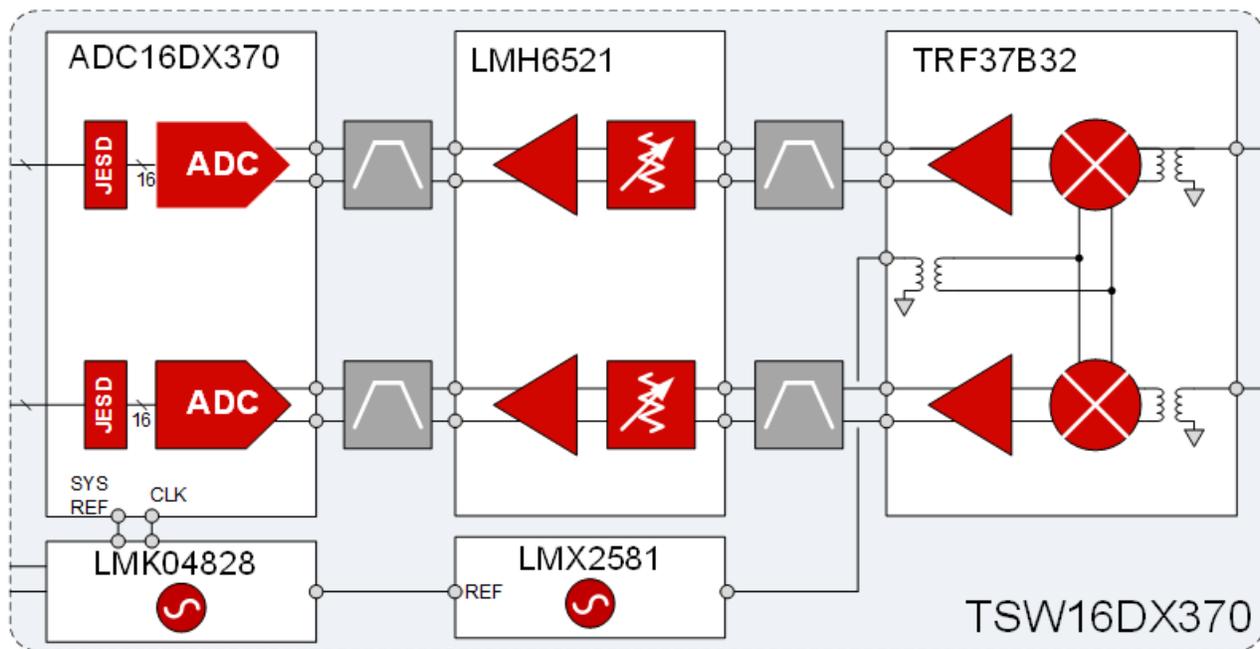


Figure 2. TSW16DX370 Receiver System Reference Design

The focused beam is of limited use without the ability to steer the beam where needed. Modifying the relative phase of each element using an inline phase-adjustment circuit steers the beam. Figure 3 shows a varactor-based analog phase-adjuster circuit. The hybrid coupler keeps the input and output return loss at reasonable levels. If the signal path includes the circuit, RF performance (particularly intermodulation distortion) degrades because of the varactor's nonlinear performance.

An alternative approach is to place the phase-adjuster circuitry in the LO path (as shown in Figure 4) where the signal is a single-frequency sinusoid and not a modulated signal. This achieves the desired phase adjustment without impacting noise or linearity performance as a function of adjustment voltage.

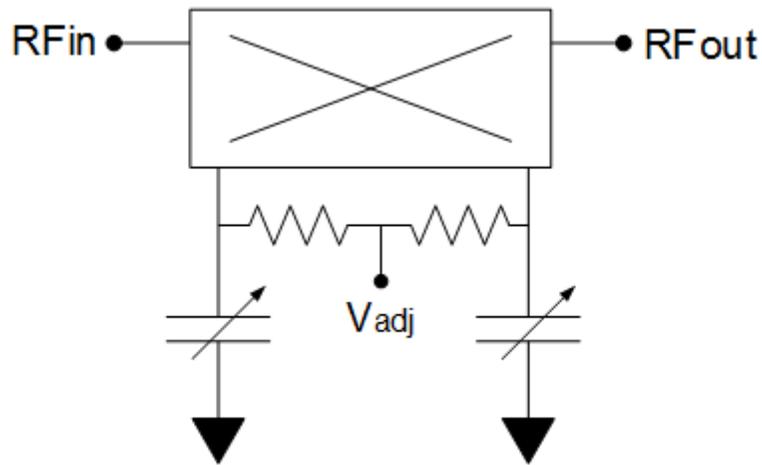


Figure 3. Phase-adjustment Circuit

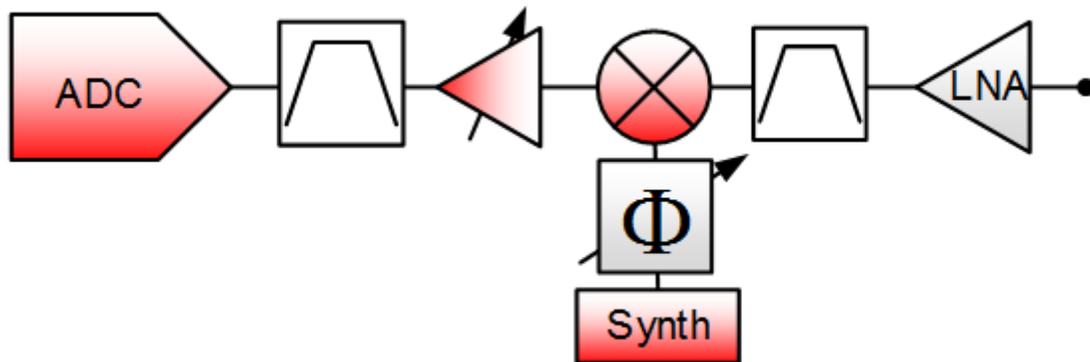


Figure 4. Super-heterodyne Architecture with Phase Adjustment in the LO Path

The proposed receiver maintains high performance at low power dissipation that easily scales to any size antenna array.

Check back next month where I discuss a receiver solution for capturing 1-GHz bandwidth signals.

Additional Resources

- Learn more about designing with data converters in [TI's Data Converter Learning Center](#).
- Read the other posts in my [RF sampling blog series](#).
- Learn more about TI's [RF sampling ADCs](#).

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