

RF Sampling: Frequency Planning Yields a Clean Spectrum



RJ Hopper

You think your radio frequency (RF) sampling design is well in hand because you selected the proper device and defined the clock source. But wait; you are not done. Even the best devices introduce degradation without proper frequency planning to ensure a clean spectrum from harmonics or clock-mixing spurs. I discussed some of these impairments in [RF Sampling: Interleaving Builds Faster ADCs](#) related to interleaving converters. Frequency planning has always been a part of good transceiver design, but it is more critical with RF sampling because the signals are already at the frequency band of interest. The RF sampling architecture does not have narrowband channel filtering to clean the spectrum like other configurations with an intermediate frequency (IF) or baseband (BB) stage.

In the transmitter, regulatory requirements restrict the level of spurious products that fall within the band of interest and just outside the band. These spurious products created in the converter cannot be filtered effectively before they reach the power amplifier (PA). Once radiated these products potentially interfere with other users.

Frequency planning with an RF sampling [digital-to-analog converter](#) (DAC) ensures that harmonic content folding back into the first Nyquist zone is not within or near the band of interest. The frequency band for a given application is fixed; it is not adjustable, but you can adjust the sample rate of the converter. Increasing the sampling rate creates a larger Nyquist zone; however, that does not guarantee an optimal plan.

Transmitter Frequency Planning Example

Look at an example of a transmitter operating in the 2.14-GHz band with a 60-MHz wide signal. [Figure 1a](#) depicts the first Nyquist zone spectrum with a high-frequency clock rate of 8,024 MHz. With this rate, the desired band (highlighted in blue) is clear, but third- and fifth-order harmonics as well as known clock-mixing spurs (highlighted in yellow) are located close to the band of interest. These spurious products would be difficult to filter.

[Figure 1b](#) shows the same band with a reduced clock rate of 5,683.2 MHz. With this clock rate, none of the high-order harmonics nor the clock-mixing spurs are located close to the desired band of interest. In this example, the lower sampling-rate approach is preferable because you can easily filter the high-order spurs.

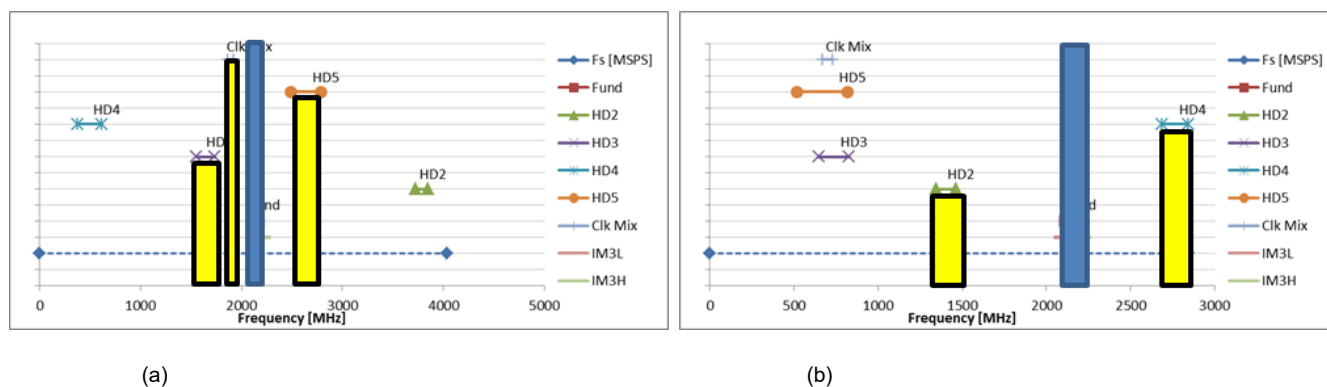


Figure 1. Spectrum Chart with 8,024-MHz (a) and 5,683.2-MHz Clocks (b)

Receiver Frequency Planning Example

The frequency-planning goal for the receiver is slightly different. Interference derived from in-band and out-of-band signals significantly impacts receiver sensitivity. You can minimize out-of-band interferers from other users' signals or from transmitter bleedthrough with proper band-limiting filtering on the RF input. You cannot filter in-band interferers. Frequency planning ensures that harmonic content from in-band interferers does not fold back within the band of interest. Unlike the transmitter case, harmonic content that folds back just outside the band is not a problem.

Figure 2 shows an example with a 100-MHz wide signal operating within a band centered at 1,950 MHz. The clock frequency is 6,144 MHz. With this configuration, all of the higher-order harmonics are outside the band. The second and fourth harmonics are close, but not within the band. A traditional low-IF architecture cannot compete. The lower sampling rate [analog-to-digital converter \(ADC\)](#) operating with the same signal bandwidth cannot achieve a clean spectrum because the folded-back harmonics cover the entire Nyquist zone.

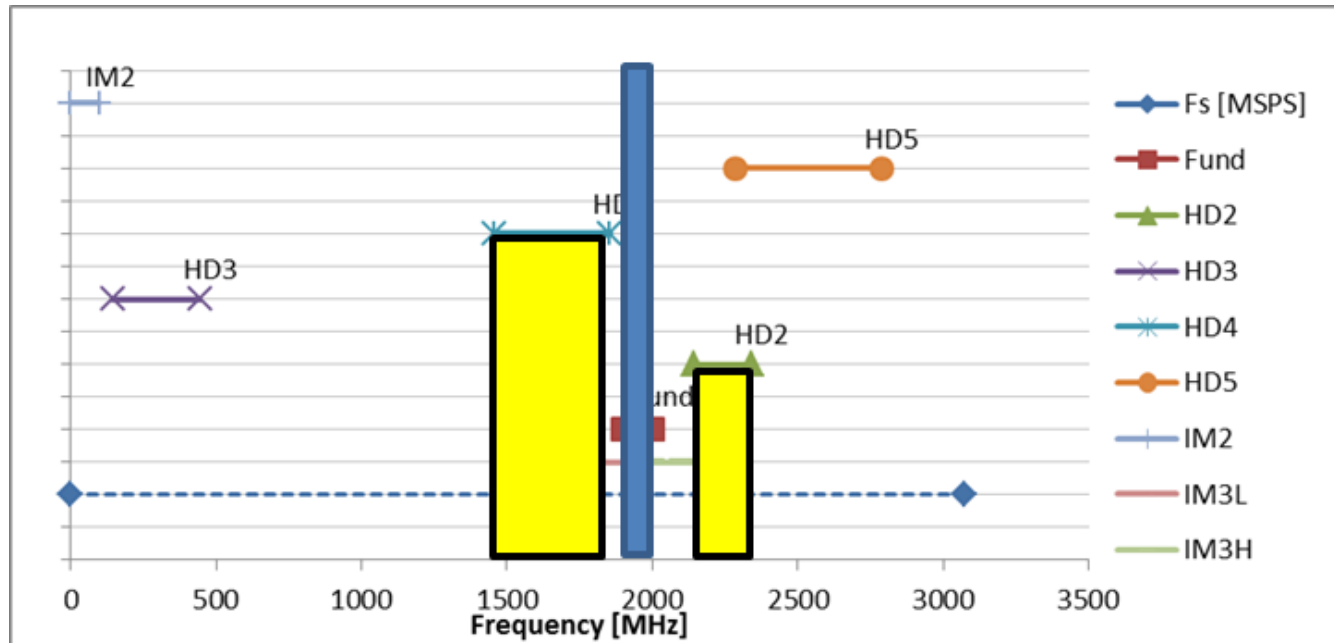


Figure 2. Spectrum Chart of a 100-MHz Wide Band Centered at 1,950 MHz with a 6,144-MHz Clock

You can modify the clock frequency to maintain a clean spectrum as the frequency band of interest changes. With traditional architectures, adjusting the frequency planning required you to modify synthesizers and IF or baseband filter stages. The RF sampling architecture allows simple frequency-planning modifications by only adjusting the sampling rate. Since operating in different bands only requires a clock-frequency adjustment, the RF sampling architecture is easily adaptable to different frequency bands and applications.

Next month, I will discuss the clocking requirements for RF sampling ADCs. Let me know what other topics you'd like to learn about designing with RF sampling converters by posting a comment below.

Additional Resources

- Learn more about designing with data converters in [TI's Data Converter Learning Center](#).

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated