Technical Article

How to improve the power factor of a PFC

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Introduction

In Power Tips #116, I talked about how to reduce the total harmonic distortion (THD) of a power factor correction (PFC). In this power tip, I will talk about another important criterion to evaluate PFC performance: the power factor, defined as the ratio of real power in watts to the apparent power, which is the product of the root mean square (RMS) current and RMS voltage in volt amperes, as shown in Equation 1:

$$PF = \frac{Real\ power}{Apparent\ power} \quad (1)$$

The power factor indicates how efficiently energy is drawn from the AC source. With a poor power factor, a utility needs to generate more current than the electrical load actually needs, which causes elements such as breakers and transformers to overheat, in turn reducing their life span and increasing the cost of maintaining a public electrical infrastructure.

Ideally, the power factor should be 1; then the load appears as a resistor to the AC source. However, in the real world, electrical loads not only cause distortions in AC current waveforms, but also make the AC current either lead or lag with respect to the AC voltage, resulting in a poor power factor. For this reason, you can calculate the power factor by multiplying the distortion power factor by the displacement power factor:

$$PF = \frac{\cos\Phi}{\sqrt{1 + THD^2}} \quad (2)$$

where φ is the phase angle between the current and voltage and THD is the total harmonic distortion of current.

As the THD requirement gets lower, the power factor requirement gets higher. Table 1 lists the power factor requirements in the recently released Modular Hardware System-Common Redundant Power Supply (M-CRPS) base specification.

Table 1. M-CRPS power factor requirements

Output power	10% load	20% load	50% load	100% load
Power factor	>0.92	>0.96	>0.98	>0.99

Equation 2 shows that to improve the power factor, the first thing to do is to reduce the THD (which I discussed in Power Tips #116). However, a low THD does not necessarily mean that the power factor is high. If the PFC AC input current and AC input voltage are not in phase, even if the current is a perfect sine wave (low THD), the phase angle φ will result in a power factor less than 1.

The phase difference between the input current and input voltage is mainly caused by the electromagnetic interference (EMI) filter used in the PFC. Figure 1 shows a typical PFC circuit diagram that consists of three major parts: an EMI filter, a diode bridge rectifier, and a boost converter.

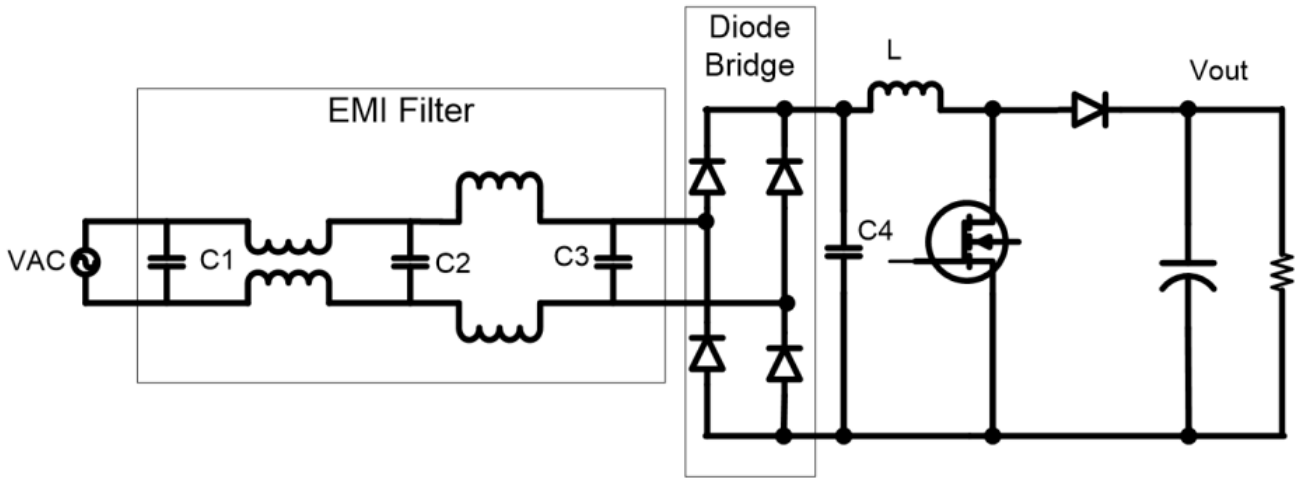

Figure 1. Circuit diagram of a typical PFC that consists of an EMI filter, diode bridge rectifier, and a boost converter. Source: Texas Instruments

In Figure 1, C1, C2, C3, and C4 are EMI X-capacitors. Inductors in the EMI filter do not change the phase of the PFC input current; therefore, it is possible to simplify Figure 1 into Figure 2, where C is now a combination of C1, C2, C3 and C4.

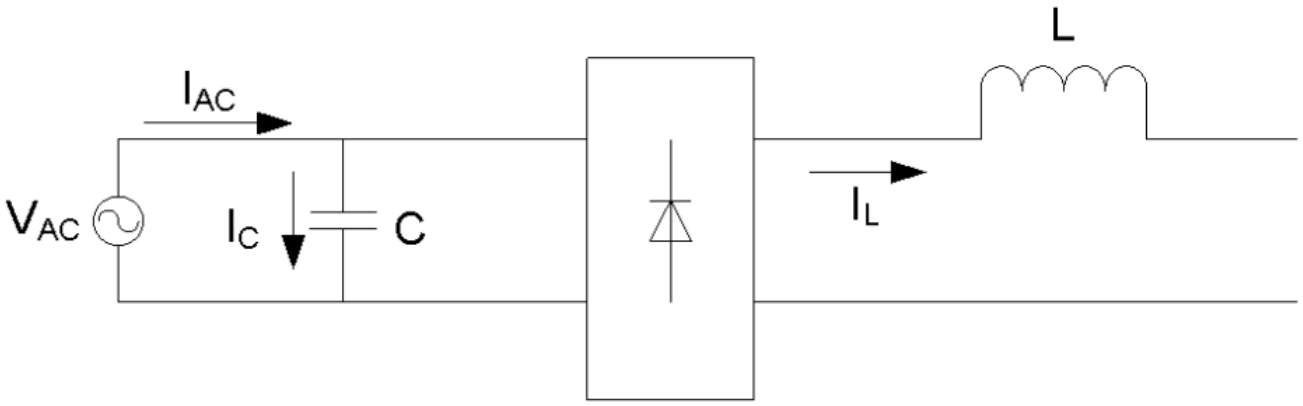

Figure 2. Simplified EMI filter where C is a combination of C1, C2, and C3. Source: Texas Instruments

The X-capacitor causes the AC input current to lead the AC voltage, as shown in Figure 3. The PFC inductor current is $\vec{I_L}$, the input voltage is $\overrightarrow{V_{AC}}$, and the X-capacitor reactive current is $\vec{I_C}$. The total PFC input current is $\overrightarrow{I_{AC}}$, which is also the current from where the power factor is measured. Although the PFC current control loop forces $\vec{I_L}$ to follow $\overrightarrow{V_{AC}}$, the reactive current of $\vec{I_C}$ leads $\overrightarrow{V_{AC}}$ by 90 degrees, which causes $\overrightarrow{I_{AC}}$ to lead $\overrightarrow{V_{AC}}$. The result is a poor power factor.

This effect is amplified at a light load and high line, as $\vec{I_C}$ takes more weight in the total current. As a result, it is difficult for the power factor to meet a rigorous specification such as the M-CRPS specification.

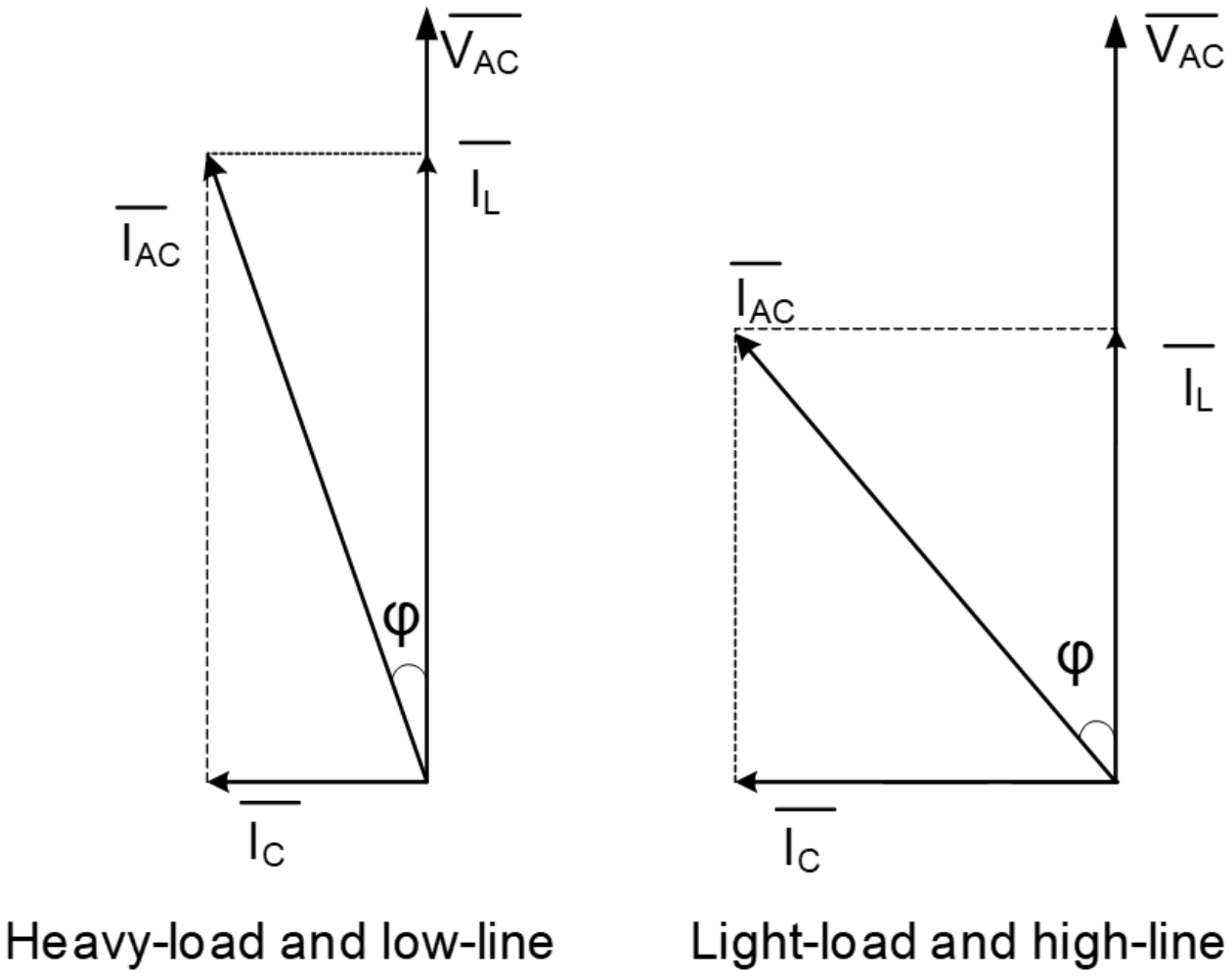

Figure 3. X-capacitor $\overrightarrow{I_C}$ causes the AC current to lead the AC voltage. Source: Texas Instruments

Fortunately, with a digital controller, you can solve this problem through one of the following methods.

Method #1

Since $\overrightarrow{I_C}$ makes the total current lead the input voltage, if you can force the $\overrightarrow{I_L}$ to lag $\overrightarrow{V_{AC}}$ by some degree, as shown in Figure 4, then the total current $\overrightarrow{I_{AC}}$ will be in phase with the input voltage, improving the power factor.

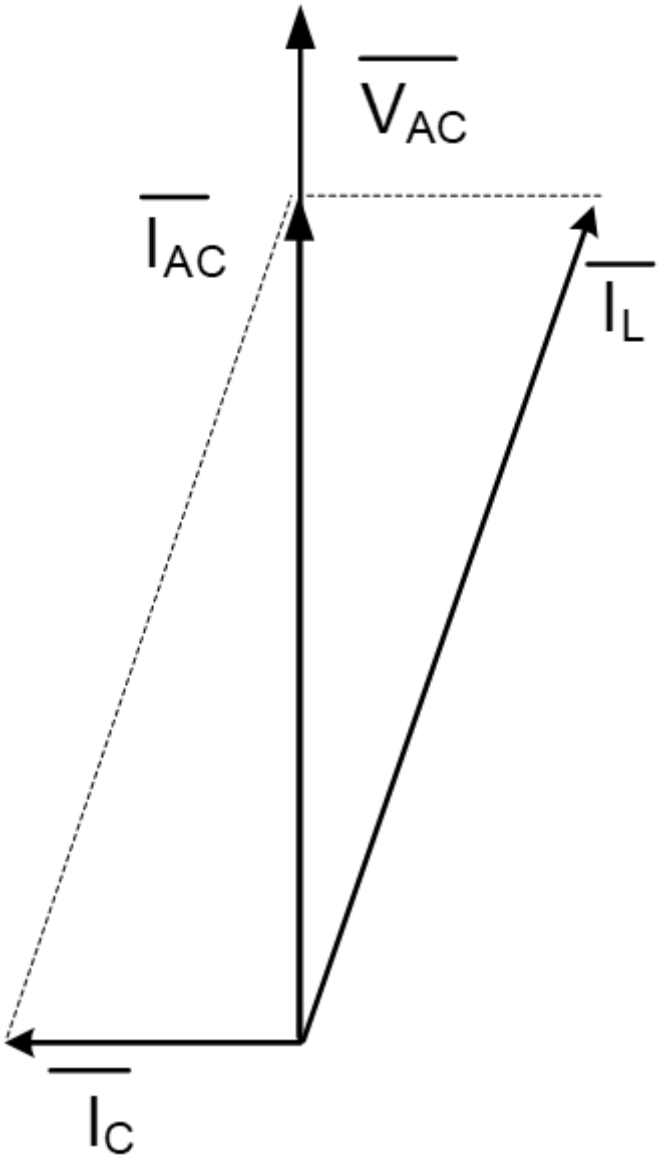

Figure 4. Forcing $\overrightarrow{I_L}$ to lag $\overrightarrow{V_{AC}}$ so that the total current $\overrightarrow{I_{AC}}$ will be in phase with the input voltage. Source: Texas Instruments

Since the current loop forces the inductor current to follow its reference, to let $\overrightarrow{I_L}$ to lag $\overrightarrow{V_{AC}}$, the current reference needs to lag $\overrightarrow{V_{AC}}$. For a PFC with traditional average current-mode control, the current reference is generated by Equation 3:

$$I_{REF} = A * B * C \tag{3}$$

Where A is the voltage-loop output, B equals $1/V_{AC\_RMS}{}^2$, and C is the sensed input voltage $V_{AC}(t)$.

To delay the current reference, an analog-to-digital converter (ADC) measures $\overrightarrow{V_{AC}}$, the measurement results are stored in a circulate buffer. Then, instead of using the newest input voltage (V_{IN}) data, Equation 3 uses previously stored V_{IN} data to calculate the current reference for the present moment. The current reference will lag $\overrightarrow{V_{AC}}$; the current loop will then make $\overrightarrow{I_L}$ lag $\overrightarrow{V_{AC}}$. This can compensate the leading x-capacitor $\overrightarrow{I_C}$ and improve the power factor.

The delay period needs dynamic adjustment based on the input voltage and output load. The lower the input voltage and the heavier the load, the shorter the delay needed. Otherwise $\overrightarrow{I_L}$ will be over delayed, making the power factor worse than if there was no delay at all. To solve this problem, use a look-up table to precisely and dynamically adjust the delay time based on the operating condition.

Method #2

Since a poor power factor is caused mainly by the EMI X-capacitor $\overrightarrow{I_C}$, if you calculate $\overrightarrow{I_C}$ for a given X-capacitor value and input voltage, then subtract $\overrightarrow{I_C}$ from the total ideal input current to form a new current reference for the PFC current loop, you will get a better total input current that is in phase with the input voltage and can achieve a good power factor.

To explain in detail, for a PFC with a unity power factor of 1, $\overrightarrow{I_{AC}}$ is in phase with $\overrightarrow{V_{AC}}$. Equation 4 expresses the input voltage:

$$v_{AC}(t) = V_{AC}\sin(2\pi ft) \tag{4}$$

where V_{AC} is the V_{IN} peak value and f is the V_{IN} frequency. The ideal input current then needs to be totally in phase with the input voltage, expressed by Equation 5:

$$i_{AC}(t) = I_{AC}\sin(2\pi ft) \tag{5}$$

where I_{AC} is the input current peak value.

Since the capacitor current is $i_C(t) = C\frac{dv_{AC}(t)}{dt}$, see Equation 6:

$$i_C(t) = 2\pi fCV_{AC}\cos(2\pi ft) \tag{6}$$

Equation 7 comes from Figure 2:

$$i_L(t) = i_{AC}(t) - i_C(t) \tag{7}$$

Combining Equations 5, 6 and 7 results in Equation 8:

$$i_L(t) = I_{AC}\sin(2\pi ft) - 2\pi fCV_{AC}\cos(2\pi ft) \tag{8}$$

If you use Equation 8 as the current reference for the PFC current loop, you can fully compensate the EMI X-capacitor $\overrightarrow{I_C}$, achieving a unity power factor. In Figure 5, the blue curve is the waveform of the preferred input current, $i_{AC}(t)$, which is in phase with $\overrightarrow{V_{AC}}$. The green curve is the capacitor current, $i_C(t)$, which leads $\overrightarrow{V_{AC}}$ by 90 degrees. The dotted black curve is $i_{AC}(t) – i_C(t)$. The red curve is the rectified $i_{AC}(t) – i_C(t)$. In theory, if the PFC current loop uses this red curve as its reference, you can fully compensate the EMI X-capacitor $\overrightarrow{I_C}$ and increase the power factor.

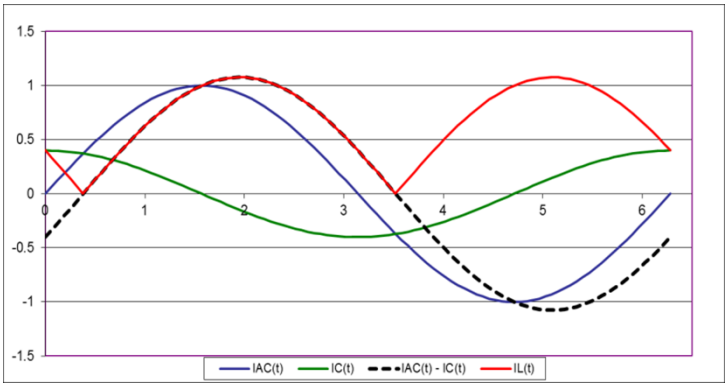

Figure 5. New current reference with $i_{AC}(t)$ (blue), $i_C(t)$ (green), $i_{AC}(t) – i_C(t)$ (red),and rectified $i_{AC}(t) – i_C(t)$ (red). Source: Texas Instruments

To generate the current reference as shown in Equation 8, you'll first need to calculate the EMI X-capacitor reactive current, $i_C(t)$. Using a digital controller, an ADC samples the input AC voltage, which the CPU then reads in the interrupt loop routine at a fixed rate. By calculating how many ADC samples are in two consecutive AC zero crossings, Equation 9 determines the frequency of the input AC voltage:

$$f = \frac{f_{isr}}{2 * N} \tag{9}$$

where f_{isr} is the frequency of the interrupt loop and N is the total number of ADC samples in two consecutive AC zero crossings.

To get the cosine waveform *cos(2πft)*, a software phase-locked loop generates an internal sine wave that is synchronized with the input voltage, making it possible to obtain the cosine waveform. Use Equation 6 to calculate $i_C(t)$, then subtract from Equation 7 to get the new current reference.

Reshaping the current reference at the AC zero crossing area

These two methods let $\overrightarrow{I_L}$ lag $\overrightarrow{V_{AC}}$ in order to improve the power factor; however, they may cause extra current distortion at the AC zero crossing. See Figure 6. Because of the diode bridge rectifier used in the PFC power stage, diodes will block any reverse current. Referencing Figure 6, during T1 and T2, $V_{AC}(t)$ is in the positive half cycle, but the expected $i_L(t)$ (the dotted black line) is negative. This is not possible, however, because the diodes will block the negative current, so the actual $i_L(t)$ remains zero during this period. Similarly, during T3 and T4, $v_{AC}(t)$ becomes negative, but the expected $i_L(t)$ is still positive. $i_L(t)$ also will be blocked by the diodes, and remains at zero.

Correspondingly, the current reference needs to be at zero during these two periods; otherwise the integrator in the control loop will build up. When the two periods are over and current starts to conduct, control loop generates a PWM duty cycle bigger than required, causing current spikes. The red curve in Figure 6 shows what the actual $i_L(t)$ would be with a diode bridge, and the red curve should be used as the current reference for the PFC current loop.

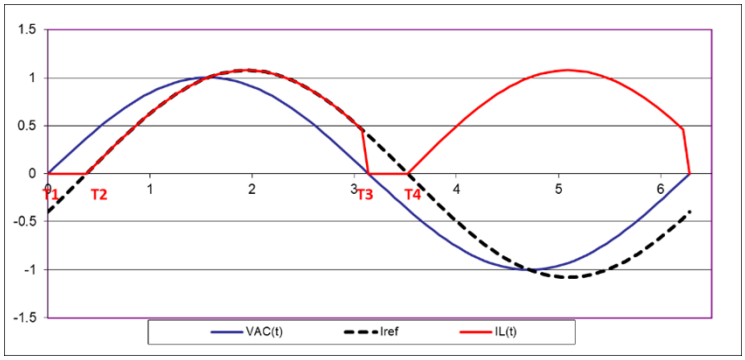

Figure 6. Final current reference curve where the red curve shows what the actual $i_L(t)$ would be with a diode bridge and should be used as the current reference for the PFC current loop. Source: Texas Instruments

Optimizing power factor

A poor power factor is mainly caused by the X-capacitor used in the PFC EMI filter, but it is possible to compensate for the effect of X-capacitor reactive current by delaying the inductor current. Now that you can use one of the two methods to delay the inductor current, you can combine them with guidance in Power Tips #116 to meet both a high-power factor and a low THD requirement.

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