

Power delivery trade-offs when preparing for the next wave of AI computing growth



IT rack power is expected to eclipse 1MW in the next two to three years. The need to achieve greater power density in AI servers has led to a shift from a 48V or 54V bus to a higher-voltage DC bus of 800 VDC. The shift to 800 VDC brings challenges in achieving high efficiency and high power density energy conversion at a system level, but also opportunities to reexamine the power delivery architecture within an IT server rack.

Moving to 800 VDC will change the power delivery architecture, as depicted in Figure 1. The input to the IT tray is now 800 VDC, which will require a higher-voltage hot-swap circuit to control current inrush and to manage safe connection to the higher-voltage bus. A high-conversion-ratio intermediate bus converter (IBC) placed on the power distribution board converts energy down from 800 VDC to a lower intermediate bus voltage. An isolation barrier (with reinforced isolation) in this system could separate the high-voltage system from the low-voltage system. The rest of the power architecture would have a similar look and feel as the 48VDC artificial intelligence (AI) computing tray, but there are several possible variations. One option is an 800V to 50V IBC followed by a 50V to 12.5V or 6.25V IBC.

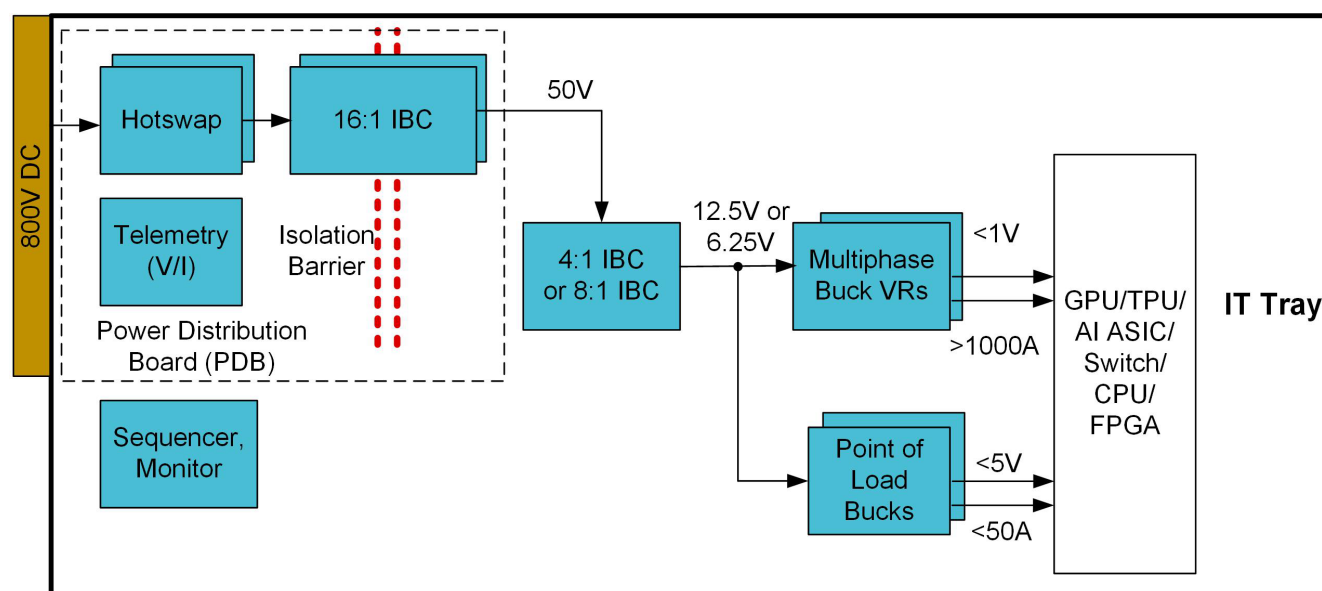


Figure 1. Example IT tray power architecture in a system with 800 VDC

With the high-level power architecture outlined, let's examine the power delivery objectives and design trade-offs. One objective of data center operators is to have high end-to-end energy conversion efficiency. This reduces data center operating expenses, reduces heat generated through power losses (and the associated heating, ventilation and air-conditioning overhead) and focuses the energy consumption at the intended load: the AI accelerator or processor and other supporting circuitry. Other important objectives are small size (limited circuit board space for power components), high reliability, and meeting performance requirements such as the transient response of multiphase voltage regulators and point-of-load buck converters.

One approach would be to simply add a higher-voltage IBC to the existing 48V power architecture. Figure 2 shows this three-stage conversion architecture. The benefit of this approach is that it is possible to reuse most of the existing 48V-based power architecture design. Let's consider a higher-voltage IBC with a 16-to-1 voltage conversion ratio (that is, a 48V output). If you assume that the peak efficiencies of the 16-to-1 ratio IBC are 98%,

the 4-to-1 IBC 98% (from 50V to 12.5V), and the multiphase voltage regulator 92% (from 12.5V to core), then the overall peak-conversion efficiency is around 88% from 800 VDC down to core.

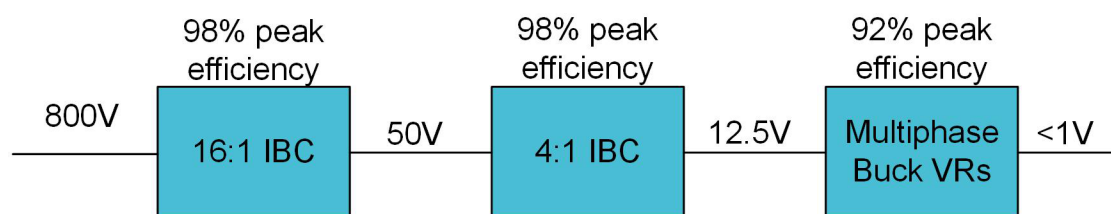


Figure 2. Three-stage conversion architecture

An important question is what to select for the intermediate bus voltage. Another architecture similar to Figure 2 would be to replace the 50V to 12.5V IBC (4-to-1 ratio) with a 50V to 6.25V IBC (8-to-1 ratio). The efficiency of the 4-to-1 IBC, now 8-to-1, would decrease marginally (approximately 97.5% peak) but the 6.25V input voltage regulator stage may have an increase in efficiency to perhaps 92.5% peak. The overall efficiency could be similar at about 88% peak. The benefit of a lower voltage regulator stage input voltage is the ability to switch at a higher frequency, which can reduce size, improve transient performance, and enable backside mounting (vertical power delivery, or VPD).

You may be asking yourself why three conversion stages are necessary, and if it's possible to simplify the power delivery architecture to two stages: a high-efficiency, high-conversion-ratio IBC and a high-performance voltage regulator. Let's examine that architecture, as shown in Figure 3.

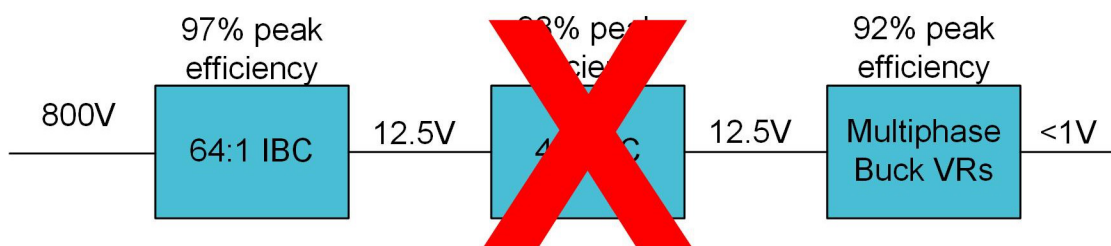


Figure 3. Two-stage conversion architecture with a 64-to-1 IBC

By removing the 4-to-1 IBC, the 64-to-1 IBC could output 12.5V directly with an assumed peak efficiency of 97%. The overall peak efficiency from 800V down to the core rail is then roughly 89%. This simplified analysis also doesn't consider the losses in the printed circuit board from the output of the 64-to-1 IBC to the voltage regulator input. But if it is possible to keep those losses to <1%, the overall efficiency remains the same. This approach could save size and minimize cost, since the 4-to-1 IBC is no longer necessary. Figure 4 illustrates this potential architecture.

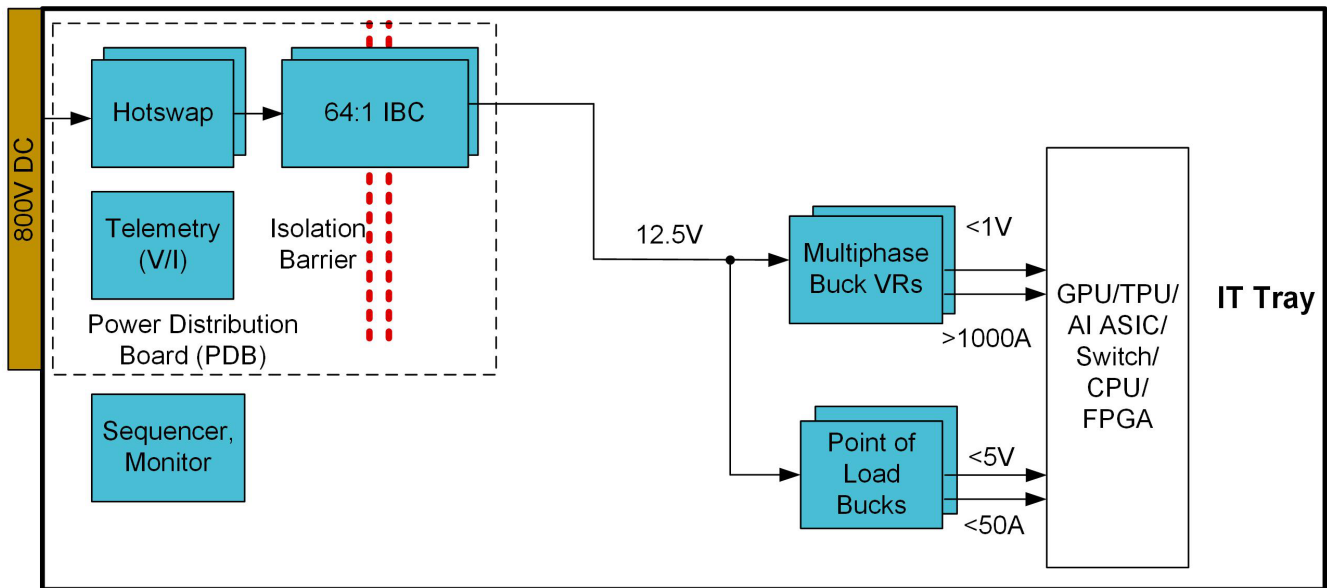


Figure 4. 800V two-stage conversion architecture with 64-to-1 IBC

Taking this two-stage conversion architecture one step further, Figure 5 shows the implementation of the 64-to-1 IBC with a 128-to-1 voltage-conversion ratio with a 6.25V output. As mentioned, a lower input voltage to the multiphase voltage regulator enables higher frequency operation, smaller size and vertical power delivery (mounting on the backside of the board underneath the processor). The estimated 800V-to-core efficiency is 89% peak (not including circuit board losses).

The challenge with this architecture is that the output current of the 128-to-1 IBC is very large. Assuming that the power delivered by the system is around 15kW to 20kW, there would be 2.4kA to 3.2kA at 6.25V. Keeping circuit board losses on the 6.25V intermediate bus to a reasonable level (<1 or 2%) will require very large conductors (for example, busbars). The 128-to-1 IBC will likely require multiple paralleled modules to reach the intended current level.

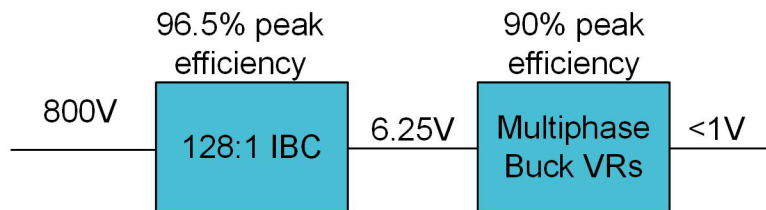


Figure 5. 800V two-stage conversion architecture with a 128-to-1 IBC

Conclusion

The transition to an 800 VDC power architecture fosters a renewed discussion about how to design power delivery given the trade-offs in overall conversion efficiency, size and performance. TI's portfolio of gallium nitride (GaN) power stages, digital power controllers, multiphase buck voltage regulators, DC/DC point of load buck converters, hot-swap controllers, isolated gate drivers and more enable the industry to navigate this transition.

Through collaboration with NVIDIA to develop power-management solutions that support an 800 VDC architecture, TI's products ensure reliable voltage conversion at critical points in the power architecture and offer the protection, monitoring and telemetry capabilities necessary for 48V and 800V ecosystems – all while delivering highly efficient and high-density power conversion from the grid to the AI accelerator gate. Learn more about [TI data center & enterprise computing](#).

Trademarks

All trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated