Application Note

Crystal Oscillator and Crystal Selection for the CC13xx, CC26xx, CC23xx, and CC27xx Family of Wireless MCUs

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ABSTRACT

The CC13xx, CC26xx, CC23xx, and CC27xx family are low-power wireless microcontrollers (MCU) platforms supporting multiple standards (that is, Bluetooth® low energy, IEEE® 802.15.4, and proprietary RF protocols). The document is valid for all CC13xx, CC26xx, CC23xx, and CC27xx family devices, unless otherwise noted. The generic term *CC devices* is used for simplification. The CC devices have integrated 24MHz (CC13x0 and CC26x0) or 48MHz (CC13x2, CC26x2, CC23xx, CC27xx) and 32.768kHz crystal oscillators TI designed for use with low-cost quartz crystals. The 24MHz and 48MHz oscillator (XOSC-HF for CC13xx and CC26xx; HFXT for CC23xx and CC27xx) generates the reference clock for the RF blocks and the MCU system. RF systems are dependent on accurate clocks for correct operation. A deviation in clock frequency is reflected as a deviation in radio frequency. This deviation can degrade RF performance, violate regulatory requirements, or lead to a nonfunctioning system. In power-down mode, the high-frequency oscillator is typically turned off and a low-frequency oscillator is the system clock. For time-synchronized protocols such as Bluetooth low energy, a tight tolerance on the sleep clock enables longer time in low-power mode and reduced power consumption important in battery-powered applications. For this low-frequency oscillator, typically a 32kHz crystal oscillator (XOSC-LF for CC13xx and CC26xx; LFXT for CC23xx and CC27xx) is used.

The scope of this application report is to discuss the requirements and trade-offs of the crystal oscillators for this CC devices and provide information on how to select an appropriate crystal. This document also presents steps to configure the device to operate with a given crystal. You must configure the CC devices based on the crystal used (that is, adjust the internal capacitor array to match the loading capacitor of the crystal for the XOSC-HF). This application report also discusses some measurement approaches that can be used to characterize certain performance metrics, including crystal oscillator amplitude, and start-up time.

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1 Oscillator and Crystal Basics

This section explains fundamentals of a quartz crystal and the oscillator operations required to understand the trade-offs when selecting a crystal for the CC devices. The complete crystal oscillator circuit includes the loading capacitance, crystal, and the on-chip circuitry.

1.1 Oscillator Operation

The circuit used as high-accuracy clock source for TI's low-power RF products is based on a Pierce oscillator as shown in Figure 1-1. There is no on-chip damping resistor and none must be added by the customer. The oscillator circuit consists of an inverting amplifier (shown as an inverter), a feedback resistor, two capacitors, and a crystal. When operating, the crystal and the capacitors form a pi filter that provides an 180-degree phase shift to the internal amplifier, keeping the oscillator locked at the specified frequency.

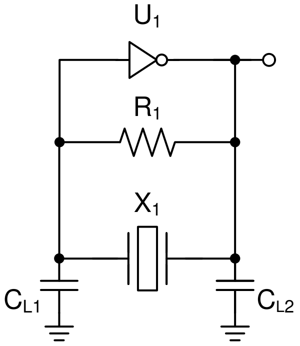

Figure 1-1. Pierce Oscillator

1.2 Quartz Crystal Electrical Model

A quartz crystal is a piezoelectric device that transforms electric energy to mechanical energy. This transformation occurs at the resonant frequency. Figure 1-2 shows the simplified electric model that describes the quartz crystal, where C_0 is the shunt capacitance, L_M is motional inductance, C_M is motional capacitance, and R_M is motional resistance. The model in Figure 1-2 is a simplified model and includes only the fundamental oscillation frequency. In reality, crystals can also oscillate at odd harmonics of the fundamental frequency.

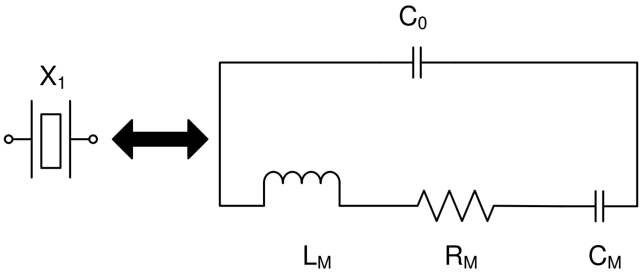

Figure 1-2. Crystal Symbol and the Electrical Model of a Quartz Crystal

1.2.1 Frequency of Oscillation

A crystal has two resonant frequencies characterized by a zero-phase shift. Equation 1 is the series resonance.

$$f_s = \frac{1}{2\pi\sqrt{L_M \times C_M}} \quad (1)$$

Equation 2 is the anti-resonant frequency.

$$f_a = \frac{1}{2\pi\sqrt{L_M \times \frac{C_M \times C_0}{C_M + C_0}}} \quad (2)$$

As specified in the data sheet of the crystal, the frequency of oscillation is between the resonance frequencies. See Equation 3.

$$f_s < f_{XTAL} < f_a \quad (3)$$

1.2.2 Equivalent Series Resistance

The Equivalent Series Resistance (ESR) is the resistance the crystal exhibits at the series resonant frequency. Equation 4 gives the ESR.

$$\mathrm{ESR} = R_M\left(1 + \frac{C_0}{C_L}\right)^2 \quad (4)$$

Because C_0 is typically on the order of 1pF and C_L is 5–9pF for the high frequency crystal and 6-12pF for the low frequency crystal, ESR is approximately R_M for many crystals, sometimes ESR is approximated as motional resistance.

1.2.3 Drive Level

The drive level of a crystal refers to the power dissipated in the crystal. The maximum drive level of a crystal is often specified in the data sheet of the crystal in µW. Exceeding this value can damage or reduce the life of the crystal. Equation 5 gives the drive level in W.

$$DL = 2 \text{ x } ESR\ (\pi f(CL + C0)\ V_{PP})^2 \quad (5)$$

where, V_{pp} is the peak-to-peak voltage on the crystal pin.

Calculating the DL and comparing this value to the maximum specified DL in the crystal data sheet can reveal if the crystal is likely to have reliability issues during operation. Section 5 describes how to measure the value of V_{pp}.

1.2.4 Crystal Pulling

The crystal frequency can be pulled by changing the load capacitance presented to the crystal. The parameter ΔF is the resonance frequency change of the crystal due to a change in the load capacitance on the board, whether this is internal or externally configured on the Launchpad. The pulling is given by Equation 6 around the specified (parallel) resonance frequency of the crystal.

$$\Delta F = \frac{F \times C_M}{2} \frac{C_{LMAX} - C_{LMIN}}{(C_0 + C_{LMAX})(C_0 + C_{LMIN})} \quad (6)$$

C_{LMAX} and C_{LMIN} are the maximum and minimum load capacitance that can be presented to the crystal. These are different parameters from the CL specified on crystal data sheets. For more information, see *CC13xx/ CC26xx Hardware Configuration and PCB Design Considerations*.

1.3 Negative Resistance

Negative resistance (R_N) is a parameter of the complete oscillator circuit, including capacitor values, crystal parameters, and the on-chip circuit. The CC devices dynamically adjust the oscillator parameters to make sure of sufficient oscillator margin during crystal startup, then relax the margins for steady state to decrease the current consumption. This means that when using a crystal within the requirements outlined in the CC data sheets, proper start-up and steady-state margin is verified over operating conditions.

Equation 7 approximates the negative resistance and shows that a low C_L gives a larger negative resistance.

$$R_N \approx \frac{-g_m}{(2\pi f)^2 (2C_L)^2} \tag{7}$$

where:

g_m	is the transconductance of the active element in the oscillator.
C_L	is the load capacitance specified in the crystal data sheet.

Note

For CC23xx and CC27xx, the transconductance (g_m) can be approximated as 19 milli-Siemens for the high frequency crystal oscillator during start-up phase.

For CC13xx and CC26xx, the transconductance (g_m) can be approximated as 7 milli-Siemens for the high frequency crystal oscillator.

For the low frequency crystal, the transconductance (g_m) can be approximated as 30 micro-Siemens.

Users can also find the negative resistance of the circuit by introducing a resistor in series with the crystal. To avoid parasitic effects, TI recommends using a 0201 resistor for this task. The threshold of the sum of the extra 0201 external resistance and ESR or the crystal where the oscillator is unable to start up is approximately the same as the circuit negative resistance.

To make sure of a robust start-up of the crystal oscillator, TI recommends that the magnitude of the negative resistance be at least 10 times greater than the ESR during the initial start-up of the crystal and at least 5 times greater than the ESR during steady-state operation for automotive applications.

While, in certain use cases and applications, these values can be minimized to at least 3 times during start-up, TI recommends to use both initial and steady-state software amplitude compensation found in the SysConfig page. TI does not recommend operating values lower than these. This represents a usage limitation, and proper functionality cannot be verified at these reduced margins.

1.4 Time Constant of the Oscillator

The start-up time of a crystal oscillator is determined by transient conditions at turn-on, small-signal envelope expansion due to negative resistance, and large-signal amplitude limiting. The envelope expansion is a function of the total negative resistance and the motional inductance of the crystal. The time constant of the envelope expansion is proportional to the start-up time of the oscillator given by Equation 8.

$$\tau = \frac{-2L_M}{(R_M + R_N)} \approx \frac{-2L_M}{R_N}, \ |R_n| \gg |R_m| \tag{8}$$

A crystal with a low L_M gives a shorter start-up time and so does a high-magnitude R_N (low C_L). A trade-off exists between pull-ability due to low-motional capacitance (C_M) and fast start-up time due to low-motional inductance (L_M), because the frequency of the crystal is dependent on the both C_M and L_M. Crystals in smaller package sizes have larger L_M, and start more slowly than those in larger package sizes (see Section 1.2.1).

Table 1-1 summarizes crystal parameters and the values for the reference crystals recommended by TI for use with the CC devices.

Table 1-1. Crystal Parameters

Parameters	Description	24MHz Crystal Used in TI CC26x0 Characterization	TI-Characterization CC23XX 32.768kHz Crystal	TI-Characterization CC27XX-Q1 32.768kHz Crystal	TI-Characterization CC27XX-Q1 48MHz Crystal
Motional Inductance (L_M)	Partly determines crystal response time (how quickly the crystal responds to a change from the oscillator). Lower L_m → crystal responds more quickly to changes from the oscillator. Along with C_M, a major determiner of the crystal quality factor	12.6 mH	3.69 kH	2.95 kH	3.30 mH
Motional Capacitance (C_M)	Partly determines crystal response time. Lower C_M → crystal responds more slowly to changes from the oscillator.	3.4 fF	6.4 fF	8 fF	3.40fF
Motional Resistance (R_M)	At resonance, L_m and C_M cancel and R_M is presented to the oscillator. $R_M \simeq$ ESR assuming $C_L >> C_O$.	20Ω (60Ω maximum)	120 kΩ max	70 to 75 kΩ	30Ω
Load Capacitance (C_L)	The amount of load capacitor to tune the crystal to the correct frequency. This load capacitance also helps determine drive level.	9pF	7pF	7pF	7pF
Shunt Capacitance (C_0)	This is a parasitic capacitance due to crystal packaging and helps determine the acceptable drive level.	1.2pF	1.3pF	1.5pF	0.84 pF
ESR	Equivalent Series Resistance. If $C_L >> C_O$, then ESR $\simeq R_M$	20Ω (60Ω maximum)	120 kΩ max	70 to 75 kΩ	30Ω
Drive Level	The maximum level of power in the crystal for reliable long-term operation, see Equation 5	200 μW	<500 uW	<500 uW	50 μW Typical to 200 μW max

2 Overview of Crystal Oscillators for CC devices

The CC devices have integrated 24MHz, 48MHz and 32.768kHz crystal oscillators that TI designed for use with low-cost quartz crystals. High-frequency (48MHz) and low-frequency (32kHz) RC oscillators are also available on the CC devices, which are beyond the scope of this application note.

2.1 24MHz and 48MHz Crystal Oscillator

Figure 2-1 shows a simplified block diagram of the XOSC-HF. The oscillator circuit consists of an inverting amplifier, a feedback net, capacitors, and a crystal. The CC devices have an internal capacitor array that can be adjusted and eliminates the requirement for external loading capacitors. The cap-array can be adjusted by the Customer Configuration Flash (CCFG) within a range of 3.5pF to 10pF. For reliable operation, TI requires operating the crystal with C_L from 5 to 9pF. The CC13xx/CC26xx Hardware Configuration and PCB Design Considerations application note shows how to set this value. If no external capacitors are used, then the value of C_L is determined by the internal loading capacitors plus board parasitic capacitance C_P.

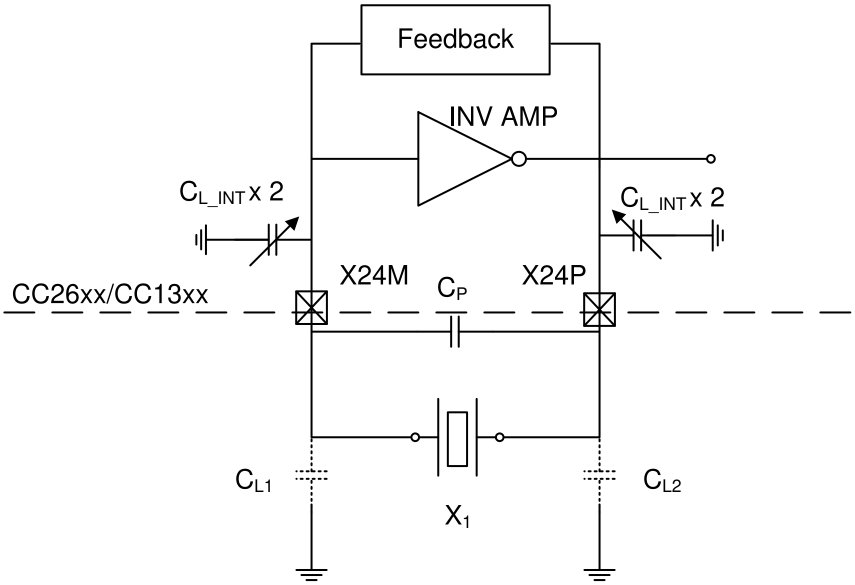

Figure 2-1. Simplified Block Diagram of the CC Devices High-Frequency Oscillator With Quartz Crystal

The 24MHz or 48MHz crystal is controlled with a control loop described in Section 2.2 and Section 2.3.

2.2 24MHz and 48MHz Crystal Control Loop

TI intends the amplitude control loop to regulate the amplitude of the oscillations of the crystal for best performance. The following are the two primary portions of the control loop:

- Start-up: The control loop injects as much current as possible into the oscillator that drives the crystal resonator to reduce the startup time. Once the amplitude reaches the desired value, the current is reduced to a steady state level.
- Steady state regulation: The amplitude of the crystal oscillator can be regulated in a steady state manner if required.

To turn on the crystal so that the radio can operate, start-up is required. Steady state amplitude regulation is not required for the crystal or radio to function.

2.3 32.768kHz Crystal Oscillator

Figure 2-2 shows a simplified block diagram of the 32.768kHz crystal oscillator. The oscillator circuit consists of an inverting amplifier, a feedback net, capacitors, and a crystal. The 32kHz crystal lacks internal capacitors and requires external loading capacitors.

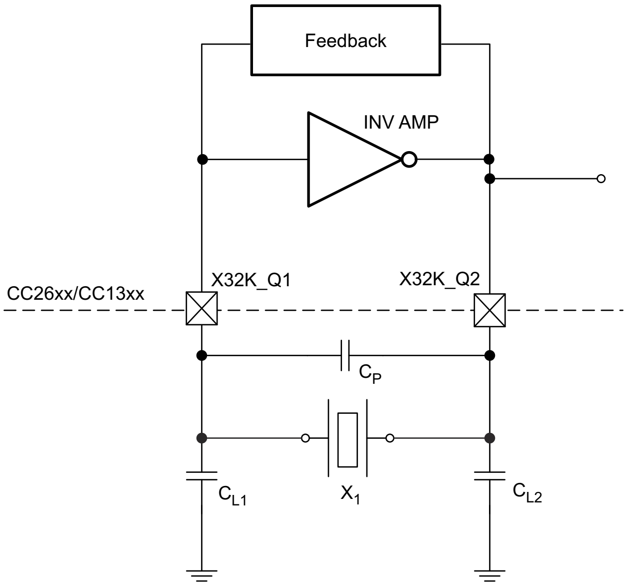

Figure 2-2. Simplified Block Diagram of the 32.768kHz Oscillator With Quartz Crystal

3 Selecting Crystals for the CC devices

This section presents some important considerations when selecting crystals for the CC devices. Selecting a crystal for a specific application depends on the following three factors:

- Size (footprint area and height)
- Performance (accuracy over temperature, lifetime, power consumption, and start-up time)
- Cost

Consider the following when selecting a crystal:

- Crystals must be selected to meet requirements listed in the CC data sheets or specifications.
  - ESR must not be greater than can be driven by the CC device.
  - Capacitive loading and frequency tolerance must meet the specifications of the standard used (for example, Bluetooth low energy).
  - Motional inductance must also meet specifications. Many crystal manufactures provide only motional inductance data upon customer request.
- Some other considerations when selecting a crystal include the following:
  - To improve start-up time and reduce power consumption, the crystal must have the following:
    - Low-capacitive loading, at the expense of greater susceptibility to frequency variation caused by the environment
    - Low-motional inductance
    - Low-motional resistance

3.1 Mode of Operation

Quartz crystals are used at the fundamental resonance frequency for frequencies relevant to the CC devices, but there are crystals that operate at an odd overtone of the fundamental frequency. TI recommends using a crystal that operates at the fundamental mode for the CC devices.

3.2 Frequency Accuracy

The total tolerance of the frequency accuracy of a crystal is dependent on several factors:

- Production tolerance
- Temperature tolerance
- Aging effects
- Frequency pulling of the crystal due to mismatched loading capacitance

When selecting the crystal, consider these parameters. Equation 9 gives the total crystal tolerance.

$$Tol_{tot} = Tol_{prod} + Tol_{temp} + Tol_{age} + Tol_{pull} \left(ppm\right) \tag{9}$$

These values are given in parts per million (ppm) and can be found in the device-specific data sheet of the crystal manufacturer, except pulling, which can be calculated by the formula in Section 1.

3.2.1 24MHz and 48MHz Crystal

Because the 24MHz and 48MHz crystal oscillators are used as a reference to generate the RF signal, any crystal frequency deviation is directly transferred to deviation of the RF signal. For example, 10ppm frequency deviation leads a deviation in RF carrier frequency of 10ppm. Select a crystal with performance within the limits of the RF specifications.

- For 802.15.4 (Thread/ ZigBee®), the maximum deviation in carrier frequency is limited to ±40 ppm (see [1]).
- For Bluetooth® low energy, the limit is ±40 ppm (see [2]).
- Customers of CC13X2 who require frequency accuracy tighter than the crystal can provide can also use a TCXO.

3.2.2 32.768kHz Crystal

The 32.768kHz crystal oscillator is used as the Read Time Clock (RTC) and is kept running when the device is in Standby mode. Because Bluetooth® low energy is a time-synchronized protocol, an accurate clock also enables longer periods of time in a low-power mode. If a lower-accuracy crystal is used, the device must wake up early to accommodate for the lower accuracy of the clock. To be compliant with Bluetooth® low energy, the clock must have a maximum of ±500 ppm of inaccuracy. For more information, see [2]. TI recommends using a tighter tolerance 32.768kHz crystal to reduce the average power consumption in a typical Bluetooth® low energy connection. In the *SimpleLink™ CC2650 EVM Kit 4XD (CC2650EM-4XD) v1.0.3 Design Files*, TI uses the Epson FC-135 crystal. If a crystal with different specifications is used, this setting must be adjusted for in the Bluetooth® low energy stack. For more details, see the BLE Stack Users Guide.

Note that low-frequency tuning fork crystals have a resonance frequency that changes with temperature with a parabolic coefficient of $(-0.04 \times 10^{-6}) / °C^2$ typically. Figure 3-1 shows an example. In Figure 3-1, 40ppm accuracy is maintained only from –10°C to 50°C.

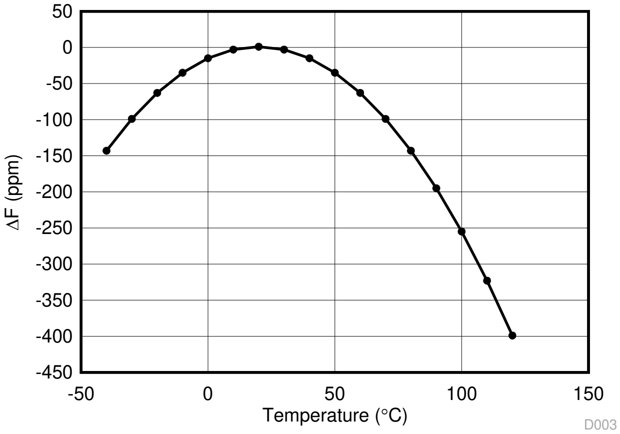

Figure 3-1. Typical Frequency vs Temperature Curve for a 32.768kHz Tuning Fork Crystal

3.3 Load Capacitance

The crystal oscillator frequency is dependent on the capacitive loading of the crystal. The crystal data sheet provides the required load capacitance for the crystal, C_L, for the oscillation to be at the correct frequency. The total C_L consists of the loading capacitors and the parasitic capacitance of the layout and packaging. C_{L1} and C_{L2} are in series with respect to the crystal. Therefore, the effective load capacitance C_{L1} and C_{L2} present is $C_{L1}/2$, assuming $C_{L1}=C_{L2}$. Extra capacitance between board traces that connect to the crystal increases the effective C_L.

Using external capacitors to get the correct frequency means that the internal caps must be set to minimum. For example, an application can use near minimum on-chip capacitance of approximately 2-3pF and an off chip capacitance of 7pF to provide C_L = 9pF to the crystal.

Only for CC13xx, Table 3-1 shows using external caps this way gives slightly worse frequency stability with temperature than using internal capacitors. Certain sub-1GHz users can need to use external load capacitors to reduce spurs at an offset of twice the crystal frequency from the RF carrier frequency.

Table 3-1. Using External Capacitor Results in Worse Frequency Stability Over Temperature

	9pF Internal C_L	Minimum Internal C_L, External C_L
Frequency variation –40°C to +90°C	Set by crystal	Set by crystal + 5ppm
Voltage accuracy, ppm/V	6.9	9

The following presents the relative advantages of crystals with different C_L values.

The disadvantages of lower C_L are as follows:

- Crystals with < 7pF C_L are more difficult to source with short lead times.
- Frequency becomes more sensitive to changes in board capacitance as C_L decreases. This is possible to meet frequency stability specifications with a C_L as low as 3pF.
- Lowering C_L results in degraded RF phase noise.

Advantages of lower C_L are as follows:

- Lower C_L causes a much faster start-up time. (Start-up time is proportional to $C_L{}^2$.)
- Lower C_L causes a faster amplitude control loop response time.
- Lower C_L is easier to use small size crystals (2.0 × 1.6 and so on) and maintain a start-up time at or less than 400µs. Start-up time worsens with smaller crystals due to an increase in L_M.

The internal load capacitance has no appreciable impact on the shape of the frequency vs temperature of the high frequency crystal. This can be seen by looking at the following two plots. Figure 3-2 shows the frequency versus temperature curve for the crystal using 13 different but closely spaced load capacitance. Each different load capacitance shifts the curve up or down, but does not change the overall shape of the curve. This can be seen by removing the offset of each curve, as shown in Figure 3-3.

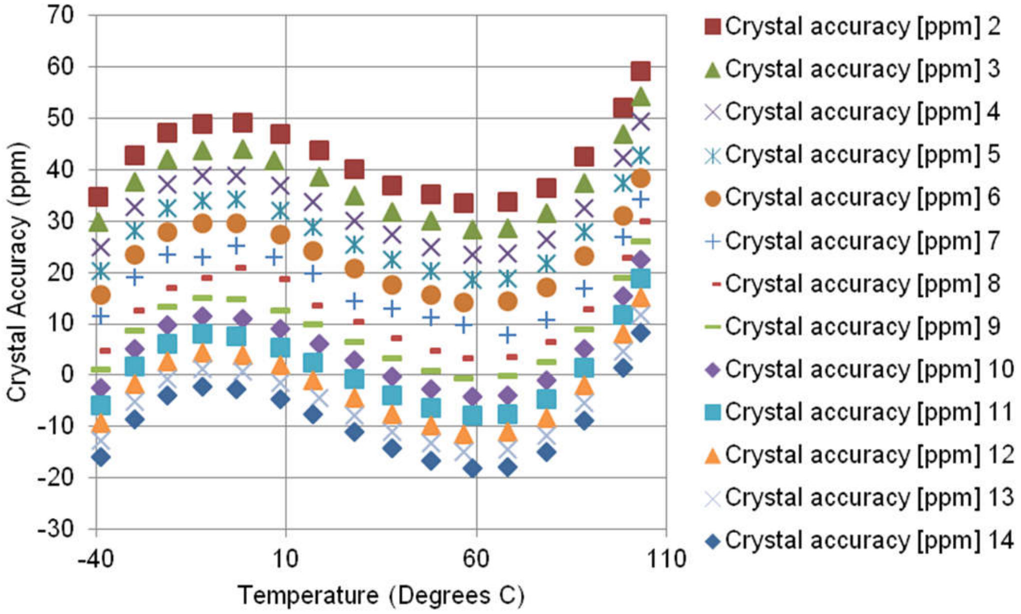

Figure 3-2. The Frequency vs Temperature Curve for the High Frequency Crystal for 13 Closely Spaced Load Capacitance Values

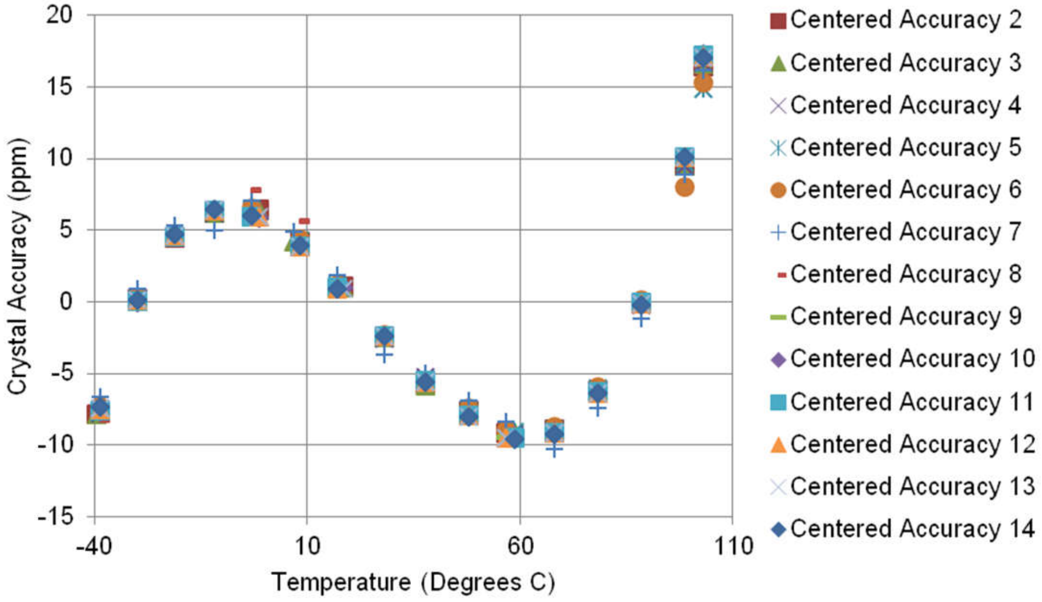

Figure 3-3. Removing the Offset of the Frequency vs Temperature Curves

Figure 3-3 shows that a change in the internal load capacitance does not influence the shape of the frequency vs temperature curve. This indicates that the internal load capacitors have minimal impact on this curve.

A method to change the on-chip load caps of the crystal is discussed in *CC13xx/CC26xx Hardware Configuration and PCB Design Considerations* application note.

3.4 ESR and Start-Up Time

ESR (equivalent series resistance) is a parameter of the crystal in the data sheet of the crystal. Negative resistance is a parameter of the complete oscillator circuit, including capacitor values, crystal parameters, and an on-chip circuit. To make sure of best start-up of the crystal oscillator, the negative resistance magnitude must be at least 3 times greater than R_N (see Equation 10 and Equation 11) during initial start up.

$$\mathrm{ESR} < \frac{|R_N|}{3} \tag{10}$$

$$R_N = \frac{-g_m}{(2\pi f)^2 (2C_L)^2} \tag{11}$$

If the negative resistance magnitude is not 3 times greater than ESR during initial start-up, then the oscillator does not operate at the best level or can fail to start in the presence of environmental changes or manufacturing variations in the crystal.

Note

Crystals with higher ESR typically result in longer start-up times than crystals with lower ESR. A higher-load capacitance decreases the negative resistance of the oscillator and increases the start-up time.

3.5 Drive Level and Power Consumption

The maximum drive level of a crystal is often specified in the data sheet of the crystal in µW. Exceeding this value can damage or reduce the lifetime the crystal. The CC13xx and CC26xx devices drive the crystal with a maximum $1.6V_{pp\_differential}$ for the 24MHz and 48MHz crystal and $600mV_{pp\_differential}$ for the 32.768kHz crystal. As Section 1.2.3 explains, Equation 5 gives the drive level in W.

A higher total capacitance load and ESR require more power to drive the crystal, increasing the power consumption of the oscillator. Because the 32.768kHz crystal is on for an extended period of time, this increase is important. Selecting a low ESR and low-C_L 32.768kHz crystal is important to achieve low-power consumption in a low-power mode.

Note

Do not use the internal DC-DC when applying a probe to the probe to the 24MHz or 48MHz crystal oscillator pins. Applying the probe can lead to the oscillator stopping and can lead to the internal DC-DC producing a high-output voltage that can damage the device.

3.6 Crystal Package Size

There are several different packages for crystals. The available board space and cost determines the package size used. Crystals with smaller packages have a higher ESR and motional inductance. These smaller packages cause a longer start-up time of the crystal oscillator. By choosing a crystal with a low C_L if a smaller package is required, this start-up time increase can be compensated.

4 PCB Layout of the Crystal

The layout of the crystal can reduce the parasitic capacitance and, more importantly, reduce noise from coupling on the input of the oscillators. Noise on the input of the oscillator can lead to severe side effects such as clock glitches, flash corruption, or system crashes because the CC26xx and CC13xx devices rely on the crystal oscillators as the high- and low-frequency system clock.

The following are a few recommendations for the layout of the crystals:

- Place the crystal as close as possible to the device to minimize the length of the PCB traces. (This placement reduces crosstalk and minimizes EMI.)
- TI recommends a solid ground plane under the crystal.
- Make sure no high-speed digital signals are close to the crystal to minimize cross-coupling of noise into the oscillator.

Figure 4-1 shows the top layer of the layout of the CC26xx reference design. The bottom layer is a solid ground plane. For more details, see the *SimpleLink™ CC2650 EVM Kit 4XD (CC2650EM-4XD) v1.0.3 Design Files*. The same crystal layout can be used with CC13xx device.

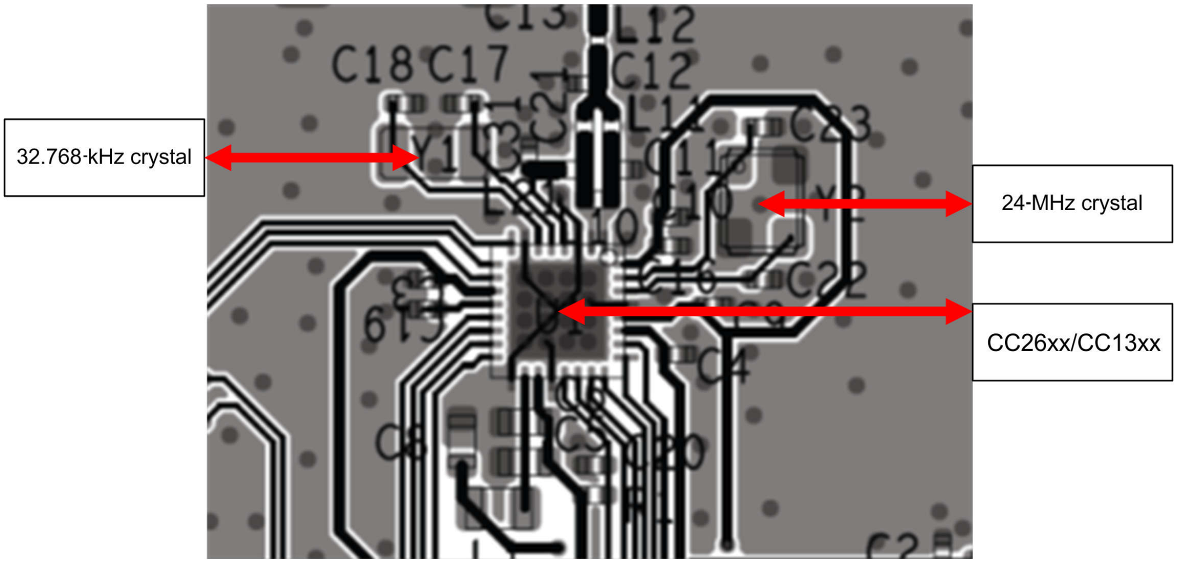

Figure 4-1. Layout of the CC26xx EVM

5 Measuring the Amplitude of the Oscillations of Your Crystal

Two functions exist in **CC26XX and CC13XX** for measuring the amplitude of the oscillations of the crystal, and comparing this amplitude to the expected amplitude. These functions are as follows:

- uint32_t OSCHF_DebugGetCrystalAmpslitude (void);
- uint32_t OSCHF_DebugGetExpectedAvarageCrystalAmplitude (void);

The first function inserted into a piece of code returns the amplitude of the crystal in mV. The second function returns the expected oscillation amplitude, also in mV. These are debug functions only. The first function uses an on-chip ADC to measure the amplitude of the crystal. If these functions return greatly different values, then the crystal can have a problem. The uncertainty of the first function is ± 50mV; a 50mV deviation from the expected value is not cause for concern.

5.1 Measuring Start-Up Time to Determine HPMRAMP1_TH and XOSC_HF_FAST_START

The following code can be used to measure the approximate turn on time of the high frequency crystal for CC26X2 and CC13X2 devices. This function works by counting the number of low frequency clock edges from the enabling of the high frequency clock to the high frequency clock being qualified. For more accurate results, external measurement equipment is required.

```
uint32_t OSCHF_DebugGetCrystalStartupTime( void )
{
   uint32_t lfEdgesFound = 0 ;
   // Start operation in sync with the LF clock
   HWREG( AON_RTC_BASE + AON_RTC_O_SYNCLF );
   OSCHF_TurnOnXosc();
   while ( ! OSCHF_AttemptToSwitchToXosc() ) {
      HWREG( AON_RTC_BASE + AON_RTC_O_SYNCLF );
      lfEdgesFound ++ ;
   }
   OSCHF_SwitchToRcOscTurnOffXosc();
   return ( lfEdgesFound );
}
```

For CC26XX and CC13XX, and CC26X2 and CC13X2 devices, the crystal startup time can also be measured using built in driverlib implementation of OSCHF_DebugGetCrystalStartupTime().

6 Crystals for CC13xx, CC26xx, CC23xx and CC27xx

Table 6-1 through Table 6-4 provide appropriate crystals for use with the CC devices.

Table 6-1. 48MHz Crystals for CC13x2, CC26x2 and CC23xx

Manufacturer	MPN	Package	ESR max [Ω]	CL [pF]	Tol [ppm]	Temp Tol [ppm]	Temp range [°C]	Compliant	Comment
KDS	DSX211S 7AF04800A1M	2016	30	8	±10	±40	-40/125	AEC-Q200	Tested by KDS on LAUNCHXL-CC26X2R1 and LP-EM-CC2340R5
Kyocera	CX2016DB 48000C0FPLC1	2016	30	7	±10	±20	-40/85		Used on LAUNCHXL-CC26X2R1
Kyocera	CX2016DB 48000C0FRLC1	2016	30	7	±10	±20	-40/105	AEC-Q200	Tested by Kyocera on LAUNCHXL-CC26X2R1
NDK	NX2016SA 48.000MHz EXS00A-CS05517	2016	40	7	±10	±30	-40/85		Used on CC26x2REM-7ID for characterization
TXC	8Y48072007	2016	40	8	-3/+7	-14/+12	-40/95		
Tai-Saw (TST)	TZ2365D	2016	40	7	±10	±25	-40/105	AEC-Q200	Used on CC26x2REM-7ID-Q1 for characterization

Table 6-2. 48MHz Crystals for CC23xx and CC27xx Only

Manufacturer	MPN	Package	ESR max [Ω]	CL [pF]	Tol [ppm]	Temp tol [ppm]	Temp range [°C]	Compliant	Comment
Epson	FA2016AA X1E000381A17100	2016	60	7	±10	±35	-40/125	AEC-Q200	Tested by Epson on LP-EM-CC2340R5
Kyocera	CX2016DB 48000C0WSRT1	2016	30	7		±40 Over all	-40/125	AEC-Q200	Tested by Kyocera on LP-EM-CC2340R5
NDK	NX2016SA 48.000MHz EXS00A-CS14953	2016	40	8		±40 Over all	-40/105		Tested by NDK on Launchpad LP-EM-CC2340R5_E3
NDK	NX1612SA 48MHz EXS00A-CS15039	1612	50	8		±40 Over all	-40/125	AEC-Q200	Tested by NDK on Launchpad LP-EM-CC2340R5_E3
Tai-Saw (TST)	TZ3908AAAO43	2016	30	7	±5	±30	-40/125	AEC-Q200	Used on Launchpad LP-EM-CC2340R5_E3 and characterization. This crystal is used on the CC2745R10-Q1 Launchpad
Murata	XRCGE48M000MXF1LR0	2016	60	7		±40 Over all	-40/125	AEC-Q200	Tested by Murata on Launchpad LP-EM-CC2340R5_E3

Table 6-3. 24MHz Crystals for CC13x0 and CC26x0

Manufacturer	MPN	Package	ESR max [Ω]	CL [pF]	Tol [ppm]	Temp tol [ppm]	Temp range [°C]	Compliant	Comment
Epson	TSX-3225 24.0000MF15X-AC3	3225	60	9	±10	±10	-40/85		Used in characterization (EMs)
Epson	TSX-3225 24.0000MF10Z-AC3	3225	60	9	±10	±10	-20/75		Similar spec to F15X, but narrower temperature range.
Epson	TSX-3225 X1E000021004800	3225	40	9	±10	±20	-40/105	AEC-Q200	CC2640Q1EM
NDK	NX2016SA 24MHz EXS00A-CS08891	2016	60	6	±10	±15	-30/85		Used in CC2640R2F WCSP char.
NDK	NX2016SA 24MHz EXS00A-CS07553	2016	60	7	±10	±15	-30/85		Tested by NDK
NDK	NX3225SA 24MHz EXS00A-CS07532	3225	50	9	±10	±15	-30/85		Tested by NDK
Kyocera	CX2016DB 24000C0WPRC1	2016	60	7	±10	±15	-40/85		Tested by Kyocera
Kyocera	CX2016SA 24000C0FRNC1	2016	30	7	±10	±25	-40/105	AEC-Q200	
TXC	8Q24030001	1612	70	5.8	±15	±15	-30/85		Tested by TXC

Table 6-3. 24MHz Crystals for CC13x0 and CC26x0 (continued)

Manufacturer	MPN	Package	ESR max [Ω]	CL [pF]	Tol [ppm]	Temp tol [ppm]	Temp range [°C]	Compliant	Comment
Murata	XRCGB 24M000FBP12R0	2016	80	6	±15	±20	-40/85		Tested by Murata

Table 6-4. 32.768kHz Crystals for CC13xx, CC26xx, CC23xx, and CC27xx

Manufacturer	MPN	Package	ESR max [Ω]	CL [pF]	Tol [ppm]	Parabolic coefficient [ppm/°C^2]	Temp range [°C]	Compliant	Comment
Epson	FC-135	3215	70k	7	±20	-0.04	-40/85		Lowest current consumption. Used in characterization (EMs)
Epson	FC-13A X1A000091001214	3215	70k	7	±20	-0.04	-40/125	AEC-Q200	Used on LaunchPad CC26x2REM-7ID-Q1_A1
Epson	FC2012AA X1A000181000318	2012	75k	7	±20	-0.04	-40/125	AEC-Q200	This crystal is used on the CC2745R10-Q1 Launchpad. Tested by Epson on LP-EM-CC2340R5
KDS	DST1610A 7BG03276AAC	1610	70k	7	±20	-0.04	-40/125	AEC-Q200	Tested by KDS on LAUNCHXL-CC26X2R1 and LP-EM-CC2340R5
NDK	NX3215SA 32.768kHz EXS00A-MU00529	3215	70k	7	±20	-0.04	-40/85		Lowest current consumption. Used in characterization
NDK	NX2012SA 32.768kHz EXS00A-MU00530	2012	80k	7	±20	-0.04	-40/85		
NDK	NX2012SA 32.768kHz EXS00A-MU01792	2012	120k	9	±20	-0.04	-40/125	AEC-Q200	Tested by NDK on Launchpad LP-EM-CC2340R5_E3
Seiko Instruments Inc.	SC-32S 6pF	3215	70k	7	±20	-0.03	-40/85		Tested by Seiko
Seiko Instruments Inc.	SC-20S 7pF	2012	70k	7	±20	-0.03	-40/85		Tested by Seiko
Seiko Instruments Inc.	SC-16S 7pF	1610	90k	7	±20	-0.035	-40/85		Tested by Seiko
Kyocera	ST3215SB 32768C0HPWBB	3215	70k	7	±20	-0.05	-40/85		Tested by Kyocera
Kyocera	ST2012SB 32768C0HPWB4	2012	70k	7	±20	-0.05	-40/85		Tested by Kyocera
Tai-Saw (TST)	TZ3359DAAO73	1610	120k	7	±20	-0.04	-40/125		Used on Launchpad LP-EM-CC2340R5_E3 and characterization
TXC	9H03270072	2012	90k	7	±20	-0.04	-40/105		

7 High Performance BAW Oscillator

The SimpleLink™ product family also has a high performance Bulk Acoustic Wave (BAW) oscillator offering that can be used to enable crystal-less radio operation. Multiple technical documents are available that describe this breakthrough technology on TI.com at *SimpleLink™ 32-bit Arm Cortex-M4F Multiprotocol 2.4GHz Wireless MCU with Crystal-less BAW Resonator*

8 CC23XX and CC27XX Software Amplitude Compensation

Overview

This section describes the software compensation and implementation details required to control the HFXT amplitude on CC23XX and CC27XX. This aims to do two things on the software level:

1. Adjust the reference current (IREF) for the HFXT to achieve an excellent amplitude.
2. Detect and handle fault conditions to make sure the system recovers gracefully.

Note

There is an optional boot-up compensation that can be configured on SysConfig to make sure that the crystal sufficiently adjusts the current to start the crystal for the first time. This does not include operation after standby.

Please check the documentation for these registers: HFXTFAULT, TRACKREFLOSS, and TRACKREFOOR for more information during debugging.

9 Internal Capacitor Array for CC23XX and CC27XX

Overview

The 48MHz HFXT (High-Frequency Crystal Oscillator) Capacitor Array is designed to fine-tune the frequency of the crystal by adjusting the load capacitance. This section provides an overview of the configuration, key considerations, and best practices.

The capacitor array is organized as 16 capacitors in series across 4 rows per pin, allowing for precise tuning of the load capacitance.

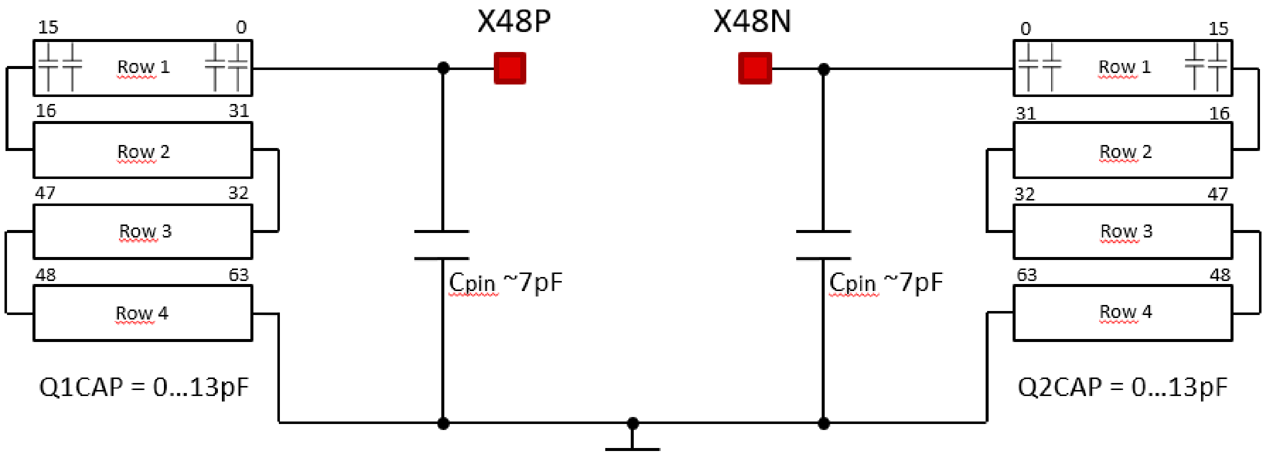

Figure 9-1. Internal Capacitor Array Diagram

Programming the Capacitor Array

The capacitor array is configurable through the syscfg file in the SDK under Device Configuration.

- Trim codes range from 0 to 63 (0x0 to 0x3F) per pin.

Note

Avoid using trim codes 16 and 48 to prevent a non-monotonic trim curve.

Load Capacitance Considerations

The total load capacitance affecting the crystal frequency consists of:

- Pin capacitance (≃7pF per pin)
- Capacitor array contribution (Q1CAP + Q2CAP, up to 13pF each)
- Additional contributions from PCB layout and package characteristics

Limitations

- Users cannot disable the capacitor array feature.
- If external load capacitors are used, then TI recommends to set Q1CAP and Q2CAP to 0 in the syscfg file. This results in an estimated total parasitic capacitance of approximately 3-4pF.
- There is a slight temperature dependence which can be more evident in temperature values above 105°C. This can be mitigated by accounting for the frequency shift since the effect is greatly predictable with structured behavior that is easily observable.

Internal Capacitor Array Values for CC23XX and CC27XX

Cap Array Value (Q1 = Q2)	Measured Capacitance on Reference Board for CC23xx (pF)	Measured Capacitance on Reference Board for CC27xx (pF)
1	3.7	3.9
2	3.7	4.0
3	3.8	4.1
4	3.9	4.1
5	4.0	4.2
6	4.1	4.3
7	4.1	4.4
8	4.2	4.4
9	4.3	4.5
10	4.4	4.6
11	4.4	4.7
12	4.5	4.7
13	4.6	4.8
14	4.6	4.9
15	4.7	5.0
16	4.7	5.0
17	4.8	5.0
18	4.9	5.1
19	5.0	5.2
20	5.1	5.3
21	5.2	5.4
22	5.3	5.5
23	5.3	5.6
24	5.4	5.7
25	5.5	5.8
26	5.6	5.9
27	5.7	6.0
28	5.8	6.1
29	5.9	6.2
30	6.0	6.3
31	6.1	6.4
32	6.3	6.6
33	6.4	6.7
34	6.5	6.8
35	6.6	6.9
36	6.7	7.0
37	6.8	7.2
38	6.9	7.3
39	7.1	7.4

Cap Array Value (Q1 = Q2)	Measured Capacitance on Reference Board for CC23xx (pF)	Measured Capacitance on Reference Board for CC27xx (pF)
40	7.2	7.5
41	7.3	7.6
42	7.4	7.8
43	7.5	7.9
44	7.6	8.0
45	7.7	8.1
46	7.8	8.2
47	7.9	8.3
48	7.9	8.3
49	8.1	8.5
50	8.3	8.7
51	8.4	8.8
52	8.6	9.0
53	8.7	9.2
54	8.9	9.3
55	9.0	9.5
56	9.2	9.7
57	9.3	9.8
58	9.5	10.0
59	9.6	10.1
60	9.8	10.3
61	9.9	10.5

For further details on tuning the crystal, please contact technical support.

10 Internal Capacitor Array for CC13xx and CC26xx

Overview

The CC26x2 and CC13x2 radios require a 24MHz or 48MHz crystal as a frequency reference. However, spurs at multiples of 48MHz can occur due to the large current flow between the crystal and XOSC tuning capacitors. These spurs can cause interference by creating voltage drops on shared power rails with the PA and VCO. Reducing the XOSC tuning capacitors to zero decreases these spurs by approximately 5dB for the largest spur.

Load Capacitance Considerations

The internal capacitor array is generally sufficient, but for systems requiring compliance with ARIB STD T-108 and Chinese regulations (470–510MHz), as well as when using the +20dBm PA, external crystal loading capacitors are recommended. Setting the internal XOSC tuning capacitors to zero in these cases helps minimize spurs. The system allows for adjustments using an offset value, which can be positive or negative, to fine-tune the capacitance.

Limitations

The internal capacitor array cannot be fully disabled unless the cap-array delta is set at or below the lowest supported value. The actual resulting capacitance includes parasitic contributions, so the lowest setting does not equate to 0pF. To verify oscillator accuracy, an unmodulated carrier wave must be measured using a spectrum analyzer. SmartRF™ Studio can be used for on-the-fly tuning of the load capacitance before finalizing values in software.

Table 10-1. Internal Capacitor Array Delta for CC13XX and CC26XX

Measured Capacitance on Reference Board (pF)	CCFG Delta Value for CC13x0/CC26x0 QFN	CCFG Delta Value for CC2640R2F WCSP	CCFG Delta Value for CC13x1/CC26x1 QFN	CCFG Delta Value for CC13x2/CC26x2 QFN	CCFG Delta Value for CC13x4/CC26x4 QFN
2.1	< -55	< -28	< -40	< -40	< -40
2.1	-55	-28	-40	-40	-40
2.2	-54	-27	-39	-39	-39
2.3	-53	-26	-38	-38	-38
2.4	-52	-25	-37	-37	-37
2.5	-51	-24	-36	-36	-36
2.6	-50	-23	-35	-35	-35
2.7	-49	-22	-34	-34	-34
2.7	-48	-21	-33	-33	-33
2.8	-47	-20	-32	-32	-32
2.9	-46	-19	-31	-31	-31
3.0	-45	-18	-30	-30	-30
3.1	-44	-17	-29	-29	-29
3.2	-43	-16	-28	-28	-28
3.3	-42	-15	-27	-27	-27
3.4	-41	-14	-26	-26	-26
3.4	-40	-13	-25	-25	-25
3.6	-38	-12	-24	-24	-24
3.7	-37	-11	-23	-23	-23
3.8	-36	-10	-22	-22	-22
3.9	-35	-9	-21	-21	-21
4.0	-34	-8	-20	-20	-20
4.1	-33	-7	-19	-19	-19
4.3	-32	-6	-18	-18	-18

Table 10-1. Internal Capacitor Array Delta for CC13XX and CC26XX (continued)

Measured Capacitance on Reference Board (pF)	CCFG Delta Value for CC13x0/CC26x0 QFN	CCFG Delta Value for CC2640R2F WCSP	CCFG Delta Value for CC13x1/CC26x1 QFN	CCFG Delta Value for CC13x2/CC26x2 QFN	CCFG Delta Value for CC13x4/CC26x4 QFN
4.4	-31	-5	-17	-17	-17
4.5	-30	-4	-16	-16	-16
4.6	-29	-3	-15	-15	-15
4.7	-28	-2	-14	-14	-14
4.8	-27	-1	-13	-13	-13
5.0	-26	0	-12	-12	-12
5.1	-25	1	-11	-11	-11
5.2	-24	2	-10	-10	-10
5.3	-23	3	-9	-9	-9
5.5	-21	4	-8	-8	-8
5.6	-20	5	-7	-7	-7
5.8	-19	6	-6	-6	-6
5.9	-18	7	-5	-5	-5
6.1	-17	8	-4	-4	-4
6.2	-16	9	-3	-3	-3
6.4	-15	10	-2	-2	-2
6.5	-14	11	-1	-1	-1
6.7	-13	12	0	0	0
6.8	-12	13	1	1	1
7.0	-11	14	2	2	2
7.1	-10	15	3	3	3
7.3	-9	16	4	4	4
7.4	-8	17	5	5	5
7.6	-7	18	6	6	6
7.7	-6	19	7	7	7
7.9	-5	21	8	8	8
8.2	-4	22	9	9	9
8.4	-3	23	10	10	10
8.6	-2	24	11	11	11
8.8	-1	25	12	12	12
9.0	0	26	13	13	13
9.2	1	27	14	14	14
9.4	2	28	15	15	15
9.6	3	29	16	16	16
9.8	4	30	17	17	17
10.1	5	31	18	18	18
10.3	6	32	19	19	19
10.5	7	33	20	20	20
10.7	8	34	21	21	21
10.9	9	35	22	22	22
11.1	10	36	23	23	23
11.1	> 10	> 36	> 23	> 23	> 23

11 Summary

TI’s CC13xx, CC26xx, CC23xx, and CC27xx families of low-power wireless MCUs rely on integrated 24MHz or 48MHz high-frequency oscillators (XOSC-HF or HFXT) as reference clocks for RF and system functions. Accurate clock sources are crucial for maintaining RF performance, regulatory compliance, and efficient system operation. In power-down mode, the high-frequency oscillator is typically off, and a 32.768kHz low-frequency oscillator (XOSC-LF or LFXT) maintains system timing, particularly for time-synchronized protocols like Bluetooth Low Energy. These oscillators use a Pierce architecture, with a crystal and associated capacitors forming a pi filter to stabilize frequency.

Key factors in selecting crystals include equivalent series resistance (ESR), motional inductance, drive level, and capacitive loading. ESR, which represents the crystal’s resistance at resonance, must be low enough to make sure of reliable startup and efficient operation. The crystal’s drive level, defined in microwatts, must not exceed manufacturer specifications to avoid damage. The transconductance (gm) of the oscillator circuit determines the ability to drive the crystal, with CC23xx or CC27xx featuring 19mS gm for high-frequency oscillators, CC13xx or CC26xx at 7mS, and low-frequency oscillators at 30µS. Start-up time depends on negative resistance, motional inductance, and overall circuit conditions.

Frequency accuracy depends on production tolerance, temperature stability, aging, and frequency pulling due to mismatched load capacitance. Load capacitance (CL) is critical for verifying correct oscillation frequency, factoring in both on-chip and external capacitors. Crystals must be chosen to meet device specifications, balancing low-capacitive loading for better power efficiency with stability against environmental variation. To make sure of reliable startup, the negative resistance must be at least three times the ESR. Excessive ESR can lead to longer startup times.

Optimizing crystal selection involves trade-offs between size, performance, and cost. Choosing a crystal with low motional resistance, low motional inductance, and appropriate capacitive loading improves start-up time and reduces power consumption. While a list of recommended crystals is provided, selection is not restricted to those alone, as long as key specifications are met. External capacitors can be used to fine-tune CL if internal capacitance settings are minimized. Proper crystal selection is essential for maintaining stable operation and efficient performance in battery-powered wireless applications.

12 References

1. IEEE, Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs), 802.15.4-2006, webpage
2. Bluetooth, Bluetooth Core Specifications, Version 4.2, webpage
3. Texas Instruments, *CC13xx/CC26xx Hardware Configuration and PCB Design Considerations*, application note.
4. Texas Instruments, *CC2650 SimpleLink™ Multistandard Wireless MCU* , data sheet
5. Texas Instruments, *SimpleLink™ CC2650 EVM Kit 4XD (CC2650EM-4XD) v1.0.3 Design Files*
6. Texas Instruments, *CC13x0, CC26x0 SimpleLink™ Wireless MCU*, technical reference manual

13 Revision History

Changes from Revision K (April 2024) to Revision L (April 2025)	**Page**
• Added the CC27xx Family	1
• Changed and added the estimated negative resistance for each device family	4
• Added the TI-characterized values for 48MHz	5

Changes from Revision J (August 2021) to Revision K (April 2024)	**Page**
• Added crystals on Table 6-1, Table 6-2, and Table 6-4 in Section 6	16

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