Application Note

How to port a product design from CC1310 to CC1311 and the 345/433/915MHz multi-band hybrid system reference design

Shuyang Zhong & Island Wei

ABSTRACT

This document was translated from a simplified Chinese source. (ZHCAG46)

Due to the increase in Flash, users can do OTA upgrades to applications using only on-chip Flash without requiring external Flash expansion, further reducing the BOM. In addition, if customers require greater transmission distance, TI has introduced the P version (Power Enhanced) on the CC1311, capable of achieving transmit power up to +20dBm.

This article describes how to port a CC1310-based project to the CC1311 platform by introducing development tools that work with the CC1311, experimenting with the Collector and Sensor example projects in the TI 15.4 protocol stack.

The main contents of this article include:

1. How to port a product design from CC1310 to CC1311
2. How to use the CC1311/CC110L combination to implement a multi-function system at 915MHz/433MHz/345MHz

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1 How to port a product design from CC1310 to CC1311

1.1 Hardware porting

To minimize porting complexity for customers, the TI SimpleLink family ensures pin-to-pin compatibility between chips of the same package and version. This means upgrading from CC1310 RGZ (7mm × 7mm) VQFN to CC1311R3 RGZ (7mm × 7mm) VQFN requires no PCB redesign — only the crystal oscillator needs replacement. It is important to note that while the CC1311P RGZ shares the same package as the CC1310R RGZ, the inclusion of an internal PA means the R and P versions are not pin-to-pin compatible. A new PCB design is required.

CC1311 comprises two versions: CC1311R3 and CC1311P3. Where the RGZ package (7x7mm QFN) of CC1311R3 is pin to pin compatible with the identically packaged CC1310. If CC1310 in the RGZ package was previously used, the pin to pin can be ported directly to CC1311R3 without any changes to the PCB layout.

In terms of peripheral circuitry, the only change is the high-speed crystal oscillator. The CC1311 requires a 48MHz crystal oscillator to provide the system clock, while the CC1310 uses 24MHz.

For specific hardware migration guidelines, refer to Hardware Migration From CC1310 to CC1312R. The document title includes CC1312R because the CC1312R chip is also compatible with CC1310 and CC1311. Consequently, this document may be directly used as a guide for porting from CC1310 to CC1311R.

If the CC1311P3 version is selected, the P version incorporates an integrated power amplifier. Therefore, it cannot be directly substituted for the CC1310 on a pin to pin basis. For the P version of the hardware design, refer to CC13xx/CC26xx Hardware Configuration and PCB Design Considerations document.

1.2 Software porting

The overall software architecture of CC1310 and CC1311 is the same, but there are some software differences that arise during the iteration of SDK. In this section, we first list the differences between the two software from the perspective of the overall software architecture, so that developers can grasp the overall software porting task. In the next chapter, we will explain the specific porting process with examples.

The software for the CC1310 and CC1311 primarily differs in the following respects:

- SysConfig
- TI-RTOS version
- Peripheral driver (including GPIO and UART)

1.2.1 System Configuration (SysConfig)

Beginning with CC13x2 generation of chips, SDK introduced the graphical code configuration tool SysConfig to assist in generating portions of code related to both the chip hardware and the protocol stack. The software engineering for CC1311 is also based on the SysConfig tool. The CC1310 SDK continues to employ the traditional full-code approach. Therefore, when porting from CC1310 to CC1311, it is essential to identify which codes are generated by SysConfig and migrate these codes to the SysConfig configuration.

Let's take a look at the list of files generated by SysConfig in the CC1311 engineering to explain what SysConfig does. Taking collector_LP_CC1311P3_tirtos7_ticlang project as an example, open the collector.syscfg in CCS by double-clicking. Click the Generated Files icon in the upper-right corner to preview the list of files generated by SysConfig:

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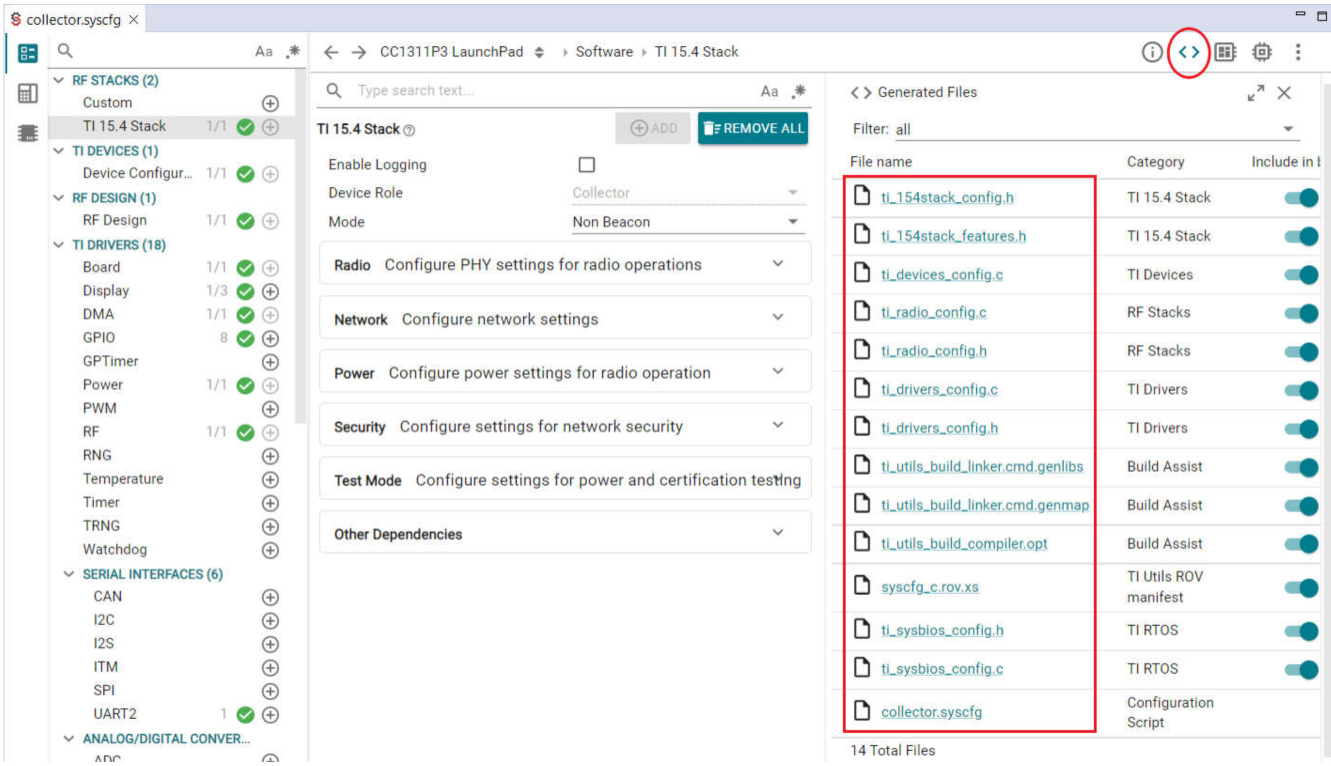

SysConfig generates a total of 14 files, the main ones related to the user software are .c and .h files, and the other files are engineering configuration and debugging files. The following table summarizes the function of SysConfig-generated code and the corresponding location of this portion of the code in the CC1310 engineering:

SysConfig generated files	Function of the code	Corresponding file within the CC1310 engineering
ti_154stack_config.h ti_154stack_features.h	TI15.4 protocol stack configuration	Application/subg/config.h Application/subg/features.h
ti_devices_config.c	Chip CCFG configuration	ccfg.c
ti_radio_config.c ti_radio_config.h	RF physical layer configuration	Application/MAC/LowLevel/mac_settings.c Application/MAC/LowLevel/mac_settings.h
ti_drivers_config.c ti_drivers_config.h	Peripheral drive configuration	CC1310_LAUNCHXL.c CC1310_LAUNCHXL.h
ti_sysbios_config.c ti_sysbios_config.h	TI-RTOS configuration	app.cfg

Please refer to SysConfig Migration section in the CC1311 SDK documentation for more detailed migration steps.

1.2.2 Port TI-RTOS to TI-RTOS 7

The software engineering for both CC1310 and CC1311 relies on the TI-RTOS real-time operating system. The TI-RTOS version has been upgraded since CC1311 SDK 5.30 version. Currently, TI-RTOS 7 is used on CC1311 and the original TI-RTOS on CC1310., without a version number.

Compared to TI-RTOS, TI-RTOS 7 introduces the following key upgrades:

- TI-RTOS 7 generates the configuration code through SysConfig
- TI-RTOS 7 improves compilation speed by removing its dependency on the XDSTools tool for compilation
- TI-RTOS 7 consumes less flash and RAM
- TI-RTOS 7 enhances the debug experience by directly entering kernel functions for single-step debugging

More detailed updates can be found at the following links:

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[FAQ] Why use TI-RTOS7? - Sub-1 GHz forum - Sub-1 GHz - TI E2E support forums

The biggest difference for users upgrading from CC1310 is that the related configuration of TI-RTOS 7 is generated by SysConfig, replacing the previous cfg configuration file. SysConfig is covered already in section 2.2.1. Detailed TI-RTOS migration steps are also available in the CC1311 SDK:

TI-RTOS to TI-RTOS7 Migration

In addition to this, some RTOS-related APIs have changed in the routine. The CC1311 adds a layer of DPL (Driver Porting Layer) for compatibility with different RTOS operating systems and uses the DPL API in routines instead of the original TI-RTOS API. Thus, you should be aware of the following API changes when porting:

- The Clock Module API, including the Clock_Struct structure and Clock_getTicks() etc., should be replaced with ClockP_Struct and ClockP_getTicks();
- The API in util_timer.c, such as Timer_start(), Timer_stop(), and so on, should be replaced with UtilTimer_start(), UtilTimer_stop(), and so on.

For a detailed description of the DPL API, refer to the Driver Porting Layer section of SimpleLink MCU SDK Driver API Reference document.

1.2.3 Peripheral driver code porting

Both CC1310 and CC1311 peripheral drivers are based on TI Drivers API. During the TI Drivers iteration, some of the driver code has changed, mainly GPIO and UART sections.

1.2.3.1 Port PIN driver to GPIO driver

In the C1310 SDK, the GPIO driver code is based on the PIN driver and GPIO driver. The CC1311 SDK has consolidated two sections of driver codes into a single and more standardized GPIO driver (GPIO++ driver).

The PIN driver is no longer supported in CC1311, so all calls to the PIN driver in CC1310 need to be ported. Refer to GPIO++ Driver Porting Guide for detailed porting steps.

1.2.3.2 Port UART driver to UART2 driver

The UART driver has also been upgraded from the UART driver to the UART2 driver in the C1311 SDK. Please note that UART2 in this designation is a renaming only to distinguish between older versions of the software and is not associated with the number of UART in the hardware. Compared to the legacy UART driver, the primary enhancement of the UART2 driver is its utilization of DMA for UART transmission and reception. This reduces the CPU processing burden during data transfer, thereby improving overall program efficiency. The porting steps from UART driver to UART2 driver can be found in UART to UART2 Porting Guide.

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2 How to use the CC1311/CC110L combination to implement a multi-function system at 915MHz/433MHz/345MHz

2.1 Solution overview

Today, in Sub1G group devices, 868MHz/915MHz is comparatively busier than 345MHz. When designing gateways requiring compatibility with established designs, 345MHz holds significant market share in existing solutions such as Honeywell 5800 series, 2GIG, and Qolsys. The design supports OOK modulators and switch upper limits to accommodate 433MHz within the same RF path as SPDT. For such scenarios, we recommend employing a CC1311+CC110L hybrid design to fulfill these requirements. We recommend the SPI interface between CC1311 and CC110L, and we have all the documentation for CC110L in the data sheet, including the documentation for the SPI interface (Chapter 5.5, 4-wire SPI).

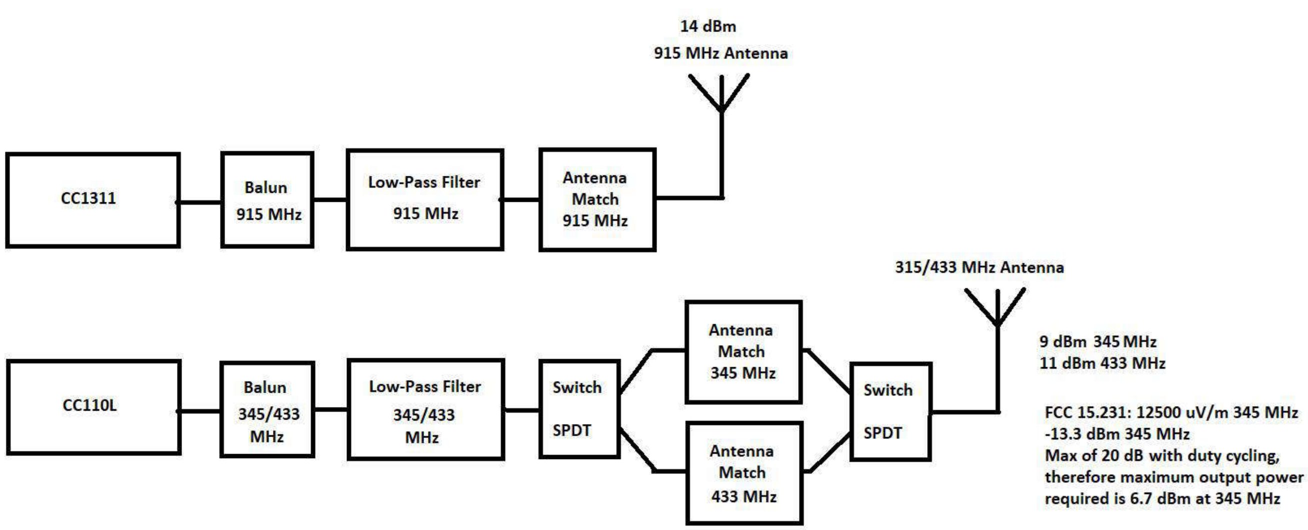
The goal of this hybrid system is to use the TI 15.4 protocol stack on 868/915MHz, the CC110L supports OOK modulation of Honeywell 5800 series sensors on 345MHz. It features only two antenna paths and must comply with FCC regulations.

According to FCC 15.231, the maximum output power is 12500uV/m at 345MHz. This correlates to -13.3dBm. Even with a maximum load cycle utilization of +20dB, this yields a maximum output power of +6.7dBm, which is permissible for very short packet lengths. Longer packet lengths and output power are further reduced under FCC regulations.

The output power of CC110L at 345MHz is +12dBm, much greater than +6.7dBm. Since dual-band operation at 345MHz and 433MHz is critical, users should not need 12/14dBm output power. Therefore, 345/433MHz antennas must feature two different antenna matches. Depending on the size of the GND plane, antenna size, and location, the antenna bandwidth for small devices is typically confined to 10–20MHz range. Therefore, two antenna matches are required to cover 345MHz and 433MHz.

Under optimal antenna matching at 345MHz and 433MHz, employing a single physical antenna will yield greater radiated output power than using individual antennas. The block diagram below uses only one antenna at 345MHz and 433MHz, as the antenna will be physically large. That is, only one antenna (345/433MHz) is used instead of two 345MHz and 433MHz antennas. If two antennas can be used to handle 345MHz and 433MHz, only one SPDT switch is required.

The RF design requires an optimal output of 14dBm at 345MHz, while the RF specification mandates >10dBm at 433MHz. We recommend the following topology:



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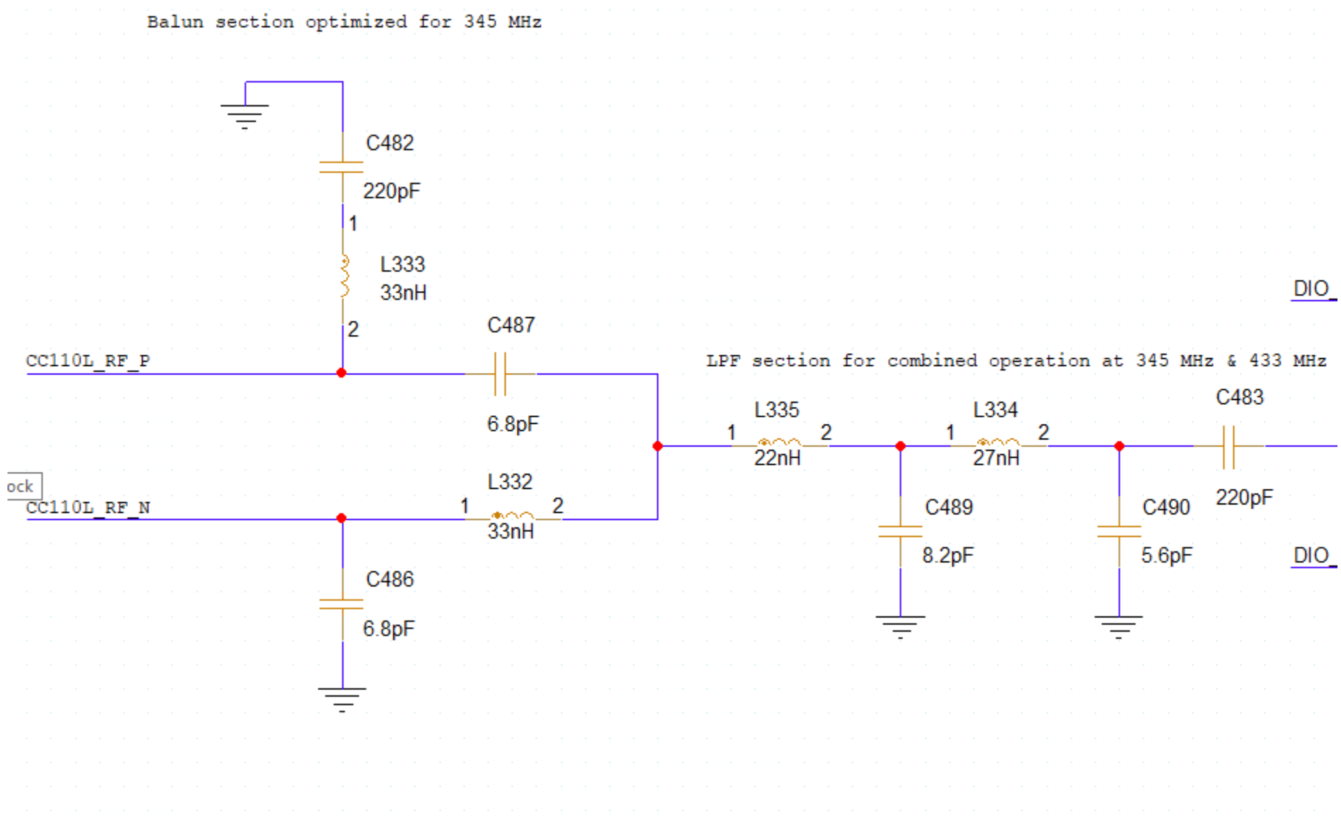
2.2 RF topology design recommendations and BOM

The BOM is primarily optimized for 345MHz, but some configuration is still required at 433MHz.



This BOM allows 12dBm at 345MHz and 433MHz. When operating at 345MHz, the LPF could always be made more stringent, but this would begin to reduce output power at 433MHz. If you add the LPF to 345MHz, the output power at 433MHz will drop to about 8dBm, but the harmonics in both bands will improve, especially 345MHz.

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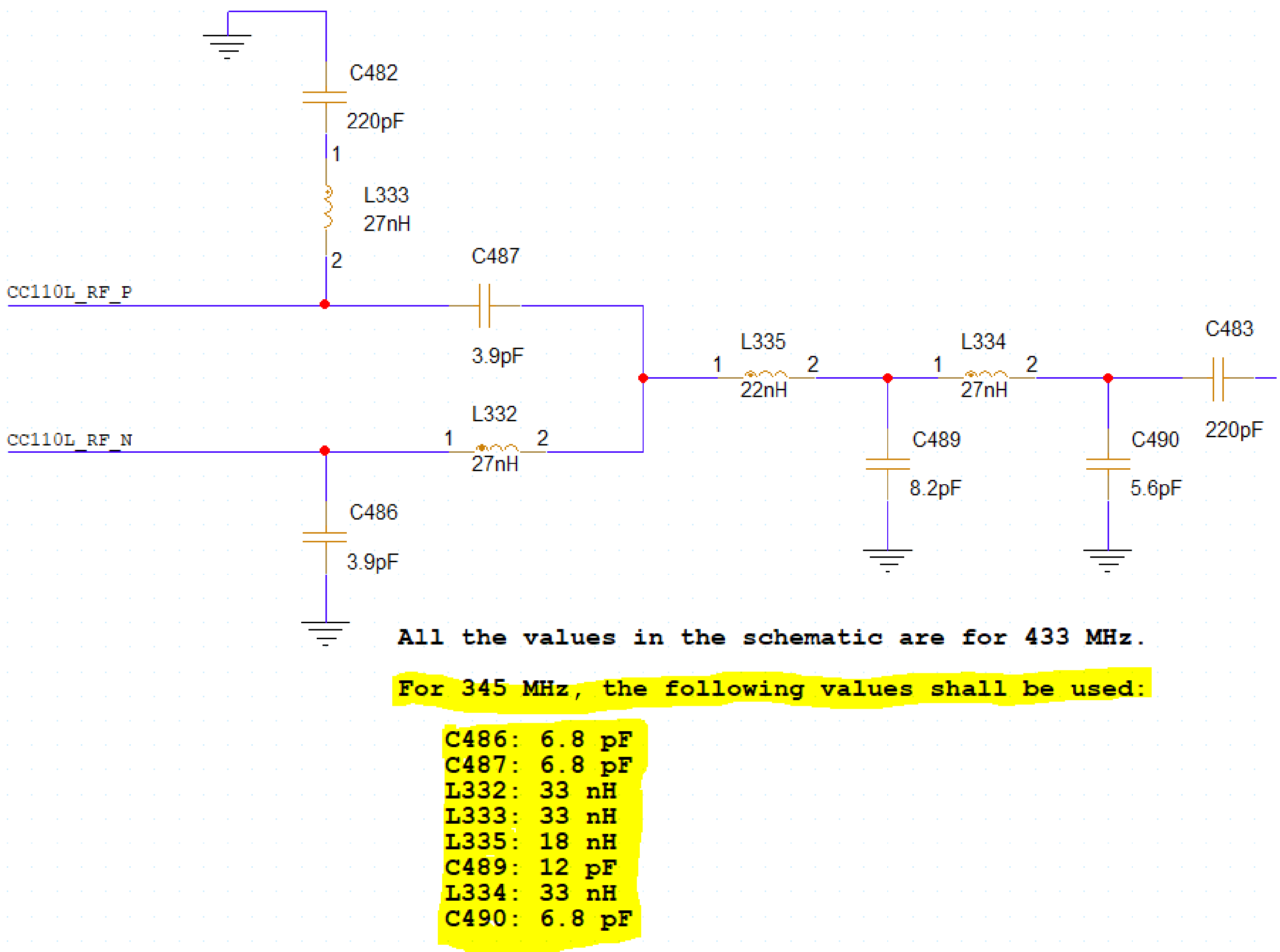
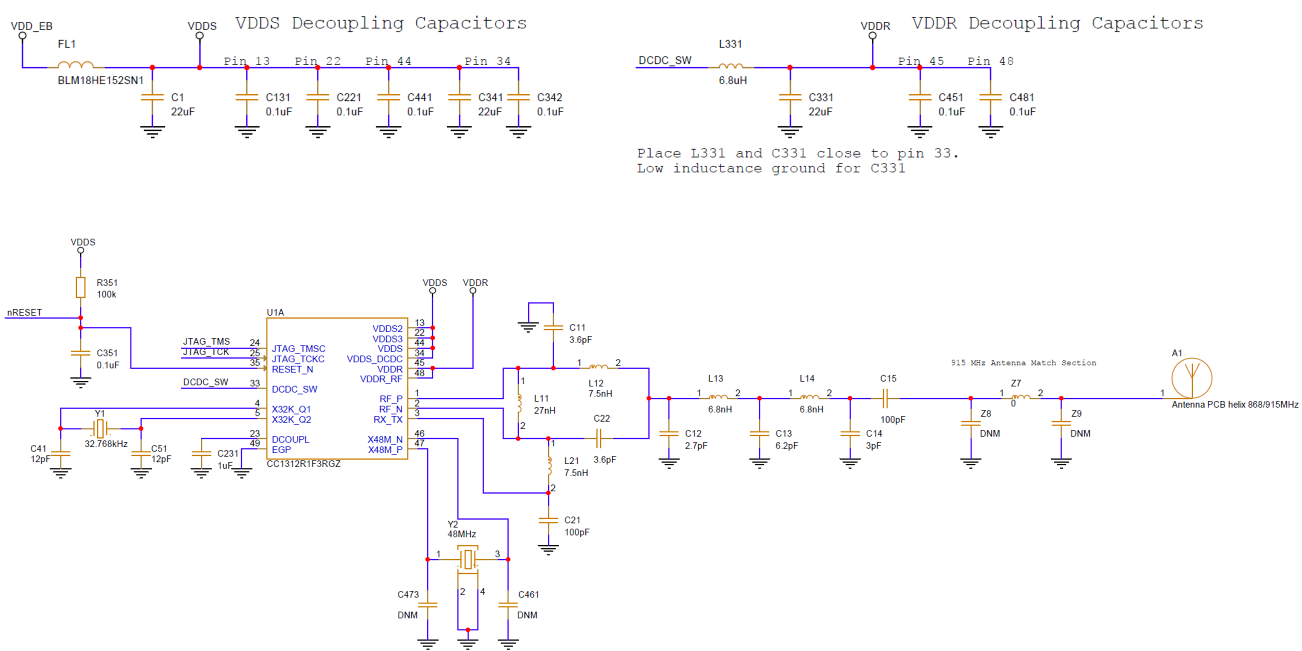


2.3 Layout design

2.3.1 CC1311 section



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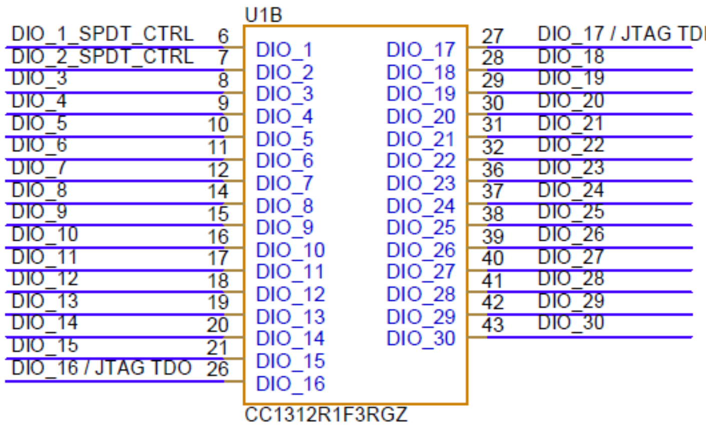
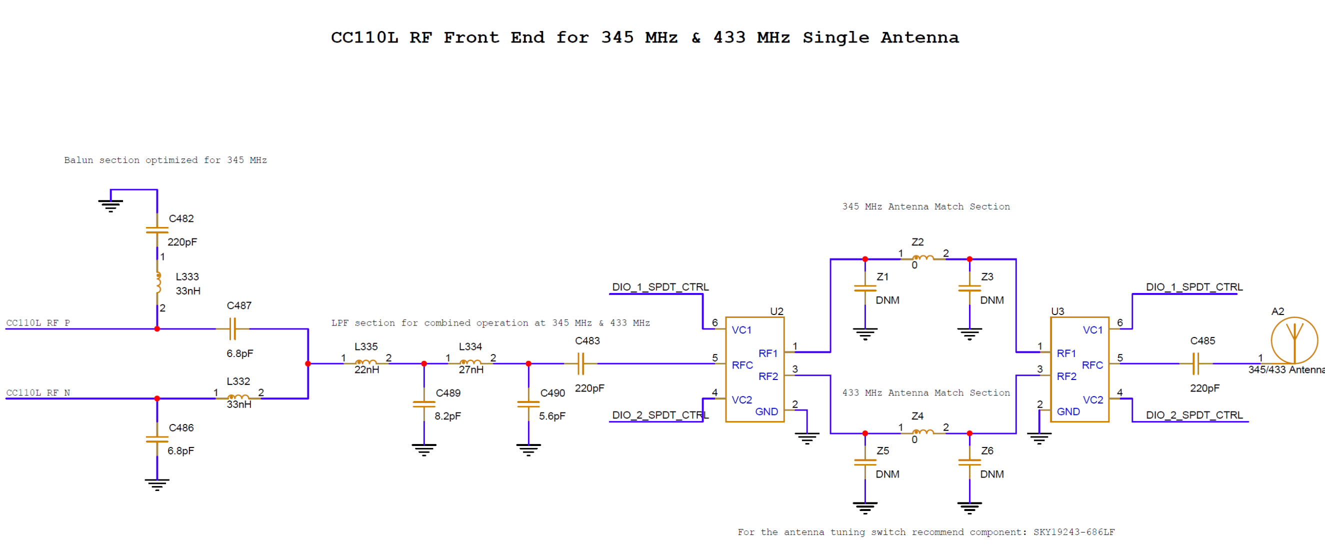


2.3.2 CC110L section



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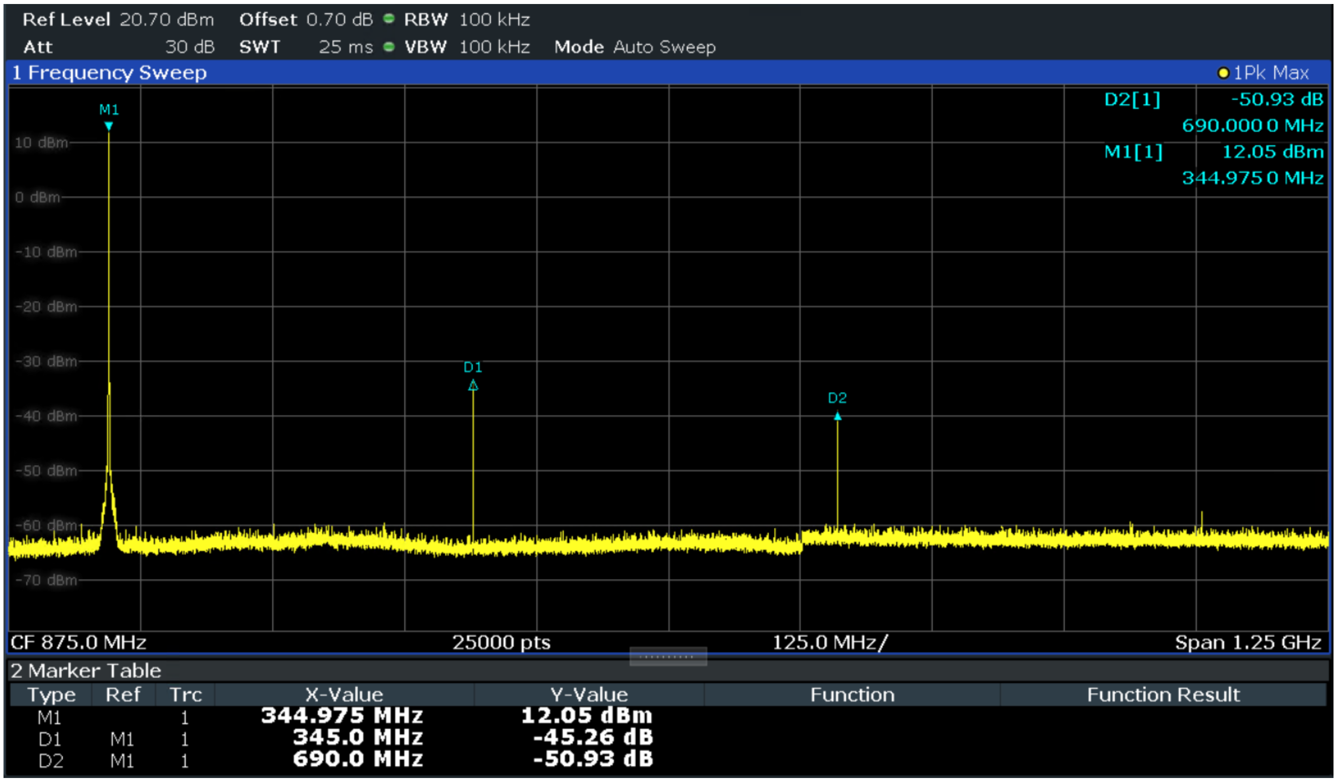
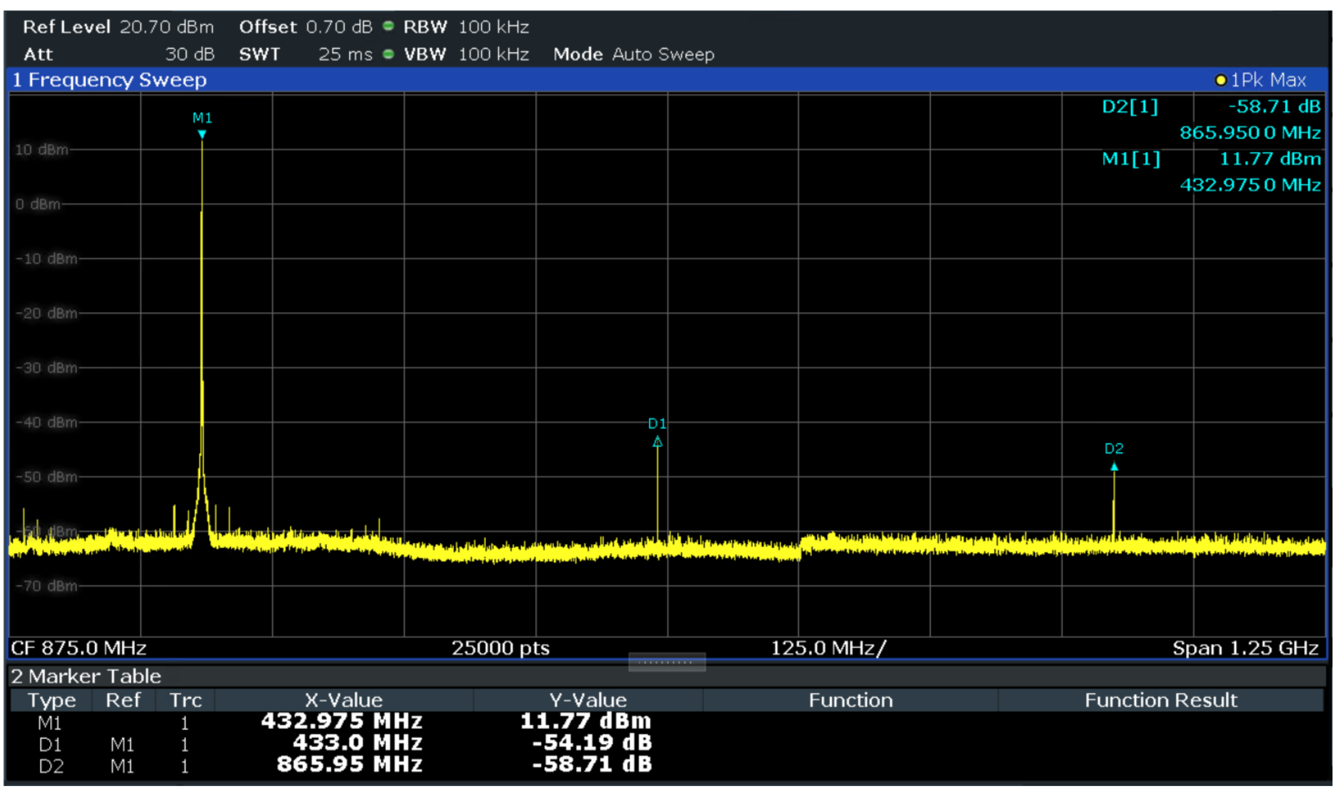
2.4 Test results

345MHz waveform following BOM modification in the BALUN section; 433MHz output frequency with PA Setting = 0xC2.



345MHz waveform following BOM modification in the BALUN section; 433MHz output frequency with PA Setting = 0xC0.



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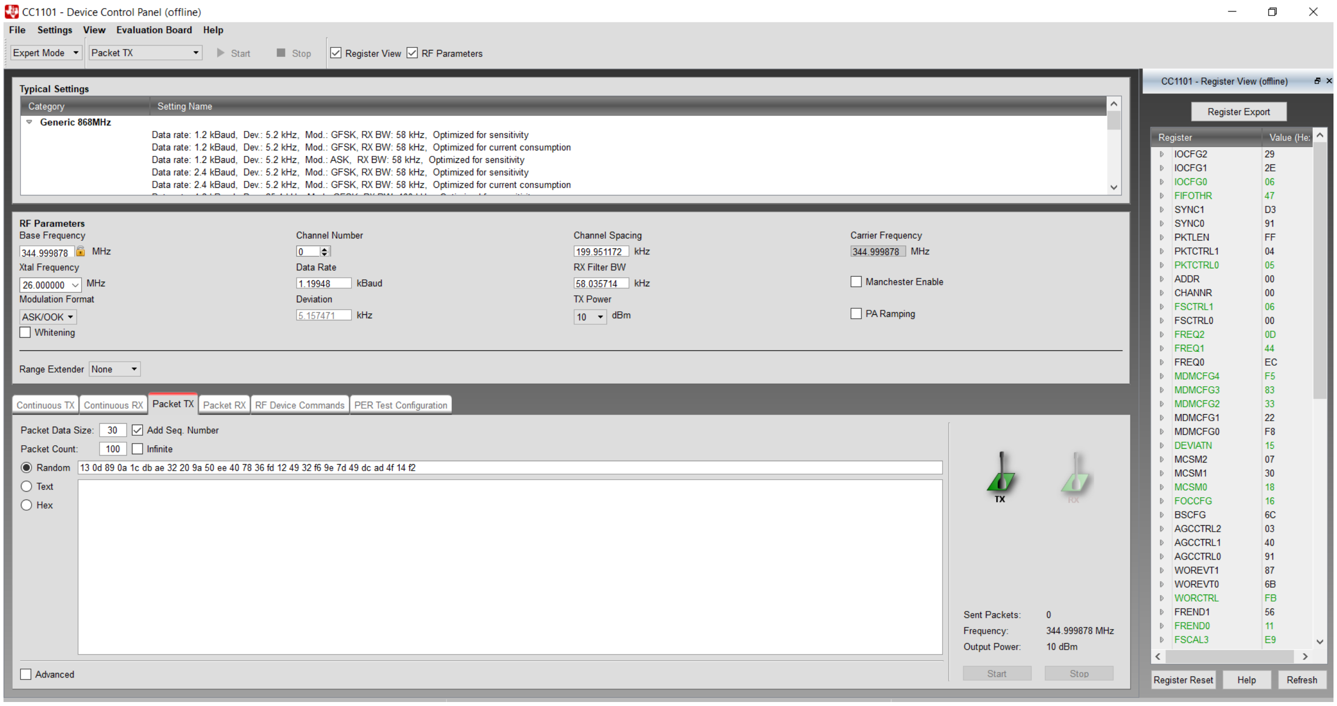
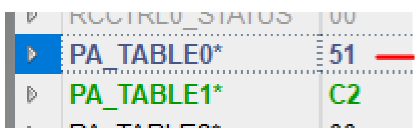
In summary, the PA register shall be set to 0xC2.



OOK is the simplest form of ASK modulation supported by CC110L. Here, the name just changed from ASK/OOK for CC1101 to OOK for CC110L. We tested in the laboratory by altering the modulation depth amplitude to 0.5. This should merely involve altering PA_TABLE0 register. Setting it to 0x51 yields an output power of 0dBm for 0 bit. In order to change the power of 0 bit PA_TABLE0, it needs to be modified. By default, it is set to 0x00, which means the PA is off. Finally, we got a sensitivity of -104.5dBm (1%BER) at your suggested matching conditions (OOK/1.2kbps/RXB 58kHz) in 345MHz band.

You can configure the modulation of the CC110L using Smart RF Studio, please read app note for OOK adjustments. The default configuration in Smart RF Studio is for (G)FSK not for OOK.



The following figure is a waveform of ASK modulation at 10kbps for this design topology:

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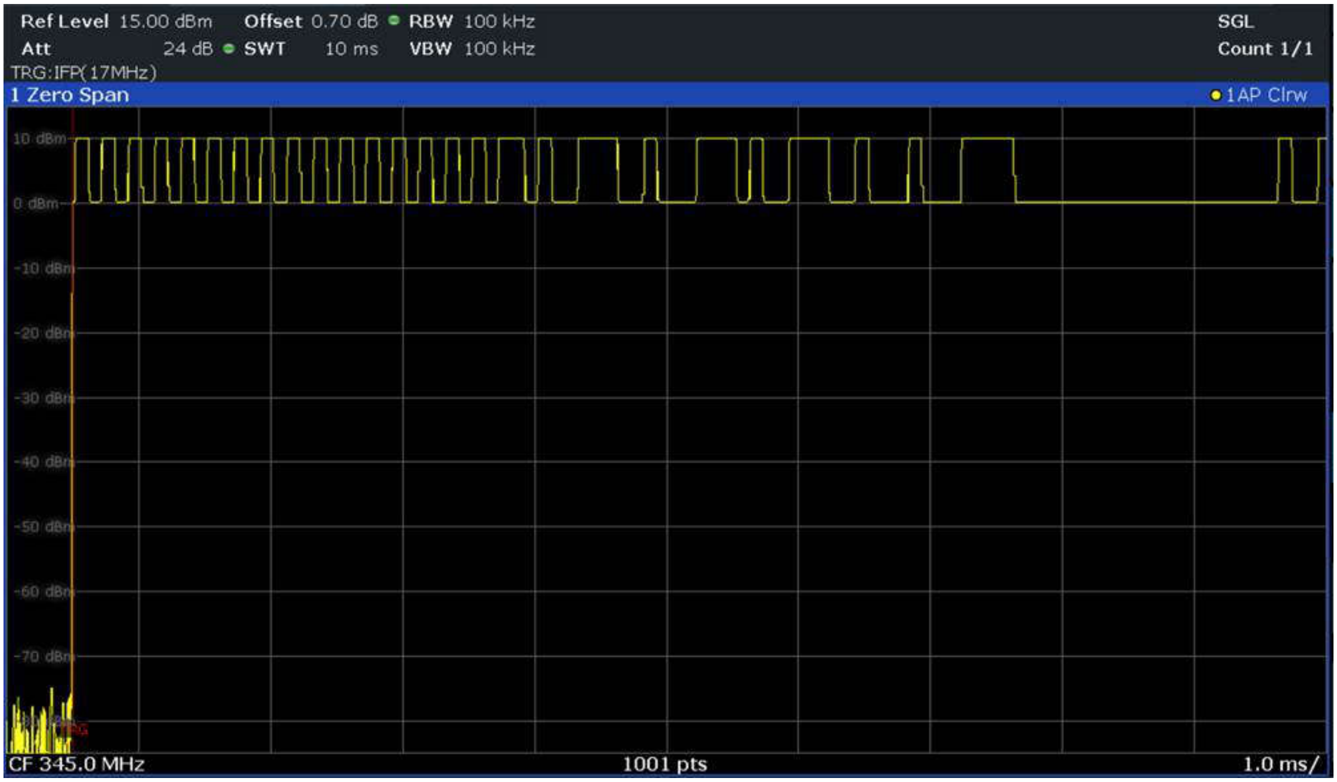

3 Reference links

- CC1311R3
- CC1311P3
- CC110L
- Smart RF Studio 7

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