

TI-RSLK

Texas Instruments Robotics System Learning Kit



TEXAS INSTRUMENTS

Module 18

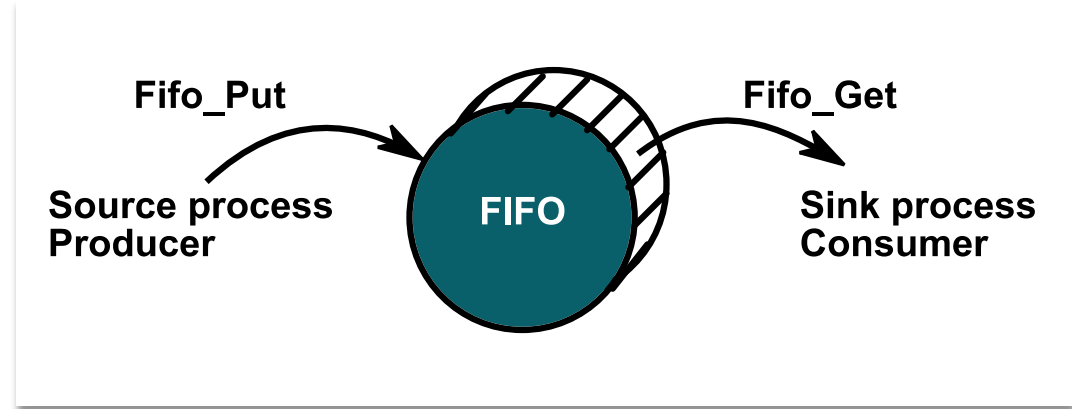
Lecture: Serial Communication - FIFO



Serial Communication

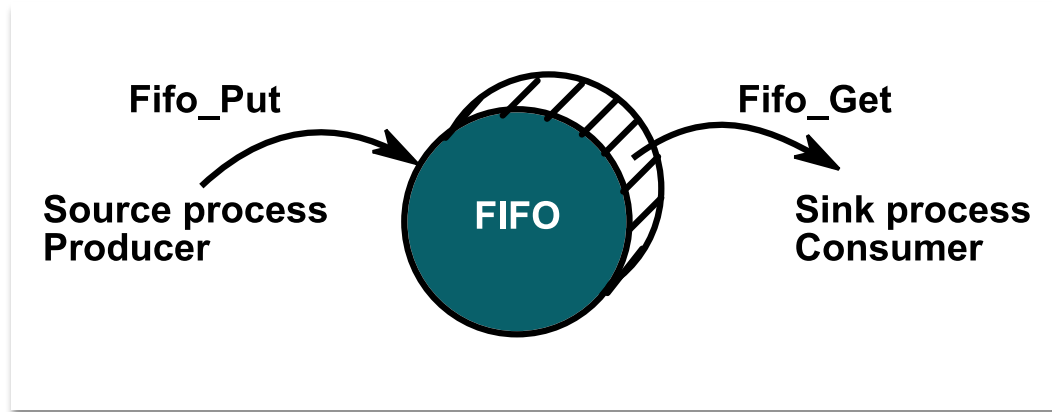
You will learn in this module

- FIFO Queues
 - Buffered I/O
 - Little's Theorem
- Performance measures
 - Bandwidth
 - Response time



First In First Out (FIFO) Queue

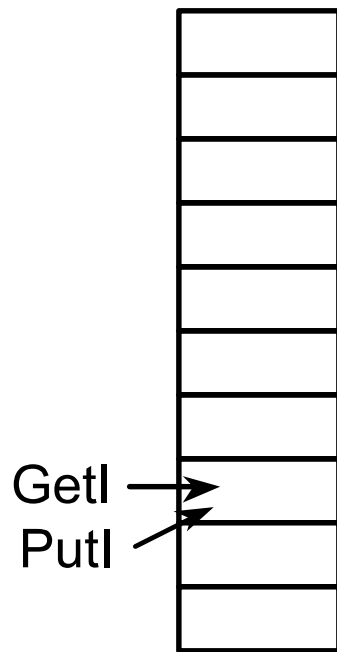
- Order preserving
- Producer puts on tail end
- Consumer gets from head end
- Buffer decouples producer & consumer
 - Even out temporary mismatch in rates





Empty FIFO

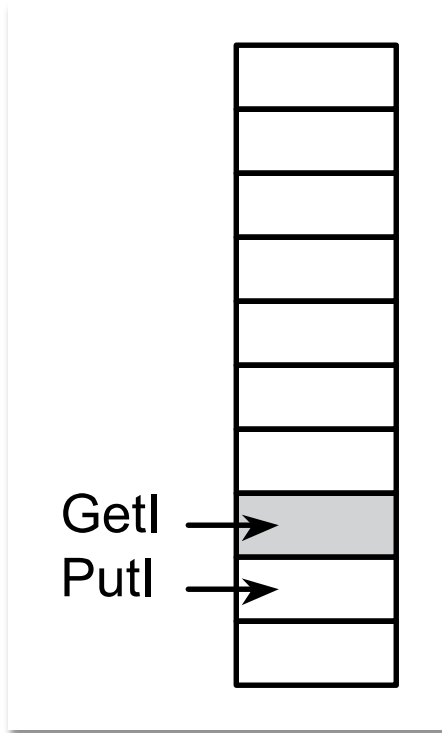
- Getl points to oldest
- Putl points to empty place
- This FIFO has 10 spaces
- It can hold up to 9 data





First Put

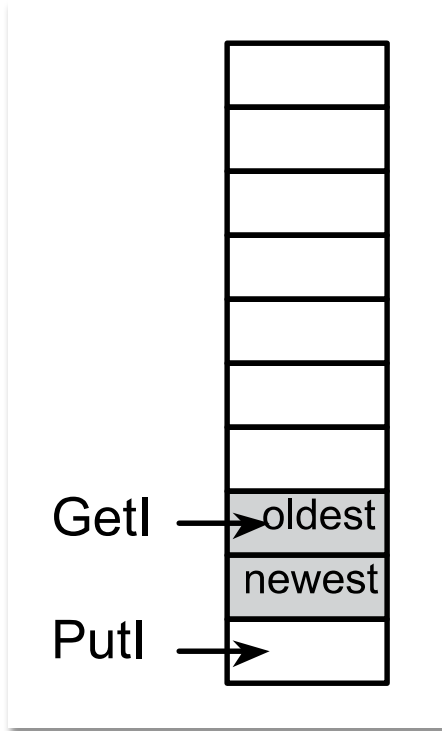
- Store at Putl
- Increment Putl





Second Put

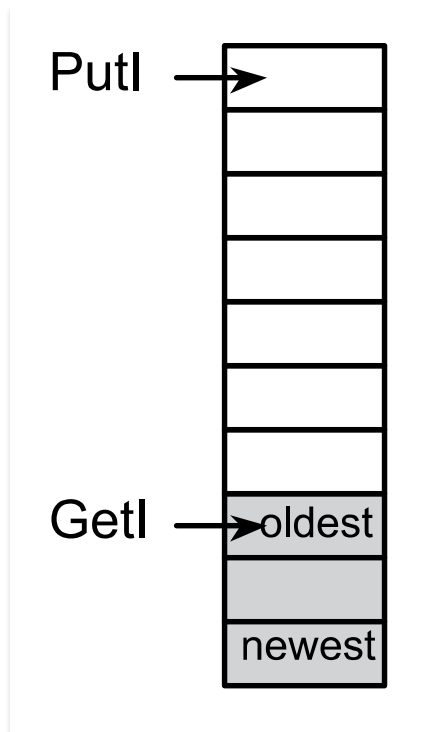
- Store at Putl
- Increment Putl





Third Put

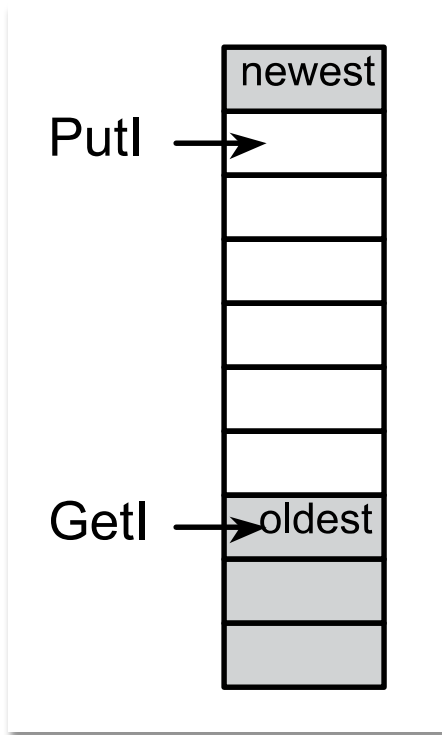
- Store at Putl
- Increment Putl (wrap)





Fourth Put

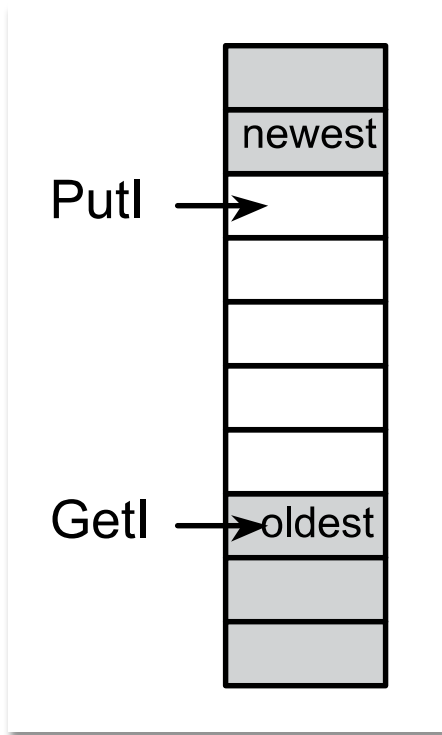
- Store at Putl
- Increment Putl





Fifth Put

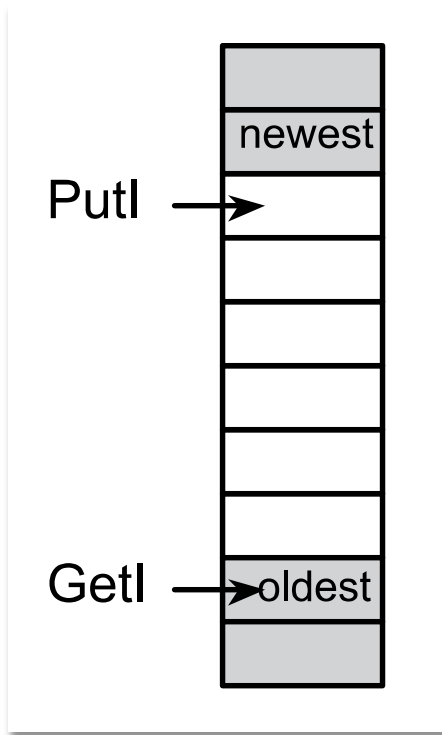
- Store at Putl
- Increment Putl





First Get

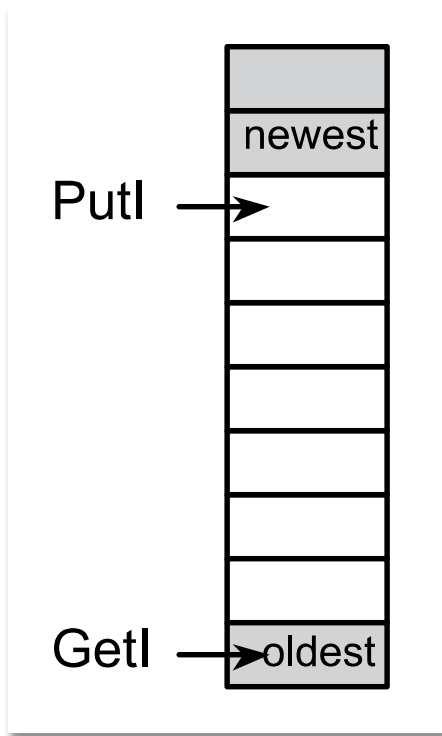
- Read from Getl
- Increment Getl





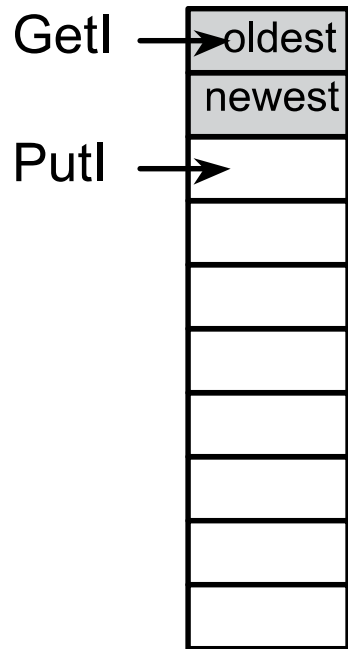
Second Get

- Read from Getl
- Increment Getl



Third Get

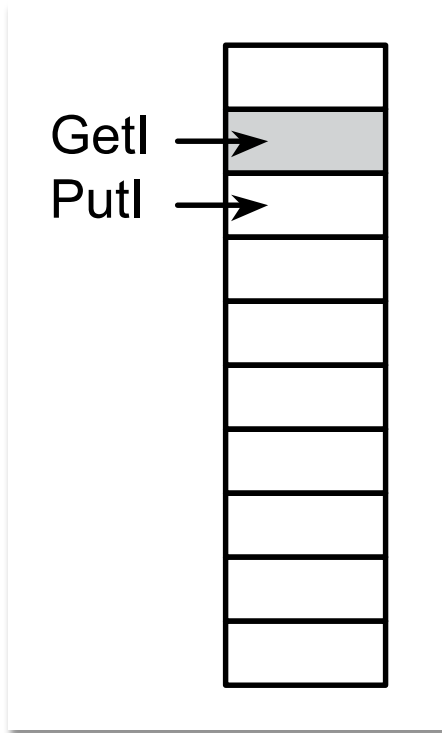
- Read from Getl
- Increment Getl (wrap)





Fourth Get

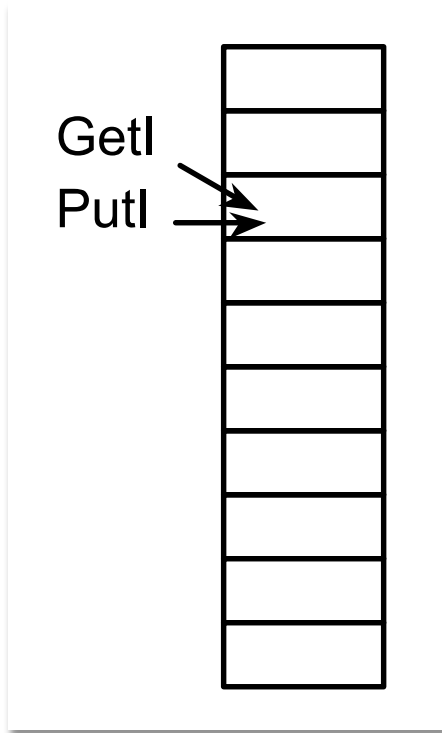
- Read from Getl
- Increment Getl





Fifth Get

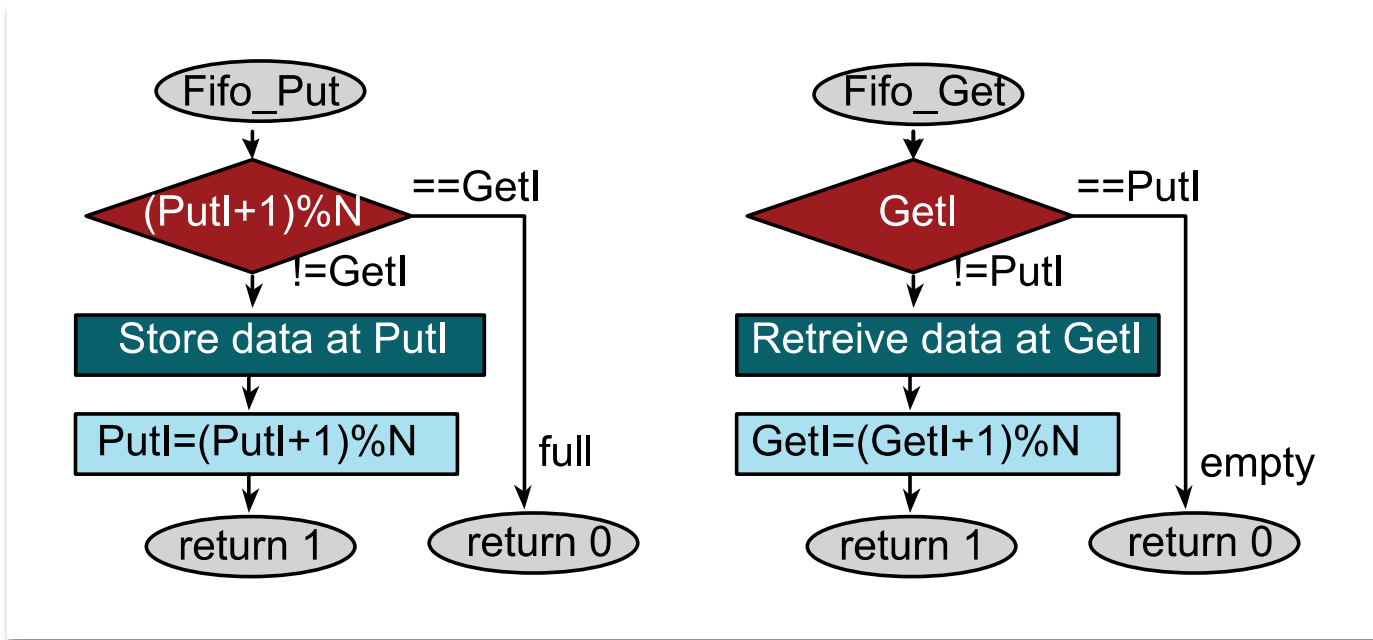
- Getl points to data to get
- Putl points to place to put





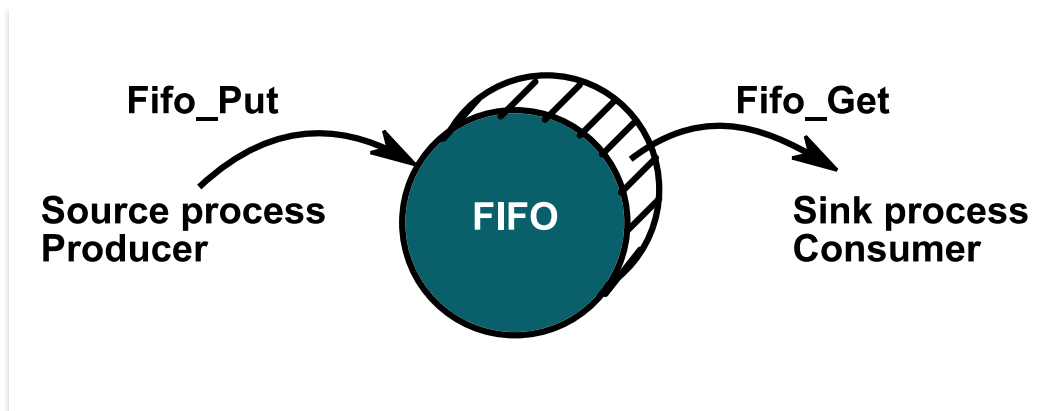
FIFO Implementation

- Getl points to data to get
- Putl points to place to put





Little's Theorem



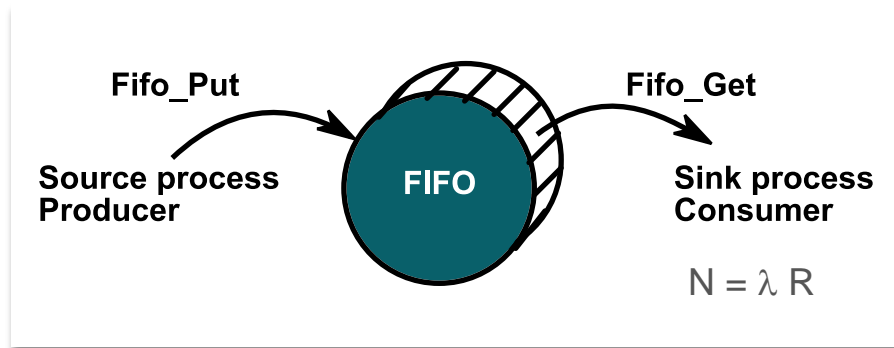
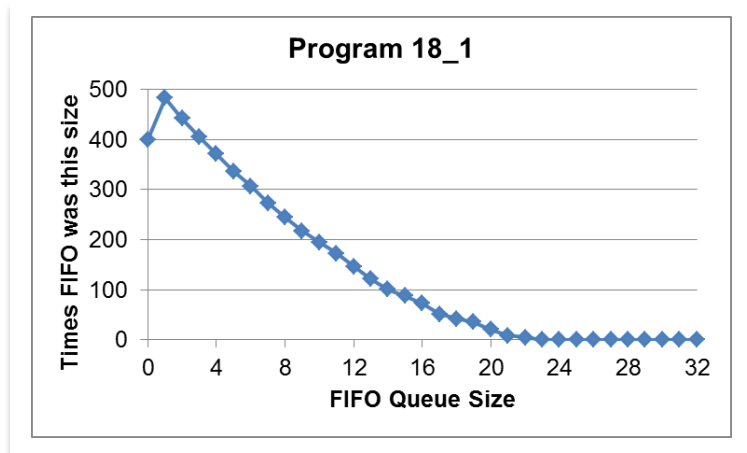
- N be the average number of data packets in the queue (plus 1)
- Let λ be the average arrival rate in packets per second (pps)
- Let R be the average response time of a packet
 - time waiting in the queue plus the
 - time for the consumer to process the packet
- Little's Theorem $N = \lambda R$



Summary

FIFO queue

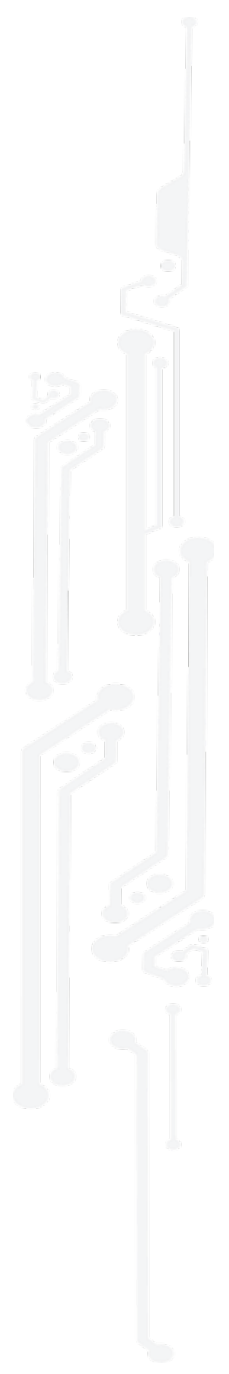
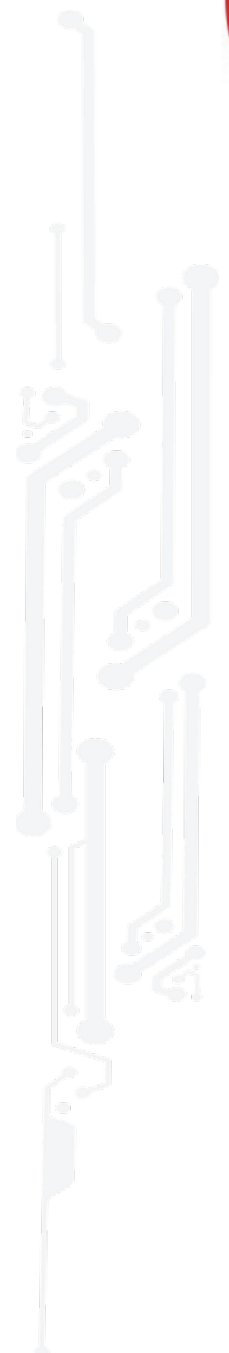
- Data flow
- Order preserving
- Full error on put
- Empty error on get
- Little's Theorem





Module 18

Lecture: Serial Communication - UART

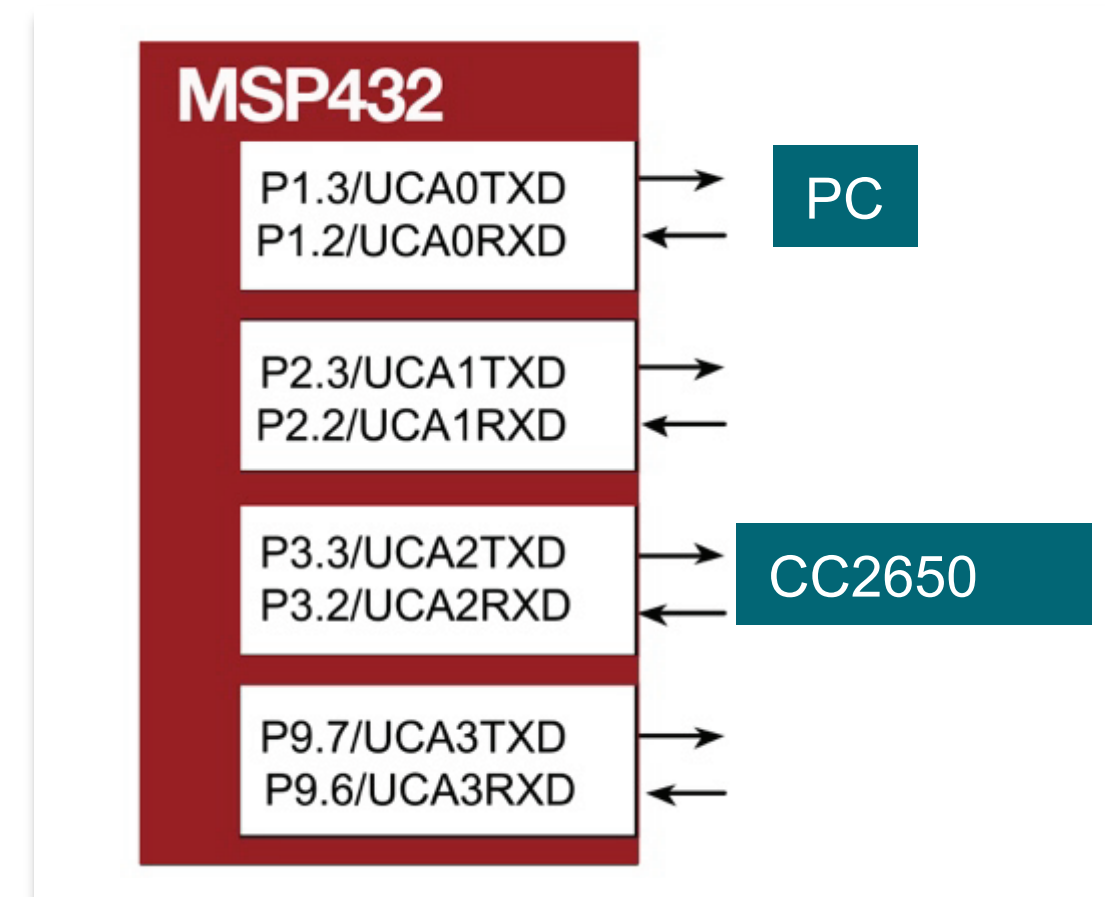




Serial Communication

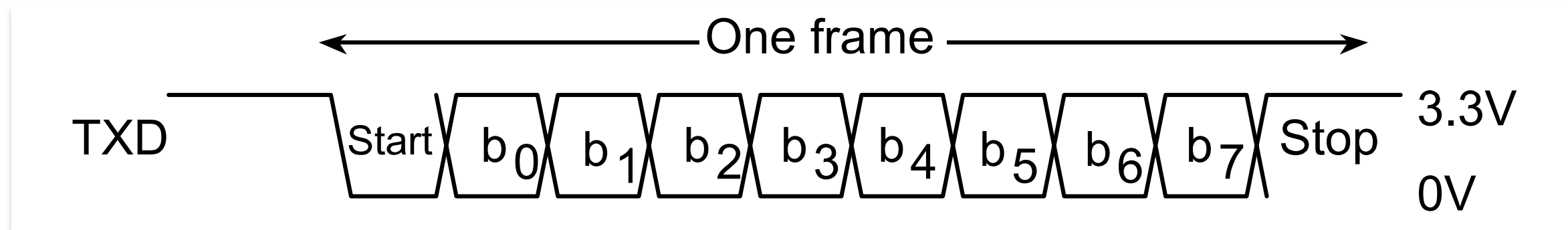
You will learn in this module

- Communication
 - Encode
 - Transmit
 - Decode
- Serial: Universal Asynchronous Receiver Transmitter
 - Interrupts
 - Baud rate
- Performance measures
 - Bandwidth
 - Response time





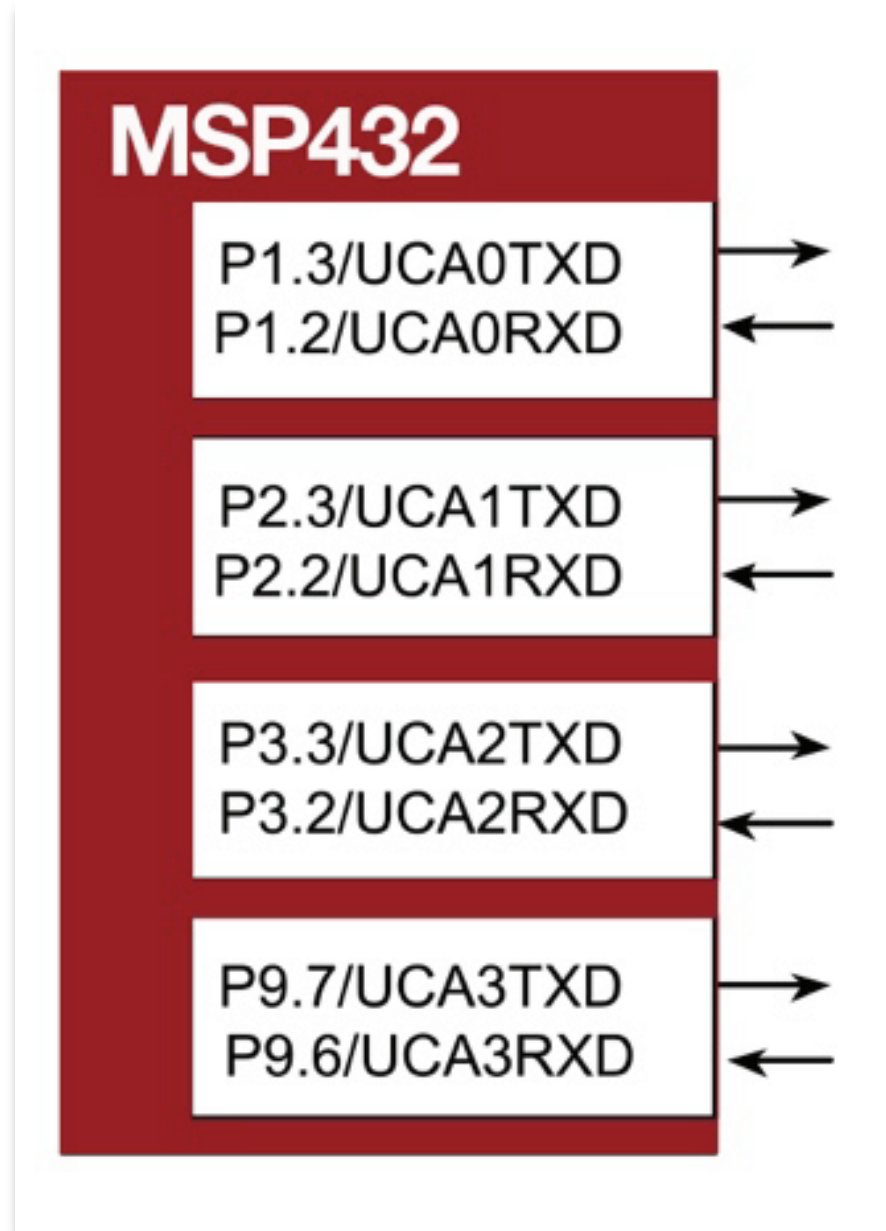
Universal Asynchronous Receiver/Transmitter (UART)



- Send/receive a **frame**
 - 1 start (low), 5-8 data bits , 1 stop (high)
 - Serial fashion, one bit every **bit-time**
 - No clock is sent, asynchronous, timing derived from data
- **Baud rate** is total number of bits per unit time
 - Baud rate = $1 / \text{bit-time}$
 - Both transmitter and receiver agree and know the baud rate
- **Bandwidth** is data or information per unit time
 - Bandwidth = $(\text{data-bits} / \text{frame-bits}) * \text{baud rate}$



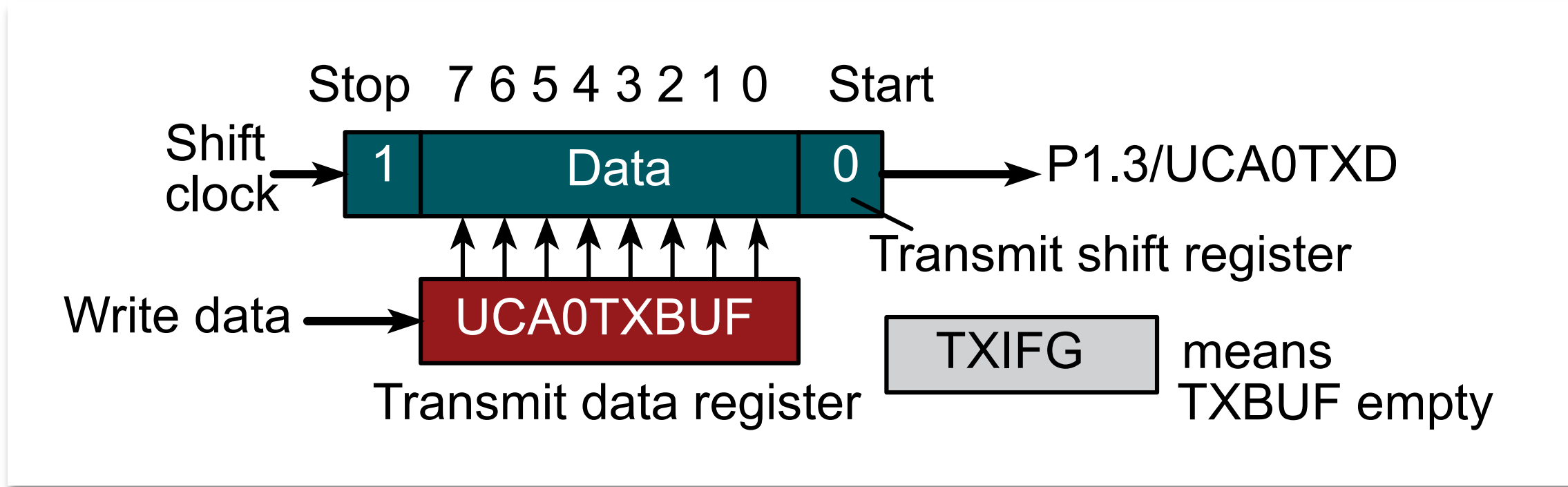
UART Port Selection



Pin	PxSEL1=0, PxSEL0=1
P1.2	UCA0RXD
P1.3	UCA0TXD
P2.2	UCA1RXD
P2.3	UCA1TXD
P3.2	UCA2RXD
P3.3	UCA2TXD
P9.6	UCA3RXD
P9.7	UCA3TXD



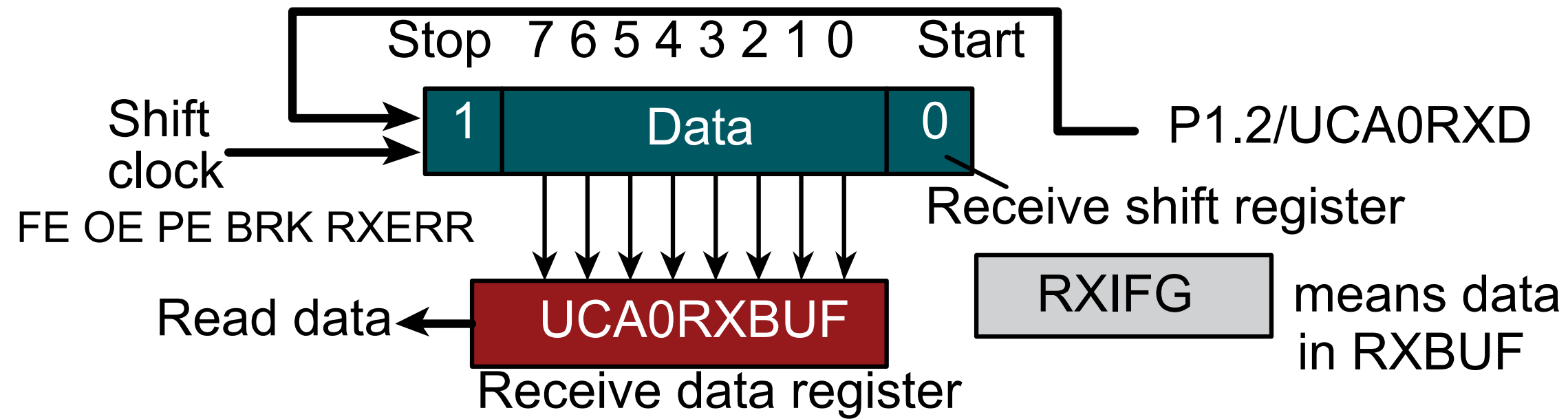
UART - Transmitter



- Interrupt on TXIFG
- Data written to UCA0TXBUF
- Add start, stop bits
- Shift out at Baud Rate clock



UART - Receiver



- Start bit synchronization, shift in at baud rate
- Interrupt on RXIFG
- Read data from UCA0RXBUF



UART - Communication



'a' = 0x61 = 01100001

- TXIFG in transmitter is 1



UART - Communication



- Transmitter writes to UCA0TXBUF ('a' = 0x61 = 01100001)
- TXIFG in transmitter becomes 0



UART - Communication



- Data is moved from TXBUF to shift register
- Start bit and stop bit added
- TXIFG in transmitter becomes 1



UART - Communication



- Start bit shifted



UART - Communication



- Data bit 0 shifted



UART - Communication



- Data bit 1 shifted



UART - Communication



- Data bit 2 shifted



UART - Communication



- Data bit 3 shifted



UART - Communication



- Data bit 4 shifted



UART - Communication



- Data bit 5 shifted



UART - Communication



- Data bit 6 shifted



UART - Communication



- Data bit 7 shifted



UART - Communication



- Stop bit shifted



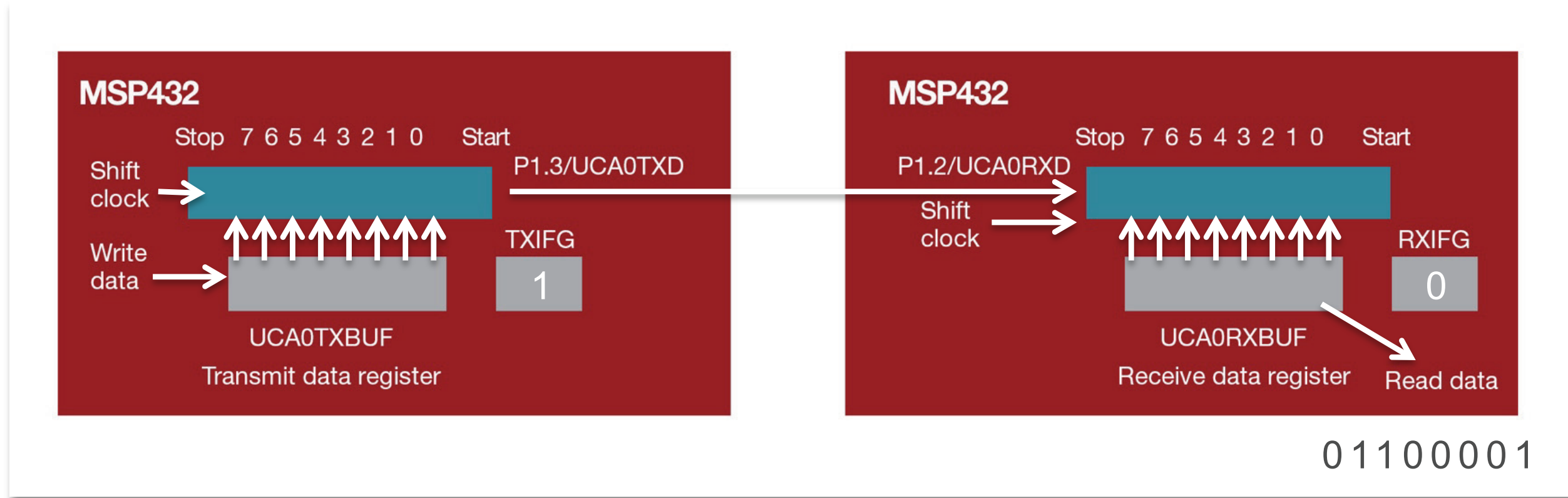
UART - Communication



- Start bit and stop bit checked
- Data is moved from shift register to RXBUF
- RXIFG in receiver becomes 1



UART - Communication



- Receiver reads from UCA0RXBUF ('a' = 0x61 = 01100001)
- RXIFG in transmitter becomes 0

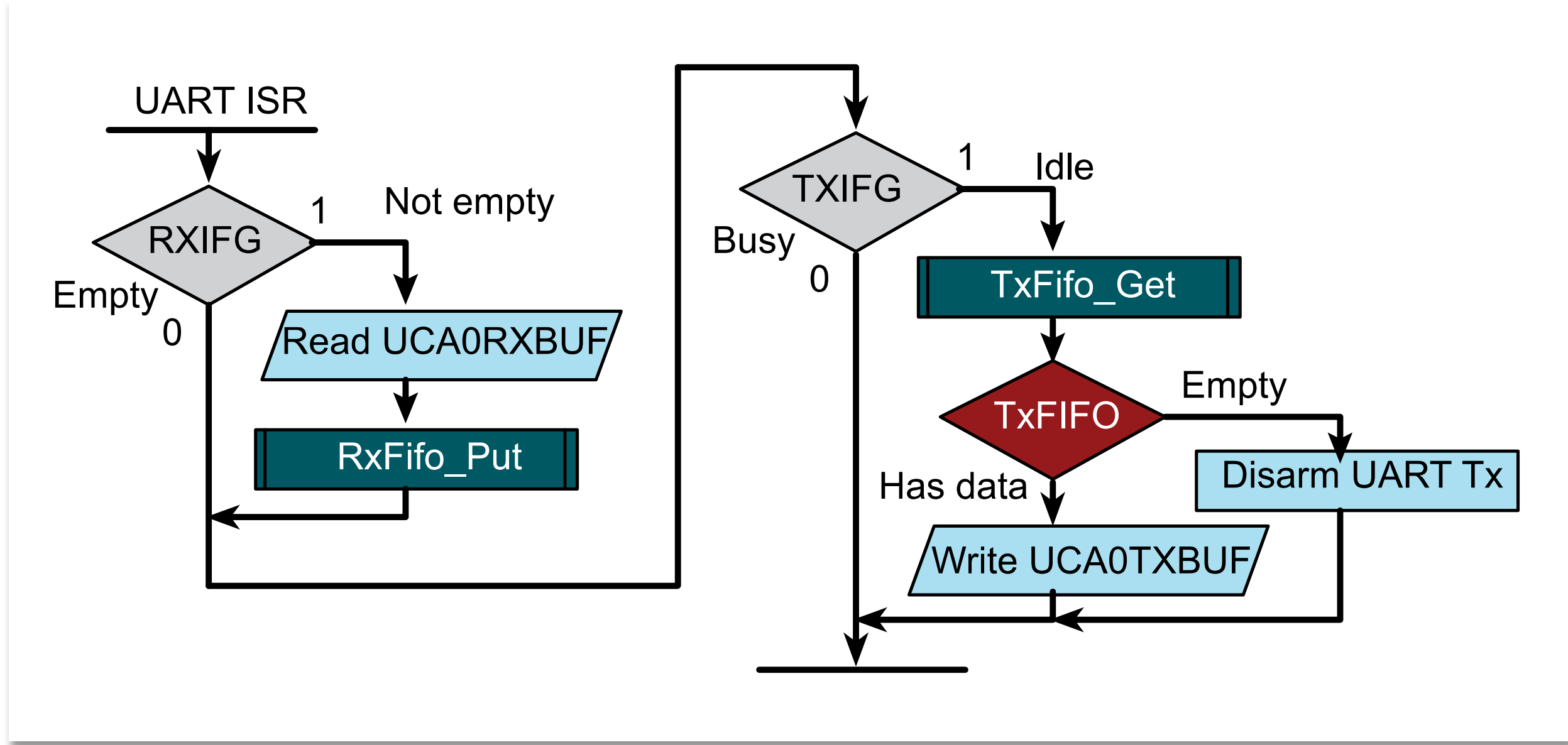


UART Registers

0x40001000	15	14	13	12	11	10	9	8	UCAxCTLW0	
	PEN	PAR	MSB	7BIT	SPB	MODEx		SYNC		
0x40001000	7	6	5	4	3	2	1	0	UCAxCTLW0	
	SSELx		RXEIE	BRKIE	DORM	TXADDR	TXBRK	SWRST		
0x40001006	15 - 0 UCBRx								UCAxBRW	
0x40001008	15 - 8			7 - 4			3 - 1		0	UCAxMCTLW
	BRSx			BRFx					UCOS16	
0x4000100A	7	6	5	4	3	2	1	0	UCAxSTATW	
	LISTEN	FE	OE	PE	BRK	RXERR	IDLE	BUSY		
0x4000100C	15 - 8			7 - 0					UCAxRXBUF	
				RXBUFx						
0x4000100E	15 - 8			7 - 0					UCAxTXBUF	
				TXBUFx						
0x4000101A	15 - 4				3	2	1	0	UCAxIE	
					TXCPTIE	STTIE	TXIE	RXIE		
0x4000101C	15 - 4				3	2	1	0	UCAxIFG	
					TXCPTIFG	STTIFG	TXIFG	RXIFG		



FIFO Usage

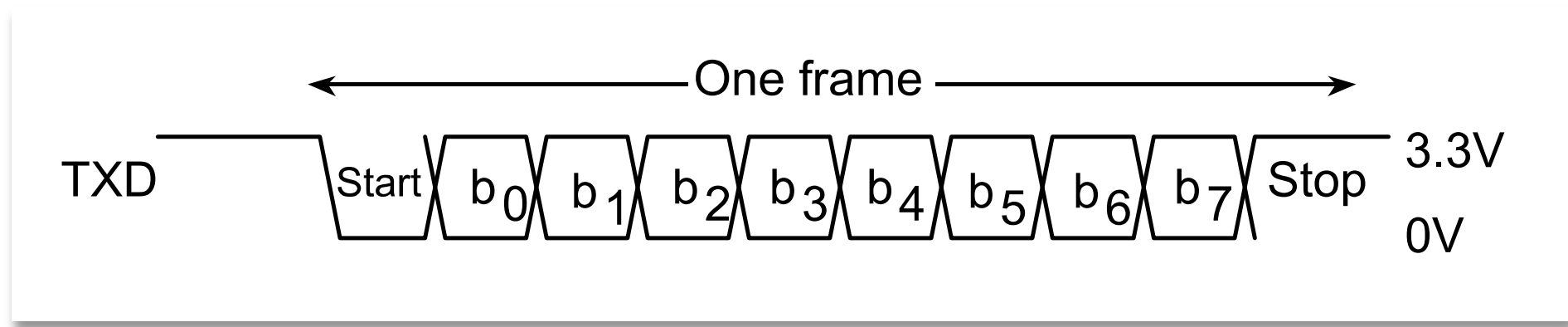




Summary

Serial Communication

- One bit at a time
- Asynchronous
- Interrupt-driven
- Baud rate
- Bandwidth



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