Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs

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Abstract

In an effort to standardize integrated-circuit (IC) package thermal-measurement methods, JEDEC has released standards for test-board designs. Typical thermal metrics reported are package thermal resistance from junction to ambient (θ_{JA}), and package thermal resistance from junction-to-case (θ_{JC}). Recent data generated by Texas Instruments (TI™) linear and logic package designers includes θ_{JA} and θ_{JC} measured, or modeled, on both a JEDEC low-thermal-conductivity (low K) PCB design and a JEDEC high-thermal-conductivity (high K) PCB design. A study showed good correlation between modeled results and data taken in a laboratory. A web page provides the new thermal data for TI packages. An additional feature of this web page allows the user to plot derating curves for each package, using the thermal data provided.

Introduction

Users of ICs need to know the thermal-dissipation performance of the plastic packages used to encapsulate the ICs. Package thermal-resistance data allows the user to compare performance of different IC suppliers, as well as determine the limits of a package in a specific end-use environment. Thermal metrics, such as θ_{JA} and θ_{JC}, are used to compare thermal performance of plastic IC packages. The thermal conductivity of all materials of the IC package and the test-board influence the thermal-resistance values reported by semiconductor manufacturers. Recent advancements in reporting of thermal data include standardized test-board designs. Prior to development of these standard test-board designs, IC manufacturers used their own PCB designs to generate thermal data; therefore, comparison of package thermal data between suppliers was not meaningful.

Background

Thermal resistance is the resistance of the package to heat dissipation and is inversely related to the thermal conductivity of the package. The source of heat in a plastic IC package is the chip. All electrical circuits dissipate some power in the form of heat. This heat is conducted through the package into the ambient environment, and, in the process, the temperature of the die (T_J) rises above ambient. The thermal conductivity of the silicon chip, die-attach epoxy, copper leadframe, and mold compound all affect the rate at which the heat is dissipated. The geometry of the package and of the printed circuit board (PCB) greatly influence how quickly the heat is transferred to the PCB and away from the chip.

The most commonly used thermal metrics for IC packages are thermal impedance measured, or modeled, from the chip junction to the ambient air surrounding the package (θ_{JA}) and thermal impedance measured, or modeled, from the chip junction to the case (θ_{JC}).

Figure 1 is a thermal representation of a typical IC plastic package, with the silicon chip and the thermal metrics identified.

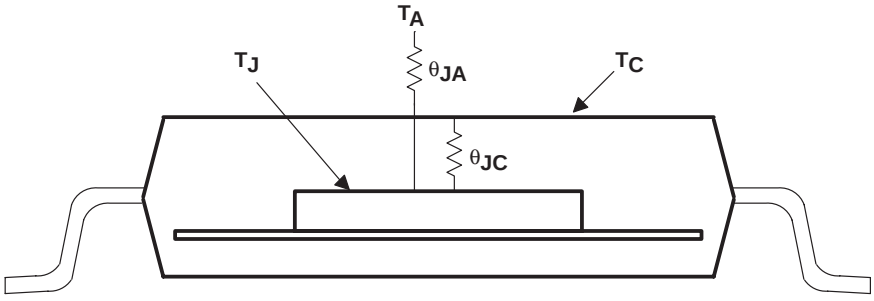

Figure 1. IC Package Thermal Metrics

Mathematically, θ_{JA} is defined as:

$$\theta_{JA} = (T_J - T_A)/P \quad \textbf{(1)}$$

Where:

T_J = junction temperature of the chip
T_A = ambient temperature
P = power to the chip

θ_{JA} is measured using the following steps:[1]

1. IC package containing a test chip is mounted on a test board.
2. Temperature-sensing component of the test chip is calibrated.
3. Package/test-board system is placed in a still-air environment.
4. Known power is dissipated in the test chip.
5. After steady state is reached, the junction temperature is measured.
6. The difference in measured ambient temperature compared to the measured junction temperature is calculated and is divided by the dissipated power.

Mathematically, θ_{JC} is defined as:

$$\theta_{JC} = (T_J - T_C)/P \quad \textbf{(2)}$$

Where:

T_J = junction temperature of the chip
T_C = package case temperature
P = power to the chip

Measurement of θ_{JC} is formalized in industry standards. Summarized, the procedure is:

1. IC package containing a test chip is mounted on a test board.
2. The package, in a “dead bug” configuration, is pressure fitted to a copper cold plate (a copper block with circulating constant-temperature fluid).
3. Silicone thermal grease provides thermal coupling between the cold plate and the package.
4. Power is applied to the device.
5. Junction temperature of the test chip is measured.
6. Temperature of the package surface in contact with the cold plate is measured by a thermocouple pressed against this surface.
7. θ_{JC} is calculated by dividing the measured temperature difference by the dissipated power.

Figure 2 is a schematic representation of the laboratory method used to measure θ_{JC}.

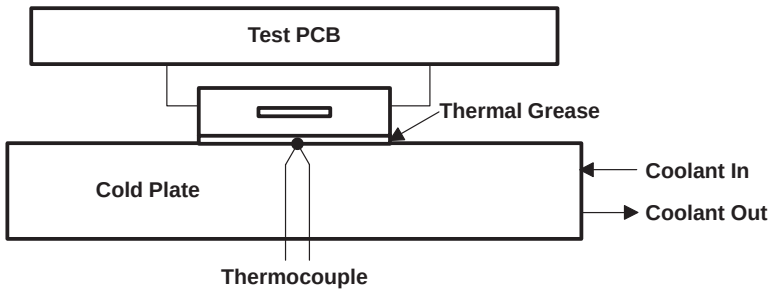

Figure 2. θ_{JC} Laboratory Measurement Method

θ_{JA} values are the most subject to interpretation. Factors that can greatly influence the measurement and calculation of θ_{JA} are:

- Whether or not the device is mounted to a PCB
- PCB trace size, composition, thickness, geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test, and airflow
- Whether or not other surfaces are in close proximity to the device being tested

To eliminate the test-board design as a variable in data reported by IC manufacturers, thermal test-board design standards have been developed and released.[2,3] In August 1996, the Electronics Industries Association (EIA) released *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages,* EIA/JESD 51–3. In February 1999, the EIA released *Test Board With Two Internal Solid Copper Planes for Leaded Surface Mount Packages,* EIA/JESD 51–7. These standards describe guidelines with parameters for thermal-test-board design for low effective thermal conductivity (one signal layer in the trace fanout area) and for PCB designs with high effective thermal conductivity (one power and one ground plane). The specified parameters include the area of the test board, the amount of copper traces on the test board, and the resulting trace fanout area, each important to the heat-sinking characteristics of the PCB. Prior to release of these standards, thermal-impedance data for similar packages varied widely within the industry due to the use of different test-board designs. As the industry adopts this standard design methodology, thermal-impedance variations from test-board design should be minimized. The critical factors of these test-board designs are shown in Table 1.

Table 1. Critical PCB Design Factors for JEDEC 1s and 2s2p Test Boards

TEST BOARD DESIGN	JEDEC LOW-K 1s (inch)	JEDEC HIGH-K 2s2p (inch)
Trace thickness	0.0028	0.0028
Trace length	0.98	0.98
PCB thickness	0.062	0.062
PCB width	4	4
PCB length	4.5	4.5
Power/ground-plane thickness	No internal copper planes	0.0014 (2 planes)

Figure 3 is an orthogonal view of a one-quarter package model for the 20-pin small-outline integrated-circuit (SOIC) package. Note the traces on the PCB extending out from the leads. Figure 4 is a cross section of the same package on a JEDEC 2s2p (high K) PCB. Note the two internal copper planes embedded in the circuit board and the trace layer on the top surface of the PCB.

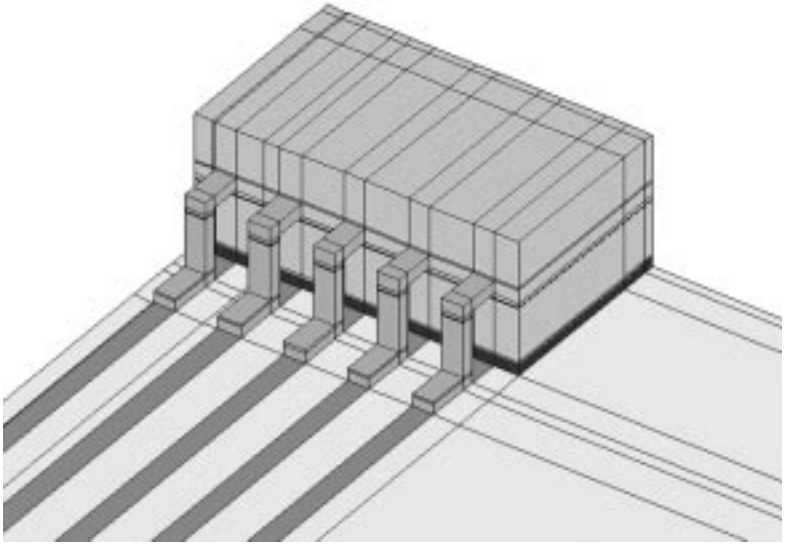

Figure 3. One-Quarter Package Model of 20-Pin SOIC Package

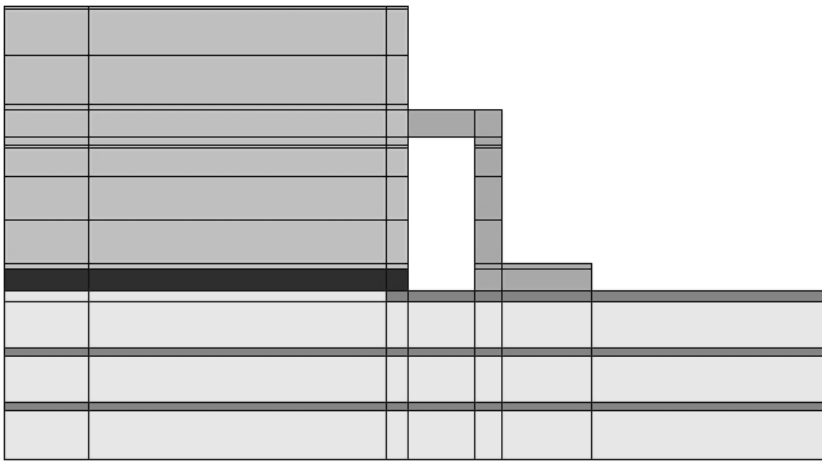

Figure 4. Cross Section of 20-Pin SOIC Package on 2s2p PCB

Correlation Study

TI uses test boards designed to JESD 51-3 and JESD 51-7 for thermal-impedance measurements. The parameters outlined in these standards also are used to set up thermal models. TI uses the thermal-model program ThermCAL, a finite-difference thermal-modeling tool. Previous data generated using the low-K PCB designs showed the models to be accurate to within 10% of measured data.[4]

Nine TI packages were tested using a JEDEC high-K test-board design and compared to ThermCAL model results for the same packages. Laboratory-measured thermal data and modeled results are shown in Table 2.

Table 2. Correlation Study Results Using JEDEC High-K PCB Design

PACKAGE PIN COUNT AND DESIGNATOR	DIE SIZE (mils)	θ_{JA} (°C/W)		DIFFERENCE (%)	θ_{JC} (°C/W)	
		MEASURED	MODELED		MEASURED	MODELED
8 PW	62 × 62	149.4	151.8	1.6	48.7	50.1
16 PW	62 × 62	108.4	99.5	–8.2	36.4	31.1
24 PW	62 × 62	87.9	79.0	–10.1	31.2	26.9
48 DGG	120 × 120	70.0	63.3	–9.6	18.2	16.4
56 DGG	120 × 120	63.8	56.4	–11.6	16.4	14.6
64 DGG	120 × 120	55.4	53.0	–4.3	10.8	12.6
64 PAG	240 × 240	42.3	39.3	–7.1	3.7	5.5
80 PN	240 × 240	44.1	41.9	–5.0	7.6	9.6
100 PZ	240 × 240	40.8	38.1	–6.6	7.8	8.1

This comparison shows modeled θ_{JA} data is accurate to within 10% of measured data for most cases when using the ThermCAL software. On average (all nine packages) the difference between measured data and modeled data was 6.9%.

After accuracy of the model results was established, other linear and logic packages were modeled using the JEDEC high-K test board. θ_{JA} and θ_{JC} data for all packages can be viewed at:

http://www.ti.com/sc/docs/products/logic/package/thrmdata.htm

Also included on this web page are copies of the JEDEC standards and related application reports. Within the thermal data page for any specific-package family (SOIC, for example) a derating curve can be viewed. This is an additional feature provided for the user.

Derating Curves

When a device reaches a state of thermal equilibrium, the electrical power delivered is equal to the thermal heat dissipated, which is transferred to the surroundings. The maximum allowable power consumption (P) at a given ambient temperature (T_A) is computed using the maximum junction temperature for the chip (T_J) and the thermal resistance of the package (θ_{JA}) as shown in equation 3:

$$P = (T_J - T_A)/\theta_{JA} \quad \textbf{(3)}$$

Over time, heat destroys semiconductors. Therefore, manufacturers usually specify a maximum junction temperature (T_J max). If the junction temperature goes above this value, irreversible damage occurs. Typically, the IC user knows the ambient temperature of the operating environment (T_A), the thermal resistance of the IC package (θ_{JA}) provided by the supplier, and a specified maximum junction temperature. Equation 3 can be used to determine the maximum power that can be applied to the particular package under the specified test conditions.

By varying the ambient temperature at a given airflow in equation 3, a derating curve can be developed for each package. By using the thermal resistance value of the package at different airflows, a derating curve can be developed for each airflow. A typical set of derating curves for the 16-pin SOIC (DW) package is shown in Figure 5. The data for the 16-pin DW package (θ_{JA}) used to calculate the curves was generated using a JEDEC 1s (low K) PCB design.

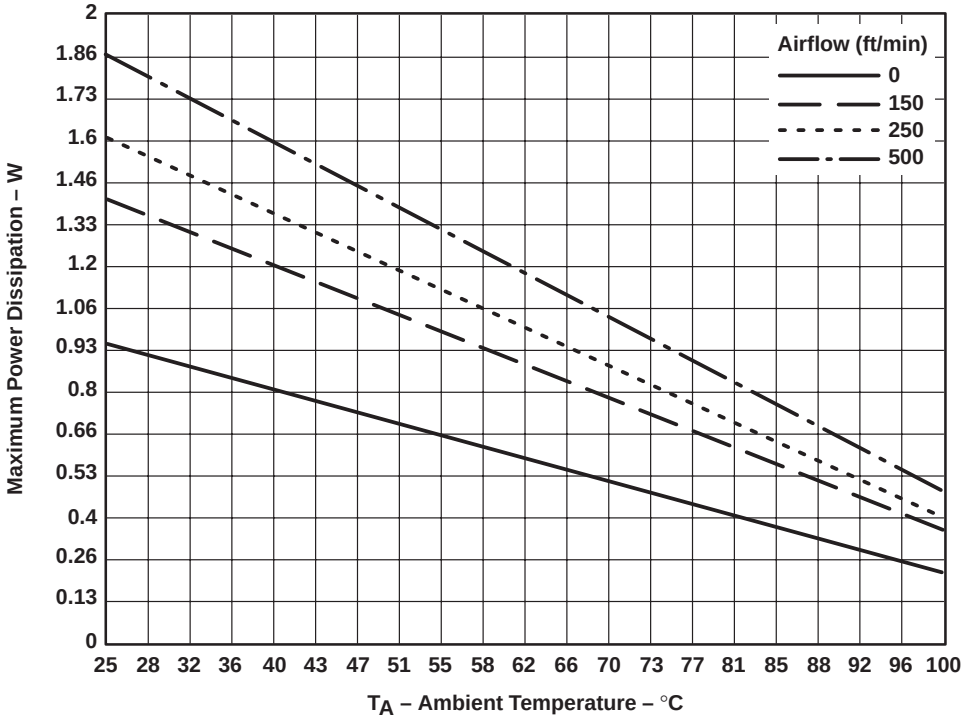

Figure 5. Derating Curves for 16-Pin DW SOIC Package

As an example, the 16-pin DW package has a θ_{JA} of 104.6°C/W at zero airflow. The maximum power that the package can withstand at T_A = 25°C and T_J = 125°C is:

$$P = (125°C - 25°C)/104°C/W = 0.956\ W \quad \textbf{(4)}$$

θ_{JA} was derived using a JEDEC low-K PCB.

For a given package, these derating curves allow the designer to see the effect of rising ambient temperature and changes in airflow on the maximum power allowed. By accessing the web page, the user can view the derating curves for each package. The program uses the θ_{JA} data shown to display the maximum power dissipation (y-axis) of the package over a range of ambient temperatures (x-axis). This maximum power dissipation of the package is equivalent to the maximum allowable consumption of the IC device. The user can vary the junction temperature and ambient temperature range used in the calculation of maximum power dissipation.

Conclusion

An improvement of 30% to 45% is seen in the thermal resistance values of TI packages when tested on a high-K board versus a low-K board. The high-K design has two copper planes embedded in the PCB. Because the high-K design is more representative of many end-user PCB designs, this new thermal data gives a more accurate representation of the performance of the package in use. TI thermal data is now easily accessible to external customers via the TI external web page.

Acknowledgment

The authors of this application report are Douglas W. Romm and Ray H. Purdom.

References

1. Edwards, Darvin, IC Package Thermal Metrics, January 1998.
2. EIA/JESD 51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages, 1996.
3. EIA/JESD 51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages, 1999.
4. Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*, literature number SCZA005, March 1998.
5. Texas Instruments, *Thermal Derating Curves For Logic-Products Packages*, literature number SZZA013, February 1999.