8-Bit Linear and Logic Families in 20-Ball, 0.65-mm Pitch, Very-Thin, Fine-Pitch BGA (VFBGA) Packages

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ABSTRACT

Texas Instruments 20-ball MicroStar Jr.™ package is a standardized JEDEC VFBGA package designed to satisfy requirements for minimizing board area. This ball grid array package provides improved thermal performance, reduced inductance and capacitance, cost savings for OEMs in the system manufacturing process, and greater package reliability. Advantages of the MicroStar Jr. package over SSOP, TSSOP, and TVSOP packages are quantified. Package marking and packing specifications are provided.

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MicroStar Jr. is a trademark of Texas Instruments.

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1 Introduction

As system and circuit complexity increases, and competitive pressures force the reduction of system prices, the requirement for cost-effective bus-interface technology creates the necessity for new solutions to system needs. The major challenge of today's digital processing industry is the reduction of overall system costs as complexity increases. These marketplace forces have resulted in circuit integration and board miniaturization becoming a necessary trend. To address these rapidly evolving customer requirements, Texas Instruments has defined a very-thin-profile fine-pitch ball grid array (VFBGA) package solution, known as the MicroStar Jr.™ package, to best serve customer needs. Modeling and experimentation have shown that the MicroStar Jr. package is an optimal solution for reducing inductance and capacitance and improving thermal performance, while minimizing board area in support of integrated bus functions. Our objective is to provide significant improvements over existing packages, as well as cost savings to the OEM manufacturing process.

The purpose of this application report is to introduce our newest VFBGA solution, the 20-ball MicroStar Jr. package. The definition of this package in terms of standardization, both physical and mechanical, was developed by TI to provide our customers with industry-compatible solutions. Additional products may be released based on market interest and customer demand. Current products are listed in Table 1 and include bus-hold options.

Table 1. 20-Ball MicroStar Jr.™ Package Releases to Date

FAMILY	DESCRIPTION	RELEASED FUNCTION
ABT	Advanced BiCMOS technology	245B, 573A, 574A
CBT	Crossbar technology	3244, 3245A
LVC	Low-voltage CMOS technology	138A, 244A, 245A, 373A, 573A, 574A, 2245A
LVT	Low-voltage BiCMOS technology	240†, 244A†, 244B, 245A†, 245B, 573†, 574†
LV	Low-voltage CMOS	245A, 373A, 374A, 573A, 574A

† With bus-hold option

2 Application Examples

2.1 Industry Requirements

The requirement to reduce board area necessitates a packaging solution that integrates logic, and addresses improved electrical and thermal packaging characteristics. The selection of the 20-ball MicroStar Jr. package addresses these issues with improved performance and standardized pinouts. In 1999, an initial study of OEMs and worldwide subcontractors revealed that customers desired BGA solutions with a pin 1 identification on the top and the bottom sides, and a pinout that allows routing traces to use minimal board space.

The MicroStar Jr. package provides this capability with single-layer routing for all pins. TI has found that 0.65-mm pitch and 0.117-mm (4.6 mil) trace width/spacing are both desired by OEMs and feasible to manufacture. Via technology has progressed to the point that a 10-mil drill is an economical technology for 1.5748-mm (62 mil) boards, and micro-via technology that employs lasers has reduced costs for vias with a 0.2032-mm (8 mil) diameter and less.

More recently, technology has progressed even further, with respect to trace width and spacing. Many offshore printed circuit board (PCB) manufacturers currently produce 0.0508-mm (2.2 mil) boards with via-in-pad interconnects. This capability is, however, more expensive and must be balanced with production volumes and pay-back considerations. Because of these reduced-pitch efforts, the 0.117-mm (4.6 mil) capabilities have experienced increased yields through similar process and material innovations, and are becoming common technology.

Informal discussions with United States PCB manufacturers reveal that a majority of the domestic industry has process capabilities down to the 0.107-mm (4.4 mil) level. This percentage of manufacturers is even higher in the Asian market. By not pushing the envelope for PCB vendors, TI has determined that 0.65-mm pitch is the optimal choice at this time, given current technology and raw-board yields.

The MicroStar Jr. package offered by TI supports customer requirements and enables easier, economical, PCB design/layout, along with improved solder-joint reliability based on life-cycle studies, all while reducing consumption of valuable board space. Experiments and modeling also have shown a 3× improvement in board-level reliability over land grid array (LGA) packages due to increased seating height. The VFBGA package also provides significant improvements in parasitic capacitance and inductance over the 20-pin thin shrink small-outline package (TSSOP) and thin very small-outline package (TVSOP). Improved thermal performance and an overall height of less than 1 mm makes the MicroStar Jr. package ideal for height-constrained applications, such as PCMCIA. A more detailed package comparison is provided in other subsections of this application report.

2.2 Customer Requirements

Each customer has unique requirements. However, there are common issues across the industry to be addressed, and our goal is to provide a targeted solution to these needs. Within the personal computer (PC) industry, the trend is to integrate as much logic as possible into smaller packages to save space on motherboards and peripheral cards. Due to space constraints, PC cards require dense integration and small footprints with improved electrical and thermal performance. Commonality of package types for clocks, registers, and memory chips on dual-inline memory modules (DIMMs) can be achieved by the use of the MicroStar Jr. package, thus creating cost-effective and common manufacturing processes for OEMs. In the telecommunications industry, base stations are becoming small and ubiquitous, requiring the repackaging of many circuits into denser boards. Also, within the telecommunications industry, new, complex, and smaller equipment must interface with legacy systems to provide cost-effective upgrade solutions to existing capabilities. The reduced footprint of a MicroStar Jr. package will enable these requirements to be met without sacrificing performance.

2.3 Comparison of Alternative Solutions

Comparisons of footprint areas for the 20-Ball MicroStar Jr. package shows space savings up to 62.5% when compared to the 20-pin TVSOP, and space savings up to 71% compared to the 20-pin TSSOP. Table 2 compares physical dimensions and area savings of the 20-ball MicroStar Jr. package to alternative packages. Table 3 compares area-to-bit ratios and weight savings.

Table 2. 20-Ball MicroStar Jr.™ Package Area Savings

PIN COUNT	PACKAGE TYPE	PITCH (mm)	PACKAGE DIMENSION (mm)	FOOTPRINT (mm^2)	MAXIMUM HEIGHT (mm)	AREA SAVINGS (%)
20	MicroStar Jr.	0.65	3×4	12.0	1.0	
20	TVSOP	0.4	5×6.4	32.0	1.2	62.5
20	TSSOP	0.65	6.4×6.5	41.6	1.2	71.15
20	PLCC	0.5	9.905×9.905	98.11	4.57	87.77
20	SSOP	0.65	7.2×7.8	56.16	2.0	78.63

Table 3. Area/Bit Ratio Comparison

PIN COUNT	PACKAGE TYPE	FOOTPRINT (mm^2)	AREA/BIT (mm^2)	WEIGHT (g)
20	MicroStar Jr.	12.0	1.5	0.022
20	TVSOP	32.0	4.0	0.055
20	TSSOP	41.6	5.2	0.075
20	PLCC	98.11	12.26	0.62
20	SSOP	56.16	7.02	0.151

3 Physical Description

3.1 Package Characteristics

Figure 1 shows a cross-section view of the MicroStar Jr. package.

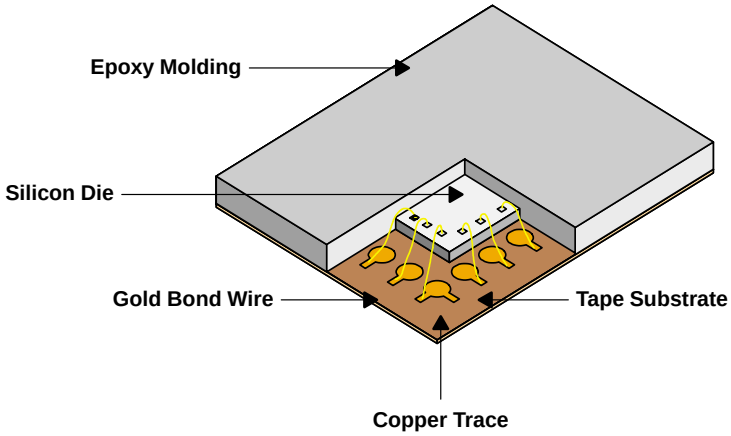


Figure 1. MicroStar Jr.™ Package Cross Section

Table 4 summarizes the package attributes for the 20-ball MicroStar Jr. package.

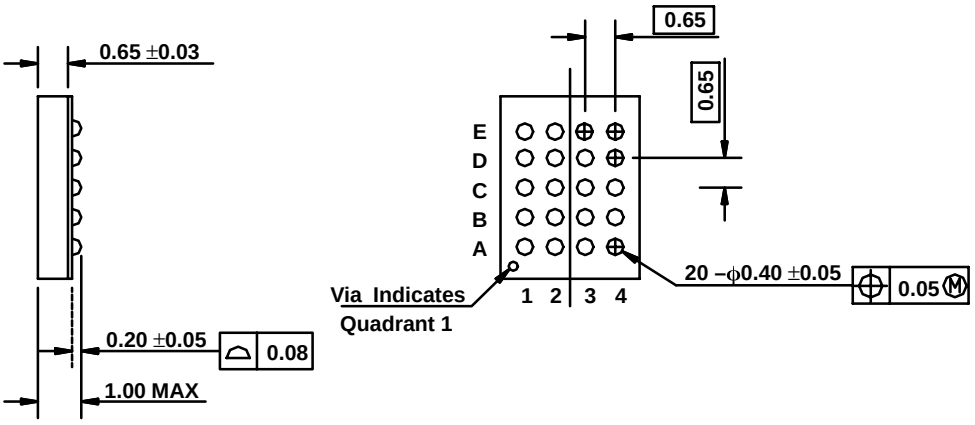
Table 4. 20-Ball MicroStar Jr.™ Package Attributes

ATTRIBUTE	MicroStar Jr. PACKAGE
Ball count	20
Ball configuration (rows, columns)	3 × 4
Ball-to-ball pitch (mm)	0.65
Square/rectangular	Rectangular
Ball diameter (mm)	0.35 minimum
Package body width (mm)	3
Package body length (mm)	4
Package thickness (total height, mm)	1 maximum
Package weight (g)	0.022
Shipping media, tape and reel (units)	1000
Desiccant pack	Level 2A†

† Package qualified at JEDEC level 2 moisture condition, 220°C reflow

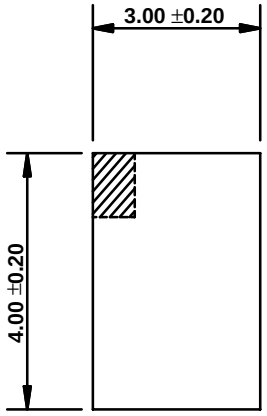
3.1.1 MicroStar Jr.™ Package Dimensions

Figures 2 and 3 show the physical dimensions of the 20-ball MicroStar Jr. package. Pin A1 quadrant is identified by the via.



All dimensions are in millimeters.

Figure 2. 20-Ball MicroStar Jr.™ Package, Profile and Bottom Views



All dimensions are in millimeters.

Figure 3. 20-Ball MicroStar Jr.™ Package, Top View

3.1.2 MicroStar Jr.™ Package Pinout Configurations

The pinout configuration in Figure 4 has the same naming convention that is applied in the industry to logic devices in 20-pin packages (i.e., TSSOP, TVSOP, SSOP).

	A	B	C	D	E
4	19§	18‡	16‡	14‡	12‡
3	20†	3‡	15‡	7‡	11‡
2	1§	17‡	5‡	13‡	9‡
1	2‡	4‡	6‡	8‡	10¶

† = V_{CC}
‡ = I/O and signal
§ = Control
¶ = Ground

Figure 4. 20-Pin Function Pin Assignment, Top View

3.1.3 Package Reliability

The 20-ball MicroStar Jr. package was qualified at the Joint Electronics Device Engineering Council (JEDEC) Moisture Level 2, and released at Level 2A. For optimum reliability, reflow(s) should be completed as soon as practical after removing components from dry pack, however, JEDEC Level 2A allows up to four weeks before baking is required (assuming ambient conditions of 30°C and 60% relative humidity).

Table 5 summarizes the package reliability data obtained during qualification testing. The test chip was an LVTH2245, die size 1.22 mm × 2.28 mm (48 mil × 90 mil), with preconditioning at JEDEC Level 2 (85°C and 60% relative humidity with three infrared (IR) reflows at 220°C).

Table 5. Package Reliability Qualification Results

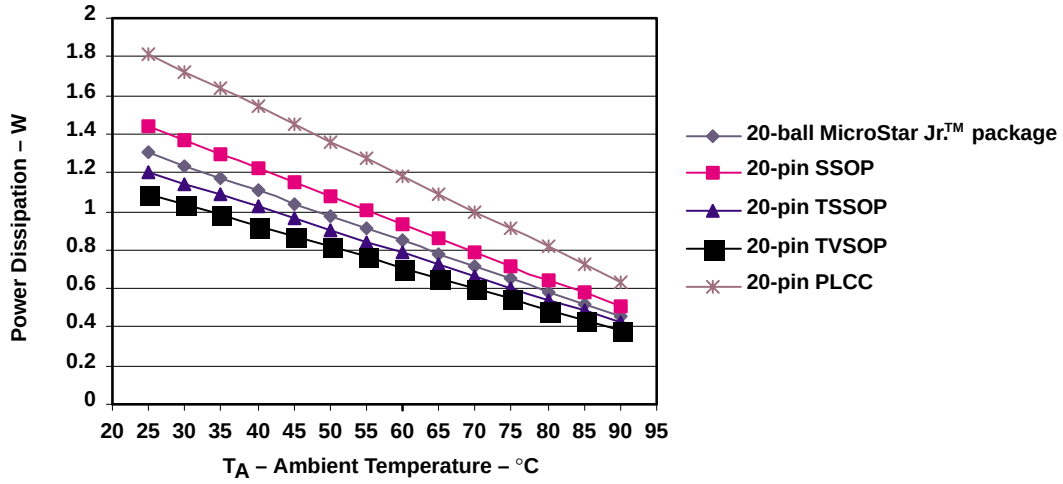
RELIABILITY QUALIFICATION TEST		SAMPLE SIZE/FAILS		
		QUALIFICATION LOT 1	QUALIFICATION LOT 2	QUALIFICATION LOT 3
Steady-state life test (150°C, 500 hours)		39/0	39/0	39/0
Highly Accelerated Stress Test (HAST) (130°C and 85% relative humidity)		26/0	26/0	26/0
Autoclave (121°C for 96 hours)		77/0	77/0	77/0
Solderability (8 hours steam age)		8/0	8/0	8/0
Flammability	UL	5/0	5/0	5/0
	IEC	5/0	5/0	5/0
Thermal shock (–85°C to 150°C, 1000 cycles)		77/0	77/0	77/0
Salt atmosphere		22/0	22/0	22/0
Moisture-sensitivity Level 2		12/0	12/0	12/0
High-temperature storage (150°C for 1000 hours)		45/0	45/0	45/0
X-ray		5/0	5/0	5/0
Physical dimensions		15/0	15/0	15/0
Manufacturability		Pass	Pass	Pass

Board-level reliability (BLR) testing was conducted using a packaged daisy-chain die measuring 2.0 mm × 1.0 mm. The package was soldered to a nonsolder-mask defined (NSMD) single-sided, 0.8-mm (31 mil)-thick board, with organic solder preservative (OSP)-finished copper pads of 0.40-mm diameter. Eutectic solder was used. Temperature-cycling parameters were –40°C to 125°C, with a 15-minute dwell at the extremes. The units passed 2460 thermal cycles with zero failures, and the test was terminated. Further BLR evaluations are planned and will incorporate temperature cycling on thicker boards plus four-point bending, torque, vibration, and shock tests. The results will be published when available.

3.1.4 Power Dissipation

Because of its small size, convective cooling per unit area is more efficient with the 20-ball MicroStar Jr. package compared to larger packages. However, conduction is the dominant mode of transfer, with a minor contribution from radiation. In the conduction mode, the balls serve as the sink path to the PCB. The number and weight of the metal layers, plus component layout and proximity to other power sources, have a significant effect on dissipation. Thermal performance is also significantly influenced by die size because conduction efficiency depends on the number of balls overlapped by the chip. However, PCB design has the largest effect, and models show that the introduction of a thermal via of 0.30-mm (12 mil) diameter at the ground ball improves performance up to an additional 12% to 17% on multimetal-layered PCBs. The performance data in Figure 5 was modeled using the JEDEC 1S2P test board, with thermal conductivity of approximately 18 W/mK. It must be emphasized that system-level performance is extremely dependent on numerous factors, such as PCB design, component layout and proximity to other power sources on the PCB, airflow, PCB orientation, and board-to-board spacing in the system upper-level assembly. The values for thermal impedance in Table 6 should be used only as guidelines for further system-level modeling, not as an indication of total system thermal performance.

Figures 5 through 7 compare the MicroStar Jr. package thermal performance to alternative packages, and illustrate the effect of forced cooling air on power dissipation, both with and without thermal vias.

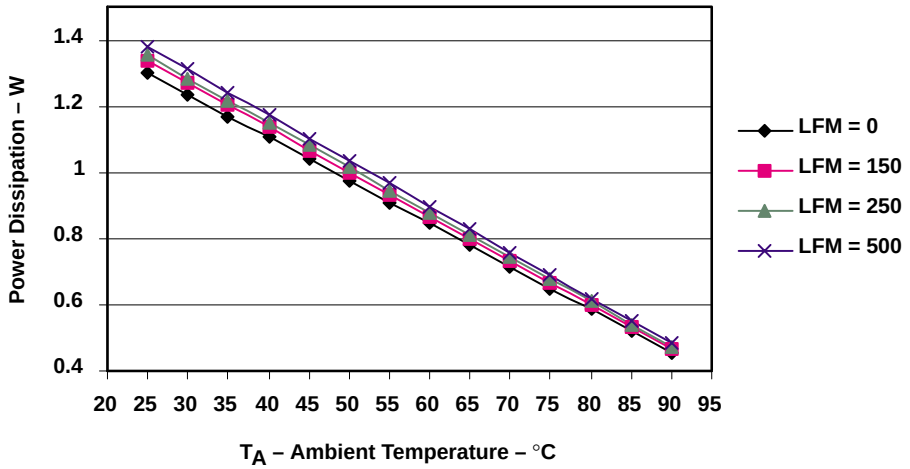


NOTE A: Power dissipation is calculated using T_J = 125°C. Die is 1.23 mm × 1.88 mm.

Figure 5. MicroStar Jr.™ Package Thermal Comparison on Multilayer JEDEC 1S2P Test Board, Zero Airflow, No Thermal Vias

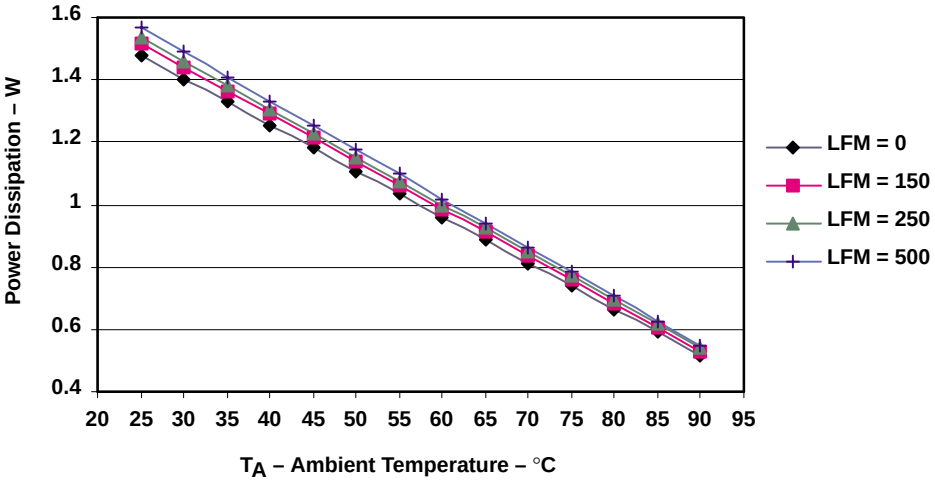
Table 6. Thermal-Impedance Guidelines

	AIR VELOCITY (LFM)			
	0	150	250	500
θ_{ja} (°C/W)	76.9	74.9	73.9	72.5
θ_{jc} (°C/W)	53.5			
θ_{jb} (°C/W)	36.3			



NOTE A: Power dissipation is calculated using T_J = 125°C, with thermal via at pin E1. Die is 1.23 mm × 1.88 mm.

Figure 6. MicroStar Jr.™ Package Thermal Performance on Multilayer JEDEC 1S2P Test Board, at Various Airflow Velocities, No Thermal Vias



NOTE A: Power dissipation is calculated using T_J = 125°C, with thermal via at pin E1. Die is 1.23 mm × 1.88 mm.

Figure 7. Effect of Thermal Vias on MicroStar Jr.™ Package Thermal Performance on JEDEC 1S2P Test Board at Various Airflow Velocities

Table 7. Effect of Vias on Thermal Impedance

	AIR VELOCITY (LFM)			
	0	150	250	500
θ_{ja} with vias (°C/W)	67.8	65.9	65	63.8
Via effect on power dissipation	17%	14.85%	13.7%	12%

A comparison of the area normalized thermal dissipation for the TSSOP, TVSOP, and 20-ball MicroStar Jr. package shows that the 20-ball MicroStar Jr. package at 25°C (zero airflow and no thermal vias) exceeds TVSOP by 68% and TSSOP by 73% (see Figure 8).

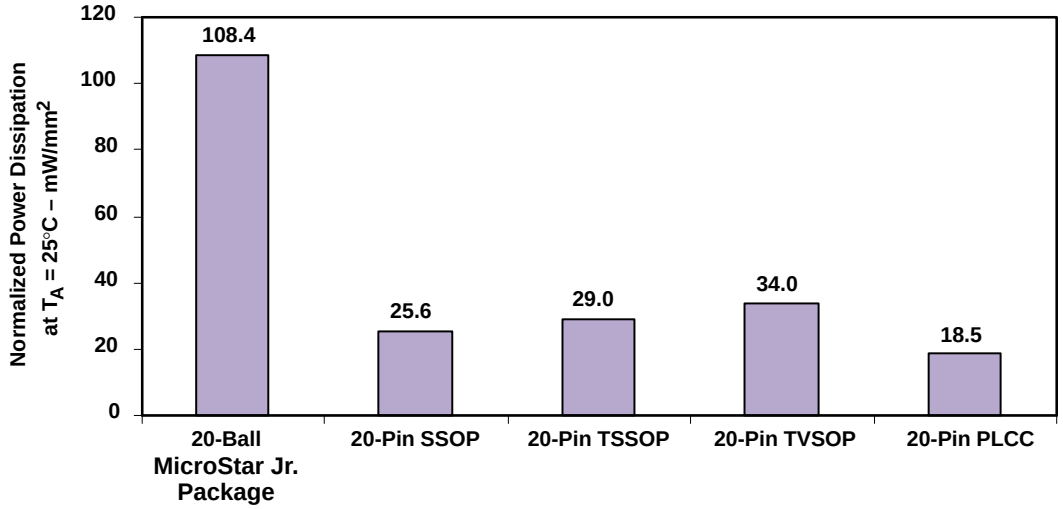


Figure 8. Area Normalized Power Dissipation at T_A = 25°C Using JEDEC 1S2P Test Board

3.2 Electrical Characteristics

3.2.1 Package Parasitics

Inductance is directly related to the length of a wire and its proximity to the ground plane. Any wire naturally creates an inductor. The longer the wire, the greater is its inductance. Inductance occurs when current is induced into a wire, creating an electromagnetic field. The closer this induced electromagnetic field is to ground, the less effective it becomes. As the wire gets shorter and/or closer to the ground plane, its inductance decreases.

Capacitance is created when two plates (wires, lines, or layers) overlap and are separated by a given distance. This distance can be insulated by air, plastic, glass, or other material. Capacitance can be calculated by the following formula:

$$C = \frac{(0.225 \epsilon_r A)}{d} \quad (1)$$

Where:

C = capacitance
ϵ_r = dielectric value of insulator
A = area of plates overlap
d = distance between plates

Area (A) is the part of the equation that changes the most from package to package. The distance between the plates (wires or balls) varies somewhat, while the package material and the dielectric value of the insulator (ϵ_r) remain constant. The plate area is greatly reduced in the BGA package because solder balls are used instead of the standard wire solder leads seen in other packages. Two adjacent balls create a much smaller overlap area than two adjacent wire leads. As the spacing between plates increases, capacitance decreases.

The 20-ball MicroStar Jr. package is the smallest package offered by TI for 20-pin devices. The reduced size has a positive effect on inherent inductance and capacitance of a packaged device.

Table 8 summarizes the parasitic inductance and capacitance characteristics of the 20-ball MicroStar Jr. package. Minimum, mean, and maximum values are given for all 20 balls in the package.

Table 8. Electrical Characteristics of the 20-Ball MicroStar Jr.™ Package

	L (nH)	C (pF)
Minimum	0.896	0.064
Mean	1.317	0.113
Maximum	2.088	0.190

Table 9 summarizes the differences between the 20-ball MicroStar Jr. package and other 20-pin package alternatives. The 20-ball MicroStar Jr. package offers 62% less inductance and 73% less capacitance than the 20-pin SSOP package. Resistance values were virtually unchanged and are omitted.

Table 9. Comparison of 20-Ball MicroStar Jr.™ Package Parasitics to Alternative Packages

PACKAGE	L (nH)	C (pF)	%ΔL	%ΔC
20-ball MicroStar Jr.	1.317	0.113		
20-pin TSSOP	2.694	0.156	51.1	27.6
20-pin TVSOP	2.561	0.342	48.6	67
20-pin SSOP	3.495	0.420	62.3	73
20-pin PLCC	2.610	0.389	49.5	71

3.3 JEDEC Definition

The 20-ball VFBGA received final registration from JEDEC JC-11 under semiconductor package standard MO-225. The device pinout was submitted to the JC-40 Council, and passed a final council vote in March 2001.

3.4 VFBGA Benefits

In summary, key features and corresponding advantages for logic products assembled in the MicroStar Jr. VFBGA package are:

- Minimum footprint available in the industry allows use of the smallest board area among all industry-standard packages. Required trace width and spacing is well defined for major PCB manufacturers.
- Vastly improved parasitic capacitance and inductance provides better high-speed performance.
- JEDEC standard package under MO-225 meets worldwide mechanical and pinout specifications.
- No external components required, other than decoupling capacitors, which translates to lower cost, lower maintenance, and higher reliability
- Improved thermal performance over TSSOP and TVSOP packages. Improved device reliability over alternative packages.
- Lower ground bounce provides more noise margin.
- Minimized skew pattern provides additional design margin for high-speed buses.
- High assembly yields, with documented defect levels of 4 ppm and less

3.5 Evaluation Units

For evaluation units, contact authorized distributors or, for more information, refer to:

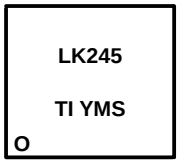
http://www.ti.com/sc/msjunior

4 MicroStar Jr.™ Package Marking and Packing

4.1 Marking

TI uses a laser to mark the product number, year and month manufactured, lot trace code, manufacturing site, and pin 1 location.

A device marking example for the LVTH2245 is shown in Figure 9.



Part Number: LVTH2245
Year, Month, Site
o: Pin 1 Location

Figure 9. Device Marking Example

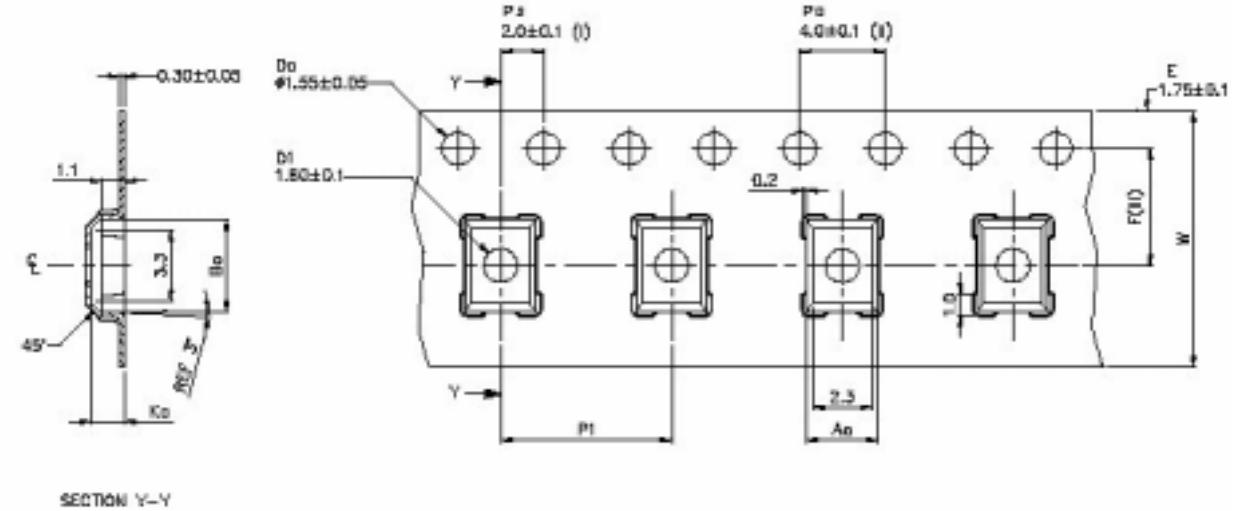
The namerule for the MicroStar Jr. VFGBA package is rule C1, with seven characters maximum. Table 10 shows the namerule logic and how each marking is derived. The key to the naming convention is to first note the alphanumeric code under namerule A. This code under namerule A is condensed into the codes under namerules B and C, and the remaining function numbers are added on in place of the asterisks. For example, to mark an SN74ALVCH374 VFBGA device, note that the code under namerule A is SN74ALVCH***. Namerule C applies to VFBGA, therefore, SN74ALVCH is replaced by the code VB found under namerule C. The remaining function numbers (374) are added onto VB to get VB374.

Table 10. Samples of Name Markings for Various 20-Ball MicroStar Jr.™ Package Offerings

DEVICE NAME	NAMERULE A	NAMERULE B	NAMERULE C	TOP-SIDE MARKING
SN74ALVCH374	SN74ALVCH***	ALVCH***	VB***	VB374
SN74ABT245B	SN74ABT2***	ABT2***	AA***	AA245B
SN74ALVC244	SN74ALVC***	ALVC***	VA***	VA244
SN74CBT3245A	SN74CBT32***	CBT32***	BV***	BV3245A
SN74LV573A	SN74LV***	LV***	LV***	LV573A

4.2 Tape and Reel

Embossed tape and reel feed is the preferred method for automatic pick and place machines. TI offers tape and reel packaging for the 20-ball MicroStar Jr. package. The standard quantity is 1000 units per reel. Packaging materials include the carrier tape, cover tape, and reel. All materials used meet industry guidelines for ESD protection and comply fully with EIA Standard 481-A, *Taping of Surface Mount Components for Automatic Placement*. The dimensions of interest to the end user are tape width (W), pocket pitch (P), and quantity per reel. Figure 10 and Table 11 show the carrier tape dimensions. Figure 11 gives dimensions of the reel assembly.



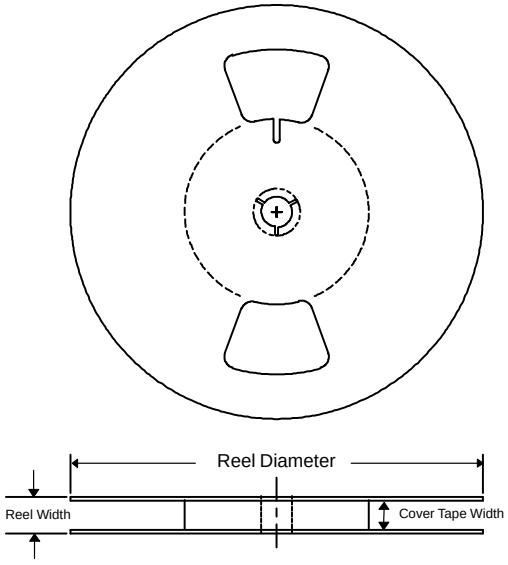
NOTE A: All dimensions are in millimeters.

Figure 10. Tape Dimensions

Table 11. Carrier Tape Dimensions†

CARRIER TAPE WIDTH (W)	POCKET PITCH (P1)	POCKET WIDTH (A0)	POCKET LENGTH (B0)	POCKET DEPTH (K0)	HOLE-TO-POCKET CENTERLINE (P2)	HOLE-TO-POCKET CENTERLINE (F)	SPROCKET HOLE PITCH (P0)	DEVICE QUANTITY PER REEL
12.00 ± 0.3	8.00 ± 0.1	3.30 ± 0.1	4.30 ± 0.1	1.60 ± 0.1	2.0 ± 0.1	5.50 ± 0.1	4.0 ± 0.1	1000

† All dimensions are in millimeters.



REEL WIDTH (mm)	REEL DIAMETER (mm)
12.00 +2.0/–0	330 maximum

NOTE A: Standard quantity is 1000 devices per reel, however, this is subject to change per market demand.

Figure 11. Reel Assembly Dimensions

4.3 Sockets and Socket Ordering Information

Loranger part number: 040030020U6617

Loranger International Corporation
817 Fourth Avenue
Warren, PA 16365
Telephone: (814) 723-2250

5 Conclusion

This application report shows that the 20-ball MicroStar Jr. package is the optimal solution for addressing performance and economic issues such as:

- PCB area savings of up to 71% over TSSOP
- Minimized skew by reducing pin-to-pin inductance, thereby enabling support for high-speed applications with greater bandwidth
- Improved thermal dissipation
- Improved board-mount assembly yields inherent in BGA processes

The spacing between balls for this 0.65-mm VFBGA package is equal to that of other 0.8-mm-pitch BGA packages, therefore, defect rates due to solder bridging are similar to those of larger BGA packages. AC performance of the MicroStar Jr. package has a definite advantage over other standard packages. The simultaneous-switching data and graphs [see *16-Bit Widebus™ Logic Families in 56-Ball, 0.65-mm Pitch, Very Thin Fine-Pitch BGA (VFBGA) Packages* application report (SZZA029)] clearly show this smaller package, with its lower capacitance and inductance, has speed and noise advantages over the SSOP, TSSOP, and TVSOP packages. Designers using the MicroStar Jr. package can take advantage of the win-win combination of electrical and physical properties offered.

With the introduction of the MicroStar Jr. VFBGA packages by TI, OEMs are assured of a standardized JEDEC package, pinout, and availability of the previously stated product families and functions. More device families and functions will be included in the MicroStar Jr. package as market interest dictates.

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