Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4 High Tg	5.00mil	4.2	
5	Signal Layer 1	Copper	1.40mil		
6	Dielectric 2	FR-4 High Tg	24.40mil	4.2	
7	Signal Layer 2	Copper	1.40mil		
8	Dielectric 3	FR-4 High Tg	5.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACE WIDTH: 10 MIL
MIN. CLEARANCE: 2.9 MIL
MIN. VIA HOLE SIZE: 18 MIL
MINIMUM ANNULAR RING: 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 40 MIL (1.0mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:
SILKSCREEN: ☒ TOP ☐ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

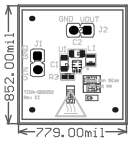
ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☒ 6.1MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]

TEXAS INSTRUMENTS

PROJECT TITLE: TPS6290X
DESIGNED FOR: Public Release
FILE NAME: TIDA-050052.PcbDoc

ENGINEER: Tahar Allag	LAYOUT BY: Fred Illguth
SCALE: 0.72	ALTIUM DESIGNER VERSION: 18.1.11.251

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric 1	FR-4 High Tg	5.00mil	4.2	
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9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION:
MIN. TRACE WIDTH: 10 MIL
MIN. CLEARANCE: 2.9 MIL
MIN. VIA HOLE SIZE: 18 MIL
MINIMUM ANNULAR RING: 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 40 MIL (1.0mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [ ] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[X] 6.1MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
[ ] OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
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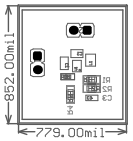

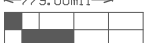

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]

ALTIUM DESIGNER DRAWING CODE	A	BOARD NO: TIDA-050052	REV: A	SUNEREG: Not to be reproduced	
LAYER NAME = Assembly Drawing Bottom		TID #: .TIDDIT.	# DIT		
PLOT NAME: Layer 1 Assembly Drawing GENERATED :: 8/12/2021 8:01:25 AM				TEXAS INSTRUMENTS	

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TEXAS INSTRUMENTS

PROJECT TITLE: TPS6290X

DESIGNED FOR: Public Release

FILE NAME: TIDA-050052.PcbDoc

ENGINEER:	LAYOUT BY:
Tahar Allag	Fred Illguth
SCALE: 0.72	ALTIUM DESIGNER VERSION: 18.1.11.251

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
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9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
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DESIGN INFORMATION:
MIN. TRACE WIDTH: 10 MIL
MIN. CLEARANCE: 2.9 MIL
MIN. VIA SIZE: 18 MIL
MINIMUM ANNULAR RING: 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 40 MIL (1.0mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [ ] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
[X] 6.1MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
[ ] XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
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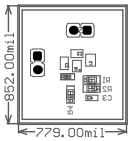

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]

	A	BOARD #	REV: A		
LAYER NAME = Bottom		TID #: .TIDIT.	:# DIT		
	Layer 2Assembly	GENERATED :: 8/12/2021		TEXAS INSTRUMENTS	

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TEXAS INSTRUMENTS

PROJECT TITLE: TPS6290X
DESIGNED FOR: Public Release
FILE NAME: TIDA-050052.PcbDoc

ENGINEER:	LAYOUT BY:
Tahar Allag	Fred Illguth
SCALE: 0.72	ALTIUM DESIGNER VERSION: 18.1.11.251

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
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THICKNESS: [X] 40 MIL (1.0mm) +/-10% [ ] OTHER
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[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [ ] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

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[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
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PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
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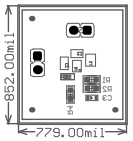

1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
ASSEMBLY VARIANT: [No Variations]

TEXAS INSTRUMENTS

PROJECT TITLE: TPS6290X
DESIGNED FOR: Public Release
FILE NAME: TIDA-050052.PcbDoc

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ENGINEER:	LAYOUT BY:
Tahar Allag	Fred Illguth
SCALE: 0.72	ALTIUM DESIGNER VERSION: 18.1.11.251

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