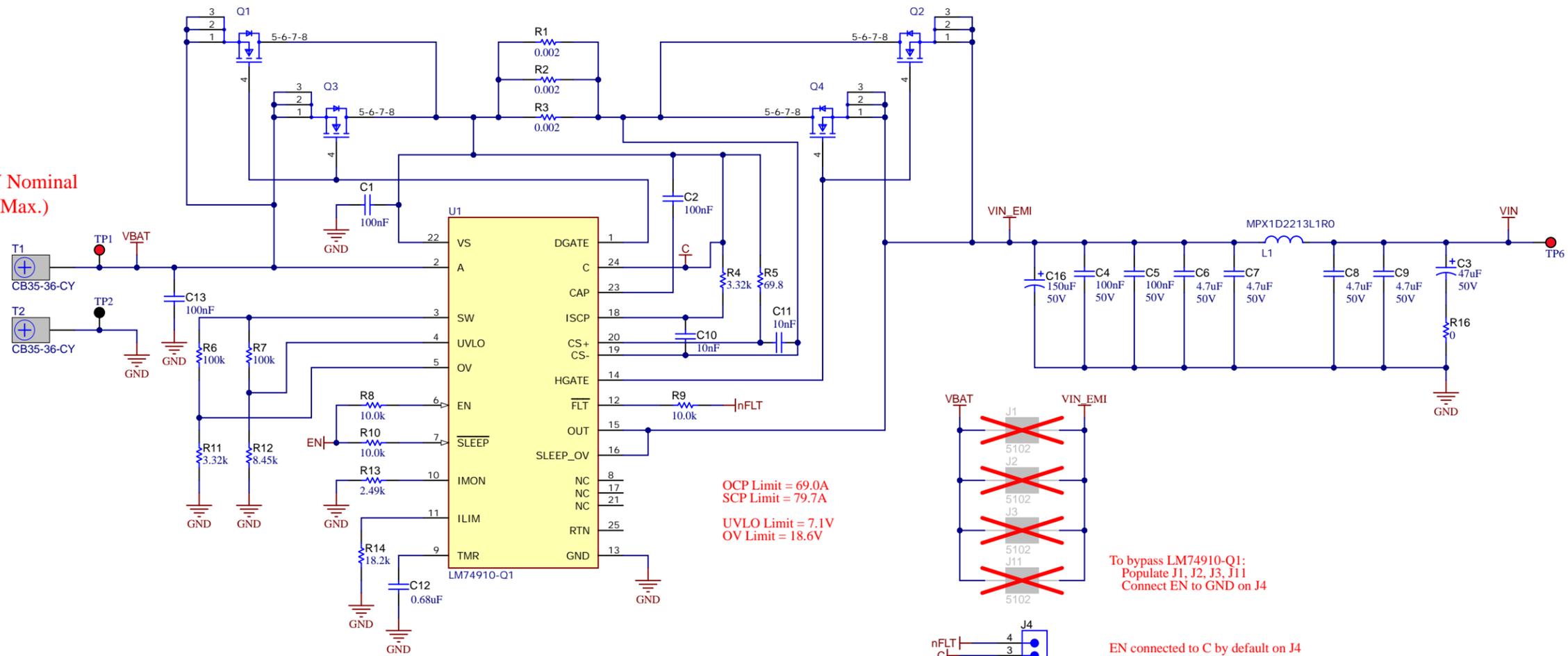


Input Voltage = 12V Nominal
(8V Min.; 18V Max.)

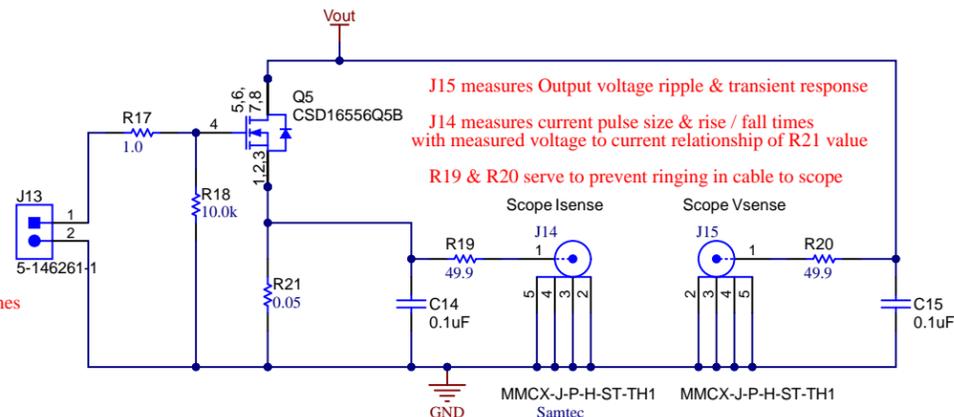


OCP Limit = 69.0A
SCP Limit = 79.7A
UVLO Limit = 7.1V
OV Limit = 18.6V

To bypass LM74910-Q1:
Populate J1, J2, J3, J11
Connect EN to GND on J4

EN connected to C by default on J4

Signal generator in "Pulse" mode
Start with 1.0 msec pulse at 10 Hz for 1% duty
Adjust pulse height to get desired current pulse size
Adjust pulse rise / fall to get desired current rise & fall times



J14 & J15 each mate with Amphenol 523-095-850-206-024 which mates with BNC male to male cable, which then plugs into Scope input

Orderable: ChangeMe in variant	Designed for:	Mod. Date: 10/31/2024
TID #: N/A	Project Title:	
Number: PMP23578	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 1 of 5
Drawn By:	File: PMP23578_3xMistral_FrontEnd.SchDoc	Size: B
Engineer: Matthew Bowers	Contact: http://www.ti.com/support	

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A

B

C

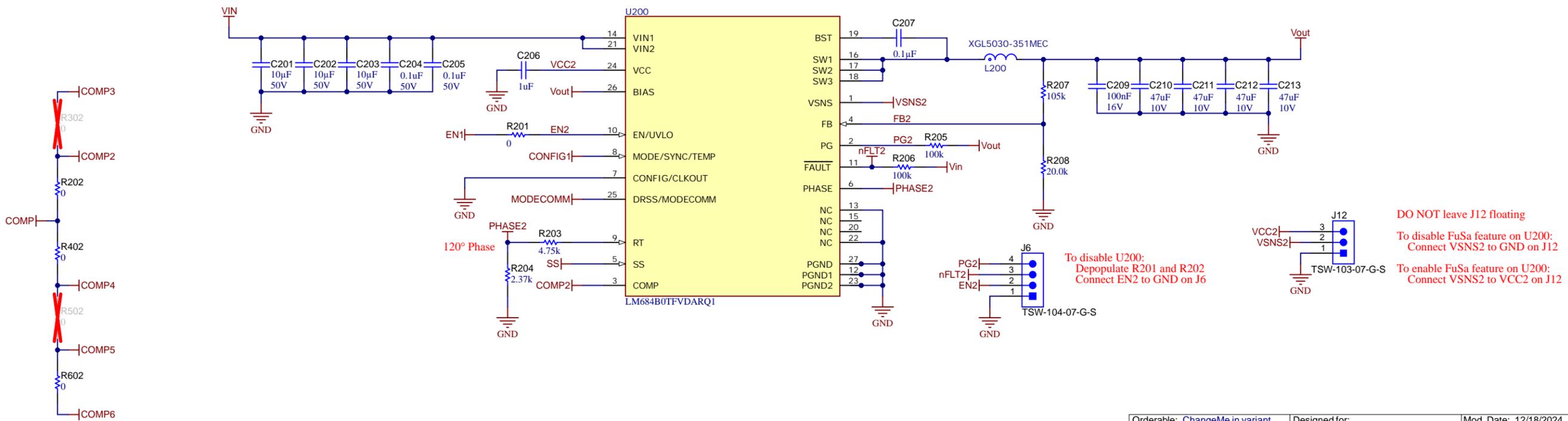
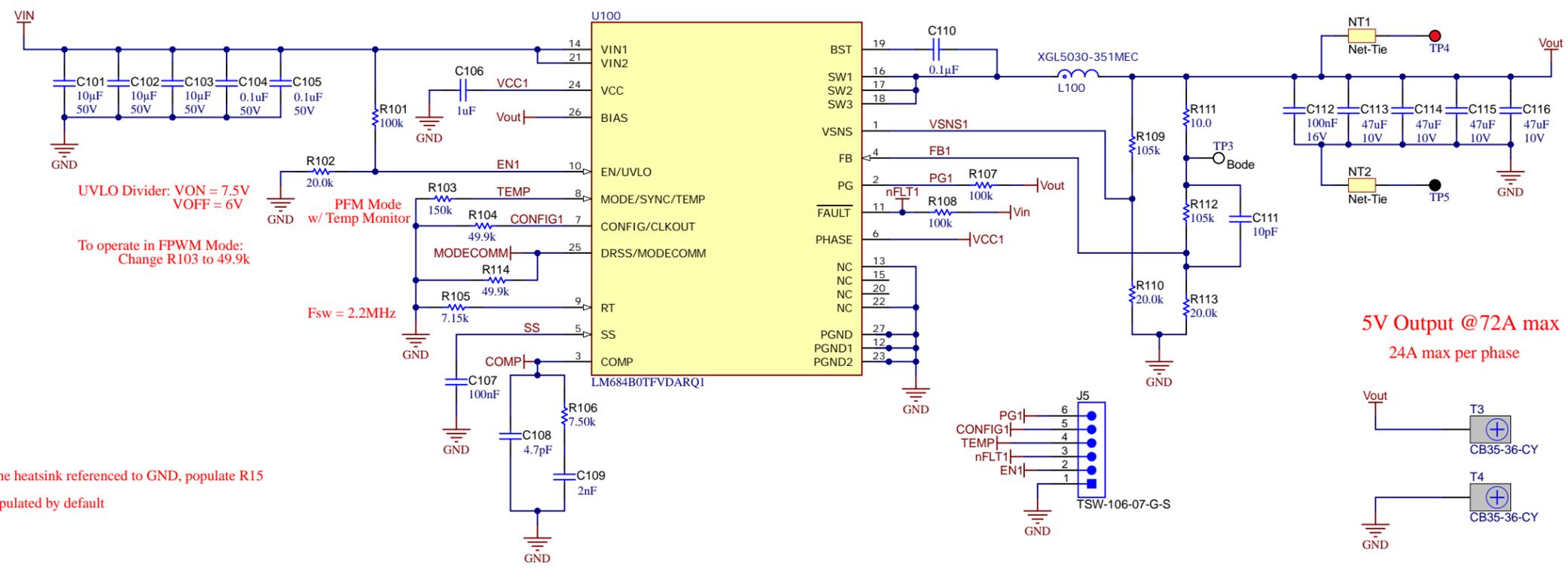
D

A

B

C

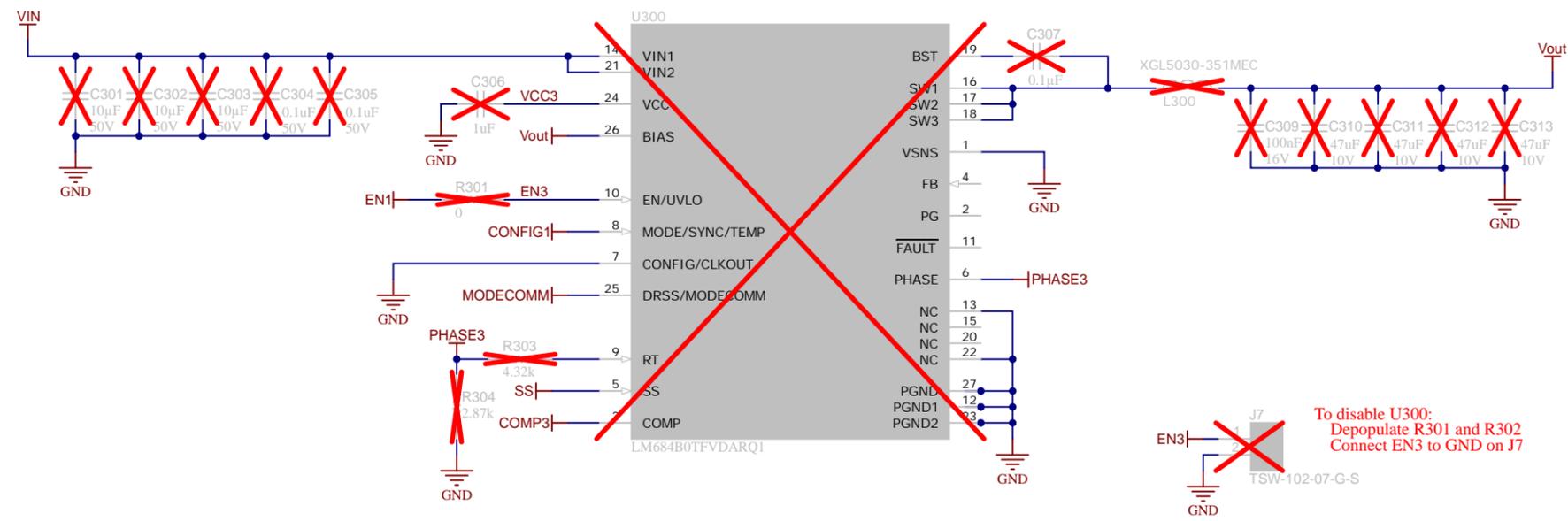
D



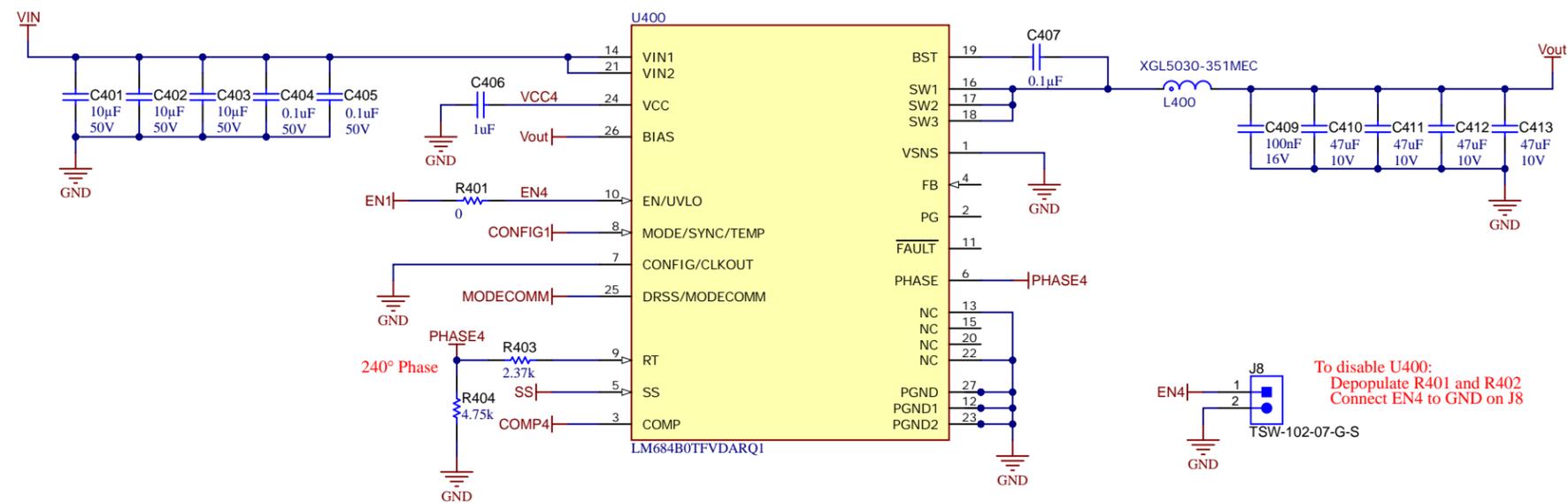
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Orderable: ChangeMe in variant	Designed for:	Mod. Date: 12/18/2024
TID #: N/A	Project Title:	
Number: PMP23578	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001	Sheet 2 of 5
Drawn By:	File: PMP23578_3xMistral_Phase1_Phase2.SchDoc	Size: B
Engineer: Matthew Bowers	Contact: http://www.ti.com/support	





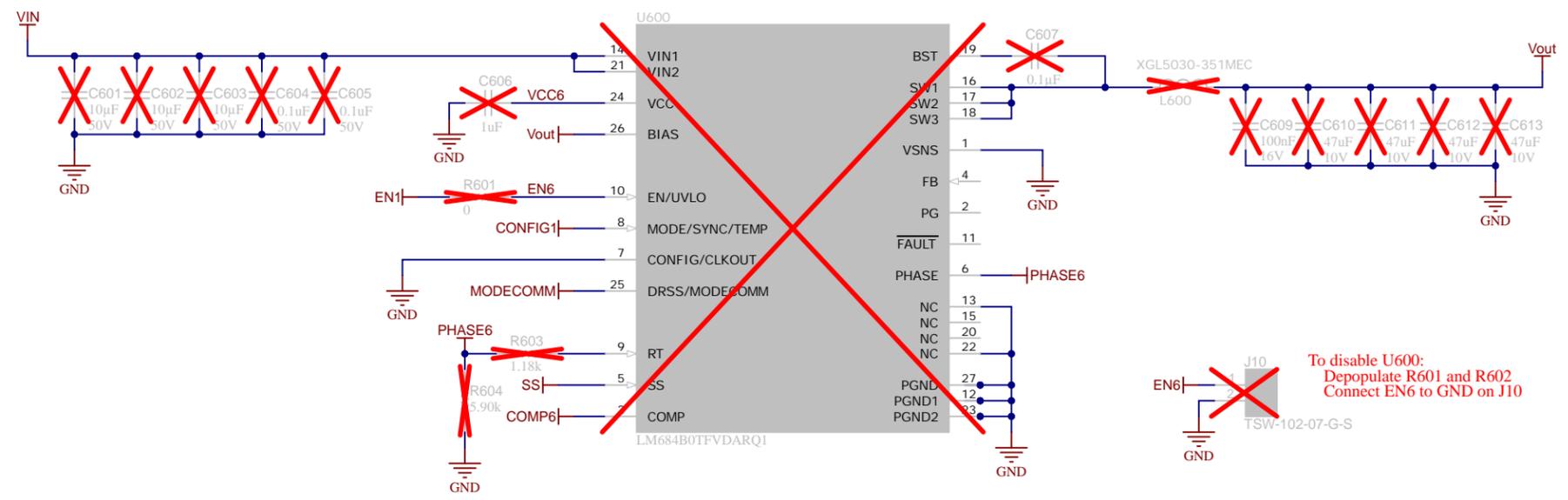
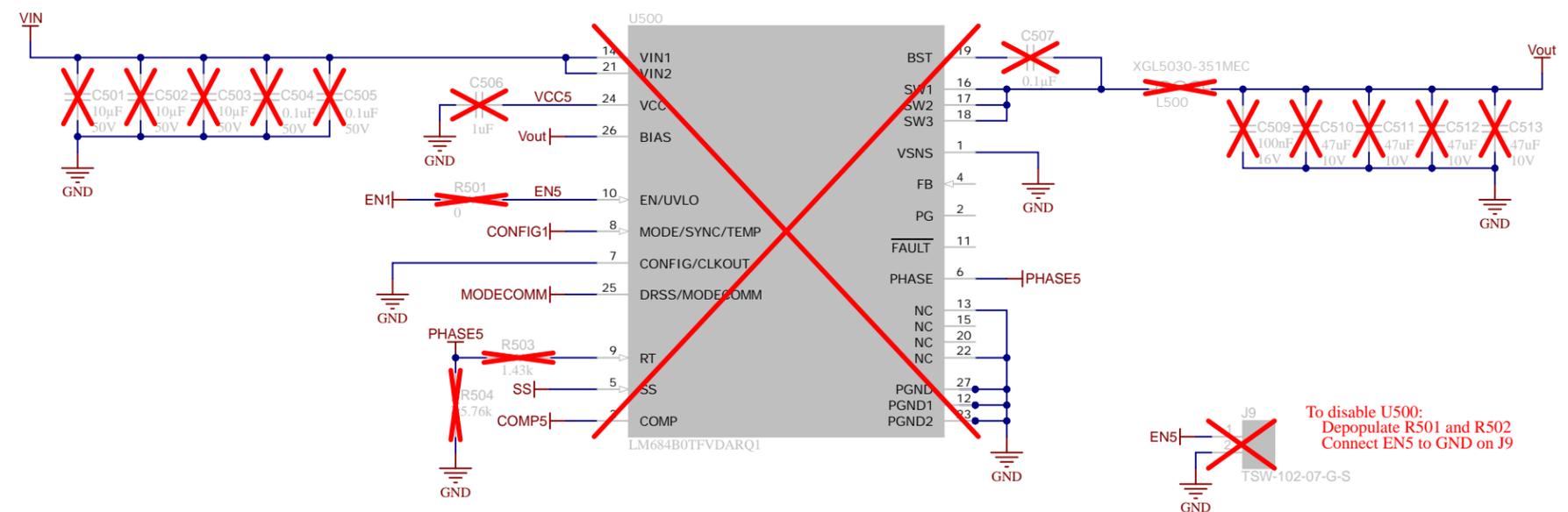
To disable U300:
 Depopulate R301 and R302
 Connect EN3 to GND on J7



To disable U400:
 Depopulate R401 and R402
 Connect EN4 to GND on J8

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Orderable: ChangeMe in variant	Designed for:	Mod. Date: 12/18/2024
TID #: N/A	Project Title:	
Number: PMP23578	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 3 of 5
Drawn By:	File: PMP23578_3xMistral_Phase3_Phase4.SchDoc	Size: B
Engineer: Matthew Bowers	Contact: http://www.ti.com/support	



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Orderable: ChangeMe in variant	Designed for:	Mod. Date: 12/18/2024
TID #: N/A	Project Title:	
Number: PMP23578	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 4 of 5
Drawn By:	File: PMP23578_3xMistral_Phase5_Phase6.SchDoc	Size: B
Engineer: Matthew Bowers	Contact: http://www.ti.com/support	



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H1 NY PMS 440 0025 PH
 H2 NY PMS 440 0025 PH
 H3 NY PMS 440 0025 PH
 H4 NY PMS 440 0025 PH

H5 1902C
 H6 1902C
 H7 1902C
 H8 1902C

H9 PMSSS 440 0025 PH
 H10 PMSSS 440 0025 PH
 H11 PMSSS 440 0025 PH
 H12 PMSSS 440 0025 PH
 H13 PMSSS 440 0025 PH
 H14 PMSSS 440 0025 PH

~~FID1~~
~~FID2~~
~~FID3~~

PCB Number: PMP23578
 PCB Rev: A

PCB LOGO
 Texas Instruments



PCB LOGO
 FCC disclaimer

PCB LOGO
 WEEE logo



Variant/Label Table

Variant	Label Text
001	

LBL1
 PCB Label
 THT-14-423-10
 Size: 0.65" x 0.20 "

ZZ1
 Label Assembly Note
 This Assembly Note is for PCB labels only

ZZ2
 Assembly Note
 These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
 Assembly Note
 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
 Assembly Note
 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: ChangeMe in variant	Designed for:	Mod. Date: 12/4/2024
TID #: N/A	Project Title:	
Number: PMP23578	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 5 of 5
Drawn By:	File: PMP23578_3xMistral_Hardware.SchDoc	Size: B
Engineer: Matthew Bowers	Contact: http://www.ti.com/support	

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