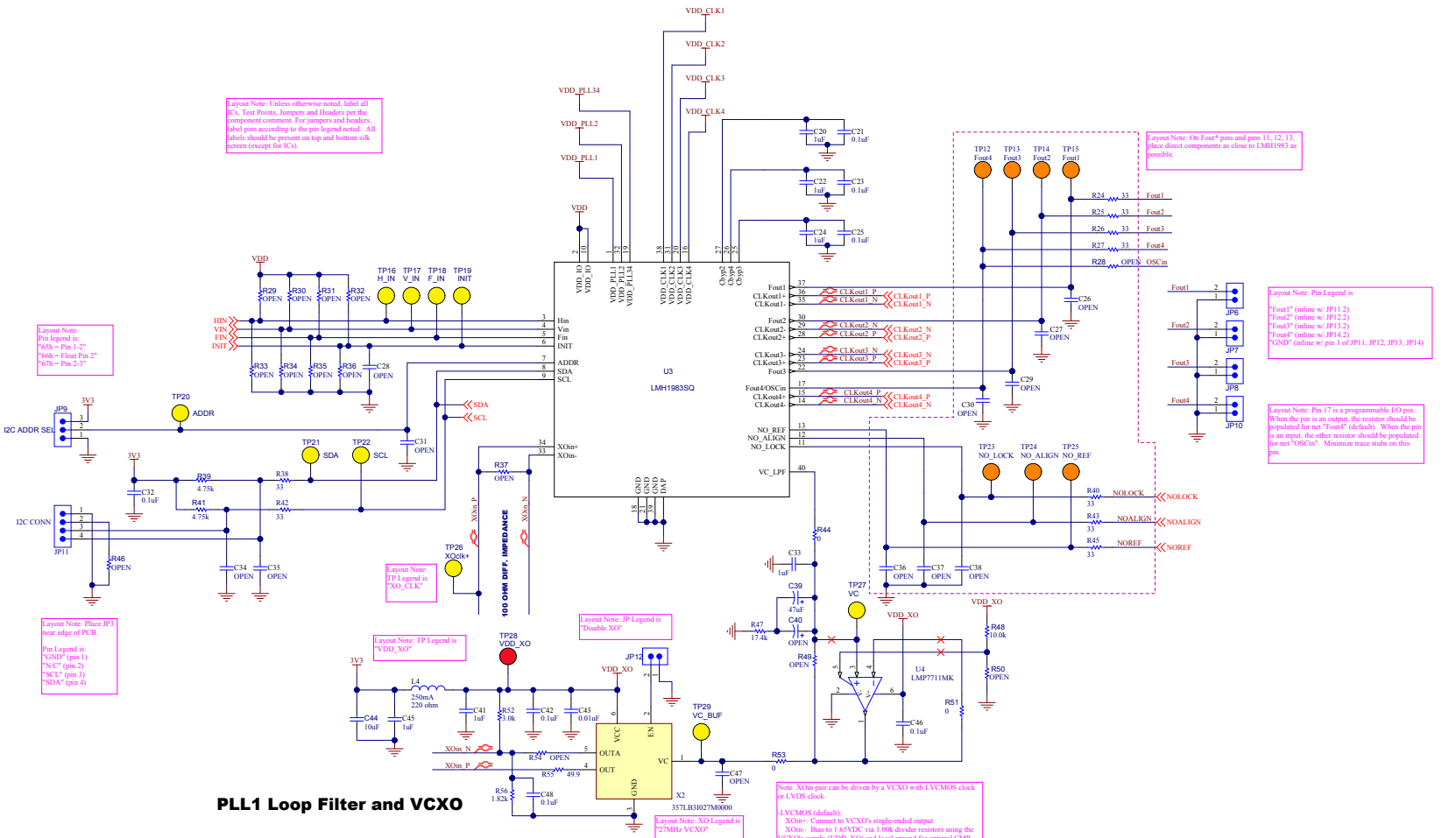
Layout Note: Unless otherwise noted, label all ICs, Test Points, Jumpers and Headers per the component comment. For jumpers and headers, label pins according to the pin legend noted. All labels should be present on top and bottom silk screen (except for ICs).
Layout Note: On Fout* pins and pins 11, 12, 13, place direct components as close to LMH1983 as possible.
Layout Note: Pin Legend is
"Fout1" (inline w/ JP11.2)
"Fout2" (inline w/ JP12.2)
"Fout3" (inline w/ JP13.2)
"Fout4" (inline w/ JP14.2)
"GND" (inline w/ pin 1 of JP11, JP12, JP13, JP14)
Layout Note: Pin 17 is a programmable I/O pin. When the pin is an output, the resistor should be populated for net "Fout4" (default). When the pin is an input, the other resistor should be populated for net "OSCin". Minimize trace stubs on this pin.
Layout Note: Pin legend is: "65h = Pin 1-2" "66h = Float Pin 2" "67h = Pin 2-3"
Layout Note: Place JP3 near edge of PCB. Pin Legend is: "GND" (pin 1) "N/C" (pin 2) "SCL" (pin 3) "SDA" (pin 4)
Layout Note: TP Legend is "XO_CLK"
Layout Note: JP Legend is "Disable XO"
Layout Note: TP Legend is "VDD_XO"
Layout Note: XO Legend is "27MHz VCXO"
Note: XOin pair can be driven by a VCXO with LVCMOS clock or LVDS clock.
-LVCMOS (default):
XOin+: Connect to VCXO's single-ended output.
XOin-: Bias to 1.65VDC via 1.00k divider resistors using the VCXO's supply (VDD_XO) and local ground for optimal CMR.
OUTA (VCXO pin 5): No connect (N/C)
-LVDS:
XOin+/-: Connect to VCXO's LVDS output and terminated with 100R differential.
OUTA: Complementary LVDS output pin. Remove 1k resistors and 0.1uF cap and install series resistor.
100 OHM DIFF. IMPEDANCE
PLL1 Loop Filter and VCXO
TIDA-00424 Video Sync Clock Generator
Title: TIDA-00424(Video Sync Clock Generator) - LMH1983
Size: C
Number:
Revision: B
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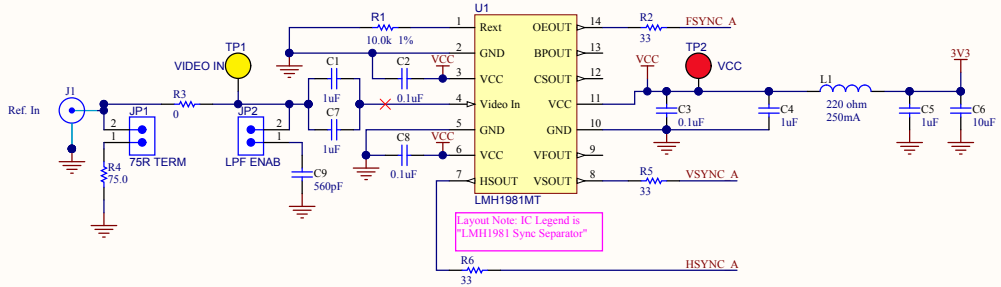
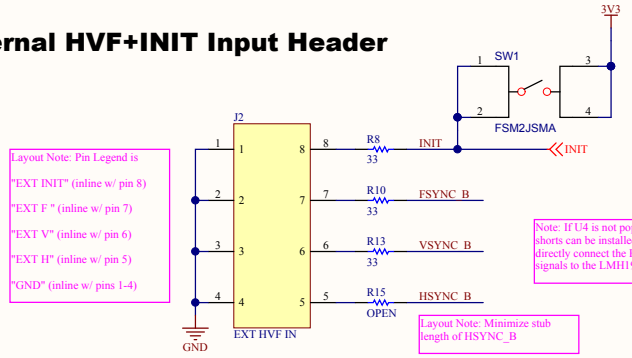
File: C:\Users\...\TIDA-00424 LMH1983 Sch.DsnDrawn By:

Analog Input and LMH1981 Sync Separator



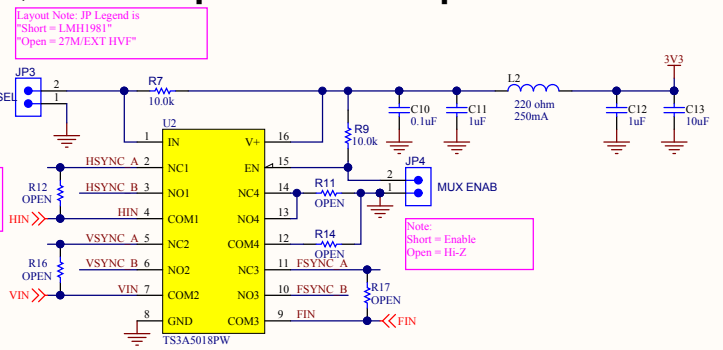
Layout Note: Unless otherwise noted, label all ICs, Test Points, Jumpers and Headers per the component comment. For jumpers and headers, label pins according to the pin legend noted. All labels should be present on top and bottom silk screen (except for ICs).

External HVF+INIT Input Header

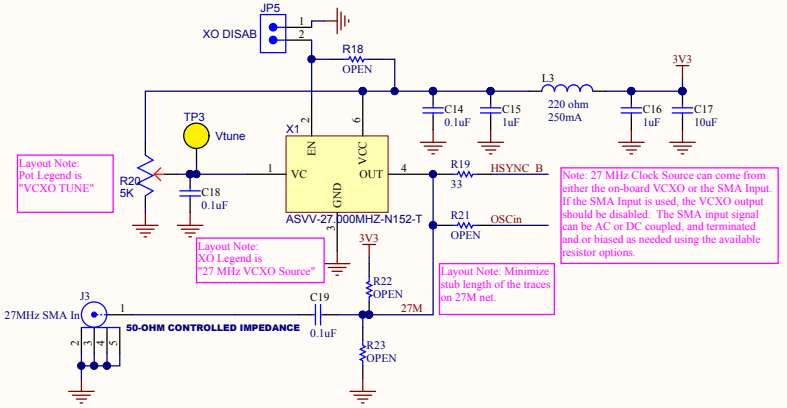


Note: If U4 is not populated, shorts can be installed to directly connect the HVF signals to the LMH1983 inputs.

Quad SPDT Input MUX with Output Hi-Z

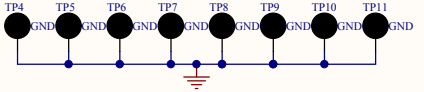


27 MHz Clock Source from VCXO or SMA Input



Note: 27 MHz Clock Source can come from either the on-board VCXO or the SMA Input. If the SMA Input is used, the VCXO output should be disabled. The SMA input signal can be AC or DC coupled, and terminated and/or biased as needed using the available resistor options.

Layout Note: Distribute GND test points around the PCB.



Title: TIDA-00424(Video Sync Clock Generator) - LMH1981		
Size: B	Number:	Revision: B
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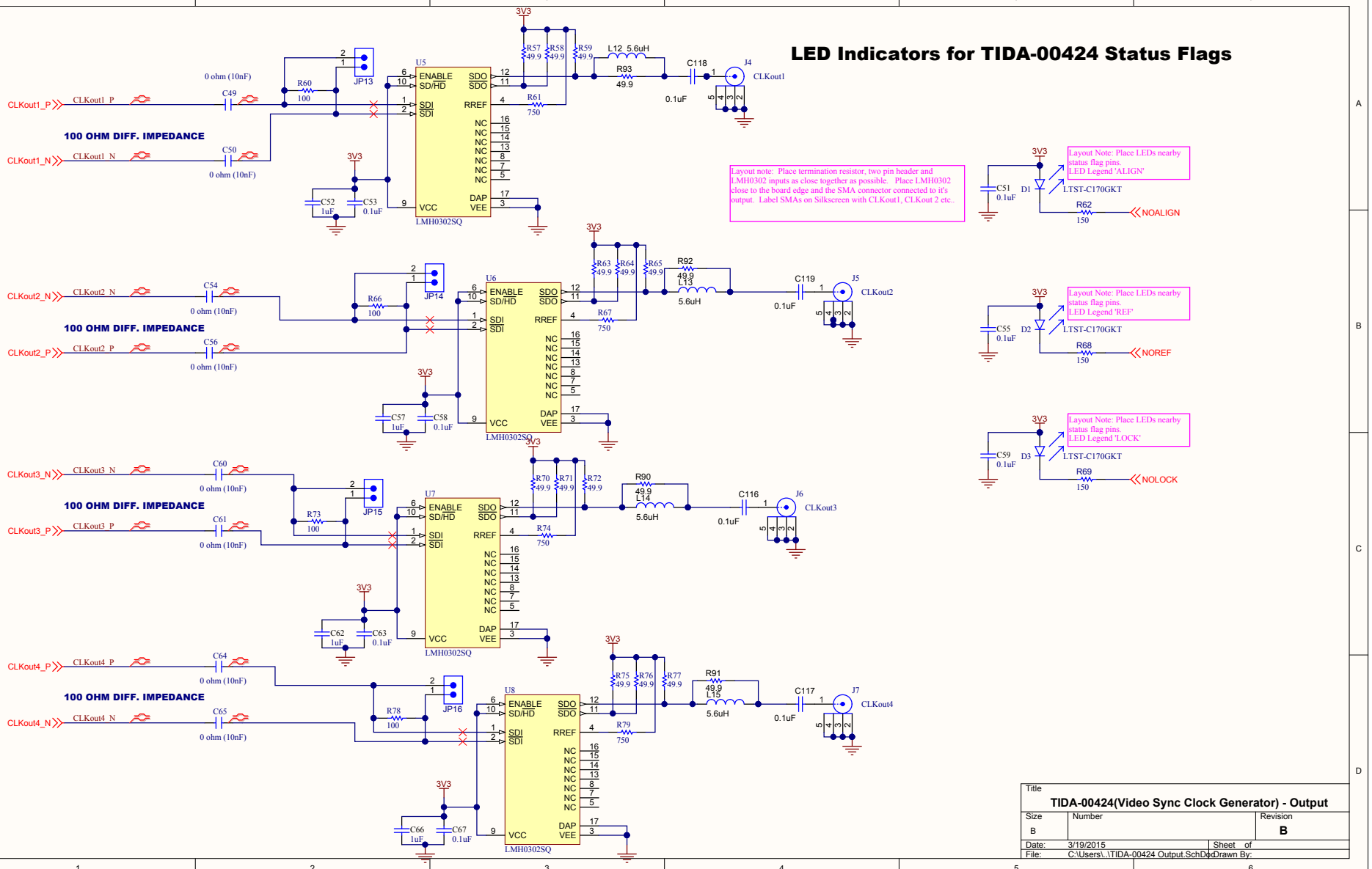
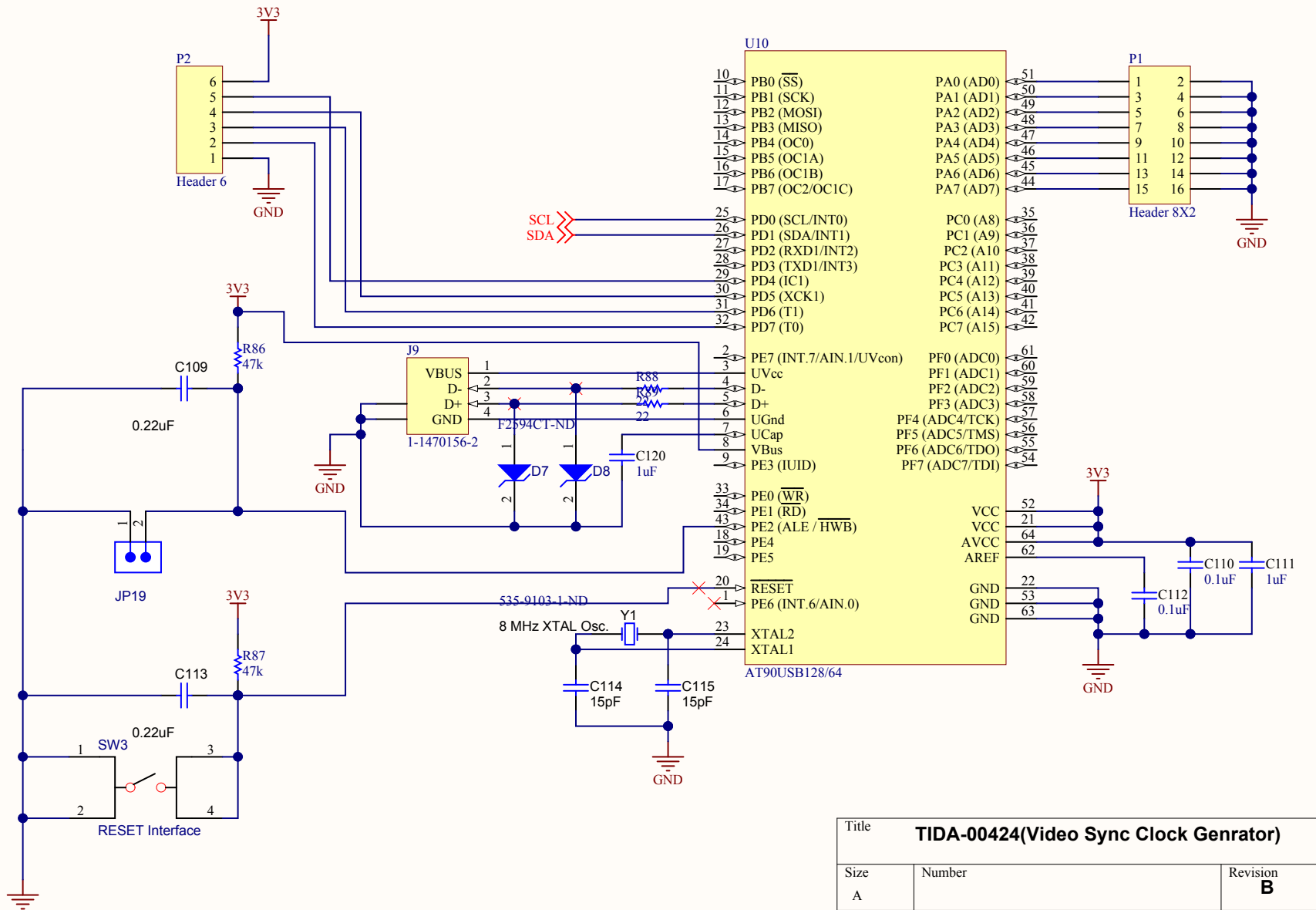
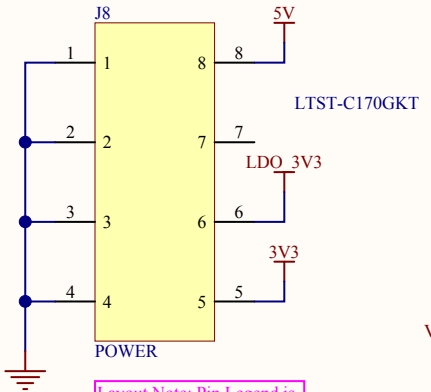

LED Indicators for TIDA-00424 Status Flags
CLKout1_P
CLKout1_N
CLKout2_P
CLKout2_N
CLKout3_P
CLKout3_N
CLKout4_P
CLKout4_N
100 OHM DIFF. IMPEDANCE
0 ohm (10nF)
U5
U6
U7
U8
LMH0302SQ
ENABLE
SD/HD
SDI
SDO
RREF
VCC
VEE
DAP
NC
3V3
JP13
JP14
JP15
JP16
J4
J5
J6
J7
CLKout1
CLKout2
CLKout3
CLKout4
L12 5.6uH
L13
L14
L15
R93
R92
R90
R91
Layout note: Place termination resistor, two pin header and LMH0302 inputs as close together as possible. Place LMH0302 close to the board edge and the SMA connector connected to it's output. Label SMAs on Silkscreen with CLKout1, CLKout 2 etc..
Layout Note: Place LEDs nearby status flag pins. LED Legend 'ALIGN'
Layout Note: Place LEDs nearby status flag pins. LED Legend 'REF'
Layout Note: Place LEDs nearby status flag pins. LED Legend 'LOCK'
LTST-C170GKT
D1
D2
D3
NOALIGN
NOREF
NOLOCK
Title
TIDA-00424(Video Sync Clock Generator) - Output
Size
B
Number
Revision
B
Date: 3/19/2015
Sheet of
File: C:\Users\..\TIDA-00424 Output.SchDoc
Drawn By:



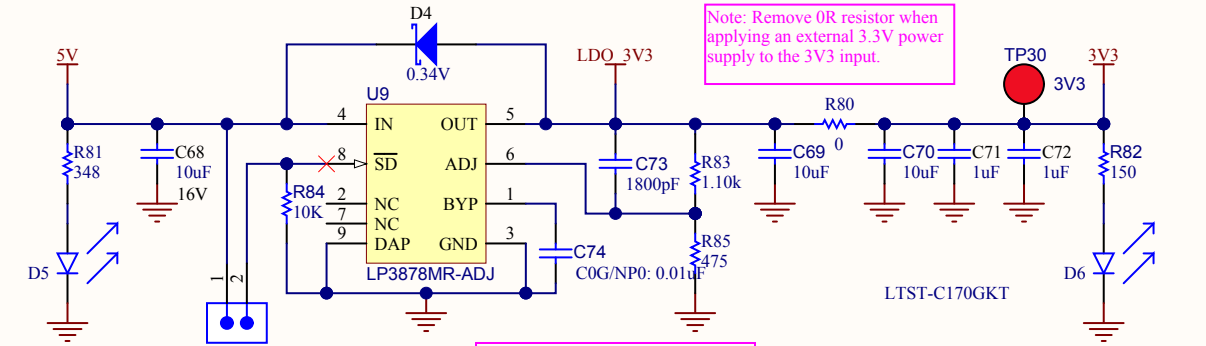
Title	**TIDA-00424(Video Sync Clock Genrator)**	
Size: A	Number:	Revision: **B**
Date: 3/19/2015	Sheet 4 of 5	
File: C:\Users\..\TIDA-00424 USB Interface.SchDoc	Drawn By:	

Power Supply Input and Low-Noise 3.3V LDO Regulator

Layout Note: Unless otherwise noted, label all ICs, Test Points, Jumpers and Headers per the component comment. For jumpers and headers, label pins according to the pin legend noted. All labels should be present on top and bottom silk screen (except for ICs).



Layout Note: Pin Legend is
"5V IN" (pin 8)
"N/C" (pin 7)
"LDO 3.3V" (pin 6)
"3.3V" (pin 5)
"GND" (pins 1-4)

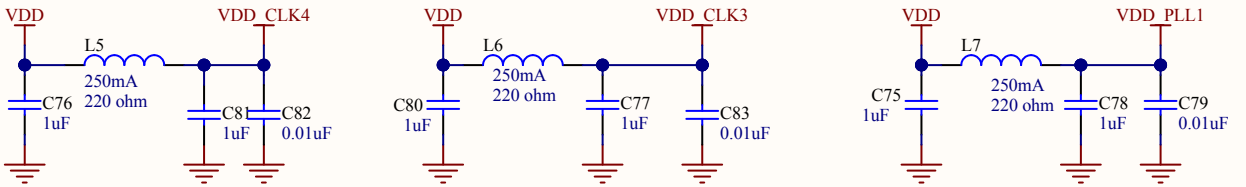


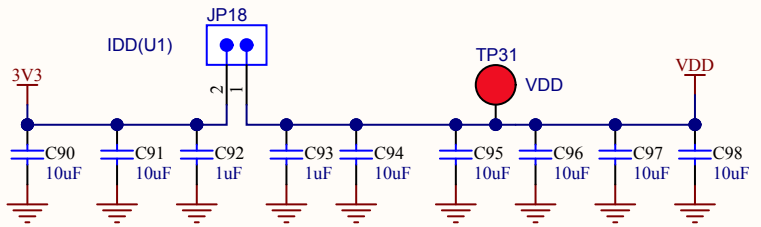
Note: Remove 0R resistor when applying an external 3.3V power supply to the 3V3 input.

Layout Note: LED Legend is "5V IN"

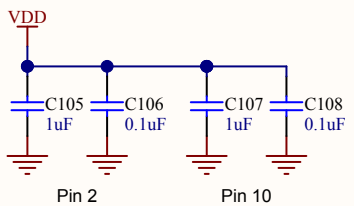
Note: LDO output voltage
Vout 1V*(1+R_hi/R_lo) = 3.30V

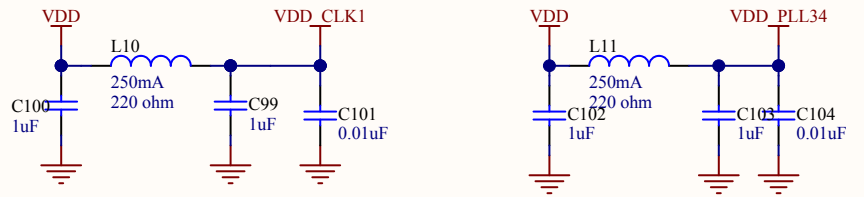
Layout Note: LED Legend is "3.3V"





Layout Note: Distribute caps around the 4 sides of LMH1983 for decoupling the VDD power supply plane.





Title: **TIDA-00424(Video Sync Clock Generator) - Power**		
Size: A	Number:	Revision: **B**
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File: C:\Users\..\TIDA-00424 POWER SUPPLY.DSN	Drawn By:	

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