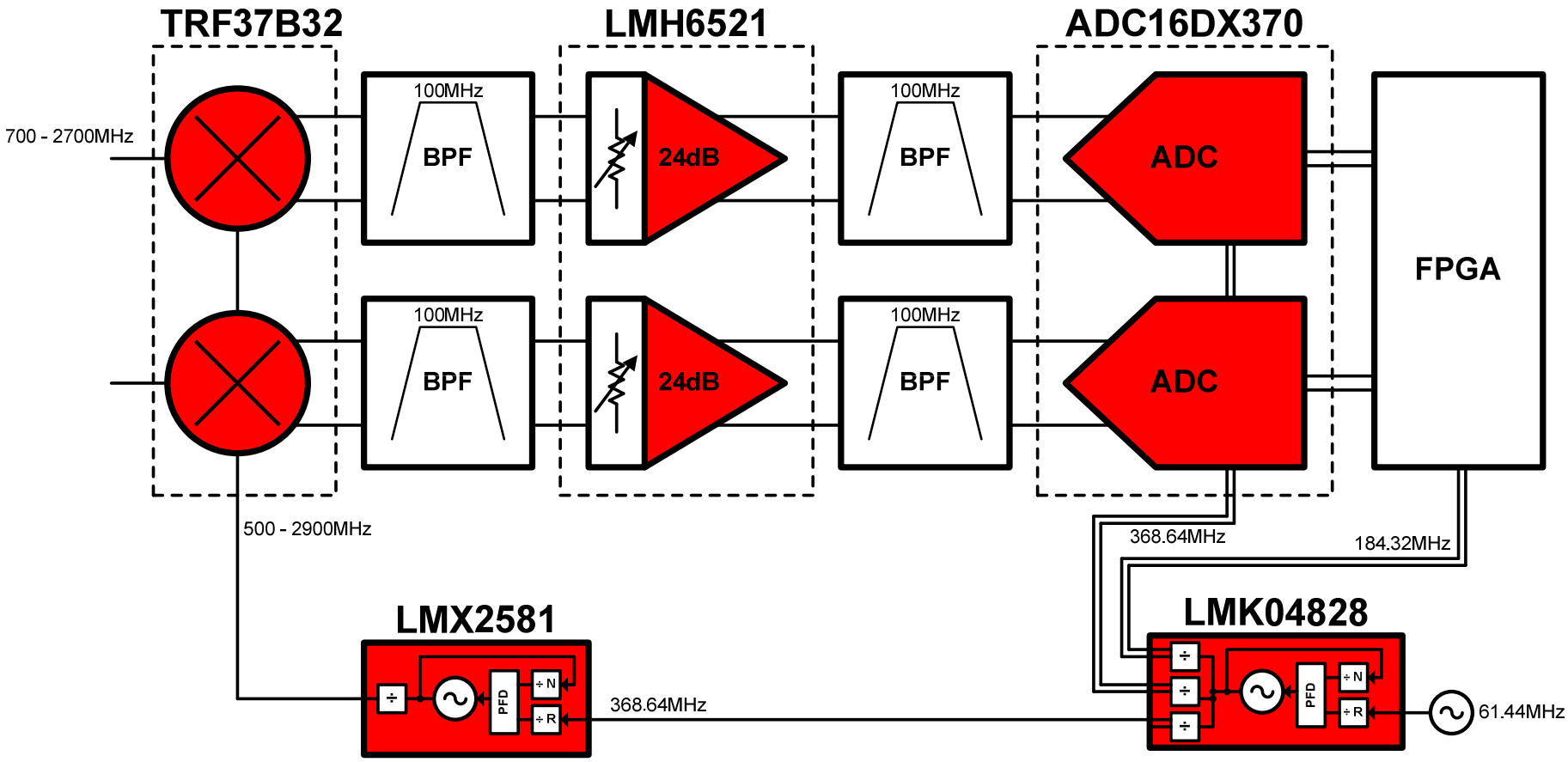
TSW16DX370EVM Rev.B Performance Summary

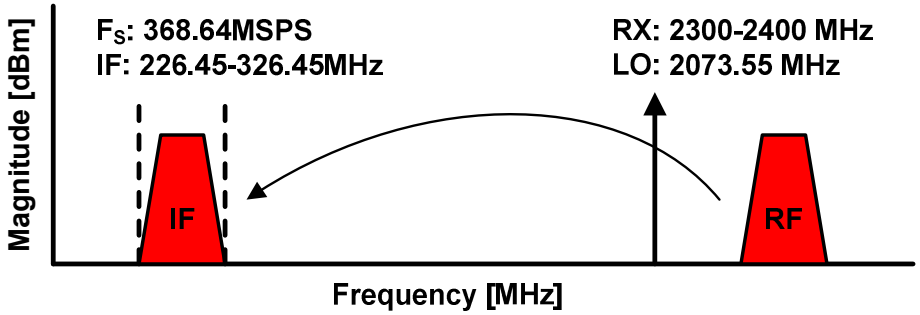
2/3/2015

Block Diagram



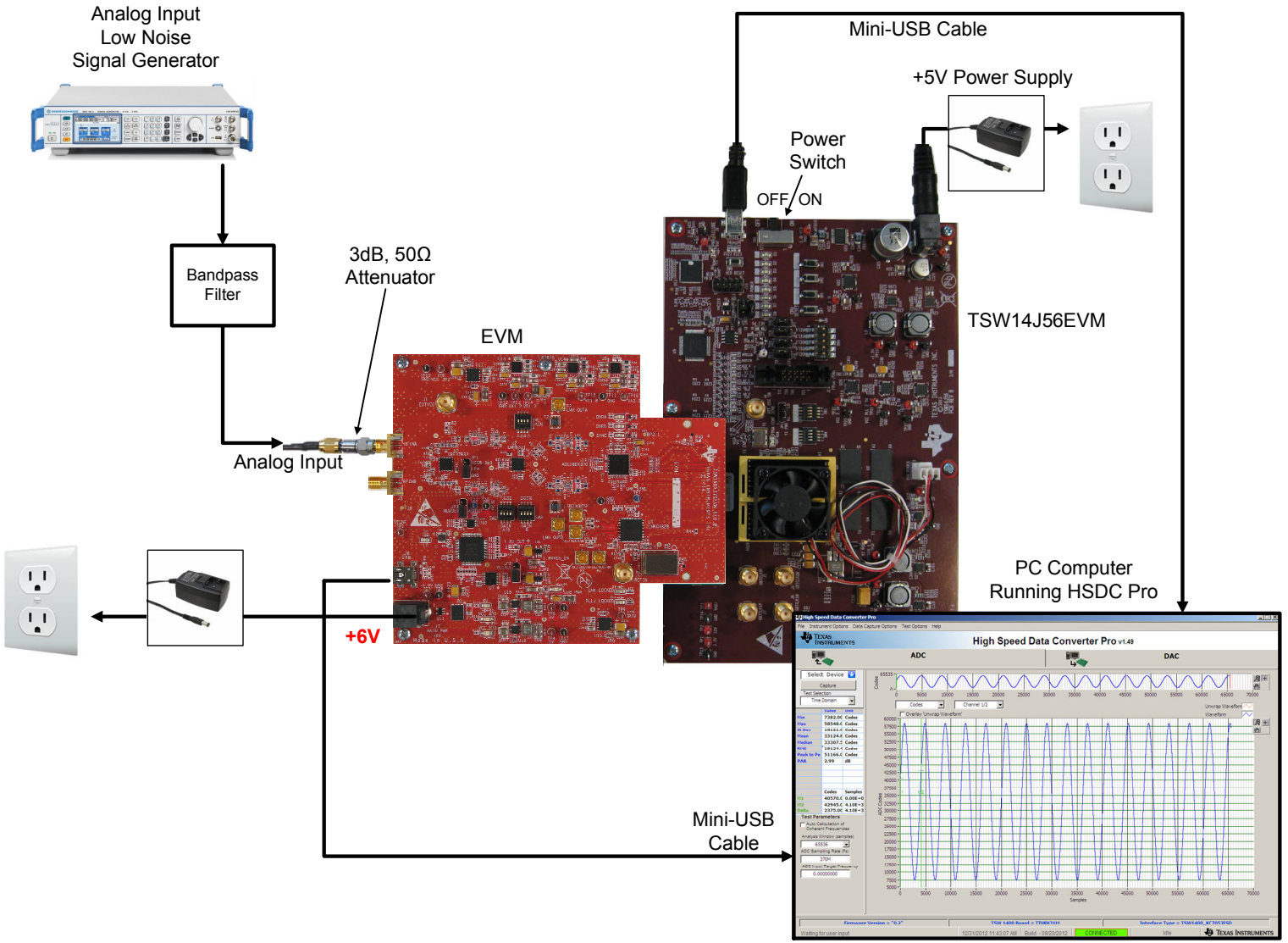
Frequency Plan

- RF Input Range: 700 – 2700 MHz
- Mixer LO range: 500 – 2900 MHz
- LO RF Synthesizer Reference: 368.64 MHz
- IF Center Frequency: ~277 MHz
- IF 1dB Bandwidth: 100 MHz
- ADC Sampling Rate: 368.64 MHz



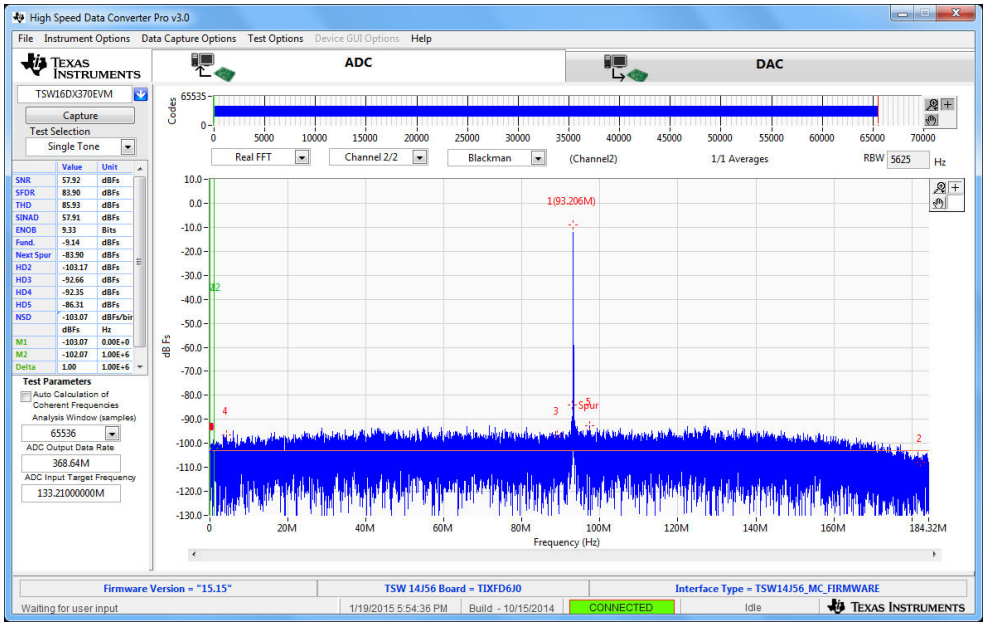
- System Reference Clock: 61.44 MHz
- Output Digital Data Rate: 7.3728 Gb/s/lane
- FPGA SERDES Reference: 184.32 MHz

Bench Evaluation



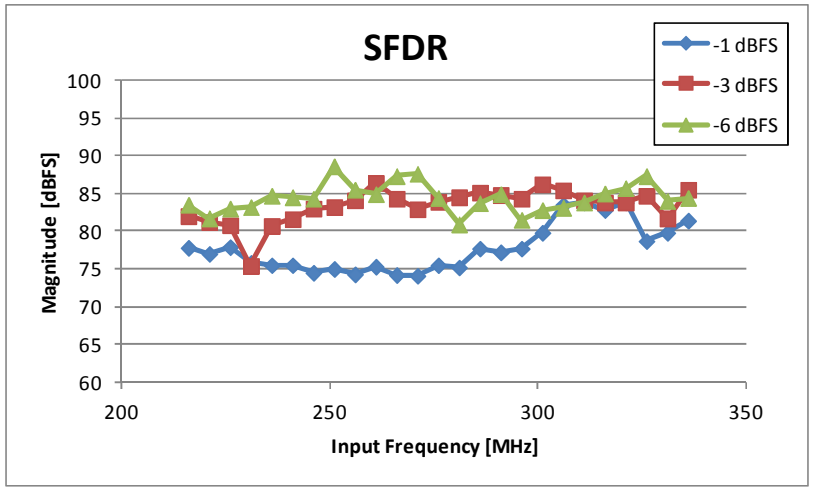
Gain

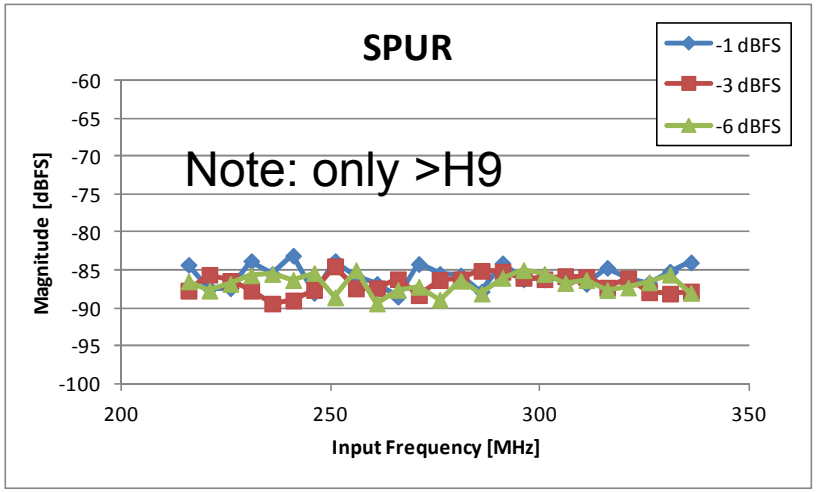
- -25dBm power output from signal generator, 1750MHz
- -32.5dBm at output of 6dB attenuator on Spectrum analyzer
- -9.4 dBFS at ADC output for DVGA Att. = 0dB
- -33.4 dBFS at ADC output for DVGA Att. = 24dB
- +5.6dBm is ADC full scale (100ohm term)
- Gain = 28.7 dB (max), -2.8 dB (min)



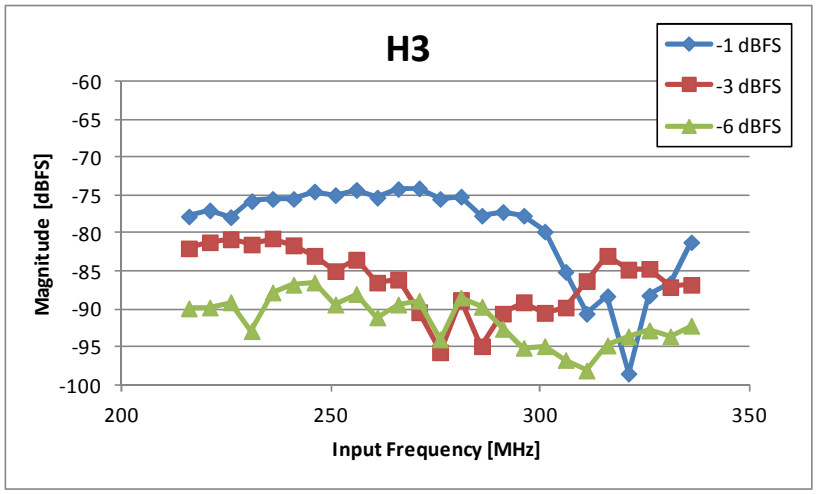
Distortion (Single-Tone)

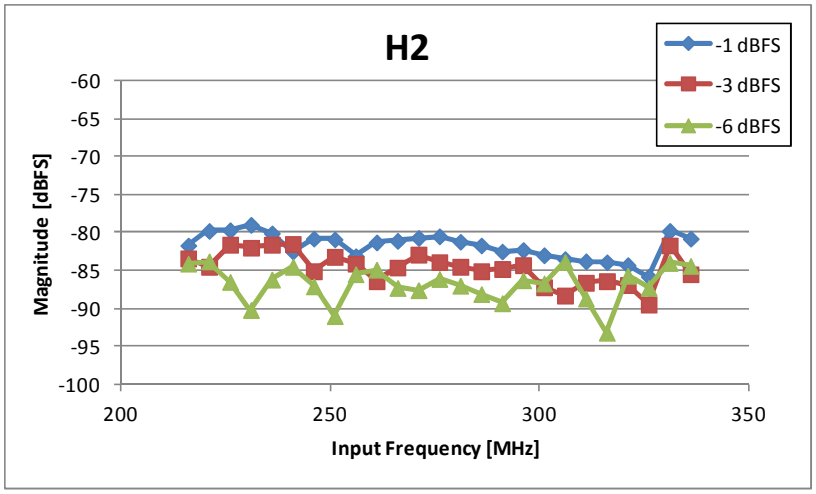
- LO = 1474 MHz, **DVGA Attenuation = 0 dB**





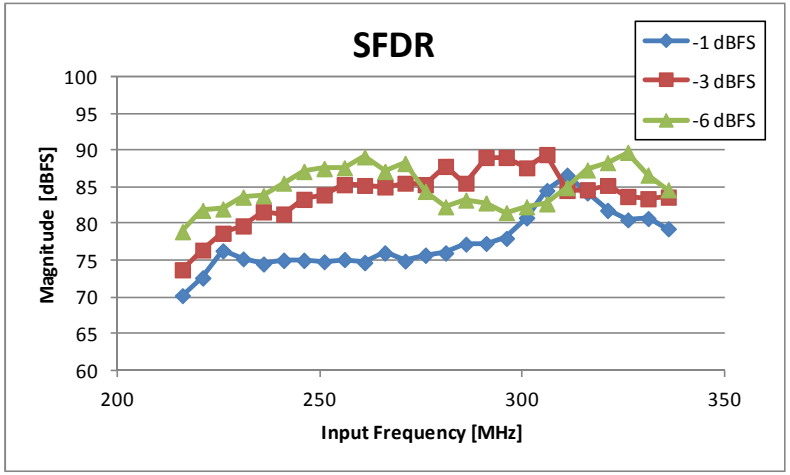
Note: Some limitations due to H5-H9



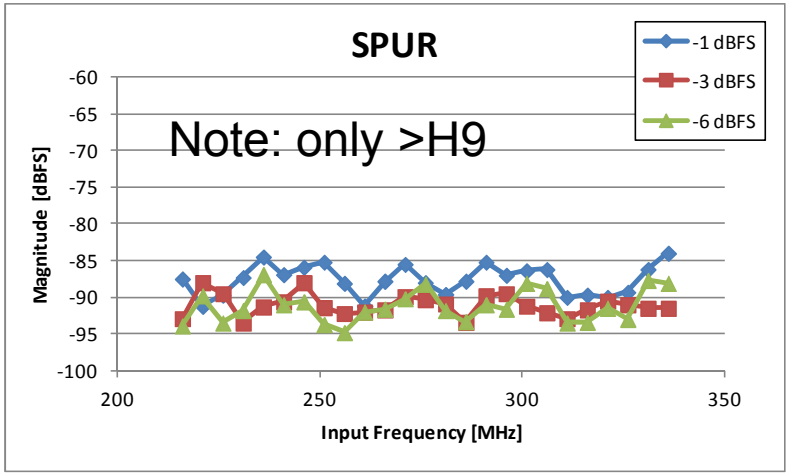


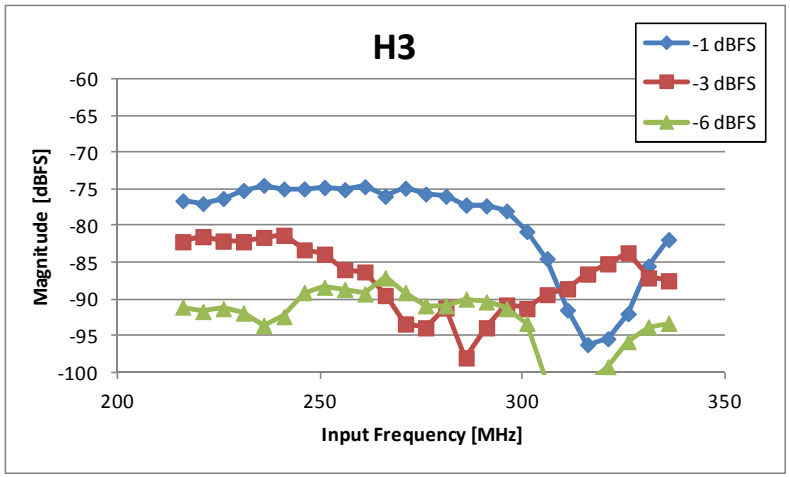
Distortion Across Frequency (Single-Tone)

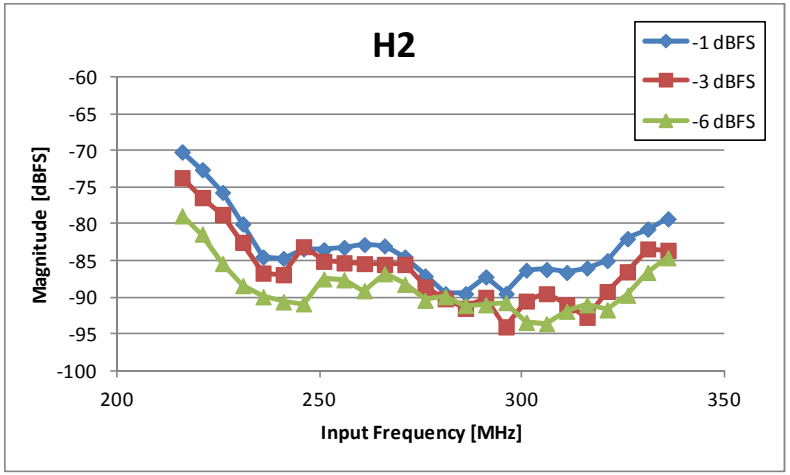
- LO = 1474 MHz, **DVGA Attenuation = 24 dB**



Note: Some limitations due to H5-H9



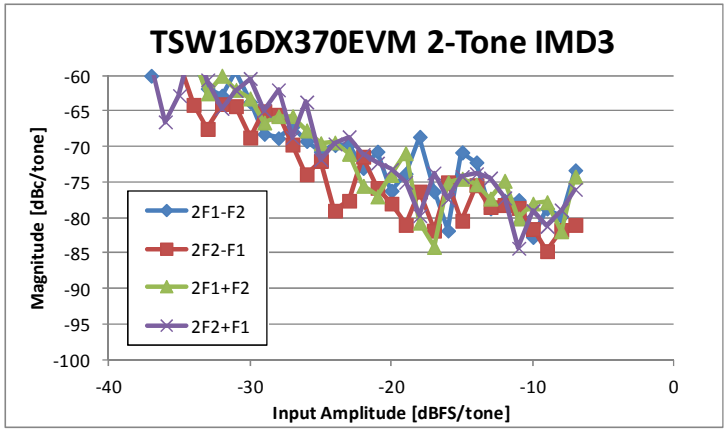


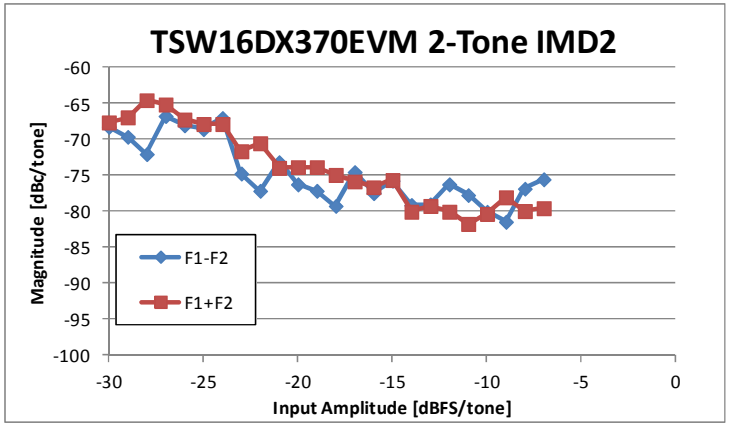


Note: Low-side H2 caused by LMH6521 at high attenuation settings

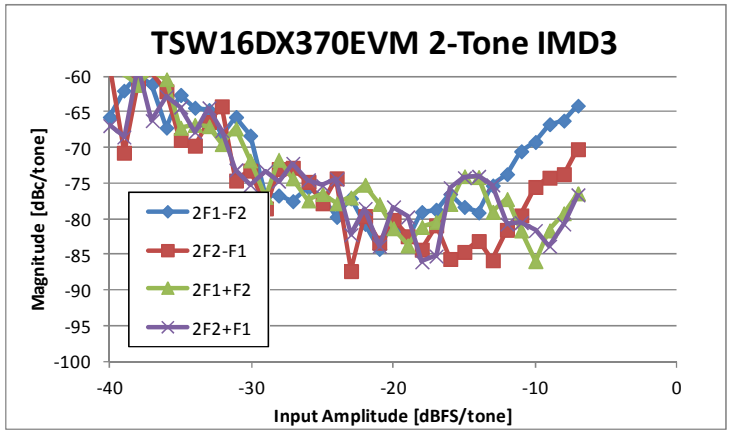
Distortion Across Amplitude (Two-Tone)

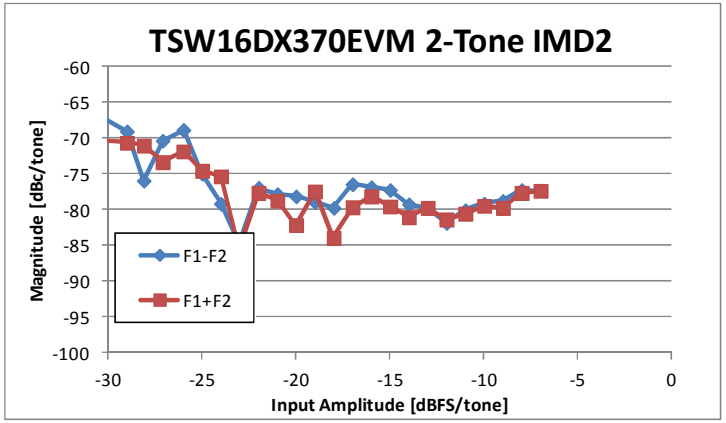
- LO = 1474 MHz
- Input Freq = 1700/1710 MHz, **DVGA Att. = 0 dB**





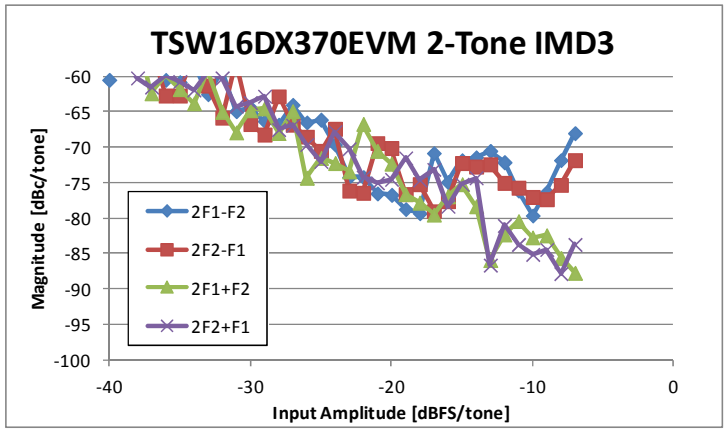
- Input Freq = 1700/1710 MHz, **DVGA Att. = 24 dB**

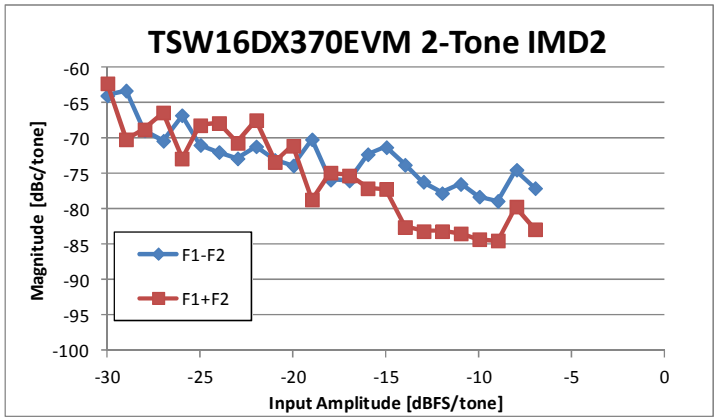




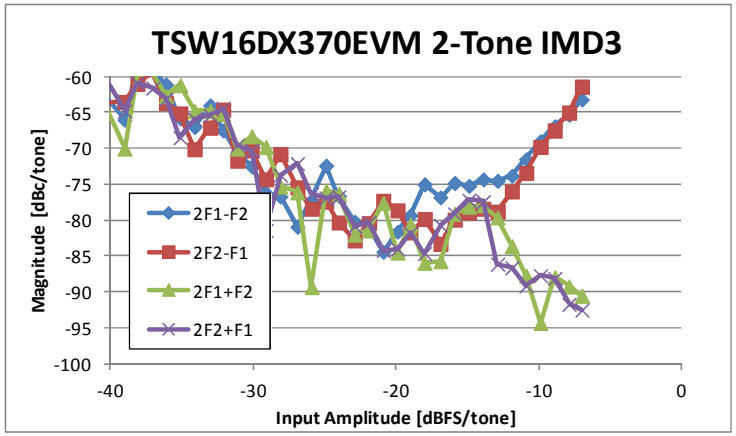
Distortion Across Amplitude (Two-Tone)

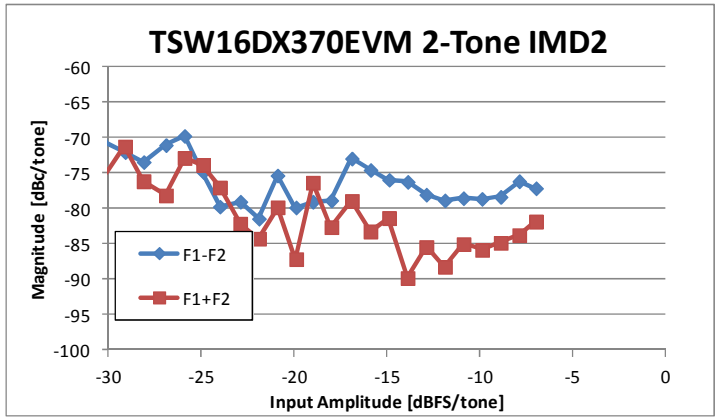
- LO = 1474 MHz
- Input Freq = 1790/1800 MHz, **DVGA Att. = 0 dB**





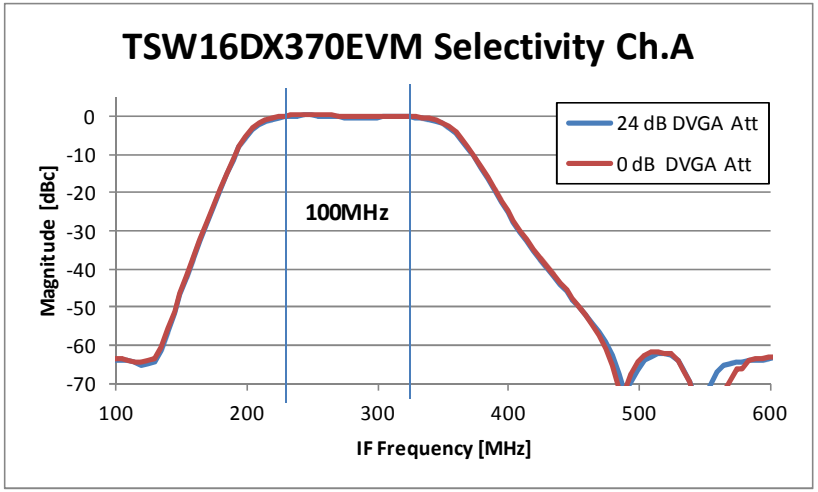
- Input Freq = 1790/1800 MHz, **DVGA Att. = 24 dB**

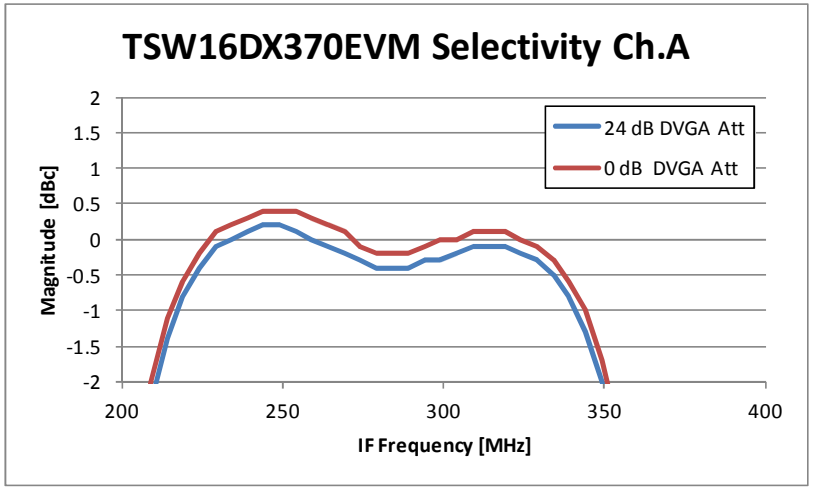




Selectivity

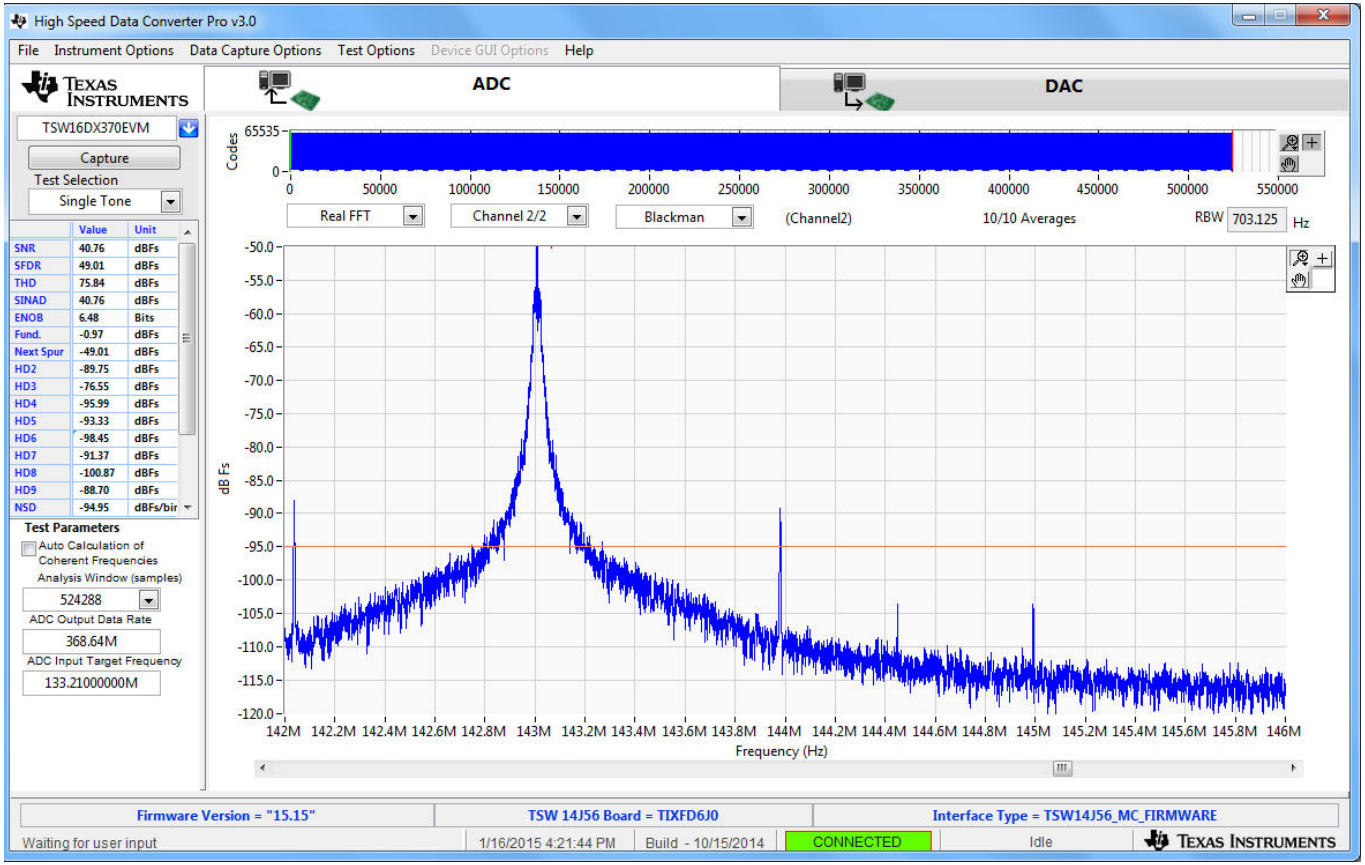
- Includes Post-mixer IF filter and Anti-Aliasing Filter
- LO = 1474MHz
- 100MHz 1dB BW
- Stopband Attenuation
  - 13dB @ 50MHz offset (from 330M)
  - 30dB anti-aliasing protection (from 330M)
  - 39dB @ 100MHz offset (from 330M)
  - 52dB H2 atten. (from 230M)





Phase Noise

- LO = 1474 MHz

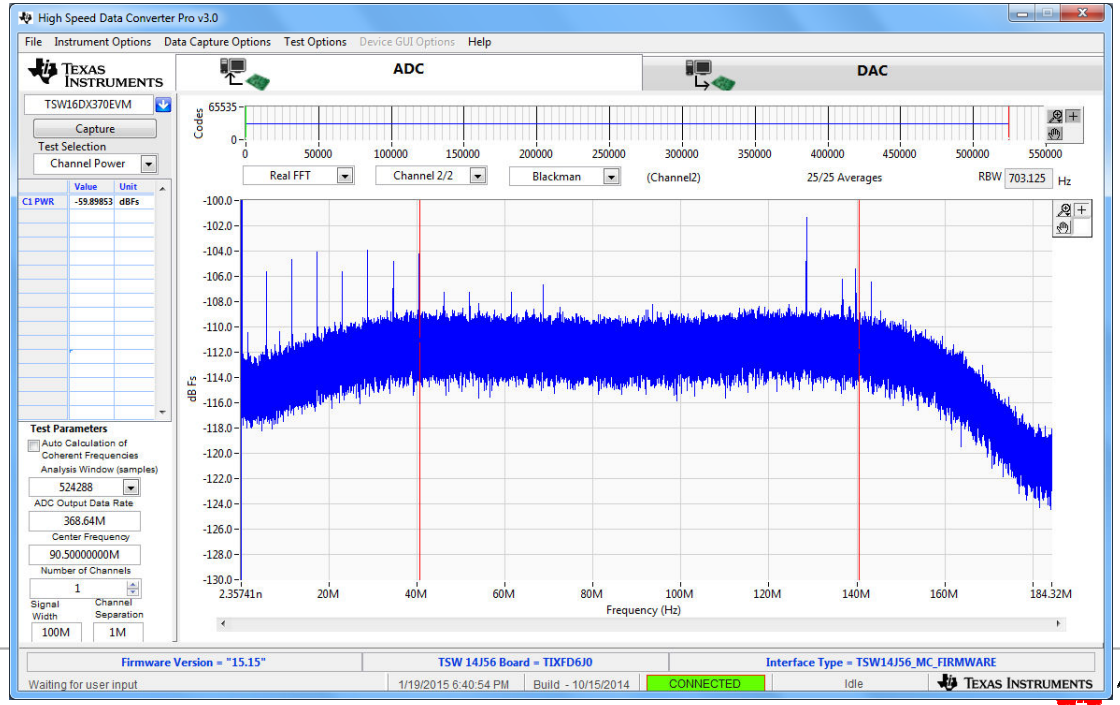


Offset	Bin Noise [dBFS/bin]	Noise [dBc/Hz]
100k	-87	-114.424
200k	-94	-121.424
500k	-101.5	-128.924
1M	-109	-136.424
2M	-113	-140.424
5M	-116	-143.424
10M	-117	-144.424

Note: Visible spurs caused by Switching power supplies

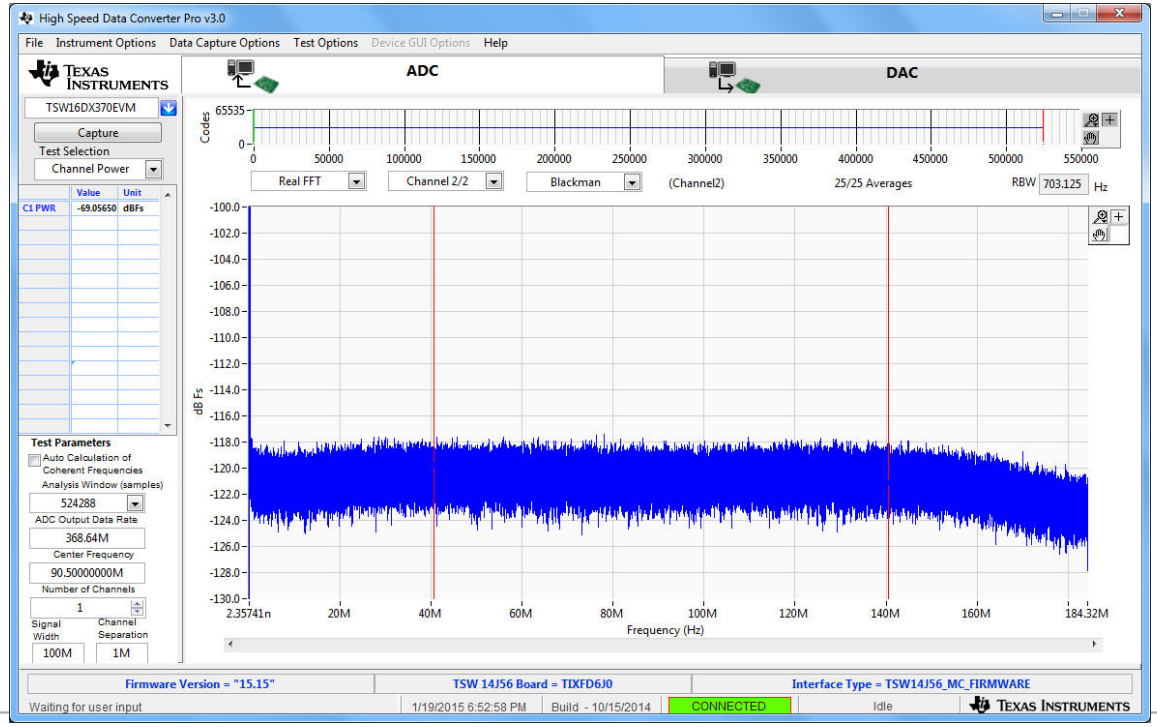
Noise Density

- LO = 1474 MHz
- **DVGA Att. = 0 dB**
- Notes: Spurs are LO PDF fixed spurs with max DVGA gain (-104dBFS)
- Noise density = -59.9 dBFS – 10log(100MHz) = -139.9 dBFS/Hz
  - -139.9 dBFS/Hz +5.6dBm = -134.3 dBm/Hz at ADC output
  - -134.3 dBm/Hz – 28.7dB (gain) = -163 dBm/Hz → 11dB NF



Noise Density

- LO = 1474 MHz
- **DVGA Att. = 24 dB**
- Noise density = -69 dBFS – 10log(100MHz) = -149 dBFS/Hz
  - -149 dBFS/Hz +5.6dBm = -143.4 dBm/Hz at ADC output
  - -143.4 dBm/Hz – 4.7dB (gain) = -148.1 dBm/Hz → 25.9dB NF



Performance Summary

Parameter	Conditions	Value	Units	Notes
Gain	DVGA Att. 0dB	+28.7	dB	
	DVGA Att. 24dB	+4.7	dB	
OIP3	Fin=1710/1700, -9dBFS/tone, DVGA Att. 0dB	+36.1	dBm	IMD=-79dBc, IIP3=+7.4dBm
	Fin=1710/1700, -9dBFS/tone, DVGA Att. 24dB	+30	dBm	IMD=-66.7dBc, IIP3~+25.3dBm
	Fin=1790/1800, -9dBFS/tone, DVGA Att. 0dB	+35.2	dBm	IMD=-77.4dBc, IIP3~+5.5dBm
	Fin=1790/1800, -9dBFS/tone, DVGA Att. 24dB	+27.3	dBm	IMD=-61.4dBc, IIP3~+22.6dBm
NF	DVGA Att 0dB	11	dB	
	DVGA Att 24dB	25.9	dB	
Phase Noise	DVGA Att. 24dB 100kHz 200kHz 500kHz 1MHz 2MHz 5MHz 10MHz	 -114.4 -121.4 -128.9 -136.4 -140.4 -143.4 -144.4	dBc/Hz	In-close noise agrees well with clock design tool simulation, dominated by LMX performance. Frequencies above 1MHz influenced significantly by broadband noise of ADC and LMH.

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