



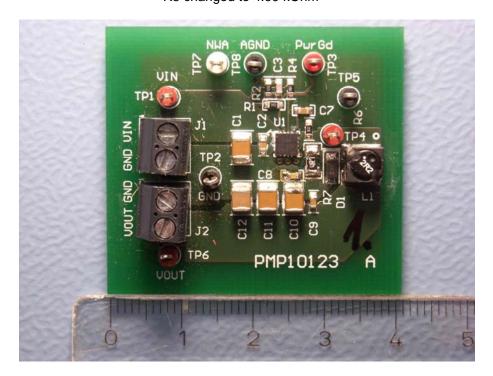
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Topology: synchronuous step down SWIFT converter

Device: TPS57112, tested board #1 at Fsw 2.19MHz (RT 82.5kOhm)

Revision B:

- RC snubber:
 - R7 changed to 4.7 Ohm
 - C8 changed to 330 pF
- Loop compensation
 - C6 changed to 22 nF
 - R5 changed to 4.99 kOhm





1 Startup

Startup sequence is shown in Figure 1.

Power Setup				Oscilloso	cope Setup		
	•		Description	Time	Scale	BW	Coupling
V_{in}	5.0V	C1	Input Voltage	2ms / div	2V / div	Full	DC 1MOhm
V_{out}	3.3V	C2	Output Voltage	2ms / div	2V / div	Full	DC 1MOhm
I _{in} I _{out}	2.0A						

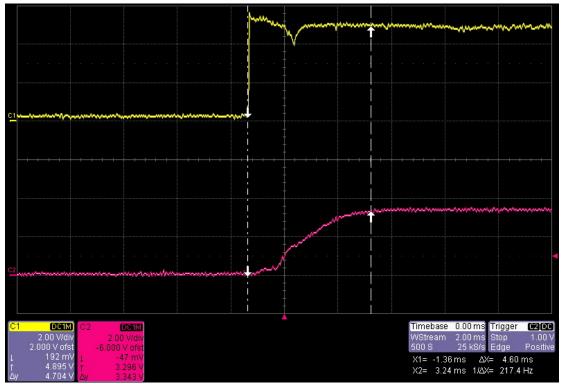


Figure 1: Startup sequence

Startup time is about 4.60 ms.



2 Shutdown

Shutdown sequence is shown in Figure 2.

Power Setup				Oscillos	cope Setup		
	•		Description	Time	Scale	BW	Coupling
V_{in}	5.0V	C1	Input Voltage	2ms / div	2V / div	Full	DC 1MOhm
V_{out}	3.3V	C2	Output Voltage	2ms / div	2V / div	Full	DC 1MOhm
I _{in} I _{out}	2.0A						

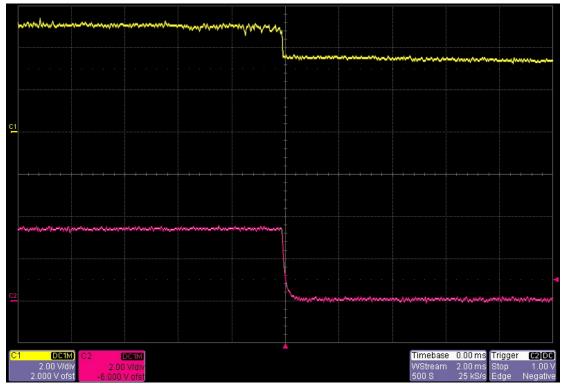


Figure 2: Shutdown sequence



3 Efficiency

The data in Table 1 were recorded. Efficiency curve is shown in Figure 3.

	Table 1									
V _{in}	I _{in}	V_{out}	l _{out}	Eff.						
5.000 V	0.1086 A	3.3240 V	0.1293 A	79.15 %						
5.000 V	0.1746 A	3.3241 V	0.2200 A	83.77 %						
5.000 V	0.3827 A	3.3240 V	0.5313 A	92.29 %						
4.999 V	0.5954 A	3.3236 V	0.8387 A	93.65 %						
4.998 V	0.7972 A	3.3228 V	1.1275 A	94.03 %						
5.002 V	1.0109 A	3.3225 V	1.4290 A	93.90 %						
5.002 V	1.2260 A	3.3224 V	1.7360 A	94.05 %						
4.999 V	1.4350 A	3.3221 V	2.0260 A	93.82 %						
5.000 V	1.6560 A	3.3215 V	2.3300 A	93.47 %						

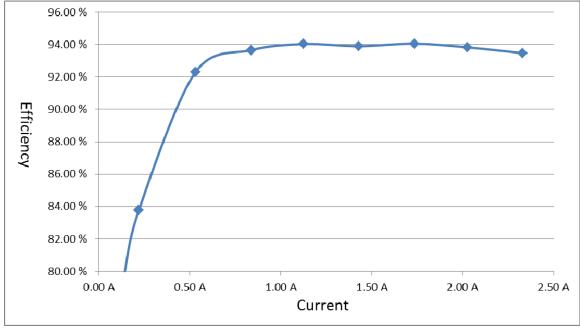


Figure 3: Efficiency over output current

Maximum efficiency 94% at 1A to 2A output current.



4 Load Regulation

Load regulation of the output is shown in Figure 4.

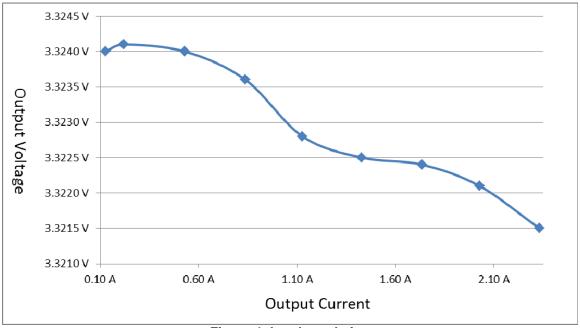


Figure 4: Load regulation

 $\begin{array}{ll} \text{Min. V}_{\text{out}}\colon & 3.3215 \text{V} \\ \text{Max V}_{\text{out}}\colon & 3.3241 \text{V} \end{array}$

V_{out} Variation: 2.6mV



5 Ripple Voltage

Input and output ripple voltage are shown in Figure 5 and Figure 6.

Power Setup				Oscillosc	ope Setup		
			Description	Time	Scale	BW	Coupling
V _{in}	5.0V	C1	Input Ripple V.	100ns / div	100mV / div	Full	AC 1MOhm
V_{out}	3.3V	C2	Output Ripple V.	100ns / div	100mV / div	Full	AC 1MOhm
I _{in} I _{out}	2.0A						



Figure 5: Input ripple voltage



Figure 6: Output ripple voltage

Input ripple voltage is 482mV peak peak. Output ripple voltage is 372mV peak peak. For EMI analysis these msrmts have been taken w/ FULL BANDWIDTH! (standard procedure bw 20MHz)



6 Control Loop Frequency Response

Figure 7 shows the loop response for 1.3A and 2.0A load.

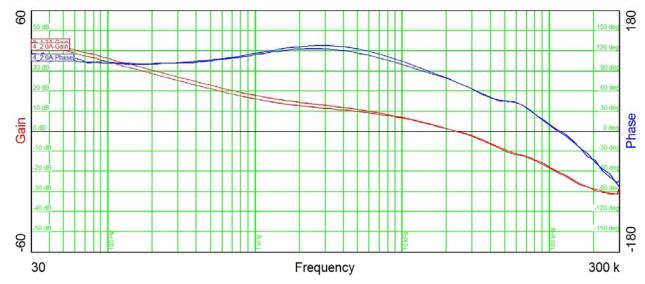


Figure 7: Control Loop Frequency Response

1.3A load:

Crossover frequency f_{co} : 23.7 kHz Phase margin at f_{co} : 72.7 deg Gain Margin: -20.6 dB

2.0A load:

 $\begin{array}{lll} \text{Crossover frequency } f_{co}\text{:} & 23.1 \text{ kHz} \\ \text{Phase margin at } f_{co}\text{:} & 74.5 \text{ deg} \\ \text{Gain Margin:} & -21.0 \text{ dB} \\ \end{array}$



7 Load Transients

Figure 8 shows the response to a load transient from 0.7A to 1.4A. Alternating frequency is 500Hz.

Power Setup				Oscilloso	ope Setup		
	•		Description	Time	Scale	BW	Coupling
V_{in}	5.0V	C1	Output Voltage	500us / div	100mV / div	20MHz	AC 1MOhm
$V_{ m out}$	3.3V	C2	Output Current	500us / div	10mV / div 10mV ^= 1A	20MHz	DC 1MOhm
l _{out}							

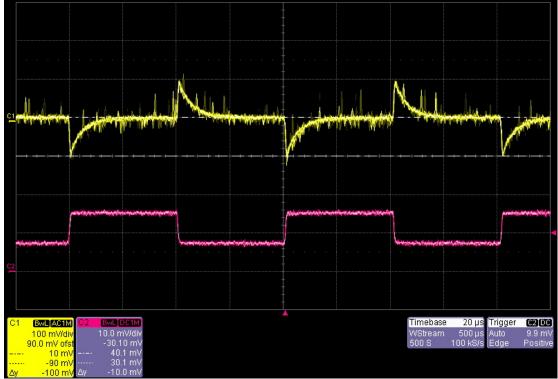


Figure 8: Load transient from 0.7A to 1.4A

The voltage drop caused by di = 700mA is 100mV, this reflects du = 3%. Standard msrmt for customer application w/ 1.3A maximum load current.

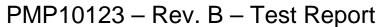




Figure 9 shows the response to a load transient from 0.15A to 1.5A. Switching frequency is 500Hz.

Power Setup				Oscilloso	ope Setup		
	-		Description	Time	Scale	BW	Coupling
V_{in}	5.0V	C1	Output Voltage	500us / div	100mV / div	20MHz	AC 1MOhm
V_{out}	3.3V	C2	Output Current	500us / div	10mV / div	Full	DC 1MOhm
l _{in}					10mV ^= 1A		
l _{out}							

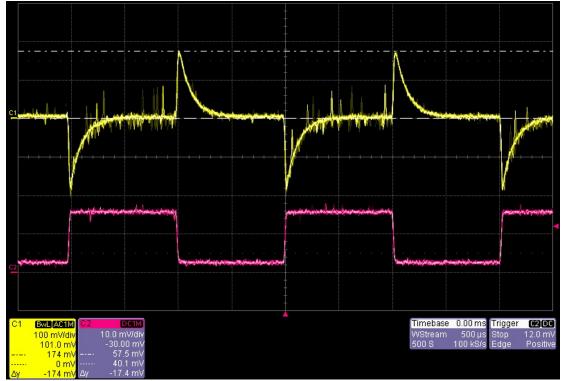


Figure 9 Load transient from 0.15A to 1.5A

The voltage drop caused by di = 1.35A is 174mV, this reflects du = 5.3% for 90% transient.

(standard procedure 50% transient, see before)

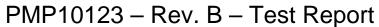




Figure 10 shows the response to a load transient from 1.0A to 2.0A. Switching frequency is 500Hz.

Power Setup				Oscilloso	ope Setup		
	_		Description	Time	Scale	BW	Coupling
V_{in}	5.0V	C1	Output Voltage	500us / div	100mV / div	20MHz	AC 1MOhm
V_{out}	3.3V	C2	Output Current	500us / div	10mV / div	20MHz	DC 1MOhm
I_{in}					10mV ^= 1A		
l _{out}							

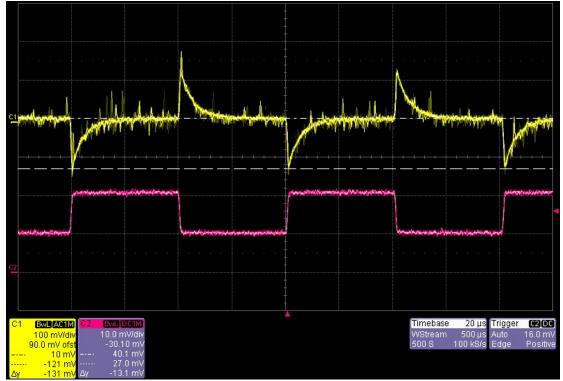


Figure 10: Load transient from 1.0A to 2.0A

The voltage drop caused by di = 1A is 131mV, this reflects du = 4%; Typical msrmt for the 2Amps device.



8 Switch node

Figure 11 shows the voltage characteristic at the switch node.

Pow	Power Setup			Oscillosc	ope Setup		
	-		Description	Time	Scale	BW	Coupling
V_{in}	5.0V	C1	SW Node Voltage	100ns / div	2V / div	Full	DC 1MOhm
V_{out}	3.3V	C2	· ·				
I_{in}							
l _{out}	2.0A						

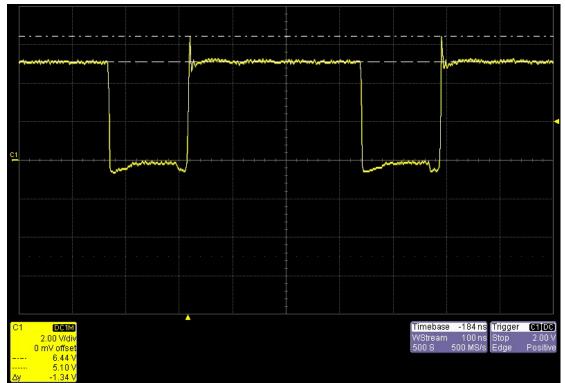


Figure 11: Switch Node

Voltage overshoot is 1.34V.

The design has been evaluated with:

- RC snubber at switch node to attenuate overshoot and RF ringing
- Bootstrap resistor to reduce rising slope slightly (effcy still 94%)
- Additional LS Schottky to prevent from Qrr of LS FET body diody, causing GND noise



Figure 12 and Figure 13 also show the ringing of the switch node, but more detailed (10ns/div). The snubber circuit consists of 4.70hm and 330pF in serial.

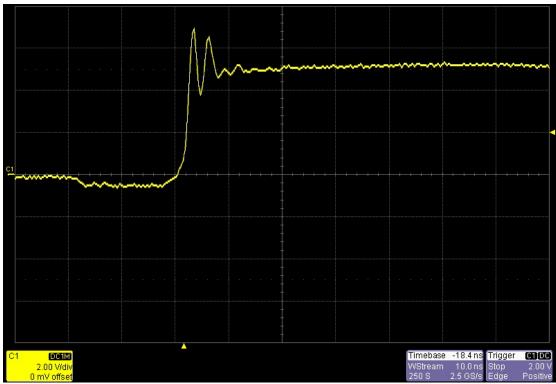


Figure 12: Voltage rise at switch node

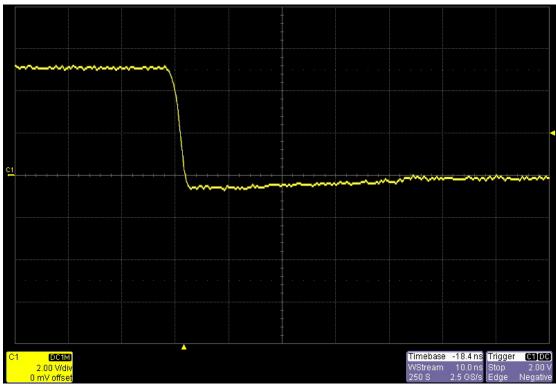


Figure 13: Voltage drop at switch node



9 Thermal image

Figure 14 and Figure 15 show the thermal image at 1.4A and 2.0A at room temperature (23 °C).

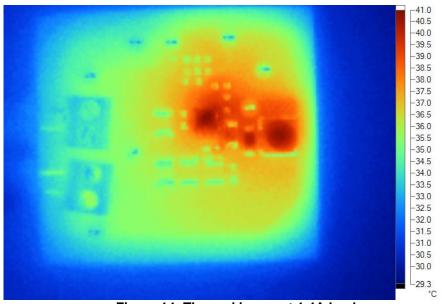


Figure 14: Thermal image at 1.4A load

Balanced temperature at device – Schottky – Inductor, no hotspot;

Temperature rise dT below +20K (!) - minor energy at snubber resistor.

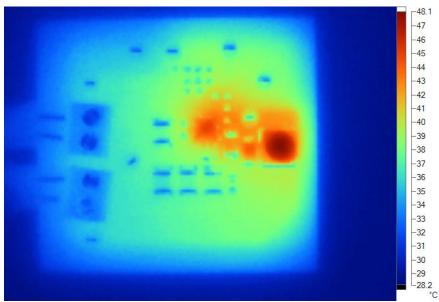


Figure 15: Thermal image at 2.0A load

Maximum temperature at 2.0A is 48.1 °C at inductor, so temperature rise dT below +25K.



Appendix: functional verification Board #2

Efficiency Board #2:

 $\begin{array}{lll} V_{in} &= 5.000V & I_{in} &= 1.418A \\ V_{out} &= 3.327V & I_{out} &= 2.000A \\ & & & & & & \\ \hline \Leftrightarrow & & & & \\ \hline \end{cases} \text{ fficiency} = 93.85 \% \text{ (similar to board #1 at 93.82\%, power stage OK)}$

Closed loop, small signal analysis in frequency domain:

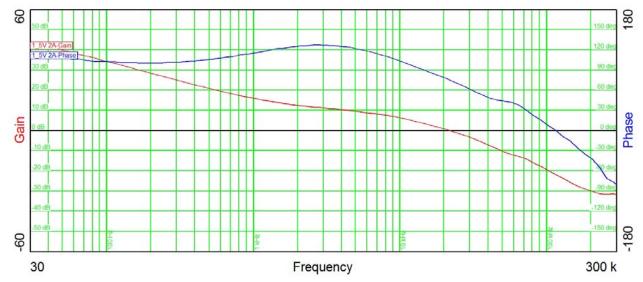


Figure 16: Control Loop Frequency Response Board #2

Measurement at load current 2.0A:

Crossover frequency f_{co} : 23.8 kHz Phase margin at f_{co} : 75.2 deg Gain Margin: -21.8 dB

(similar to board #1, loop OK)



Switch Node Board #2:

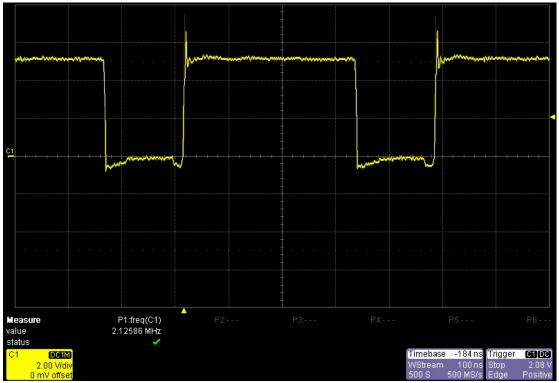


Figure 17: Switch node Board 2

 $F_{sw} = 2.13 \text{ MHz}$

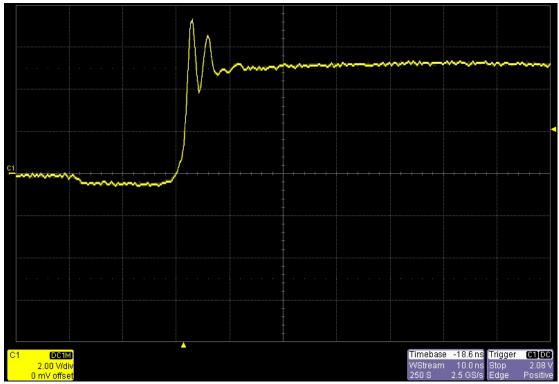


Figure 18: Voltage rise at switch node Board 2



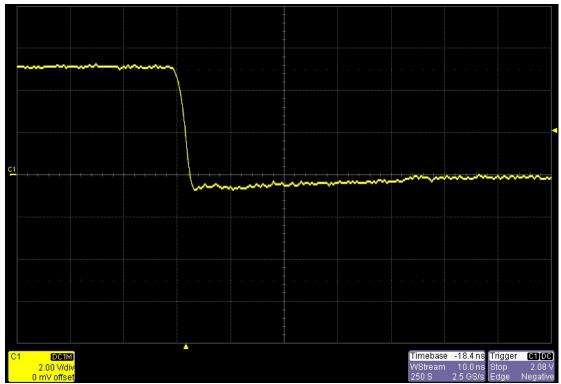


Figure 19: Voltage drop at switch node Board 2

measurements at switch node in time domain similar to board #1, same switching behavior

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