

TI Designs

Sercos III Slave For AM437x — Communication Development Platform



TI Designs

Industrial Ethernet for Industrial Automation exists in more than 20 industrial standards. Some of the well-established real-time Ethernet protocols like EtherCAT, EtherNet/IP, PROFINET, Sercos III, and PowerLink require dedicated MAC hardware support in terms of FPGA or ASICs. The Programmable Real-Time Unit inside the Industrial Communication Subsystem (PRU-ICSS), which exists as a hardware block inside the Sitara processors family, replaces FPGA or ASICs with a single chip solution. This TI design describes the Sercos III slave solution firmware for PRU-ICSS.

Design Resources

TIDEP0039	Design Folder
TMDXIDK437X	Tools Folder
AM4379	Product Folder
TIDEP0001	Tools Folder
TIDEP0003	Tools Folder
TIDEP0008	Tools Folder
TIDEP0010	Tools Folder
TIDEP0028	Tools Folder



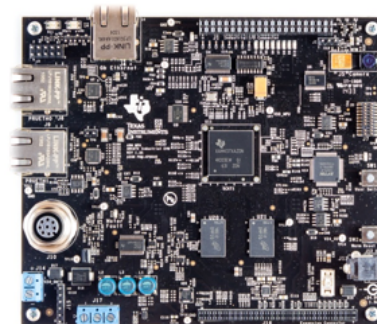
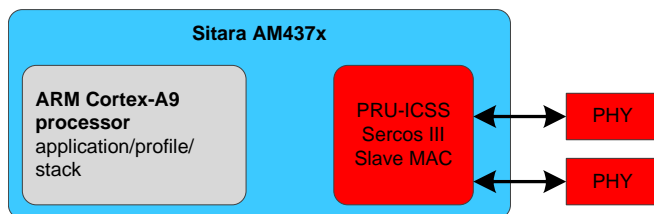
[ASK Our E2E Experts](#)
[WEBENCH® Calculator Tools](#)

Design Features

- Sercos III Slave Firmware for PRU-ICSS With Sercos MAC-Compliant Register Interface
- Board Support Package and Industrial Software Development Kit Available From TI and Third-Party Stack Provider
- Development Platform Includes Schematics, BOM, User's Guide, Application Notes, White Paper, Software, Demo, and More
- PRU-ICSS Supports Other Industrial Communication Standards (For Example, EtherCAT, PROFINET, EtherNet/IP, Ethernet POWERLINK, Profibus)
- PRU-ICSS Firmware is Sercos III Conformance Tested

Featured Applications

- Factory Automation and Process Control
- Motor Drives
- Digital and Analog I/O Modules
- Industrial Communication Gateways
- Sensors, Actuators, and Field Transmitters



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 Key System Specifications

For 25 years, Sercos has been one of the leading bus systems in factory automation applications such as mechanical engineering and construction. Sercos III is the third-generation Sercos interface and was established in 2003. The efficient and deterministic communication protocol, based on real-time technology, merges the hard real-time aspect of the Sercos interface with Ethernet. The Sercos III technology integration requires dedicated hardware to support "on-the-fly" Ethernet frame processing, which up until now was implemented in field-programmable gate arrays (FPGAs) and application specific integrated circuits (ASICs).

This design guide provides an overview of the Sercos III fieldbus technology and the implementation of the Sercos III protocol into the Sitara™ AM437x processors.

The TIDEP0039 Sercos III For AM437x — Communication Development Platform combines the Sitara processor family from Texas Instruments (TI) and the Sercos III media access control (MAC) layer into a single system-on-chip (SoC) solution.

2 System Description

2.1 Technology Introduction

In a Sercos III Industrial Ethernet network, one Sercos III master controls multiple Sercos III slave devices. Slaves are network devices such as drives, sensors, and analog and digital I/O devices (see Figure 1). In a Sercos III network, one master can control up to 511 slaves.

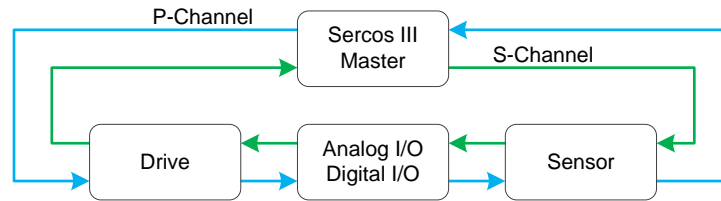


Figure 1. Example Sercos III Network in Ring Topology With P- and S-Channel

Both master and slave devices have two real-time Ethernet ports, and wiring between devices can be realized either in line or ring topology. Other wiring topologies like star or stub are not supported. To simplify wiring and to reduce installation errors, the Ethernet cable can be connected to any port on a master or slave device.

Network redundancy is only supported with ring topology. The master sends out each frame twice, one over the primary channel (P-channel) and one over the secondary channel (S-channel). The transmission of Sercos III frames by the master takes place on both channels simultaneously. This mechanism is also used to synchronize timing across all slaves (see Section 2.3).

Sercos III combines a deterministic real-time-Ethernet channel (RT) and a best-effort-Ethernet channel (UCC) on the same Ethernet cable using time multiplexing (see Figure 2). During the time slot of the Sercos III real-time channel, only the master is allowed to start the transmission of a Sercos III Ethernet frame. The frame is received by all slaves and is being processed on-the-fly, meaning each slave that receives the Sercos III Ethernet frame processes the bytes from the byte-stream without changing the overall frame length. At the end of the frame, the slave recalculates and replaces the frame check sequence (FCS) in case the content has been modified.

The overall processing delay in a slave from incoming port to outgoing port is constant and approximately 1 μ s. Therefore, the frame round-trip delay in a network with 10 slaves is 10 μ s in ring topology and 20 μ s in line topology.

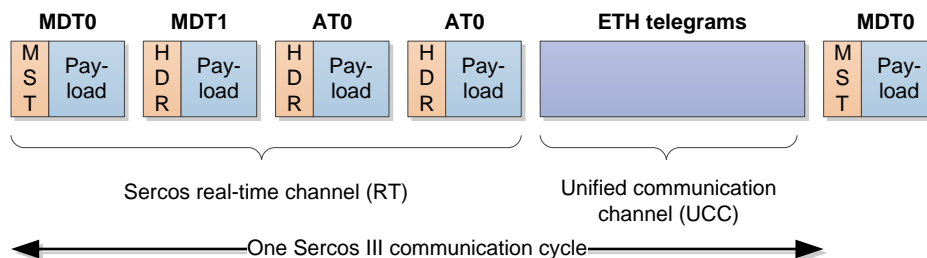


Figure 2. Sercos III Communication Cycle

During the time slot of the RT channel, only the master transmits master data telegram (MDT) and axis telegram (AT) Sercos III frames, which contain the cyclic process data and asynchronous communication data. The UCC channel is used by the master and slaves to transmit Ethernet frames using the best-effort standard Ethernet approach.

Slaves are not allowed to transmit Ethernet frames in the RT channel, and they have to buffer any UCC frames in the local memory. In line topology, it is common practice to add a service computer to the last slave to check or configure the slaves while the Sercos III network is operational. The last slave buffers UCC frames that are received during the RT channel and starts transmitting them after the UCC channel is opened.

Sercos III supports bus cycle times of down to 31.25 μ s, which are used in dedicated drive applications where the programmable logic controller (PLC) handles the motor control loop. In less demanding applications, bus cycle times in the millisecond range are used.

After startup, the Sercos III network goes through different communication phases before it reaches the operational state when real-time process data is exchanged. These are called communication phases (CP0, CP1, CP2, CP3, and CP4); it starts from CP0 (detecting of slaves) to CP4 (operational state, cyclic, and acyclic data communication).

2.2 Sercos III Frame

Only the master can generate Sercos III MDT and AT Ethernet frames. The MDT frame transfers data from the master to the slave while the AT frame transfers data from the slaves to the master. Figure 3 shows the generic Sercos III frame structure. Sercos III frames are broadcast frames. Each slave processes the frame by taking or placing data from the data field while forwarding the modified or unmodified content to the secondary port. The master receives back the modified frame; hence, in line topology, the last slave loops back the frame, and in ring topology, the frame is received on the master's secondary port.

Preamble	S F D	Destination Address	Source Address	Ethernet Type	MST	Data Field	FCS
7+1 Bytes		6 Bytes	6 Bytes	2 Bytes		46 to 1500 Bytes	4 Bytes

Figure 3. General Sercos III Frame Structure

The data field contains the cyclic and acyclic data for each slave. Each slave has a descriptor list that describes the location in the frame where it can read or write data. The slave validates the received FCS at the end of the frame. If the FCS is invalid, the frame content is not processed by the slave. If the slave has modified the content of the frame, it has to update the FCS; otherwise, the frame is corrupted and will be ignored by the next slaves or the master.

Because a Sercos III frame is based on standard Ethernet, it has a minimum and maximum frame length. The minimum frame is 72 bytes, which takes 5.8 μ s to transmit at 100 Mb/s. The longest frame is 1526 bytes, which takes 122 μ s to transmit. The frame length as well as the number of MTD and AT frames are set by the master and are configured in the slaves during CP2.

2.3 Synchronization

The master sync telegram (MST) field in the MDT0 frame is used by the master for slave synchronization. The MST field has its own FCS. Each slave validates the MST FCS and uses the MST time reference as an internal synchronization event.

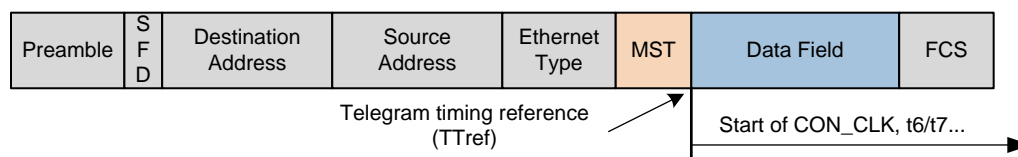


Figure 4. MDT0 Frame Synchronization Method

In CP2, the master measures the port-to-port delay of each slave, calculates the frame round-trip time and programs a different port delay time into each slave's ports. Finally, all slaves are synchronized in CP4 to the master's reference clock. The slave uses the MST synchronization events to internally synchronize the RT and UCC channel time slot as well as to generate a hardware synchronization signal called CON_CLK.

The CON_CLK hardware signal is used to synchronize a coprocessor or application to the Sercos III communication cycle.

2.4 Service Channel (SVC)

The MDT and AT frames embed an asynchronous communication channel that is used by the master to transfer communication, parameter and diagnostic data. The master issues SVC read and write requests to defined data structure (identification number [IDN]) in each slave. For example, the IDNs are used to configure Sercos III network parameters and UCC channel parameters.

2.5 Topology

A Sercos III network is configured as line or ring topology. When using line topology, a daisy-chain cabling is used and only one port of the master is connected to the first slave. The last slave in the chain loops-back the MDT/AT frames, so they are received back by the master (see [Figure 5](#)).

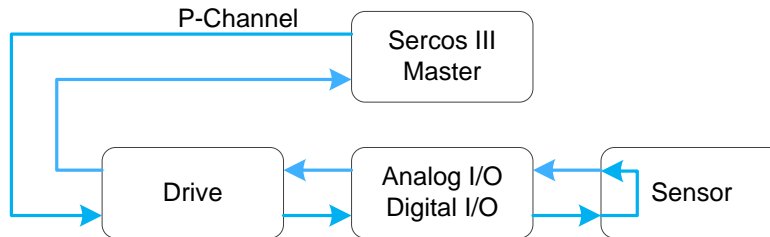


Figure 5. Line Topology With Last Device in Loopback Mode

To support network redundancy, use ring topology (see [Figure 1](#)). The primary port of the master is connected to the first slave and the secondary port is connected to the last slave. The master transmits Sercos III frames simultaneously on both ports. In case of an Ethernet cable break (called ring break), the slave that detects the break immediately starts the loopback mode. The slave sends the MDT/AT frames back on the same port where the frames were received. The master detects the ring break scenario in the status information of the AT frames. After the ring-break is physically resolved, the master issues a ring heal command to the slaves to restore the ring topology connection. Ring break and ring heal can occur anytime, but the master continues to operate the network in CP4.

3 Sercos III Slave Solution With Sitara Processors From TI

3.1 Components of Sercos III Slave

Many existing Sercos III slave solutions consist of an application processor, a FPGA, two industrial Ethernet physical layer devices (PHYs), and power management (see [Figure 6](#)). The application processor executes the customer's application, the Sercos III user profile and slave stack. The FPGA implements the Sercos III real-time Ethernet MAC that handles the real-time critical functions of the Sercos III standard. The MAC in the FPGA is connected to two industrial Ethernet PHYs that provide the Sercos III network ports. The devices need to be powered by a dedicated power management solution.

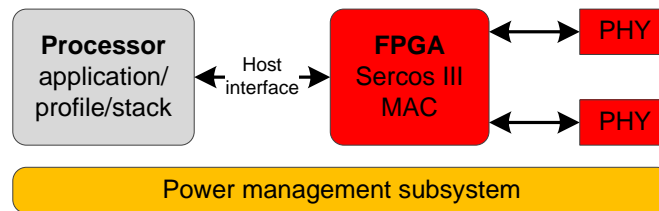


Figure 6. Sercos III Slave Solution With Processor and FPGA

The AM437x Sitara TI design (TIDEP0039) combines the Sercos III MAC function blocks of an FPGA with the application processor. This leads to an integrated solution combining the customer application, the profile, and stack with the Sercos III MAC on a single SoC (see [Figure 7](#)). The powerful ARM® Cortex®-A8 application processor handles the application, the Sercos profile, and stack. The Sercos III real-time critical functions are handled by the PRU-ICSS, which is integrated on the AM335x Sitara family of MPUs. A dedicated power management unit (PMU) device supplies the Sitara device enabling a simplified power management solution.

The fast internal interconnect between the ARM Cortex-A8, the PRU-ICSS, internal memory, and other peripherals allow fast exchange of real-time process data.



Figure 7. Integrated Sitara Sercos III Slave Solution

3.2 Sitara AM437x Peripheral Block Diagram

The Sitara AM437x device family is a low-power application processor with an ARM Cortex-A9 RISC core and a broad range of integrated industrial peripherals (see Figure 8). The ARM Cortex-A9 supports clock frequency ranges from 300 MHz for simple I/O applications up to 1 GHz for complex control applications that require more CPU performance.

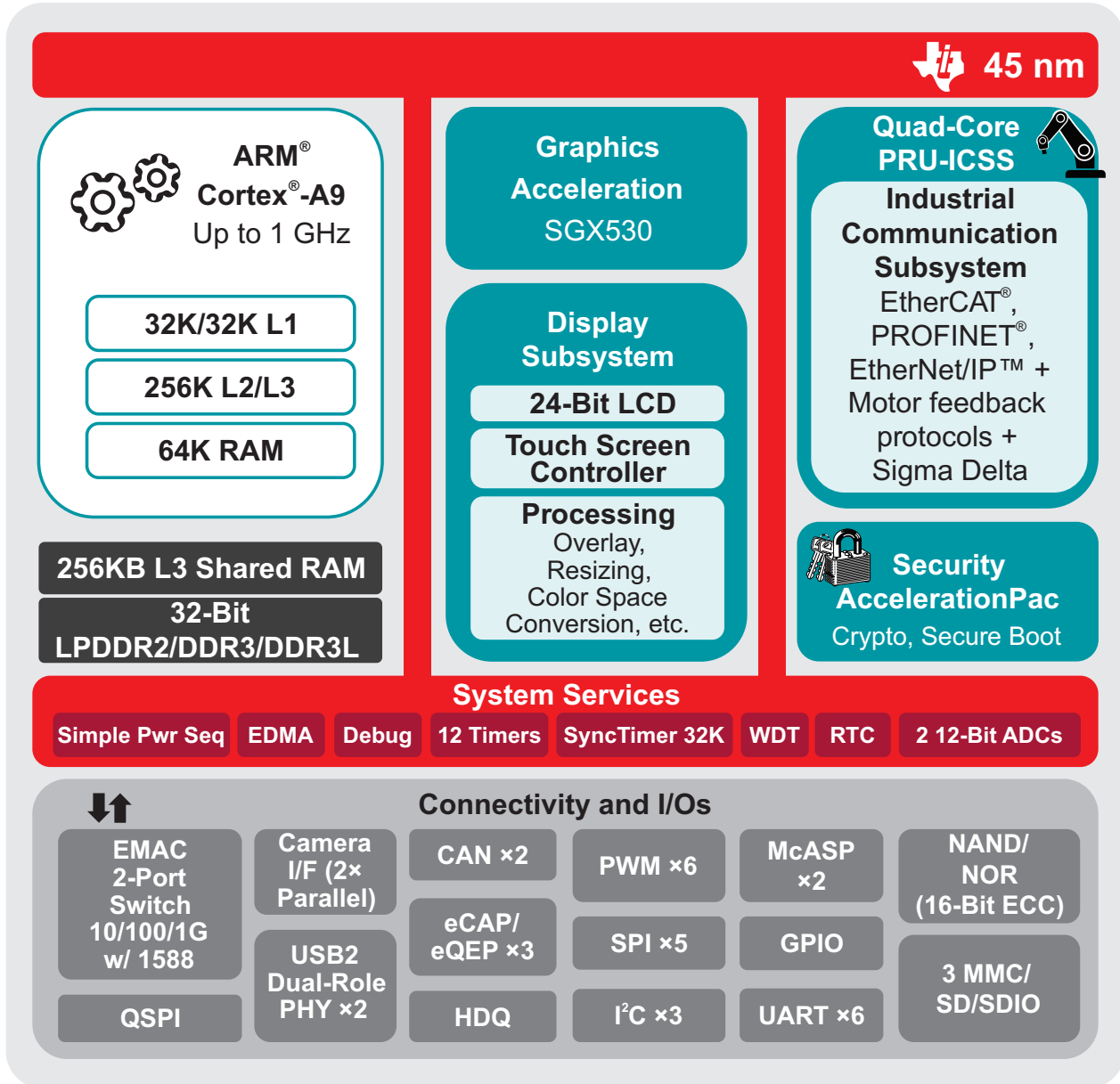


Figure 8. AM437x Family Block Diagram

3.3 Sercos III Slave System and Software Architecture

The hardware layer of Sercos III requires 100 Mb/s Ethernet for the physical layer (PHY). In the TIDEP0039, this is implemented with two TLK105L Ethernet PHYs from TI. The PHY's MII connects to the PRU-ICSS that handles the real-time functions of the Sercos III standard. The PRU-ICSS exchanges real-time data, Ethernet frames, control, and status information through the internal shared memory interface with the Sercos and Ethernet stack. The Sercos III stack and the function-specific profile (drive, I/O, and so on) provides an application programming interface (API) to the customer's application. The standard Ethernet frames are placed by PRU-ICSS in a dedicated shared memory area. Ethernet applications like web server and trivial file transfer protocol (TFTP) can access the Ethernet frames through a dedicated frame queue.

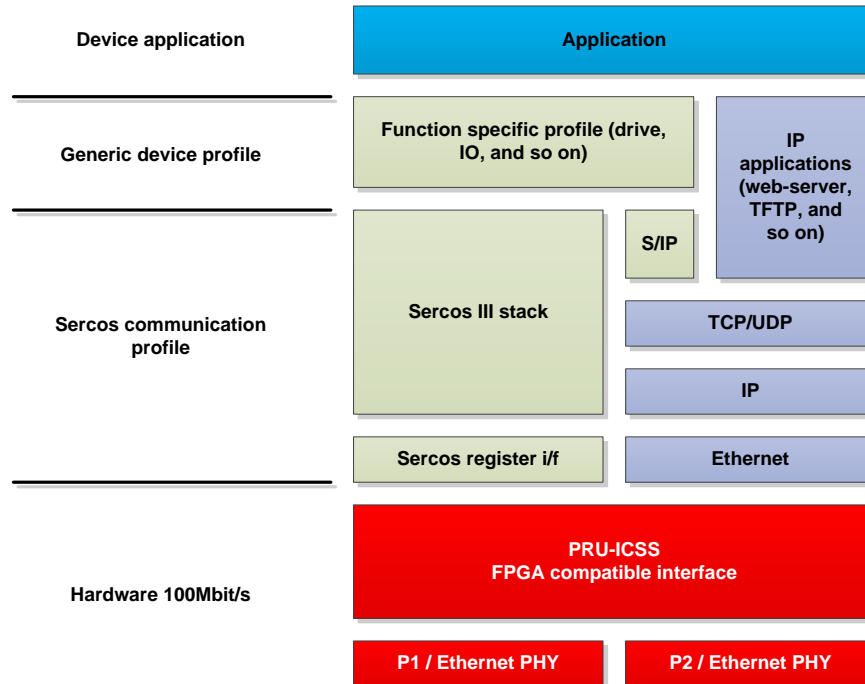


Figure 9. Sitara Sercos III Slave System and Software Architecture

3.4 Sercos III Stack Integration and Solution Validation

The TIDEP0039 solution has been validated with the Sercos III stack from third-party stack provider Cannon-Automata, using the Sercos III Conformizer validation tool. All required communication tests cases have been tested and confirmed. Customers can leverage this integrated solution by contacting the third-party stack provider, who gives them access to the validated Sercos III solution to jump start product development. The Sercos III firmware for PRU-ICSS has been implemented with a register interface equivalent to the Sercos III FPGA to allow customers to reuse existing stack solutions.

3.5 Development Tools

The TIDEP0039 solution can be evaluated with the AM437x industrial development kit (IDK) board (see [Figure 10](#)). The board is intended for developing industrial Ethernet protocols for master and slaves devices, for example, I/O modules, sensors, actuators, motor controls, and PLCs. The two real-time Ethernet ports of the PRU-ICSS are accessible by two RJ45 connectors. Additionally, the board is equipped with digital inputs and outputs through onboard connectors.



Figure 10. AM437x IDK Board

Further software development can be done using the industrial software development kit (SDK), which combines SYS/BIOS (real-time operating system (RTOS) from TI) and example projects using industrial Ethernet protocols.

One key advantage of the Sitara AM437x family is that it allows for a flexible and dynamic exchange of the industrial Ethernet protocol within the PRU-ICSS (see [Figure 11](#)). The application processor loads new fieldbus firmware in the PRU-ICSS during device initialization, making external fieldbus ASICs or FPGAs redundant. This enables customers to support various industrial Ethernet protocols, including EtherCAT, PROFINET, Sercos III, EtherNet/IP, and Ethernet POWERLINK, with one single hardware platform.

4 Block Diagram

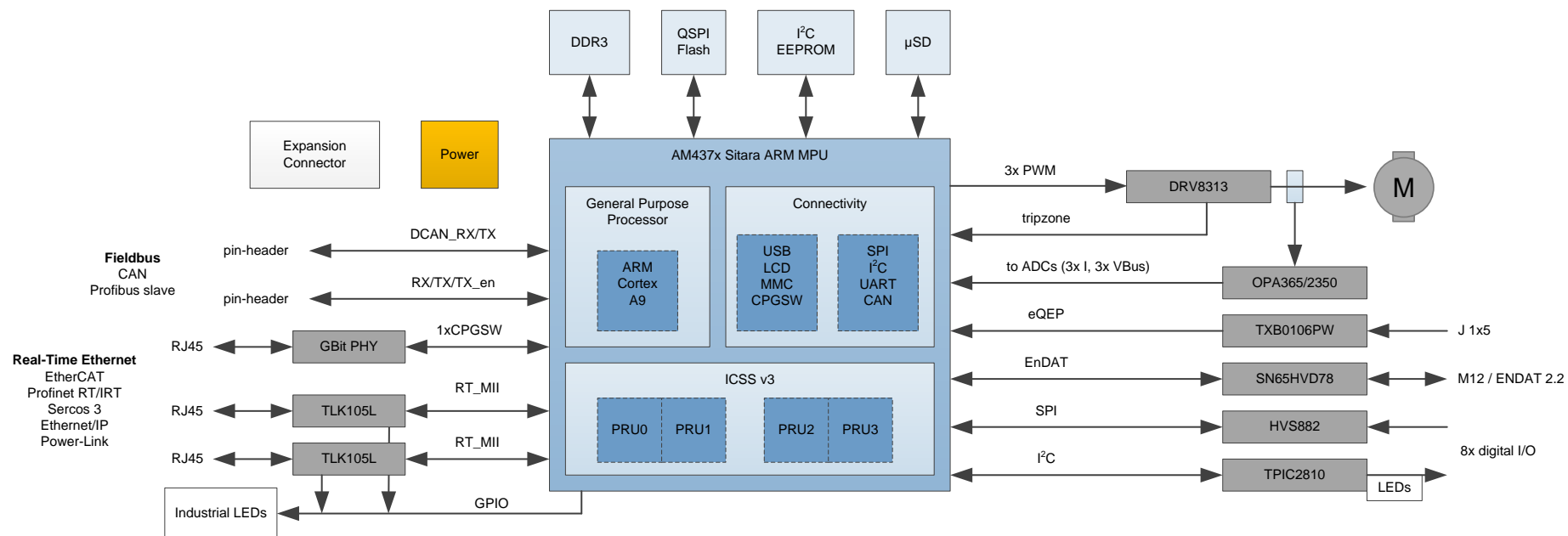


Figure 11. AM437x IDK (TMDXIDK437X) Board System Block Diagram

4.1 **Highlighted Products**

4.1.1 **AM4379 Processor**

Up to 1-GHz Sitara™ ARM Cortex-A9 32-bit RISC processor

- NEON™ SIMD coprocessor and vector floating point (VFPv3) coprocessor
- 32KB of L1 instruction and 32KB of data cache
- 256KB of L2 cache or L3 RAM
- 256KB of on-chip boot ROM
- 64KB of dedicated RAM
- Emulation and debug — JTAG
- Interrupt controller

PRU-ICSS

- Supports protocols such as EtherCAT®, PROFIBUS, PROFINET, EtherNet/IP™, EnDat 2.2, and more
- Two PRUs subsystems with two PRU cores each
- 32-bit load/store RISC processor capable of running at 200 MHz
- 12KB (PRU-ICSS1), 4KB (PRU-ICSS0) of instruction RAM with single-error detection (parity)
- 8KB (PRU-ICSS1), 4KB (PRU-ICSS0) of data RAM with single-error detection (parity)
- Single-cycle 32-bit multiplier with 64-bit accumulator
- Enhanced GPIO module provides shift-in/out support and parallel latch on external signal
- 12KB (PRU-ICSS1 only) of shared RAM with single-error detection (parity)
- Three 120-byte register banks accessible by each PRU
- Interrupt controller module (INTC) for handling system input events
- Local interconnect bus for connecting internal and external masters to resources inside PRU-ICSS
- Peripherals inside PRU-ICSS:
 - One UART port with flow control pins, supports up to 12 Mb/s
 - One enhanced capture (eCAP) module
 - Two MII Ethernet ports that support industrial Ethernet, such as EtherCAT
 - One MDIO port

On-chip memory (shared L3 RAM)

- 256KB of general-purpose on-chip memory controller (OCMC) RAM
- Accessible to all masters

External memory interfaces (EMIF)

- DDR controllers:
 - LPDDR2: 266-MHz clock (LPDDR2-533 data rate)
 - DDR3 and DDR3L: 400-MHz clock (DDR-800 data rate)
 - 32-bit data bus
 - 2GB of total addressable space
 - Supports one x32, two x16, or four x8 memory device configurations
- General-purpose memory controller (GPMC)
 - Flexible 8-bit and 16-bit asynchronous memory interface with up to seven chip selects (NAND, NOR, Muxed-NOR, SRAM)
 - Uses BCH code to support 4-, 8-, or 16-bit ECC
 - Uses hamming code to support 1-bit ECC

See the AM4379 datasheet for a complete list of features [\[1\]](#).

4.1.2 AM437X Industrial Development Kit (IDK) EVM Hardware Specification

- AM4379 ARM Cortex-A9
- 1GB DDR3, QSPI-NOR Flash
- Discrete power solution
- EnDat connectivity for motor feedback control
- 24-V power supply
- USB cable for JTAG interface and serial console

Software and Tools

- SYS/BIOS real-time OS
- StarterWare base port
- Code Composer Studio™ (CCS) integrated development environment (IDE)
- Application stack for industrial communication protocols
- Sample industrial applications

Connectivity

- PROFIBUS interface
- CANOpen
- EtherCAT
- EtherNet/IP
- PROFINET
- Sercos III
- IEC61850
- PWM
- Motor axis position feedback
- Up to 3-phase motor drive connector
- Sigma Delta decimation filter
- Digital inputs and outputs (I/O)
- SPI
- UART
- JTAG

See the AM437x IDK website for a complete list of features and design resources (<http://www.ti.com/tool/TMDXIDK437X>).

5 Test Data



SercosIII Conformance Test

General Information

Date and time: 2015-06-02 08:57:03
 Configured sercos revision: V1.1.2
 Conformizer version: 2_1_0
 SERCANS version: FWA-SERC*3-SCM-03V06-D0-TM
 SERCANS MAC: 00-60-34-A7-D0-E7
 SERCANS Server version: 975
 Execution time (hh mm ss): 02:33:35

Test Case Selections

- Latest manual communication tests
 - Latest Sercos Communication Profile tests
 - Test case selection - GDP
 - Test case selection - FSP IO
-

Test Case Statistics

Overall number of test cases: 226
 Skipped Testcases: 69
 Executed Testcases: 157
 - Failed Testcases: 0 (0 % failed)
 - Testcases with warning: 7 (4 % with warning)
 - Passed Testcases: 150 (96 % passed)

Electronic Label (SI = 0)

Component Name: Sercos III Slave Demo
 Vendor Name: Texas Instruments
 Vendor Code: 111
 Device Name: AM437x Industrial Development Kit (IDK)
 Vendor Device ID: Sitara AM437x

Figure 12. Sercos Conformizer Test Report Extract

6 Summary and Conclusion

The TIDEP0039 Sercos III slave communication development platform combines the Sercos III firmware for the PRU-ICSS and an equivalent Sercos III register interface with the TMDXIDK437X board. Third-party service provider Cannon-Automata offers customers a Sercos III reference stack and example application. Alternatively, customers can use an existing stack and interface it to the TIDEP0039 Sercos III slave solution.

With the TIDEP0039 Sercos III slave communication development platform, customers can jump start their development of Sercos III-based industrial applications like industrial I/Os, drives, sensors, and actuators. The solution saves development efforts and production cost by integrating the industrial Ethernet protocol into the microprocessor (MPU) and shortens time to market.

It also demonstrates that customers can remove the external FPGA or fieldbus ASIC without compromising the functional or operational requirements.

7 Design Files

7.1 Physical TMDXIDK437X EVM

To purchase the TMDXIDK437X the TI shop, see its product page at <http://www.ti.com/tool/tmdxidk437x>.

7.2 Schematics

To download the schematics, see the design files at [TIDEP0039](#).

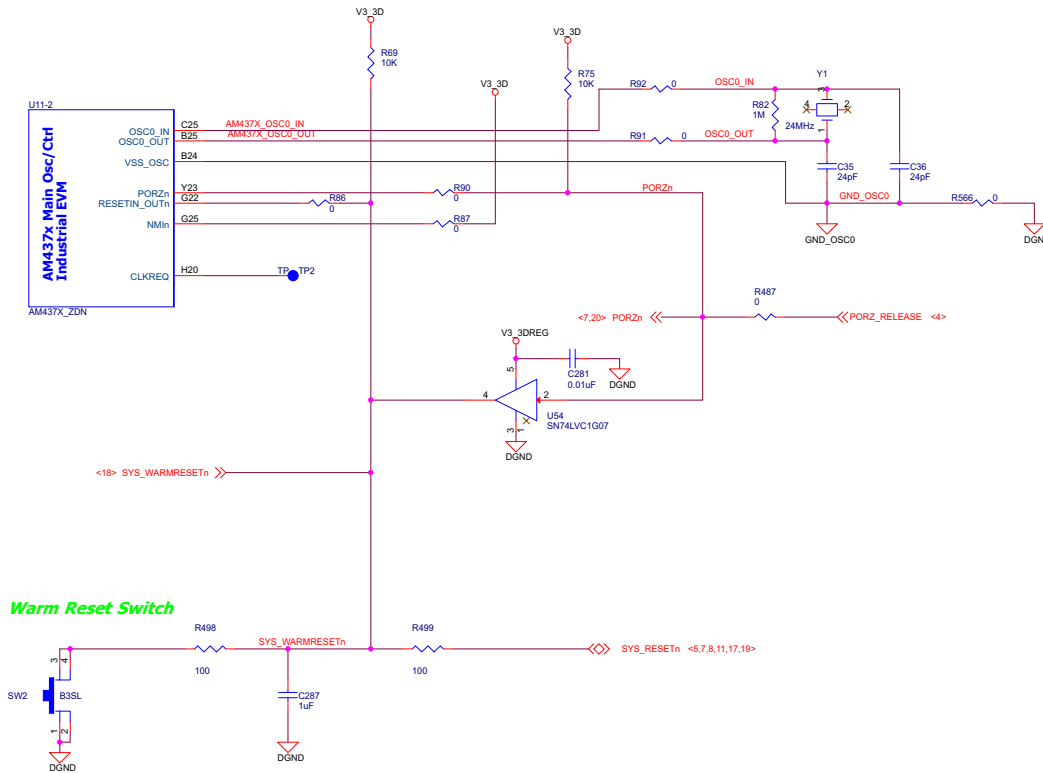
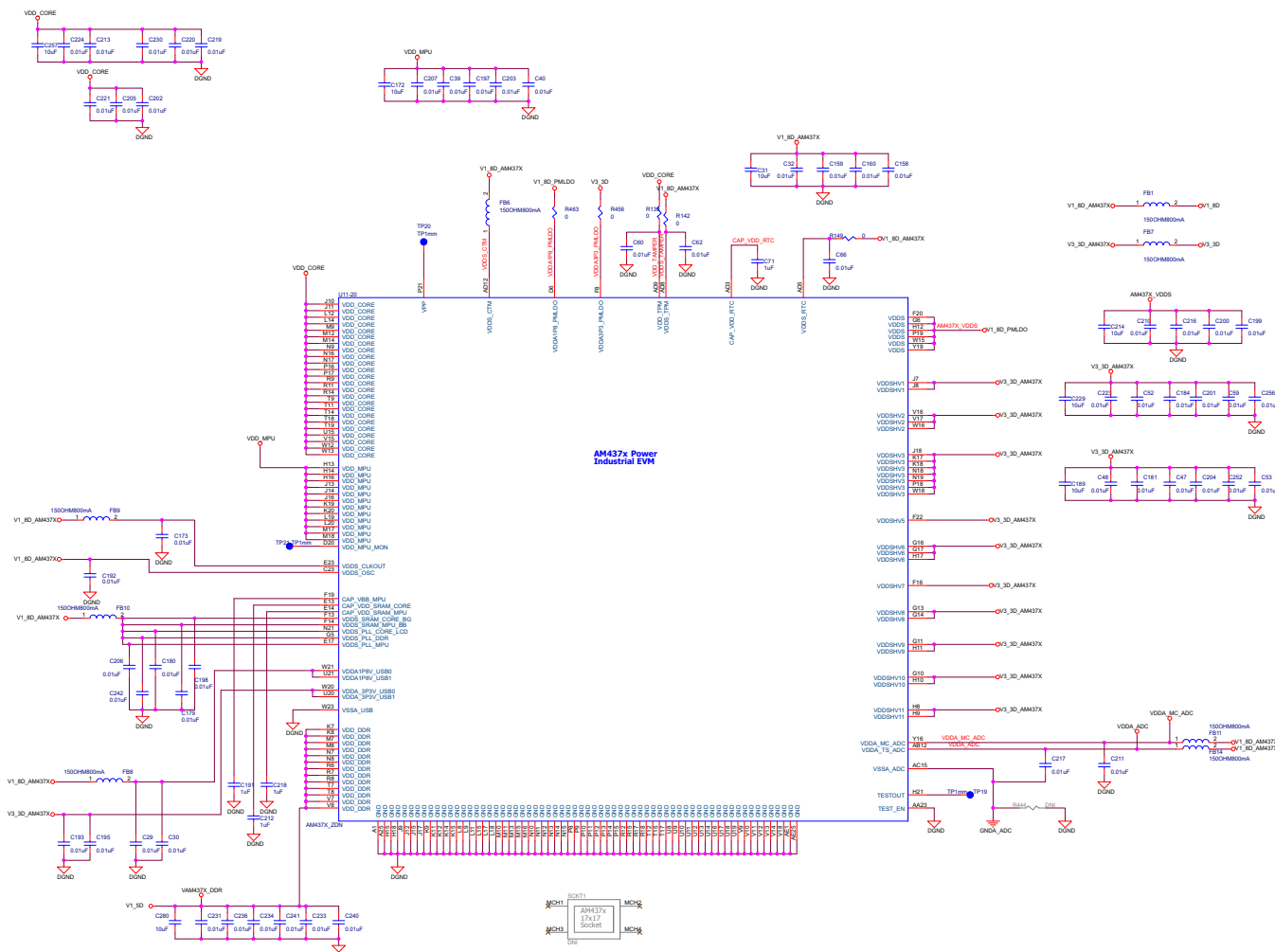


Figure 13. Processor System Schematic



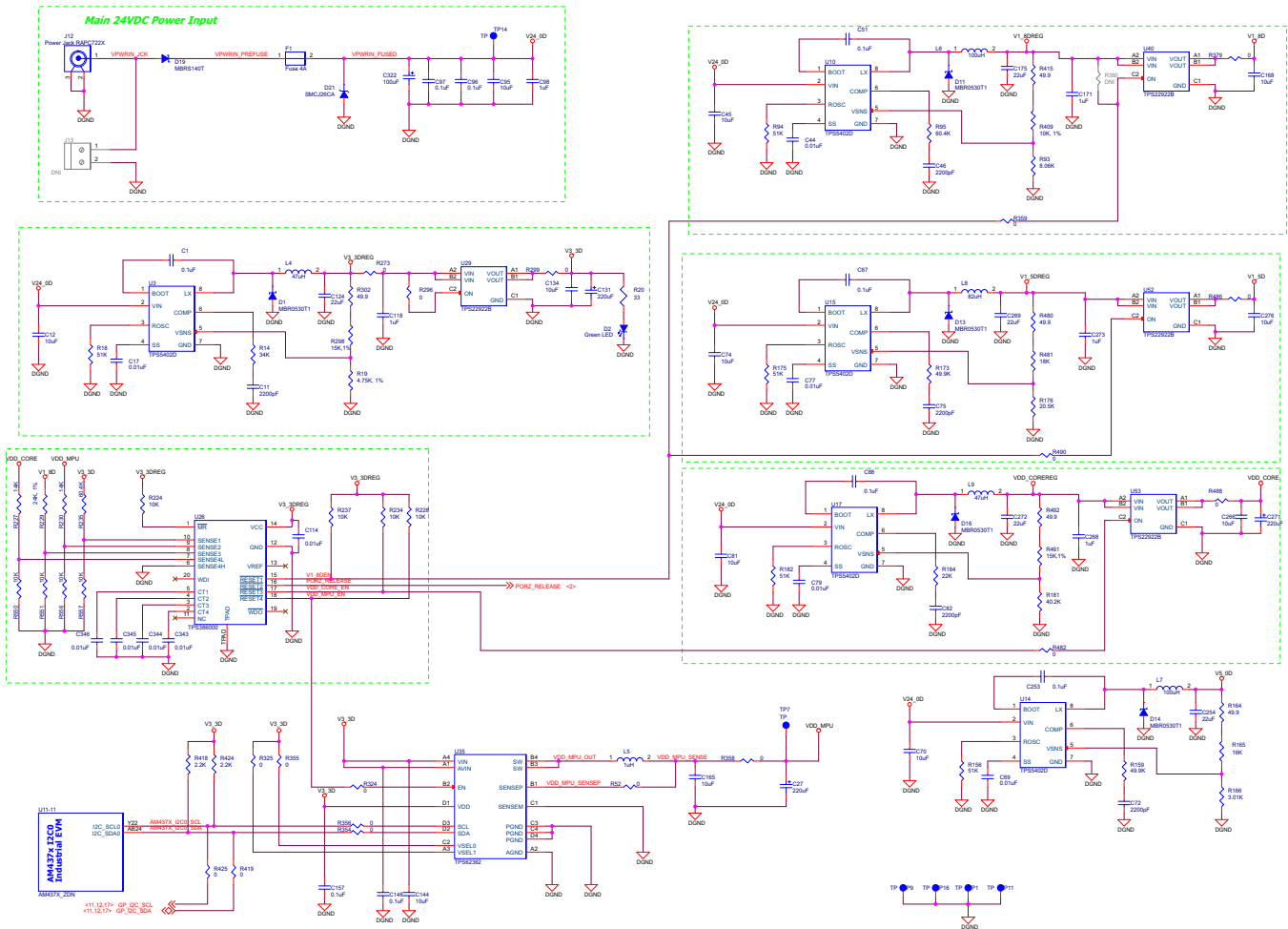


Figure 15. Power Schematic

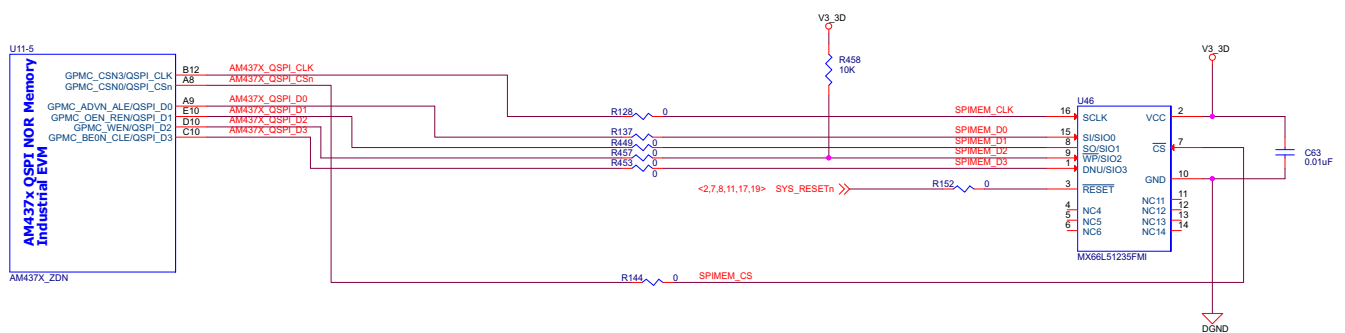


Figure 16. QSPI NOR Flash Memory Schematic

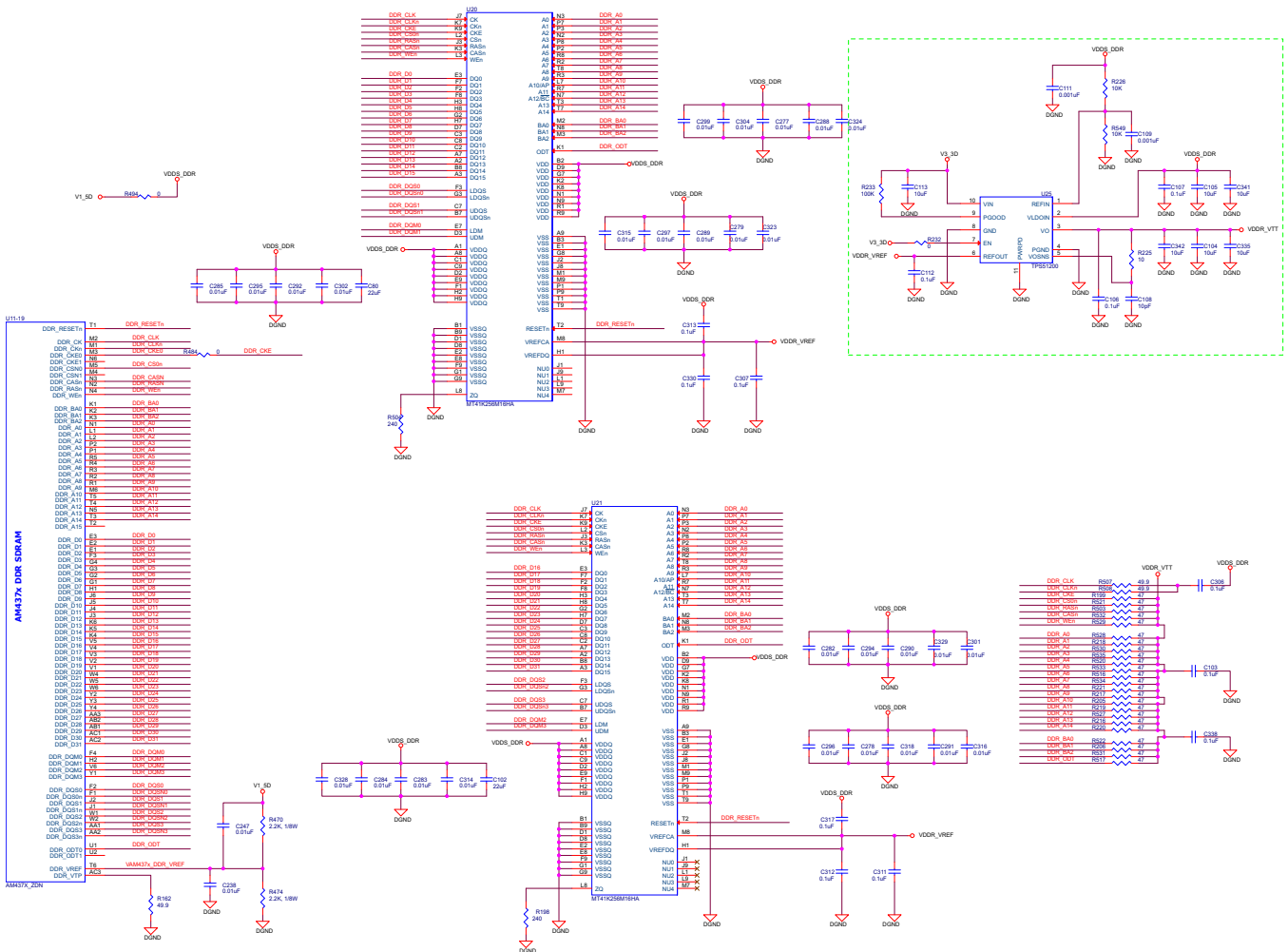


Figure 17. DDR3 SDRAM Memory Schematic

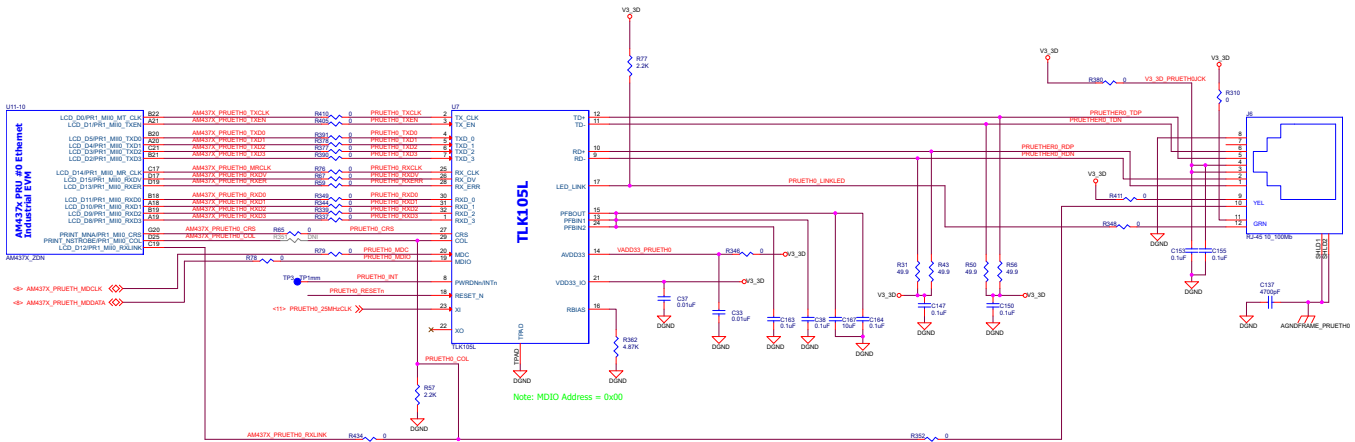


Figure 18. ICSS #0 Ethernet Schematic

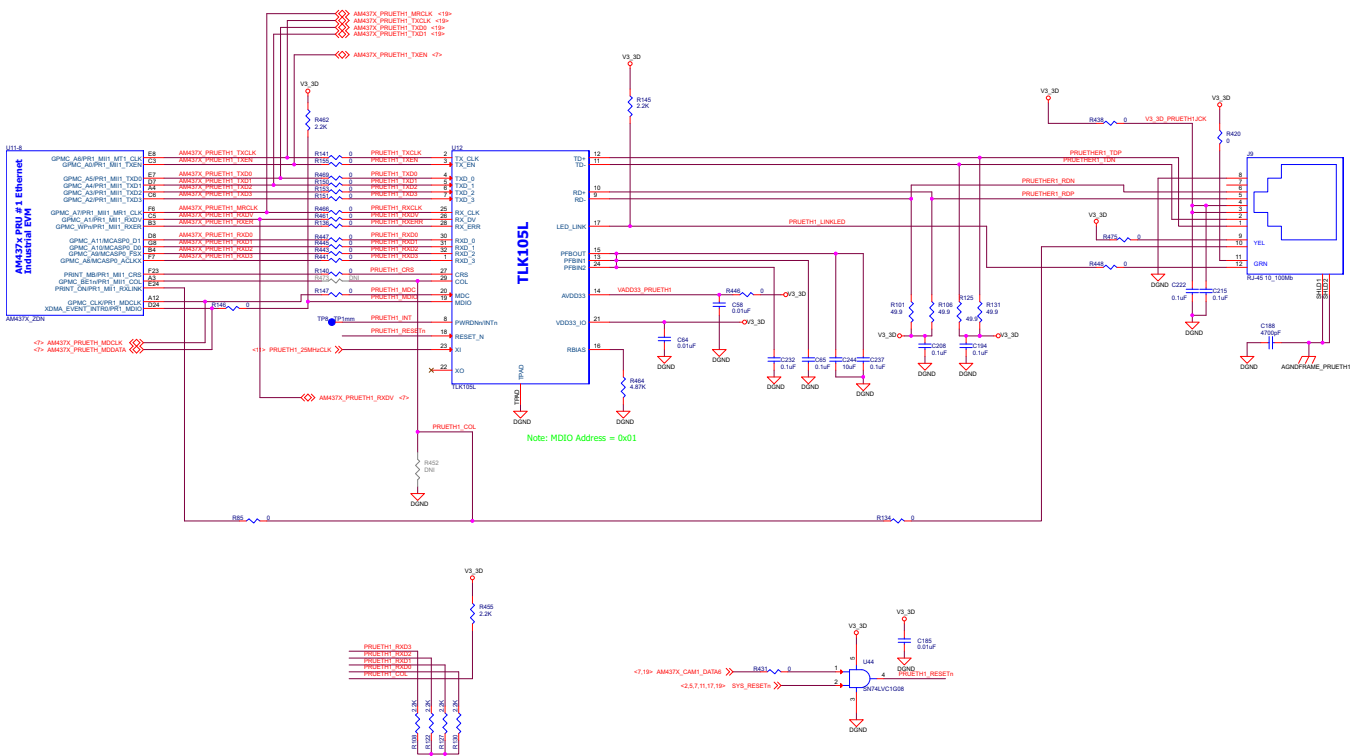


Figure 19. ICSS #1 Ethernet Schematic

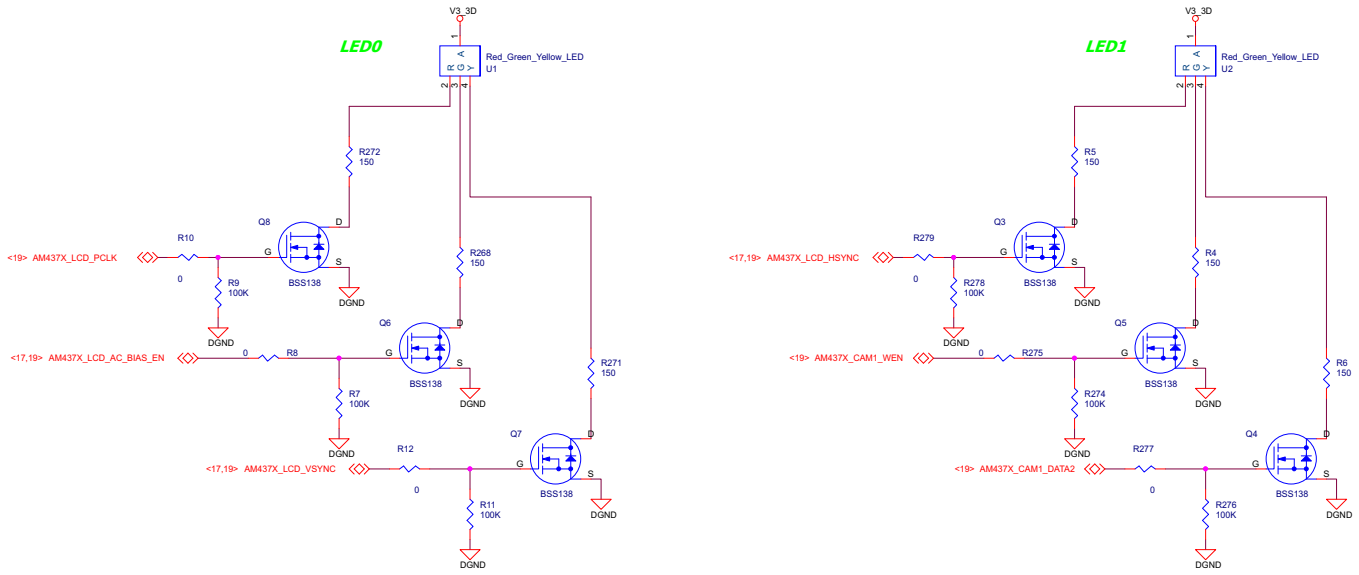


Figure 20. EtherCAT Schematic

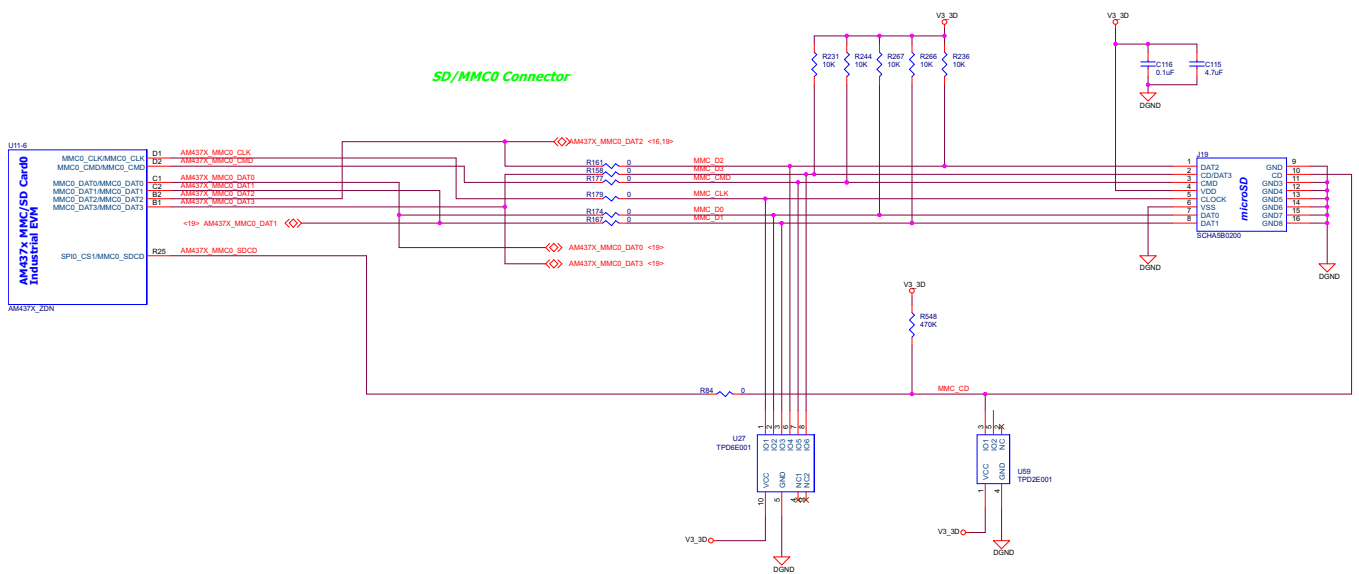
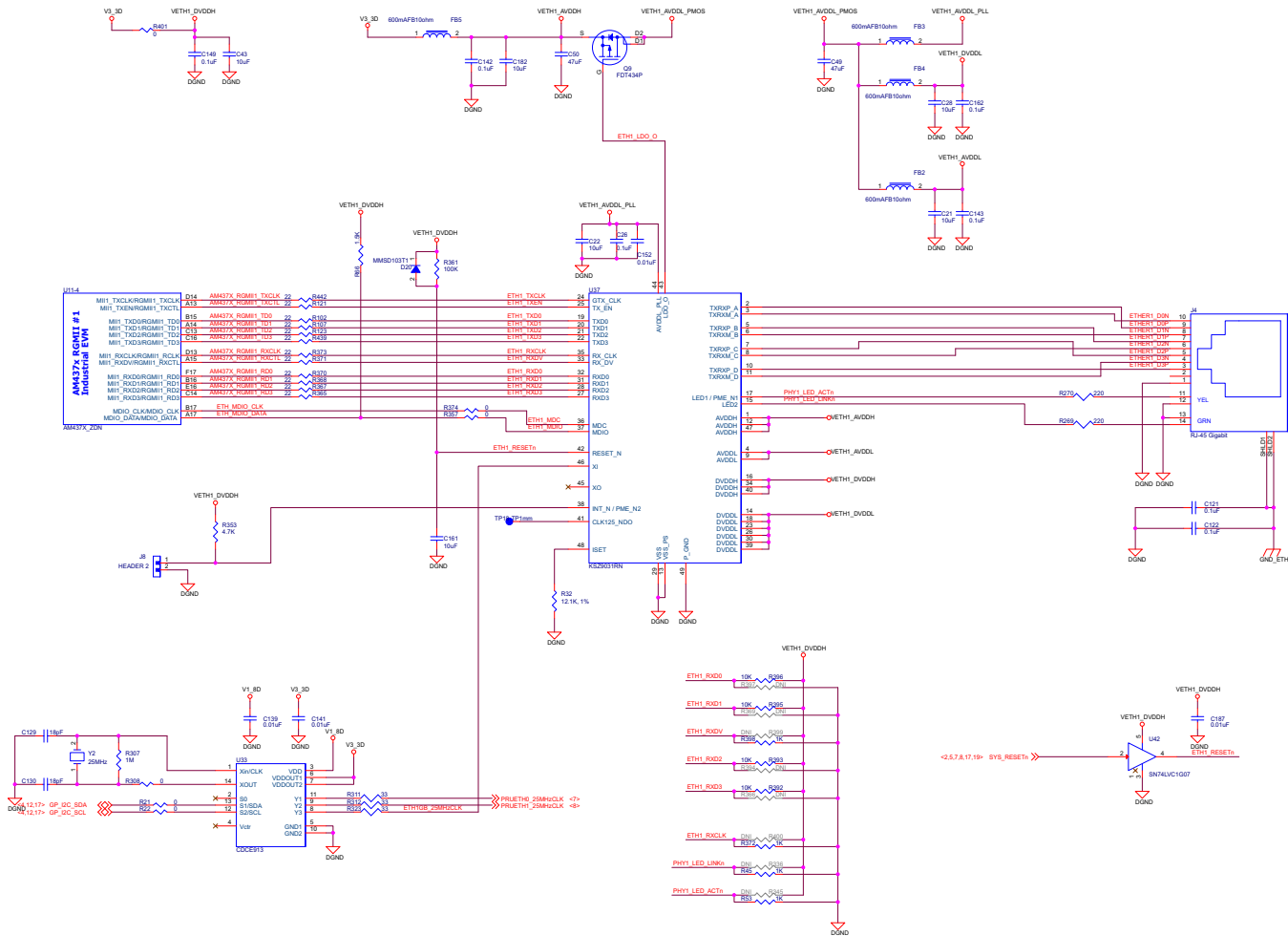


Figure 21. SDMMC #0 Interface Schematic



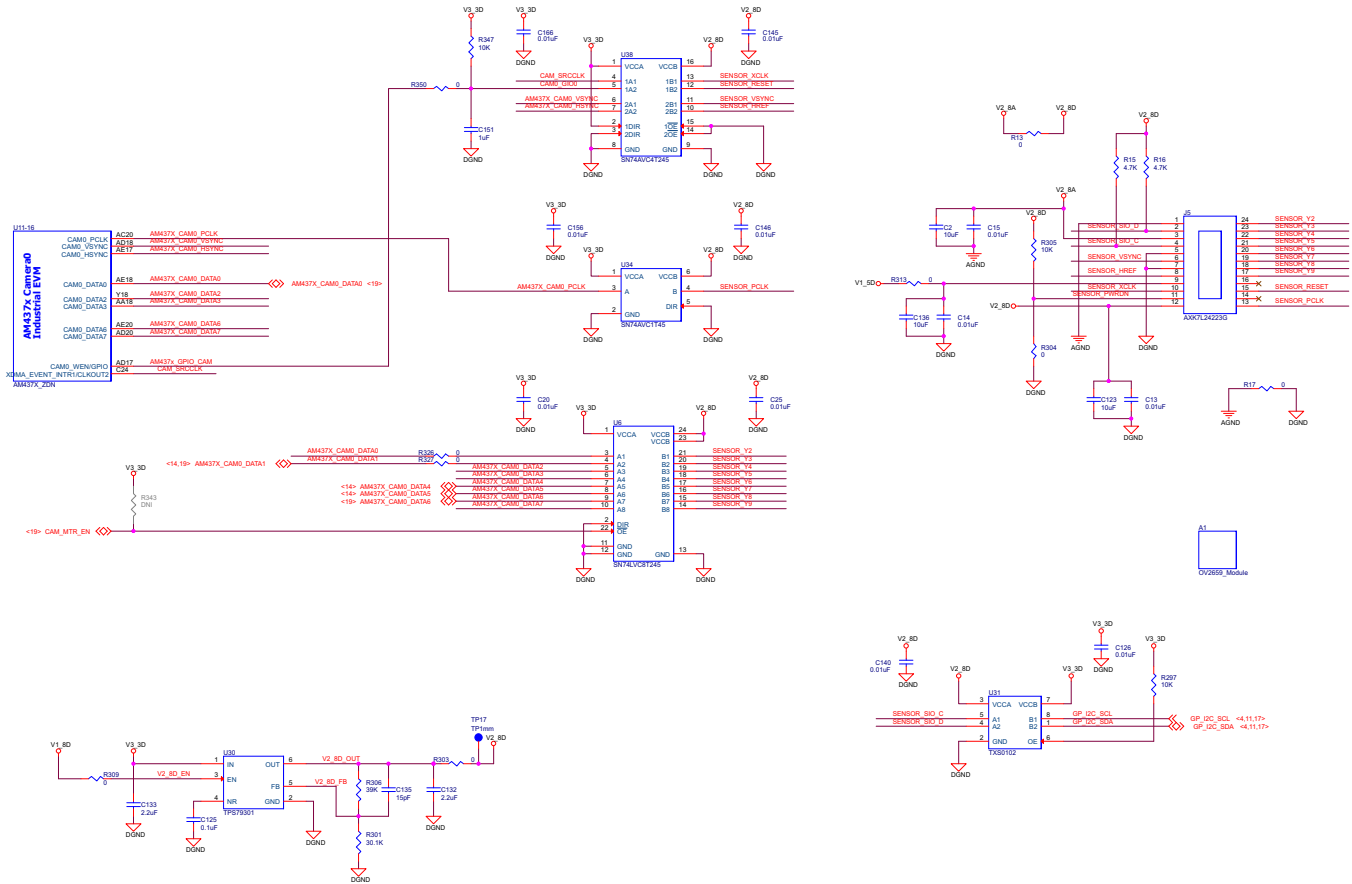


Figure 23. Camera #0 Schematic

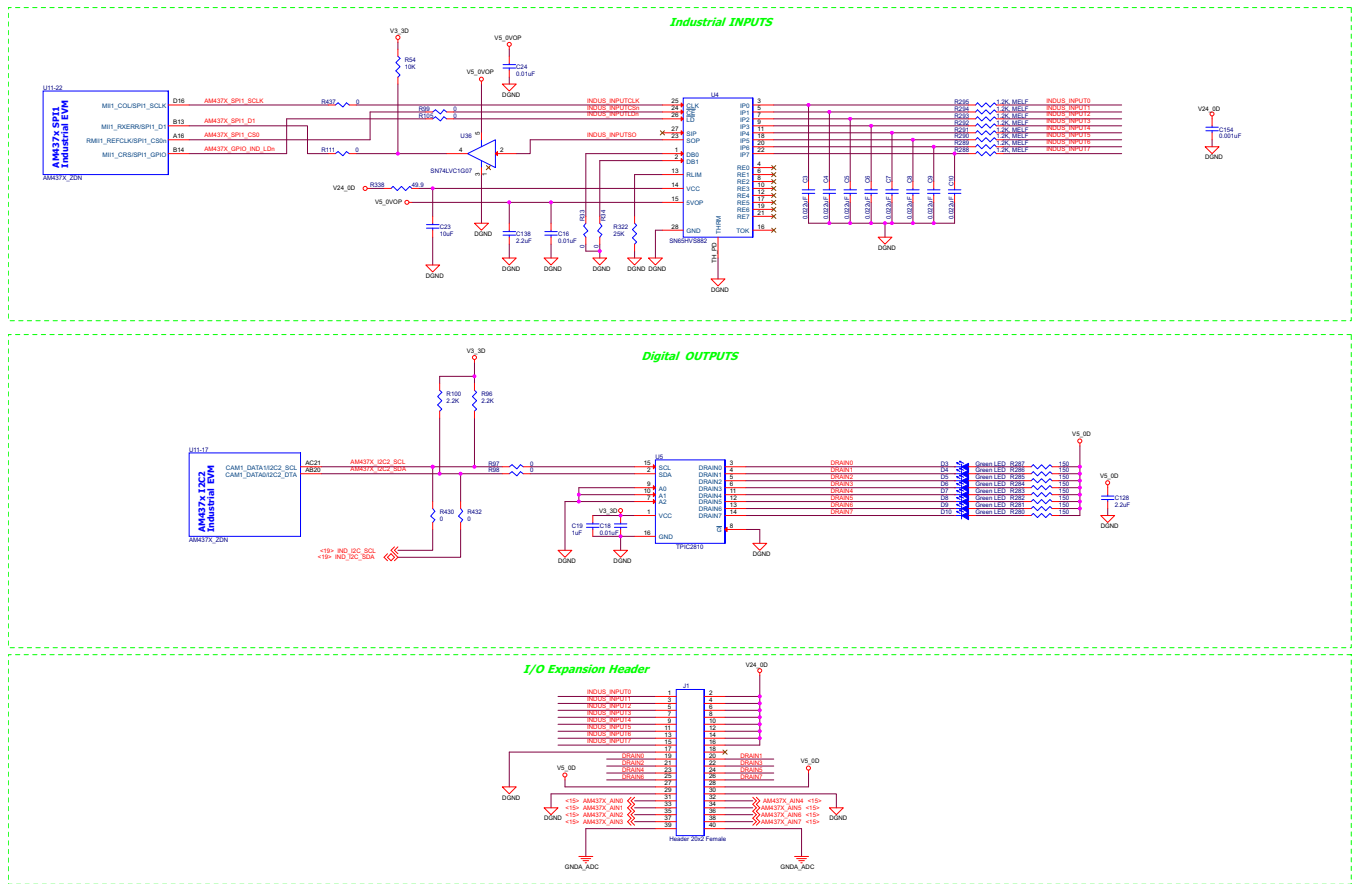


Figure 24. Industrial I/O Schematic

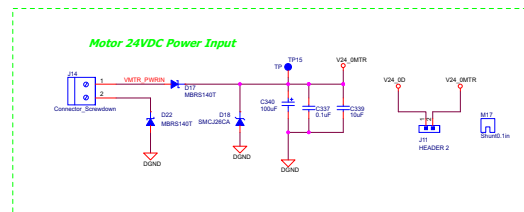
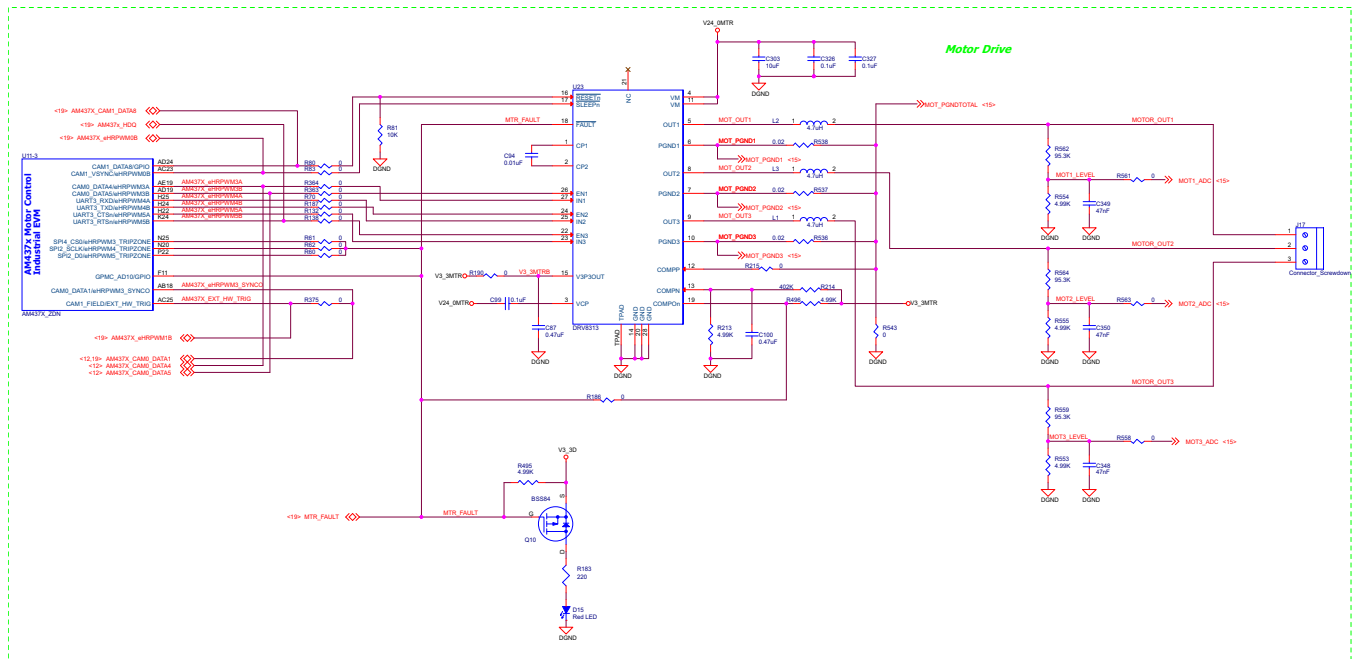


Figure 25. Motor Control Schematic

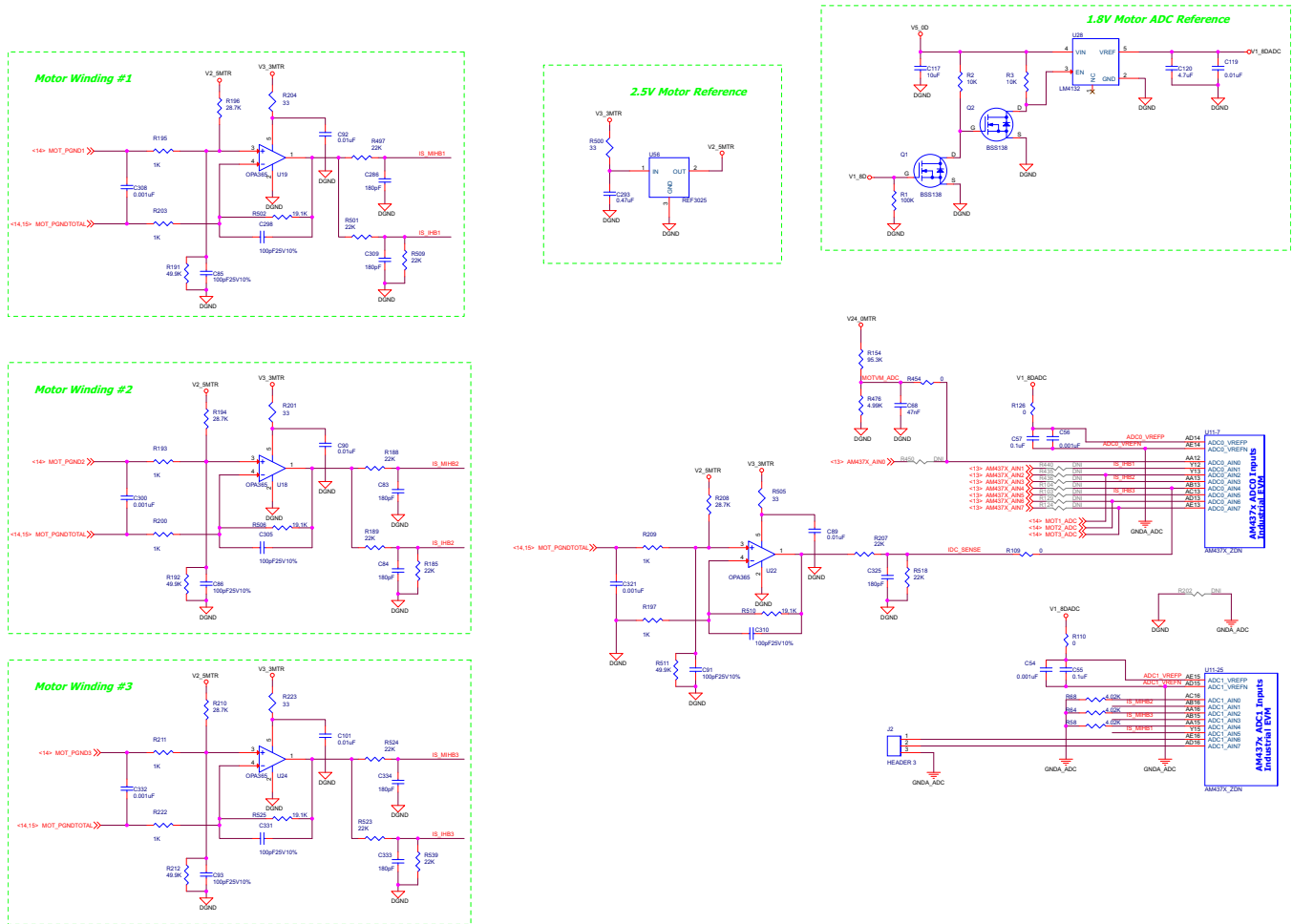


Figure 26. Motor Sense Schematic

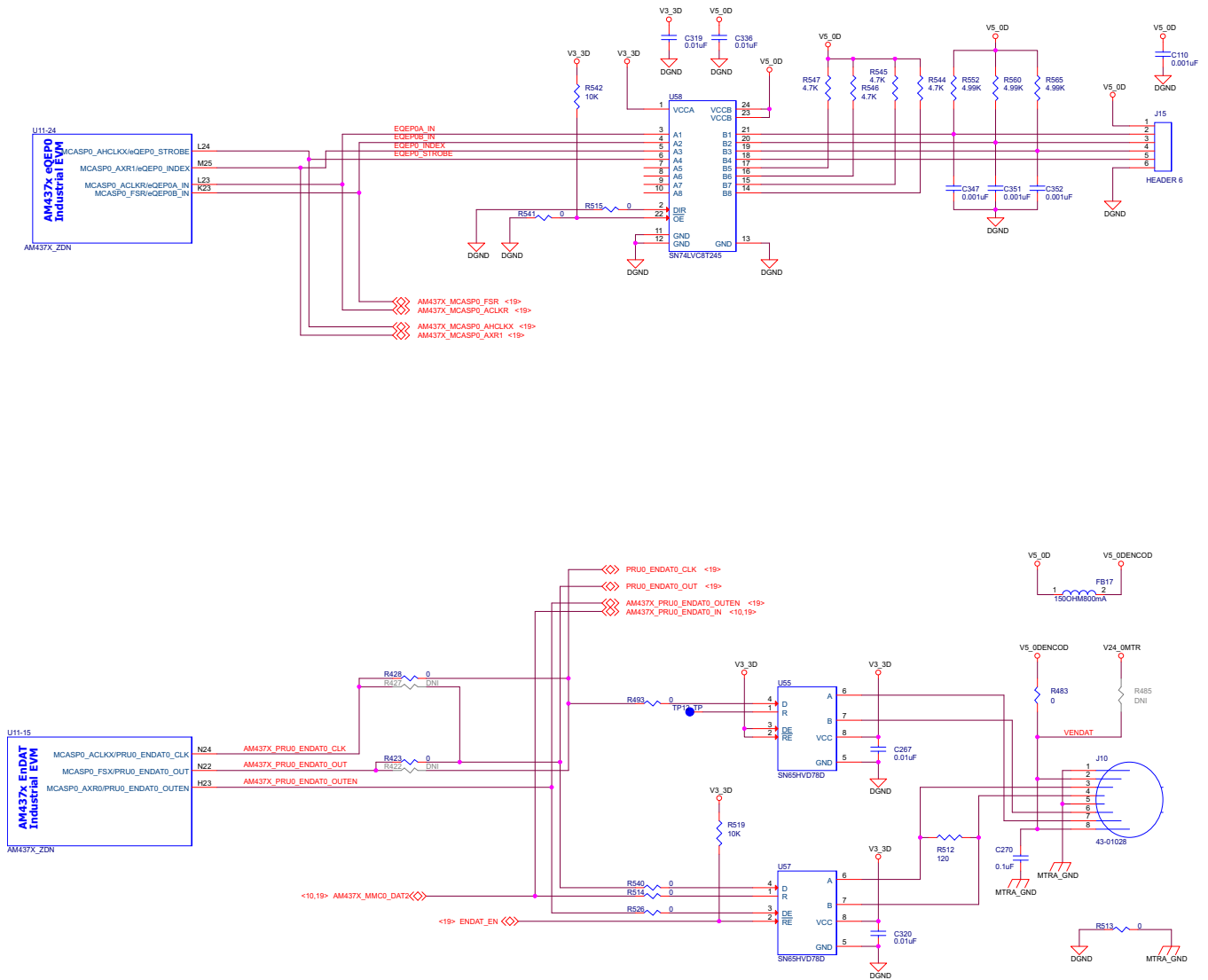


Figure 27. Motor Encoders QEP and EnDAT

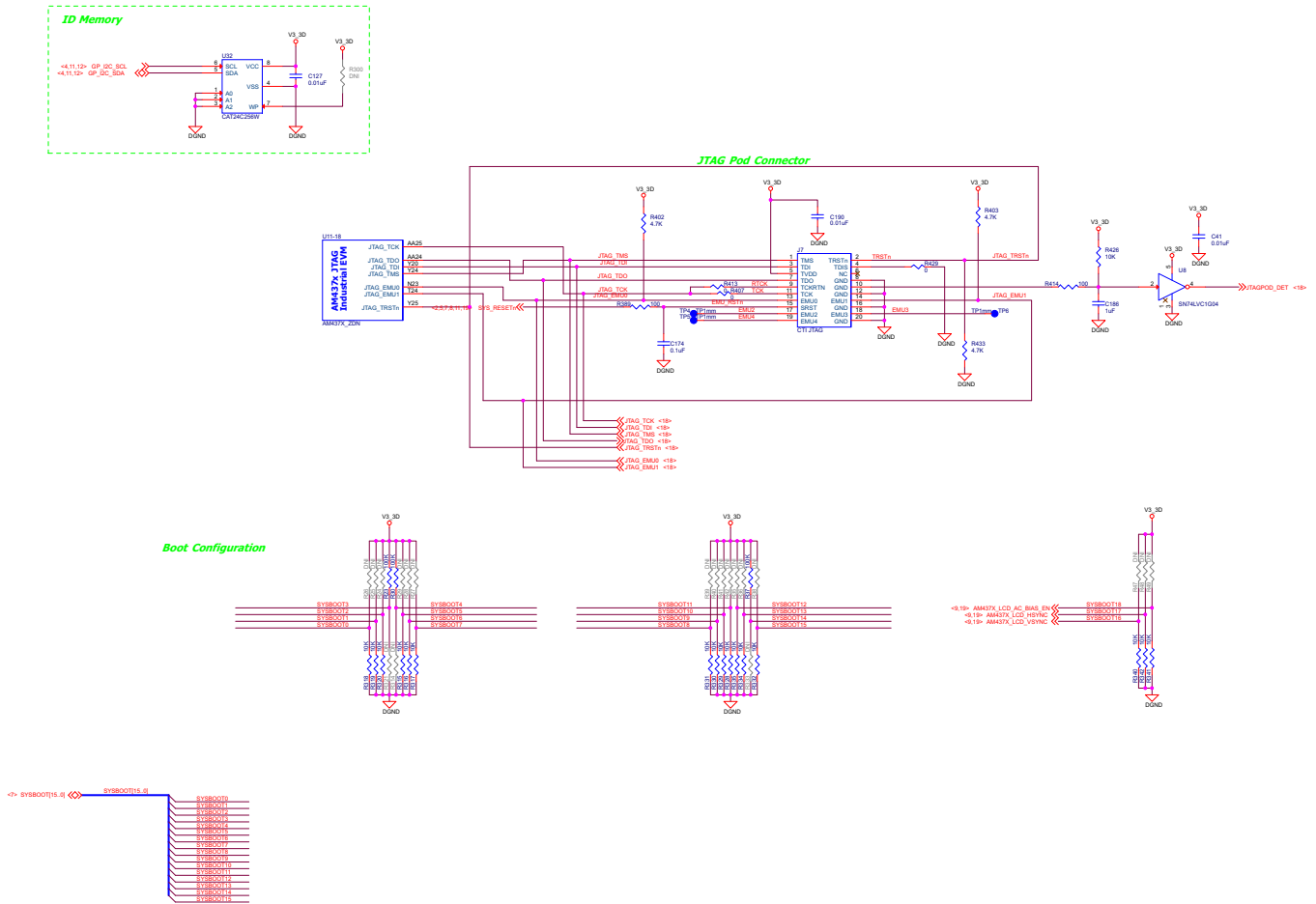


Figure 28. Debug and Configuration Schematic

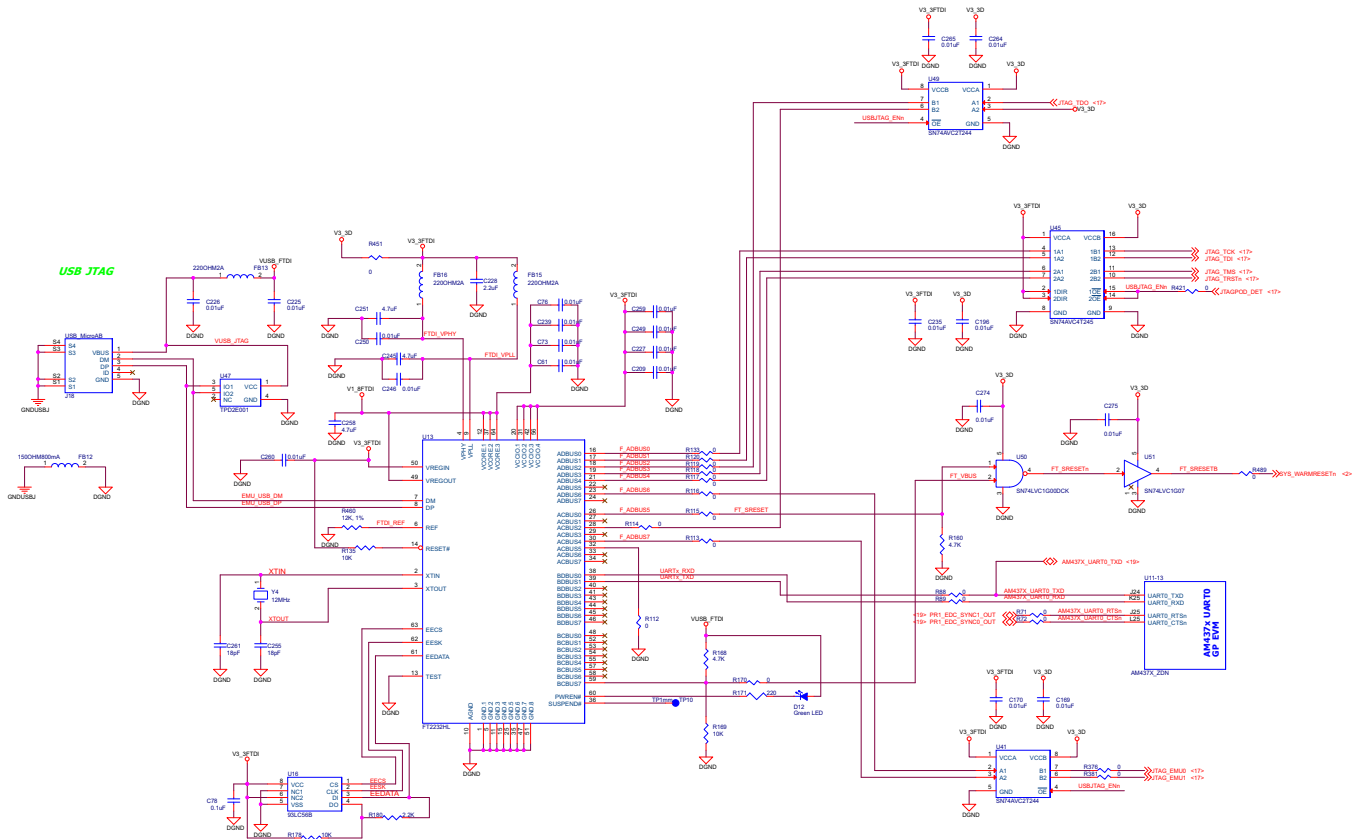
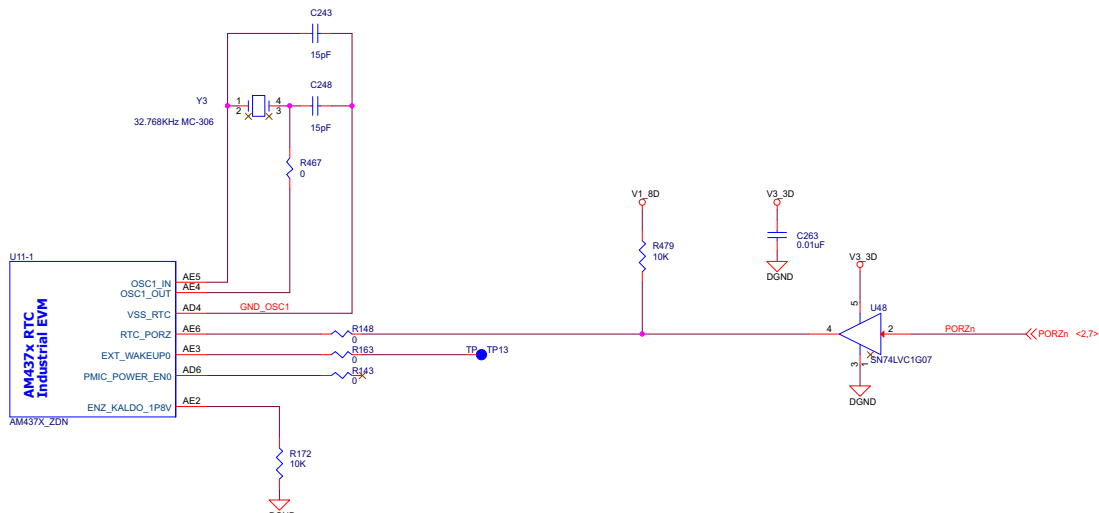
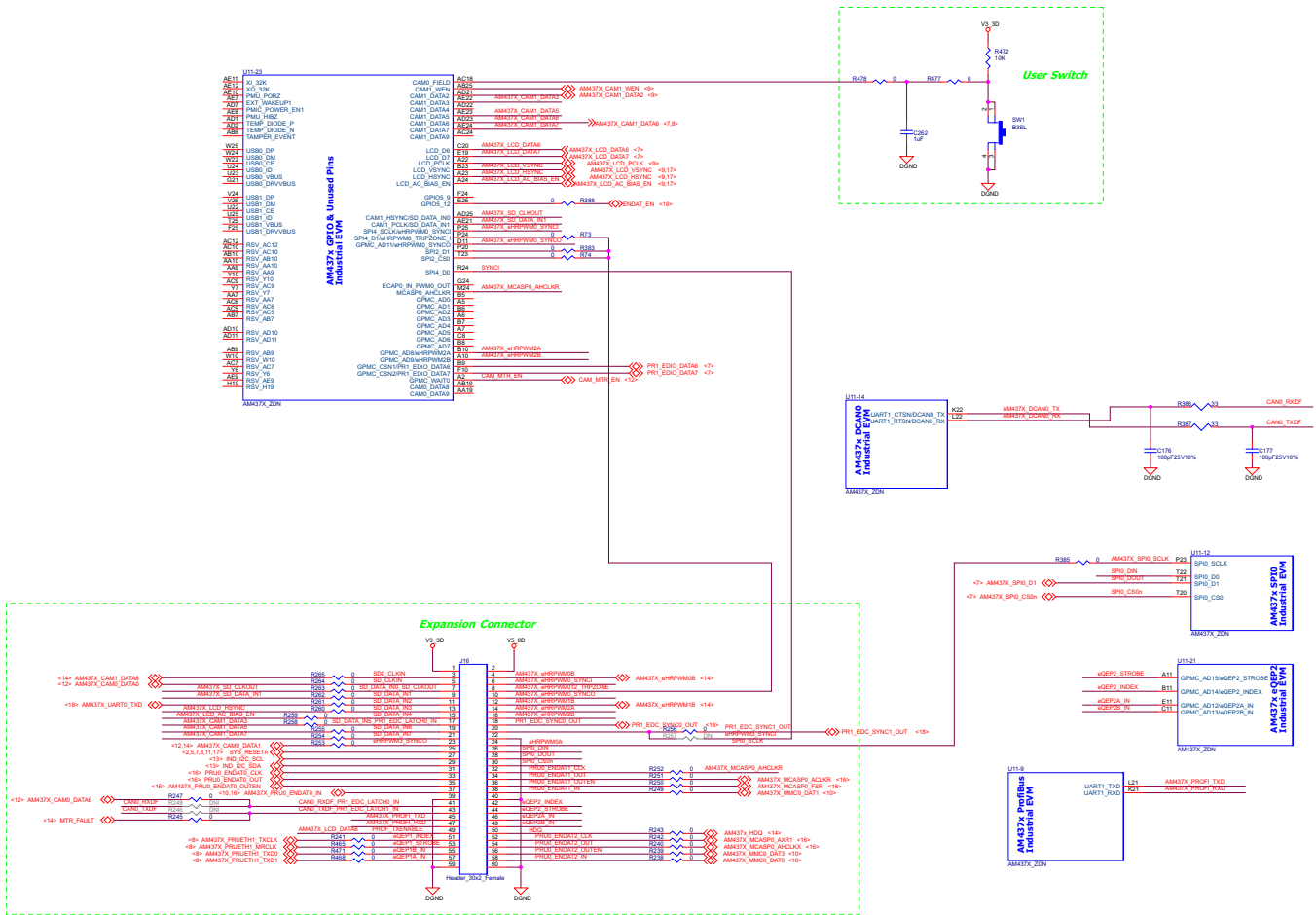


Figure 29. USB JTAG Schematic



7.3 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDEP0039](#).

7.4 PCB Layout

To download the layer plots, see the design files at [TIDEP0039](#).

7.5 Gerber Files

To download the Gerber files, see the design files at [TIDEP0039](#).

8 Software Files

To download the software files, see the design files at [TIDEP0039](#).

9 References

1. Texas Instruments, *AM437x Sitara™ Processors*, AM4379 Datasheet ([SPRS851](#))
2. Texas Instruments, *AM437x ARM® Cortex™-A9 Processors*, AM4379 Technical Reference Manual ([SPRUHL7](#))
3. Texas Instruments, *TLK10xL Industrial Temp, Single Port 10/100Mbps Ethernet Physical Layer Transceiver*, TLK105L Datasheet ([SLLSEE3](#))

10 Terminology

ICSS— Industrial Communication Subsystem

MII— Media Independent Interface

PLC— Programmable Logic Controller

PRU— Programmable Real-time Unit

RTOS— Real-time Operating System

SoC— System-on-chip

TRM— Technical Reference Manual

11 About the Author

THOMAS MAUER is a System Applications Engineer in the Factory Automation and Control Team at Texas Instruments Freising, where he is responsible for developing reference design solutions for the industrial segment. Thomas brings to this role his extensive experience in industrial communications like Industrial Ethernet, fieldbuses, and industrial applications. Thomas earned his electrical engineering degree (Dipl. Ing. (FH)) at the University of Applied Sciences in Wiesbaden, Germany.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer's systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER'S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer's safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have **not** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.