TI Designs: TIDA-00454
AC Voltage and Current Transducer With DC Analog Outputs and Digital Output Drivers

TEXAS INSTRUMENTS

Description

This TI design demonstrates using the MSP430F67791A MCU to accurately measure voltages and currents. This design also demonstrates two dc analog output channels, which can be selected to provide voltage output (±10 V) or current output (±24 mA). The design has a provision for six digital output drivers that are used to drive relays. The functionality of the design can be extended for power measurement. One advantage of this design is that it is a complete subsystem for measuring voltages and currents that also provides a dc analog output proportional to the ac voltage or current used in ac transducer applications. Another advantage of this design is the bidirectional dc analog output.

Resources

TIDA-00454	Tool Folder Containing Design Files
CSD17571Q2	Product Folder
DAC8563, DAC8771	Product Folder
ISO7341FC	Product Folder
ISO7741, ISO7841	Product Folder
MSP430F67791A	Product Folder
TPL7407L	Product Folder
TPS7A4201, TPS7A65-Q1	Product Folder
TVS3300, XTR300	Product Folder

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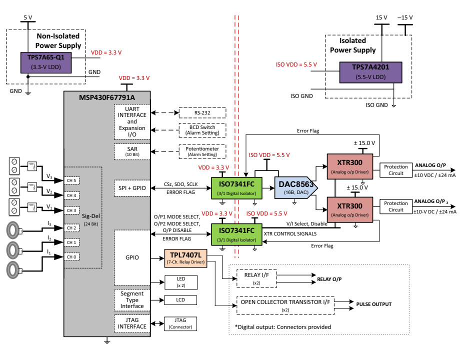
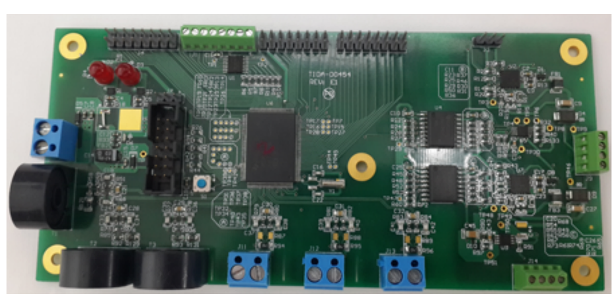
Features

- MSP430F67791A System-on-Chip (SOC) With Six Simultaneous Delta-Sigma ADCs for Measurement of Three-Phase Voltages and Currents
- Isolated, Selectable Bidirectional DC Analog Voltage or Current Outputs ±10-V DC or ±24 mA Based on Dual Output, 16-Bit DAC8563, XTR300, and ISO7341FC
- Six Open Collector Outputs to Drive Relays for Alarms or Optocouplers for Pulse Output
- AC Input Voltage Measurement Range: 10% to 120% of Rated Voltage (230 V)
- AC Input Current Measurement Range: 5% to 200% of Rated Current (5 A)
- AC Input Measurement Accuracy < ±0.5% and DC Output Accuracy < ±0.2% of Full Scale
- DC Analog Output Response Time ≈ 1000 ms
- Provides Expansion Options for Segment LCD Interface, UART Interface, and BCD Switch Interface
- Onboard Current Transformers and Potential Dividers Provided for Direct Measurement of Voltages and Currents

Applications

- Transducer
- Power Quality Meter
- Electricity Meter
- Remote Monitoring and Telemetering





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1 System Description

This TI Design showcases some of the some of the key subsystems that are used in the design of an ac transducer. Some of the key transducer subsystems addressed in this design include a measurement block used for the measurement of ac voltages and currents; a dc analog output block used to communicate the computed voltage, current, frequency, and phase-angle information to a centralized system for analysis; and a digital output block for control and indication, based on the measured parameters during overload or fault conditions. This TI design has the following blocks:

Measurement Block: The measurement block consists of an MCU with a 24-Bit ADC to measure three phase voltages and currents. The voltages are measured using potential dividers, and the currents are measured using current transformers. The MCU computes the voltage and current inputs and computes electrical parameters used for monitoring of the loads.

Data Interface Block: The measured parameters are communicated to remote terminal units or data loggers using different interfaces including RS485, RS232, Wi-Fi, LPRF, or dc analog output. This TI Design showcases interfacing the transducer to remote terminal units using dc analog output. The output can be voltage or current. The output can be programmed for unidirectional output or bidirectional output. The bidirectional output is important to convey the electric parameters with direction. The dc analog output is isolated from the host processing unit for safety. Digital Isolators with low power consumption and enhanced reliability are used against conventional optocouplers.

Digital Output Block: Additional functionalities can be included for protection and monitoring purposes, and one of the functions that can be implemented in a transducer is digital output. The digital output can be used to protect the loads during overloading or used as alarms during the operation of the loads. The above discussed subsystems can be used on the following end equipment:

- *AC Transducer*: Monitoring of the critical loads is an important factor for increasing power-system efficiency and reducing downtime. One simple way to monitor these loads is by using transducers. Transducers monitor different electrical parameters and report those parameters to a monitoring system digitally using an RS-485 communication interface or by using dc analog outputs, which can be current or voltage. An ac transducer measures a wide range of input currents and voltages and has dc analog outputs, digital outputs, and light-emitting diodes (LEDs) to indicate the status.
- *Power Quality Meter (PQM)*: A PQM is an ideal choice when continuous monitoring of a three-phase system is required. It provides metering for current, voltage, real and reactive power, energy use, cost of power, power factor, and frequency. Programmable set points and assignable output relays allow control functions to be added for specific applications. This includes basic alarm on over- or undercurrent or -voltage, unbalance, demand-based load shedding, and capacitor power-factor-correction control. More complex control is possible using the four switch inputs which also can be used for status such as breaker open or closed, flow information. and so forth.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Current inputs (with current transformer (CT))	Three inputs that measure up to 10 A rms without saturation	See Section 2.4.1.
Voltage inputs (with potential divider)	Three inputs that measure up to 270 V rms	See Section 2.4.1.
Input frequency	50 Hz or 60 Hz	See Section 2.4.1.
Current measurement accuracy (calibrated)	< ±0.5%, for 5% to 200% of rated current (I_n = 5 A)	See Section 2.4.1.
Voltage measurement accuracy (calibrated)	< ±0.5%, for 10% to 120% of rated voltage (U_n = 230 V)	See Section 2.4.1.
ADC	Six, 24-bit resolution, ΔΣ with differential inputs	See Section 2.4.4.
DC analog (transducer) output	Two, configurable as voltage or current	See Section 2.4.2.
DC current output	±24 mA (±20 mA with overload capability of 20%)	See Section 2.4.2.
DC voltage output	±10 V	See Section 2.4.2.
DC output accuracy	< ±0.2% full-scale range (FSR) at the reference temperature	See Section 2.4.2.
DAC and output driver	16-bit resolution with serial peripheral interface (SPI) and with default output set to mid-scale, power on reset to mid-scale	See Section 2.4.2.
Digital output driver	Six, open drain (maximum 30-V dc)	See Section 2.4.3.
External dc power supply input	Isolated 15 V and −15 V, non-isolated 5-V dc	See Section 2.4.5.

2 System Overview

2.1 Block Diagram

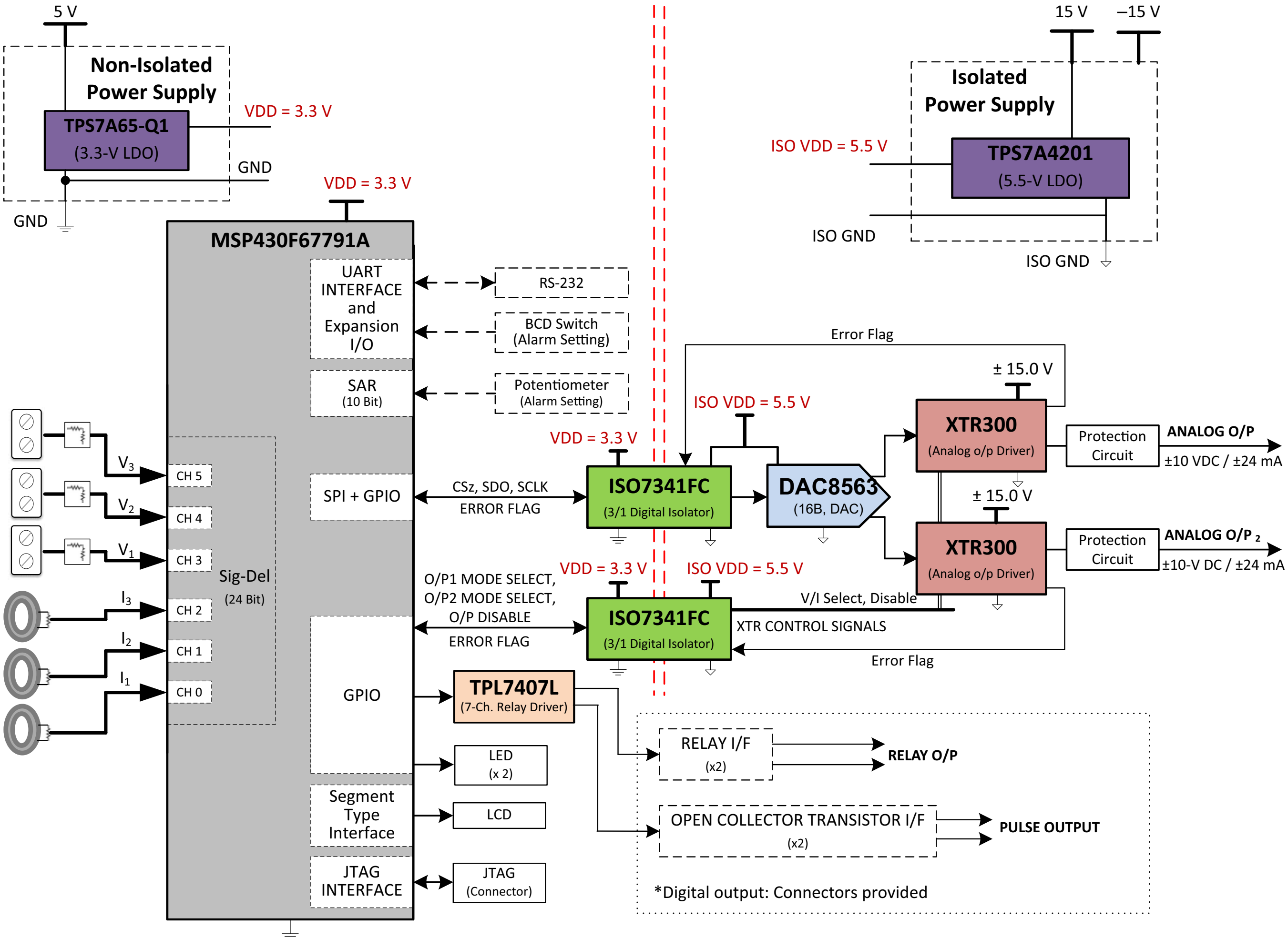

Figure 1. TIDA-00454 Functional Block Diagram

2.2 Design Considerations

Some of the key considerations during the design of TIDA-00454 include:

- ADC to use for measurement : External or Internal to MCU, SAR or delta-sigma, 16-bit or 24-bit
- DC analog output: Isolation – digital or optocoupler, basic isolation or reinforced isolation, channel-channel isolation or group isolation, DAC with external voltage or current driver or DAC with internal voltage or current output
- Interface to DAC: Serial interface – I^2C or SPI
- ADC sampling rate and DAC data-refresh rate
- Relay output with zero-cross reference

2.3 Highlighted Products

2.3.1 DAC8563—16-Bit, Dual-Voltage Output DAC

The DAC8563 device is a low-power, voltage-output, dual-channel, 16-bit DAC. This device includes a 2.5-V, 4-ppm/°C internal reference, which provides a full-scale output voltage range of 5 V. The internal reference has an initial accuracy of ±5 mV and can source or sink up to 20 mA at the V_{REFIN} / V_{REFOUT} pin.

The DAC8563 is monotonic, providing excellent linearity and minimizing undesired code-to-code transient voltages (or glitches). The DAC8563 device uses a versatile three-wire serial interface that operates at clock rates up to 50 MHz. The interface is compatible with standard serial peripheral interfaces (SPIs), quad-serial peripheral interfaces (QSPIs), and digital signal processor (DSP) interfaces. The DAC8563 device incorporates a power-on-reset circuit that ensures the DAC output powers up and remains at mid-scale until a valid code is written to the device. This device contains a power-down feature that reduces current consumption to typically 550 nA at 5 V. The low power consumption, internal reference, and small footprint makes this device ideal for portable, battery-operated equipment. Figure 2 shows the DAC856x functional block diagram.

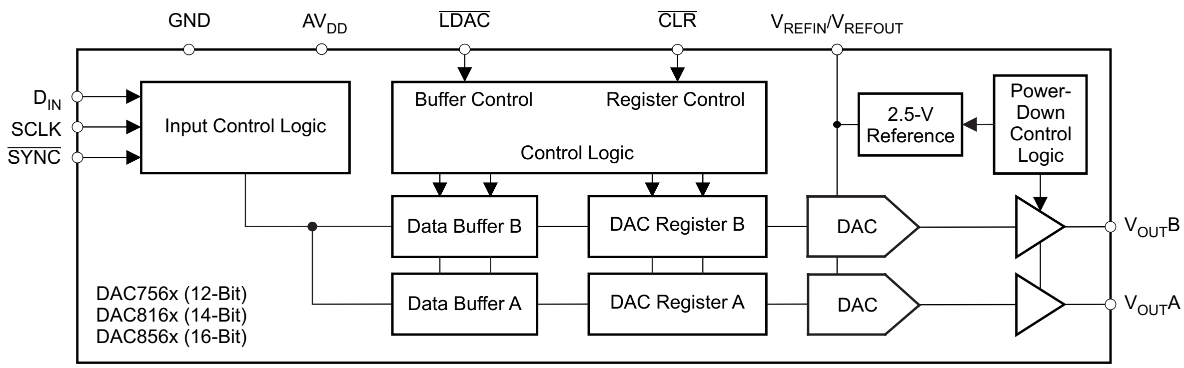

Figure 2. DAC856x Functional Block Diagram

Key features:

- Relative accuracy: DAC8563 (16-bit), 4 least significant bit (LSB) INL
- Wide power-supply range: 2.7 V to 5.5 V
- LDAC and CLR functions
- Output buffer with rail-to-rail operation
- Packages: WSON-10 (3 mm × 3 mm), VSSOP-10
- Temperature range: –40°C to 125°C

2.3.2 XTR300—Industrial Analog Current and Voltage Output Driver

The XTR300 device is a complete output driver for industrial and process control applications. The output can be configured as current or voltage by the digital I/V select pin. No external shunt resistor is required. Only external gain-setting resistors and a loop compensation capacitor are required.

The separate driver and receiver channels of the XTR300 driver provide flexibility. The instrumentation amplifier (IA) can be used for remote voltage sense or as a high-voltage, high-impedance measurement channel. In voltage output mode, a copy of the output current is provided, allowing calculation of the load resistance.

The output selection capability, together with the error flags and monitor pins, make remote configuration and troubleshooting possible. Fault conditions on the output and on the IA input (as well as overtemperature conditions) are indicated by the error flags. The monitoring pins provide continuous feedback of the load power or impedance. For additional protection, the maximum output current is limited and thermal protection is provided.

The XTR300 device is specified over the −40°C to 85°C industrial temperature range and for supply voltages up to 40 V. The XTR300 device is available in a QFN-20 package. Figure 3 shows the XTR300 functional block diagram.

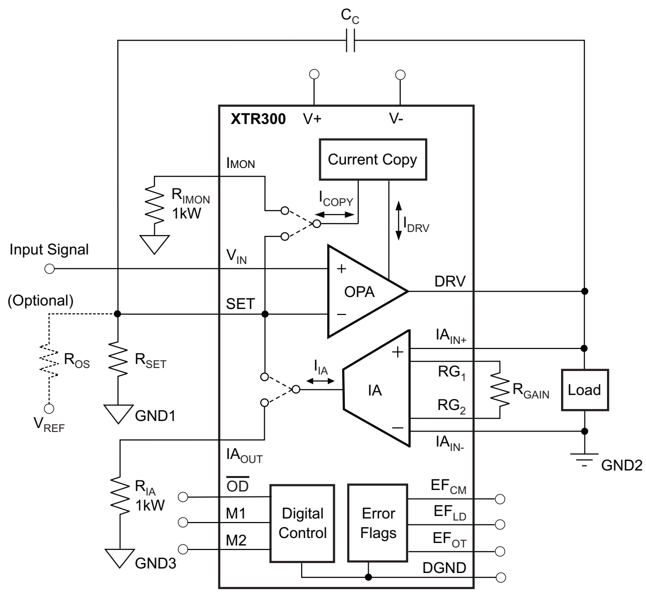

Figure 3. XTR300 Functional Block Diagram

Key features:

- User selectable: voltage or current output
- 40-V supply voltage
- V_{OUT}: ±10 V (up to ±17.5 V at ±20-V supply)
- I_{OUT}: ±20 mA (linear up to ±24 mA)
- Short- or open-circuit fault indicator pin
- No current shunt required
- Output disable for single input mode
- Thermal protection
- Overcurrent protection
- Separate driver and receiver channels

2.3.3 MSP430F67791A—Mixed Signal Microcontroller

The Texas Instruments MSP430F67xx1A family of polyphase-metering system on chips (SoCs) are powerful, highly-integrated solutions for revenue meters that offer accuracy and a low-system cost with few external components. The MSP430F67xx1A family of devices use the low-power MSP430™ MCU from TI with a 32-bit multiplier to perform all energy calculations, metering applications (such as tariff rate management), and communications with Automatic Meter Reading (AMR) and Advanced Metering Infrastructure (AMI) modules.

The MSP430F67xx1A features24-bit sigma-delta converter technology from TI. Device family members include up to 512KB of flash, 32KB of RAM, and a liquid-crystal display (LCD) controller with support for up to 320 segments.

The ultralow-power nature of the MSP430F67xx1A family of devices means that the system power supply can be minimized to reduce the overall cost. Low standby power means that backup energy storage can be minimized and critical data can be retained longer in case of a mains power failure.

The MSP430F67xx1A family executes the energy measurement software library from TI, which calculates all the relevant energy and power results. The energy measurement software library is available with the MSP430F67xx1A at no cost. Industry standard development tools and hardware platforms are available to hasten the development of meters that meet all of the American National Standards Institute (ANSI) and International Electrotechnical Commission (IEC) standards, globally.

The TIDA-00454 design utilizes the MSP430F67791A device. For cost optimization, the user can select another MSP430F67xx1A MCU-based device for design requirements such as flash, RAM, and so forth. Figure 4 shows the MSP430F67791A functional block diagram.

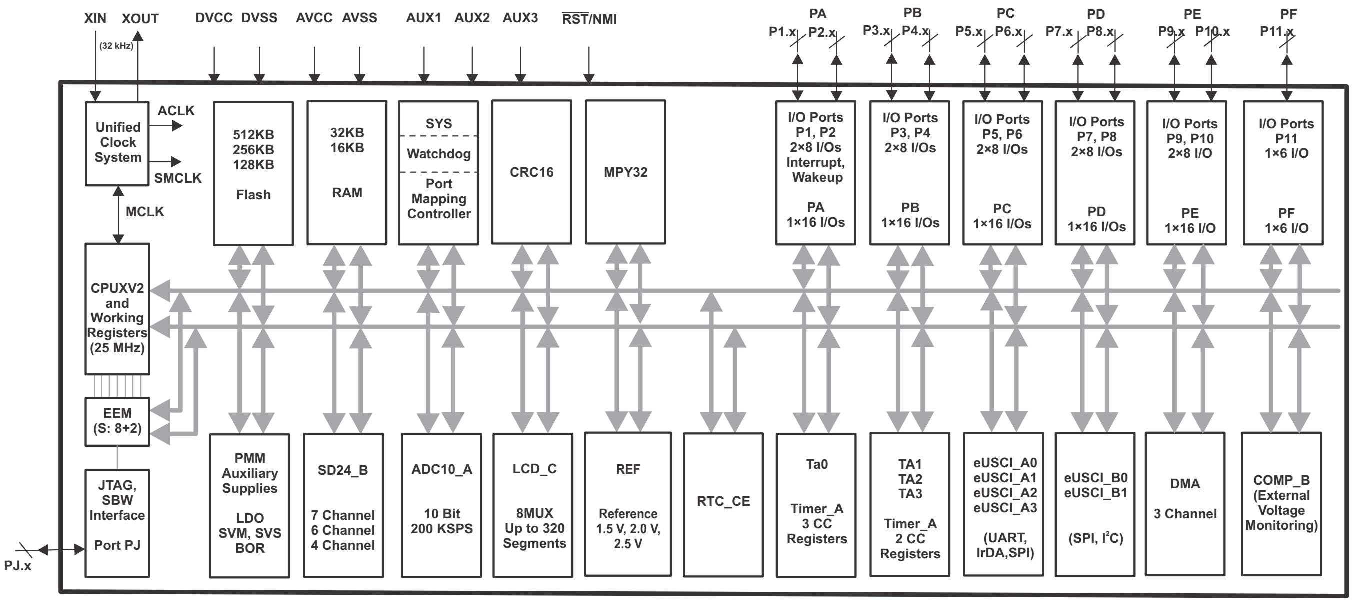

Figure 4. MSP430F67791A Functional Block Diagram

Key features:

- Meets or exceeds ANSI C12.20 and IEC 62053 standards
- Support for multiple sensors such as current transformers, Rogowski coils, or shunts
- Power measurement for up to three phases plus neutral
- Dedicated pulse output pins for active and reactive energy for calibration
- Temperature compensated energy measurements
- Flexible power supply options with automatic switching
- Multiple communication interfaces for smart meter implementations
- High-performance 25-MHz CPU with 32-bit multiplier
- Wide input supply voltage range: 3.6 V down to 1.8 V
- Multiple low-power modes
- Up to 512KB of single-cycle flash
- Up to 32KB of RAM with single-cycle access
- Up to seven independent 24-bit sigma-delta ADCs with differential inputs and variable gain
- Six enhanced communications ports configurable among four universal asynchronous receiver and transmitters (UARTs), six SPI, and two I²C interfaces
- 128-pin LQFP (PEU) package with 90 I/O pins
- Industrial temperature range of –40°C to 85°C
- For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family* user's guide (SLAU208)

2.3.4 ISO7341FC—Quad-Channel 3/1 Digital Isolator

The ISO7341FC digital isolator provides galvanic isolation up to 3000-V RMS for one minute per UL and 4242 VPK per VDE. The ISO7341FC device has four isolated channels comprised of logic input and output buffers separated by a silicon dioxide (SiO2) insulation barrier. The ISO7341FC device has three forward and one reverse-direction channels. The suffix 'F' on the end of "ISO7341FC" indicates that the default output is 'low' to account for input power loss or signal loss, if applicable. Used in conjunction with isolated power supplies, the ISO7341FC device prevents noise current on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The ISO7341FC has an integrated noise filter for harsh industrial environments where short noise pulses may be present at the device input pins. The ISO7341FC device has transistor-transistor logic (TTL) input thresholds and operates from 3- to 5.5-V supply levels (see Figure 5).

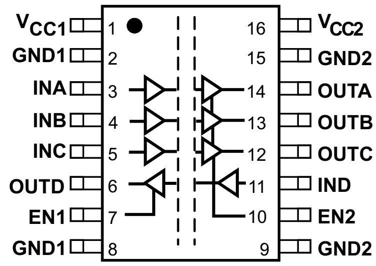

Figure 5. ISO7341FC Pin Configuration and Function

Key features:

- Signaling rate: 25 Mbps
- Integrated noise filter on the inputs
- Low-power consumption, typical ICC per channel at 1 Mbps:
  - 1.2 mA (5-V supplies),
  - 0.9 mA (3.3-V supplies)
- Low propagation delay: 31 ns
- 3.3- and 5-V level translation
- Wide temperature range: –40°C to 125°C
- 70-kV/µs transient immunity
- Robust electromagnetic compatibility (EMC)
- Operates from 3.3- and 5-V supplies
- Wide body SOIC-16 package
- Safety and regulatory approvals:
  - 4242-V_{PK} basic isolation per DIN V VDE V0884-10 and DIN EN 61010-1
  - 3-KV_{RMS} isolation for one minute per UL 1577

2.3.5 TPL7407L—40-V, Seven-Channel NMOS Array, Low-Side Driver

The TPL7407L is a high-voltage, high-current NMOS transistor array. This device consists of seven NMOS transistors that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The maximum drain-current rating of a single NMOS channel is 600 mA. The user can set the transistors as parallel for higher-current capability.

The key benefit of the TPL7407L is its improved power efficiency and lower leakage than a bipolar Darlington implementation. With the lower VOL, the user dissipates less than half the power of traditional relay drivers with currents less than 250 mA per channel.

Figure 6 shows the TPL7407L functional block diagram.

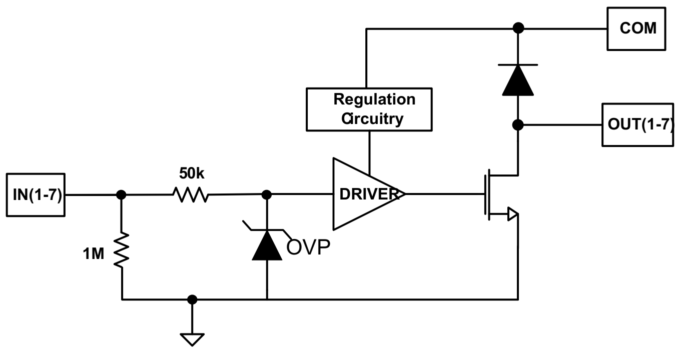

Figure 6. TPL7407L Functional Block Diagram

Key features:

- Very low output leakage < 10 nA per channel
- Extended ambient temperature range: T_A = –40°C to 125°C
- High-voltage outputs 40 V
- Compatible with 1.8- to 5.0-V MCUs and logic interface
- Internal free-wheeling diodes for inductive kick-back protection
- Input pulldown resistors allows tri-stating the input driver
- Input RC-snubber to eliminate spurious operation in noisy environments
- Inductive load driver applications
- ESD protection exceeds JESD 22
- 2-kV HBM, 500-V CDM
- Available in 16-pin SOIC and TSSOP packages

2.3.6 TPS7A4201—Low-Dropout Linear Regulator

The TPS7A42 is a very high, voltage-tolerant linear regulator that offers the benefits of a thermally-enhanced package (MSOP-8) and is able to withstand continuous dc or transient input voltages of up to 28 V.

The TPS7A42 device is stable with any output capacitance greater than 4.7 µF and any input capacitance greater than 1 µF (overtemperature and tolerance). Therefore, implementations of this device require minimal board space because of its miniaturized packaging (MSOP-8) and a potentially small output capacitor. In addition, the TPS7A42 device offers an enable pin (EN) compatible with standard CMOS logic to enable a low-current shutdown mode.

In addition, the TPS7A42 device is ideal for generating a low-voltage supply from intermediate voltage rails in telecom and industrial applications. The linear regulator can not only supply a well-regulated voltage rail, but the regulator can also withstand and maintain regulation during fast voltage transients. These features translate to simpler and more cost-effective electrical surge-protection circuitry for a wide range of applications (see Figure 7).

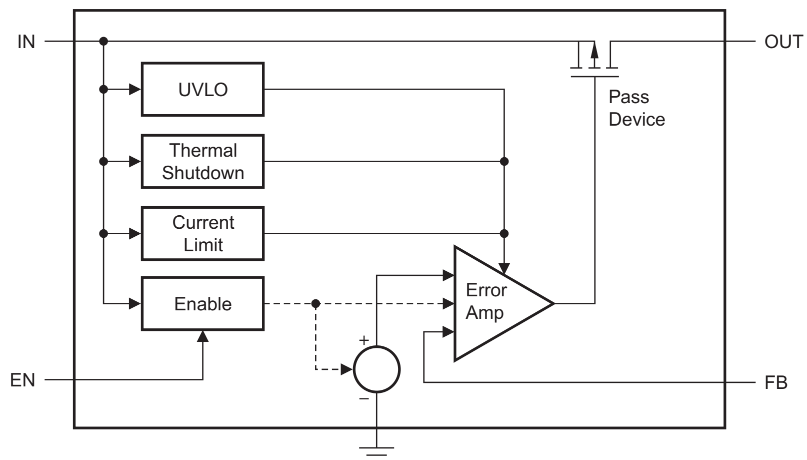

Figure 7. TPS7A42 Functional Block Diagram

Key features:

- Wide input voltage range: 7 V to 28 V
- Accuracy:
  - Nominal: 1%
  - Over line, load, and temperature: 2.5%
- Low quiescent current: 25 µA
- Quiescent current at shutdown: 4.1 µA
- Maximum output current: 50 mA
- Adjustable output voltage: approximately 1.175 V to 26 V
- Dropout voltage: 290 mV
- Built-in current-limit and thermal shutdown protection
- Package: high thermal performance MSOP-8 TI PowerPAD™ integrated circuit package
- Operating temperature range: –40°C to 125°C

2.3.7 TPS7A65-Q1—LDO With Ultralow Quiescent Current

The TPS7A65-Q1 device is a low-dropout linear voltage regulator designed for low-power consumption and quiescent current less than 25 µA in light-load applications. This device features integrated overcurrent protection and a design to achieve stable operation even with low-equivalent series resistance (ESR) ceramic output capacitors. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the requirement of using a boost converter during cold crank conditions. Because of these features, this device is well-suited in power supplies used for various automotive applications.

The TPS7A65-Q1 device is available in a thermally-enhanced power package (three-pin TO-252) and is specified for operation at temperatures from –40°C to 150°C (see Figure 8).

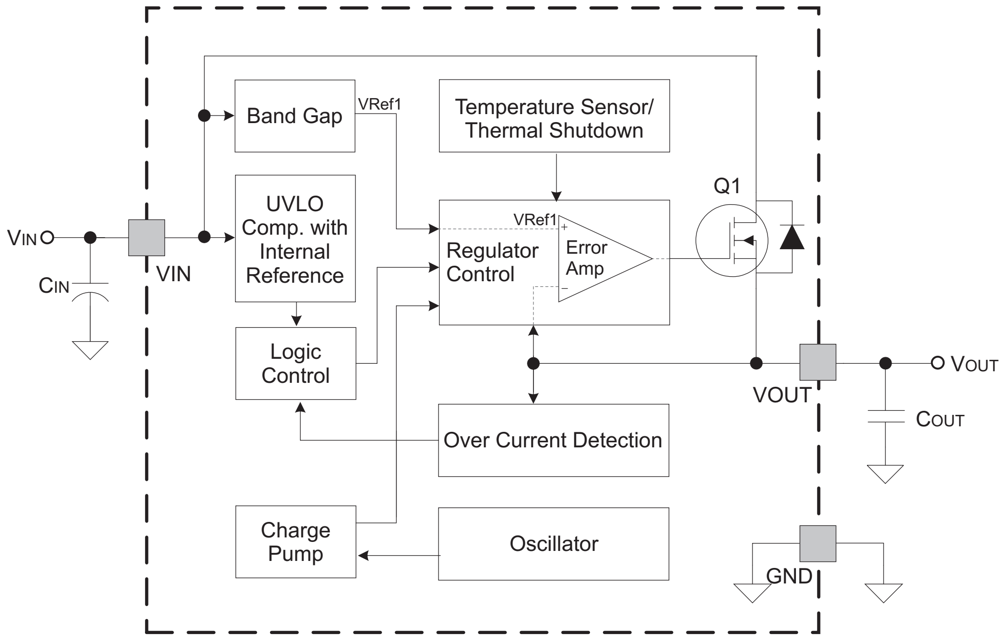

Figure 8. TPS7A65-Q1 Functional Block Diagram

Key features:

- LDO 300 mV at I_{OUT} = 150 mA
- 4- to 40-V wide input voltage range with up to 45-V transients
- 300-mA maximum output current
- 3.3-V fixed output voltage with ±2% tolerance
- Low-ESR ceramic output stability capacitor
- Integrated fault protection
  - Short-circuit and overcurrent protection
  - Thermal shutdown
- Low input-voltage tracking

2.3.8 Enhancements

The following section provides details of some of the enhancements that can be made to the TIDA-00454, including some of the TI Designs that can be leveraged.

2.3.8.1 Analog Output Design Using DAC With Integrated Programmable Current Output and Voltage Output

An alternative approach to the DAC8563 device (dual, low-power, ultralow glitch, buffered-voltage-output DAC with 2.5-V, 4ppm/°C reference) plus external XTR300 device (industrial analog current- or voltage-output driver) is to use the DAC8775 or DAC8771 device, described in the following table.

Table 2. 16-Bit DAC Selection Table

DEVICE	DESCRIPTION
DAC8771[(1)]	Single-channel 16-bit voltage- and current-output DAC with adaptive power management.
DAC8775[(2)]	16-bit quad-channel programmable current-output and voltage-output digital-to-analog converter (DAC)

(1) The DAC8771 device is used in channel-to-channel isolation applications. See DAC8771 for more details.
(2) The DAC875 device is used in group isolation applications. See DAC8775 for more details.

See the following designs based on the DAC8771 and DAC8775 devices for more details.

- *Quad-Channel Industrial Voltage and Current Output Driver Reference Design (EMC/EMI Tested)*
- *Less Than 1-W, Quad-Channel, Analog Output Module With Adaptive Power Management Reference Design*
- *Reference Design for Power-Isolated Ultra-Compact Analog Output ModuleReference Design for Power-Isolated Ultra-Compact Analog Output Module*

2.3.8.2 Digital Isolator for Isolated Analog Output Interface

There are different families of digital isolators that can be considered including digital isolators with:

- Basic or reinforced isolation
- Lower power consumption or fail-safe options

The following table provides details of different isolators that can be considered.

Table 3. Digital Isolator Selection Table

DEVICE	DESCRIPTION
ISO7841	High-Immunity, 5.7-kV rms reinforced quad-channel 3/1 digital isolator, 100 Mbps
ISO7741	High-speed, low-power, robust EMC quad-channel digital isolator
ISO7341FC	Robust EMC, low-power, quad-channel 3/1 digital isolator, fail-safe low
ISO7641FM	6-kV peak, low-power, quad-channel, 150-Mbps digital isolator
ISO7641FC	4-kV peak, low-power, quad-channel, 25-Mbps digital isolator

See the following designs for more details.

- *Reference Design for Power-Isolated Ultra-Compact Analog Output Module*
- *Isolated, Transformerless, Bipolar Supply for 24-Bit ADCs Reference Design*
- *Isolated 16-Channel AC Analog Input Module Reference Design Using Dual Simultaneously Sampled ADCs*
- *RS-232 Modem Interface Module for Protection Relay, IED, and Substation Automation Reference Design*

2.3.8.3 Adding a Communication Interface

The transducers are monitored by the remote terminal units using dc analog output or an RS-485 interface. The RS-485 communication interface is an isolated RS-485 interface. The digital isolators can be chosen with integrated power or with an external isolated power supply. TI provides a large portfolio of RS-485 transceivers that can be considered for implementing an RS-485 interface. The RS-485 interface can be half-duplex or full-duplex.The following table provides details of some of the common devices that can be used for an isolated RS-485 interface.

Table 4. RS-485 Transceiver Selection and Digital Isolator Selection

DEVICE	DESCRIPTION
SN65HVD3082	Half-duplex RS-485 transceiver
SN65HVD82	5V-supply RS-485 with IEC ESD protection
SN65LBC184	RS-485 transceiver with integrated transient voltage suppression
THVD1500	5-V RS-485 transceivers up to 300 kbps with ±8 kV IEC ESD protection
ISO7742	High-speed, low-power, robust EMC quad-channel digital isolator
ISOW7842	High-efficiency, low-emissions, reinforced digital isolator with integrated power

See the following designs for more details.

- *Isolated Power Supplies Reference Design*
- *Isolated Auto-Polarity RS-485 Transceiver Reference Design*
- *Dual Isolated Half-Duplex RS-485 Repeater Reference Design*
- *Fly-Buck Bias Solution for MCU and RS-485*
- RS-485 Automatic Direction Control Reference Design
- *Small Form Factor, Half-Duplex With Isolated & Non-Isolated RS485 Interface Reference Design*
- *Communication Module Reference Design for Functional Isolated RS-485, CAN and I2C Data Transmission*
- *Data Collector With M-Bus And RS-485 Protocol Conversion Reference Design*
- *Isolated RS-485 With Integrated Signal and Power Reference Design*

2.3.8.4 Generation of Bipolar ±15-V DC Supply

The dc analog output can be a voltage output up to ±12 V or current output up to ±24 mA and needs a ±15 V supply for generation of these outputs. There are multiple approaches to generation of the required dual power supply.

Table 5. DC-DC Converter and LDO Selection

DEVICE	DESCRIPTION
LM5017	7.5-V–100-V wide-Vin, 600-mA constant on-time synchronous buck regulator
LM5160	LM5160 wide-input, 65-V, 2-A synchronous buck / Fly-Buck™ converter
TPS65130	Split-rail converter with dual, positive and negative outputs (300 mA typ)
TPS7A39	Dual, 150-mA, wide-Vin, positive and negative low-dropout (LDO) voltage regulator

See the following designs for more details.

- *Isolated Power Supply for Programmable Logic Controller (PLC) IO Modules Reference Design*
- *Small Footprint Isolated DC/DC Converter for Analog Input Module Reference Design*
- *High Accuracy Analog Front End Using 16-Bit SAR ADC with ±10V Measurement Range Reference Design*

2.3.8.5 DC Analog Output-Transient Protection

The dc analog output is subjected to transients when exposed to harsh environments and must be protected. A transient-voltage suppressor (TVS) is used to protect the output against transients. The design calculations and testing are simplified by using a flat-clamp TVS, and the following table provides a list of TVSs that can be considered based on the application. The TVS can be used for overload protection, replacing DESD1P0RFW-7 in Figure 12 and Figure 43, and Zener SMBJ5929BE3/TR13 in Figure 19 and Figure 41.

Table 6. I/O TVS Selection

DEVICE	DESCRIPTION
TVS3300	33-V flat-clamp TVS
TVS2700	27-V flat-clamp TVS
TVS2200	22-V flat-clamp TVS
TVS1800	18-V flat-clamp TVS

2.3.8.6 On-Board Diagnostics

The transducer is installed near to a primary equipment like transformer, generator or motor and is exposed to a harsh environment including temperature and transients. The transducer must operate under a high-noise or -temperature environment. Temperature sensors can be used for diagnostics of failures. The following table provides a list of temperature sensors that can be considered.

Table 7. Analog or Digital Temperature Selection

DEVICE	DESCRIPTION
LM75	±2°C industry-standard temperature sensor with I^2C or SMBus interface
LMT87	2.7-V-capable, 10-µA, analog-output temperature sensor in SC70 and TO-9
TMP102	1.4-V-capable temperature sensor with I^2C or SMBus interface and alert function in SOT-563
LMT84	1.5-V-capable, 10-µA, analog-output temperature sensor in SC70 and TO-92
HDC2010	Low-power humidity and temperature digital sensor

On-board voltage supervisors can be used to ensure the system operates safely under harsh operating conditions. The following table provides a list of voltage supervisors that can be considered.

Table 8. On-Board Voltage Supervisor

DEVICE	DESCRIPTION
TPS3823	Supply voltage supervisor with watchdog input and manual reset
TPS3839	Ultralow-power supply-voltage supervisor
TPS3809	3-pin supply-voltage supervisor
TLV809	3-pin supply-voltage supervisor with active-low, push-pull output

2.4 System Design Theory

2.4.1 AC Input

2.4.1.1 Current Measurement

Three current input channels are available on the TIDA-00454 board. The CT burden depends on the current transformer selected and the current input range that is expected to be measured.

The filter circuit consisting of resistors and capacitors follows the burden resistor.

Equation 1 shows that the secondary current (I_{SEC}) can be calculated as:

$I_{SEC} = (N_{PRI} / N_{SEC}) \times I_{PRI}$

where

- I_{SEC} = Secondary current
- N_{PRI} = Primary winding number of turns
- N_{SEC} = Secondary winding number of turns
- I_{PRI} = Primary current (1)

The CT used in the TIDA-00454 design has 2500 secondary turns where N_{SEC} = 2500 and N_{PRI} = 1.

The voltage across the burden resistor is sensed by the ADC. The input to the MSP430F67791A SD24_B ADC must be less than the differential input range ±919 mV for the entire range of input voltages.

The following Figure 9 shows the current measurement section of the TIDA-00454.

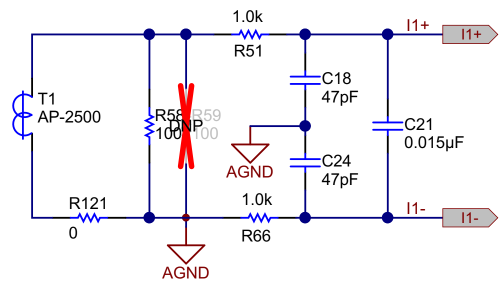

Figure 9. Circuit Diagram of Current Input

This design uses a 100-Ω burden resistor. However, the burden resistor value may vary depending on the CT ratio and the maximum current measurement. To match the required resistance, this design provides two resistors in parallel.

2.4.1.2 Voltage Measurement

The TIDA-00555 design provides three provisions for the voltage channels. The following Figure 10 shows one of the voltage input circuits.

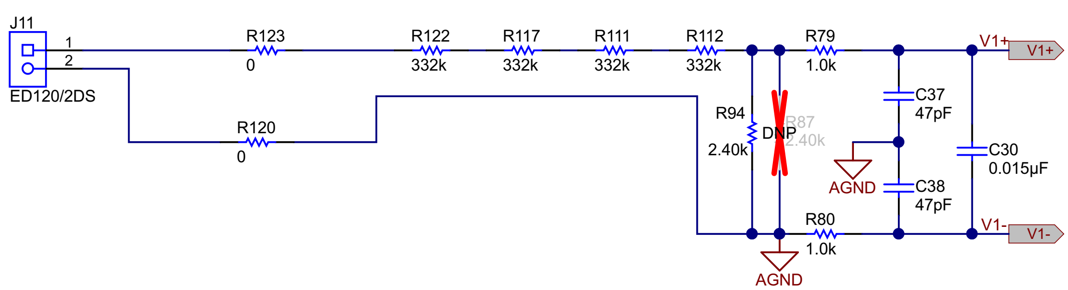

Figure 10. Circuit Diagram of Voltage Input

The voltage divider resistors for the ac input voltage channel is selected to ensure that the input to the MSP430F67791A SD24_B ADC is less than the differential input range (±919 mV) for the entire range of input voltages.

This design uses a 2.4 kΩ for R94.

To meet safety requirements, the input impedance is typically expected to be > 1 MΩ.

So, the divider resistor value, R_{UPPER} = 332 kΩ × 4 = 1.33 MΩ.

The R_{UPPER} is the addition of R122, R117, R111, and R112 (see the preceding Figure 10).

The V_{R94} voltage divider output must be less than the ADC input range of the MSP430F67791A device.

So, the effective range for V_{R94} = 919 mV / 1.414 = 649.9 mV.

Use the following voltage resistor divider calculation for Equation 2:

$$V_{R94} = R_{94} / R_{UPPER} + R_{94}) \times V_{INPUT} \tag{2}$$

Use the preceding Equation 2 to calculate the V_{INPUT}:

V_{INPUT} = 360.8 V

The TIDA-00454 design can measure a maximum input voltage up to 360 V.

2.4.2 DC Analog Output

The analog output circuitry for this two-channel combined voltage and current output driver is realized with a dual output digital-to-analog converter (DAC) and two industrial analog voltage and current output drivers. The integrated output driver allows for digital selection between voltage V_{OUT} or current I_{OUT} modes on a combined output pin, reducing the connector and wiring costs. Digital isolation for the serial peripheral interface (SPI) and general purpose input and output (GPIO) control signals is accomplished using two four-channel digital isolators.

The TIDA-00454 board implements two analog outputs. The voltage and current of any phase can be transmitted as analog outputs.

The firmware is configured to send phase voltage on analog output 0 and the respective phase current on analog output 1.

The user can select a specific phase for analog output based on jumper settings mentioned in Section 3.1.1.1.

2.4.2.1 DAC Interface

The DAC8563 is a 16-bit, dual-channel, rail-to-rail voltage-output DAC with an integrated 2.5-V reference. The DAC8563 device incorporates a power-on-reset circuit that configures the DAC output to mid-scale voltage at power-up, which sets the output of the XTR300 device to 0 V (for voltage output) or 0 mA (for current output) at power up. The MSP430F67791A MCU communicates with the DAC8563 through SPI.

The buffered voltage output DAC is a resistor or ladder-based DAC followed by an output amplifier. Just like any other amplifier, the buffered voltage output DAC has an output voltage swing to rail limitations. If the device is being used in such a way that the full-scale DAC code corresponds to the same voltage as the output amplifier supply voltage, the output voltage swing-to-rail limitation presents an error at full scale. By providing additional head-room to the DACs output amplifier, the user can reduce or completely eliminate the impact of the output voltage swing-to-rail limitation. With gain G = 2 and an internal reference of 2.5 V, the output voltage span is approximately 0 V to 5 V. So, 5.5 V is used as the AVDD for the DAC8563. By providing an additional 500 mV of headroom to the output amplifier, the device is able to swing closer to the rail. This design implements further action to avoid end-point errors by using only a subset of DAC codes.

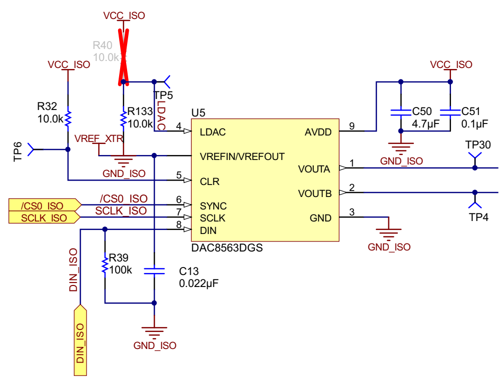

Figure 11. DAC8563 Circuit Diagram

2.4.2.2 DC Analog Output Driver—Current and Voltage

Figure 12 shows the XTR300 device, which is used as an output driver. The XTR300 device is a complete, single-channel output driver for industrial and process control applications. The XTR300 device is capable of sourcing and sinking voltage and current over the standard industrial output ranges that are configured through external gain setting resistors. The output can be configured for I_{OUT} mode or V_{OUT} mode based on a digital control signal.

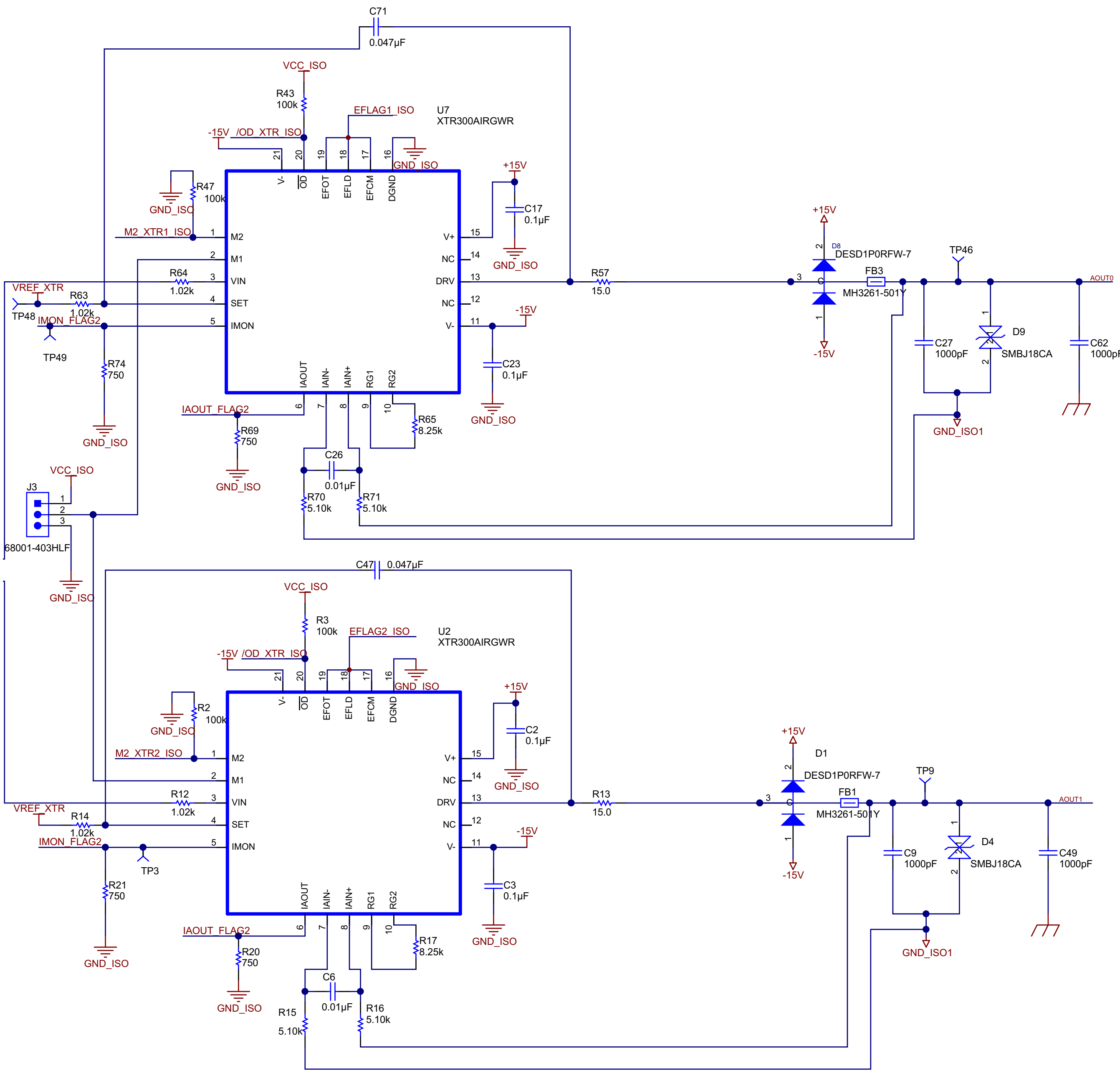

Figure 12. XTR300 Interface

The XTR300 device is configured for ±24 mA or ±10 in this design.

The resistor numbers in the below calculations are for circuits associated with the U7 integrated circuit (IC) in the schematic. The same calculations are valid for circuits associated with the U2 IC in the schematic.

The output current or voltage setting depends on the R63 (SET resistor) and the R65 (gain resistor).

Solve for I_{OUT} mode in the following Equation 3:

$$I_{OUT} = 10 \times (V_{DAC} - V_{REF}) / R63 \tag{3}$$

By rearranging Equation 3 for R63 in Equation 4:

$$R63 = 10 \times (V_{DAC} - V_{REF}) / I_{OUT}$$
$$R63 = 10 \times (4.96\ V - 2.5\ V) / 0.024\ A$$
$$R63 = 1025\ \Omega \tag{4}$$

In this design, a 1.02-kΩ 0.1% tolerance is used for R63.

For the V_{OUT} mode, see Equation 5:

$$V_{OUT} = ((V_{DAC} - V_{REF}) / R63) \times 2 \tag{5}$$

Rearrange Equation 5 for R65 in the following Equation 6:

$$R65 = 2 \times V_{OUT} \times R63 / (V_{DAC} - V_{REF})$$
$$R65 = 2 \times 10\ V \times 1020\ \Omega / (4.96\ V - 2.5\ V)$$
$$R65 = 8292\ \Omega \tag{6}$$

In this design, an 8.25-kΩ 0.1% tolerance is used for R65.

C71 is a compensation capacitor that compensates the control loop for the XTR300 output driver, providing a stable output with output capacitance. The XTR300 datasheet recommends a value of 47 nF, which has been used in this design.

The three open-collector error signals are provided to indicate output related error. These signals include overcurrent or open-load errors (EFLD) that exceed the common-mode input range at the IA inputs (EFCM) and overtemperature warnings (EFOT). Isolated monitoring of the error flags for both XTR300 devices is accomplished in this design by ORing the three open-collector error flags for each XTR300 device and then sending them individually through the digital isolator. Load monitoring is possible in both V_{OUT} mode and I_{OUT} mode using the I_{MON} and I_{AOUT} pins.

See Section 3.1.1.1 to change the analog output to voltage or current mode.

2.4.2.3 Digital Isolators for DC Analog Output Control Signals

The DAC and XTR300 device are isolated from the MCU using digital isolators. The ISO7341FC digital isolator supports data rates up to 25 Mbps with greater than 4 kV of galvanic isolation. To communicate with the DAC, control the XTR300 outputs, and monitor the XTR300 outputs, a total of six outputs and two digital inputs are required. To provide these essential outputs and inputs, two ISO7341FC devices are used and each feature three output channels and one input channel.

The following circuit diagram in Figure 13 shows all eight signals interfacing:

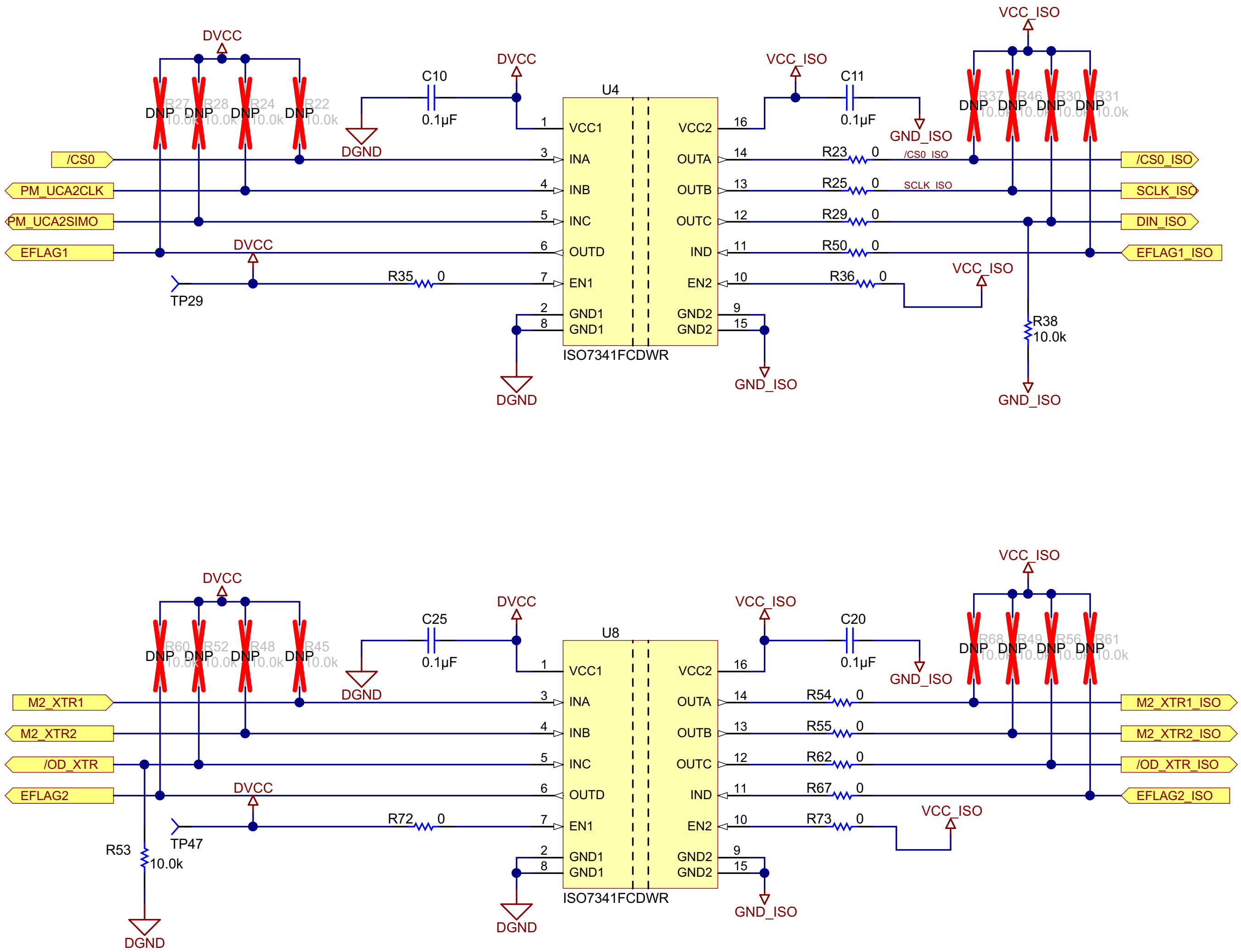

Figure 13. Circuit Diagram of Digital Isolators Interface

The ISO7341FC device provides 4242-V_{PK} basic isolation.

To obtain reinforced isolation, use the ISO7841 device, which provides an 8000-V_{PK} reinforced isolation.

2.4.3 Digital Output Drivers

This TI Design provides six high-current digital output drivers. The design features a TPL7407L low-side relay driver. The key benefit of the TPL7407L relay driver is its improved power efficiency and lower leakage in comparison to a bipolar Darlington implementation. The per channel rated drain current capacity of the TPL7407L device is 600 mA.

The COM pin is the power supply pin of TPL7407L to power the gate drive circuitry. This design ensures a full-drive potential with any GPIO above 1.5 V. The gate drive circuitry is based on low-voltage CMOS transistors that can only handle a max gate voltage of 7 V. An integrated LDO reduces the COM voltage of 8.5 V to 40 V to a regulated voltage of 7 V. Though TI recommends an 8.5-V minimum for V_{COM}, the part still functions with a reduced COM voltage, a reduced gate drive voltage, and a resulting higher Rds_{on}.

To prevent overvoltage on the internal LDO output because of a line transient on the COM pin, the COM pin must be limited to below 3.5 V/µs. TI recommends to use a bypass capacitor that limits the slew rate to below 0.5 V/µs.

The TPL7407L relay driver outputs are controlled by the MSP430F67791A port pins, as the following Figure 14 shows.

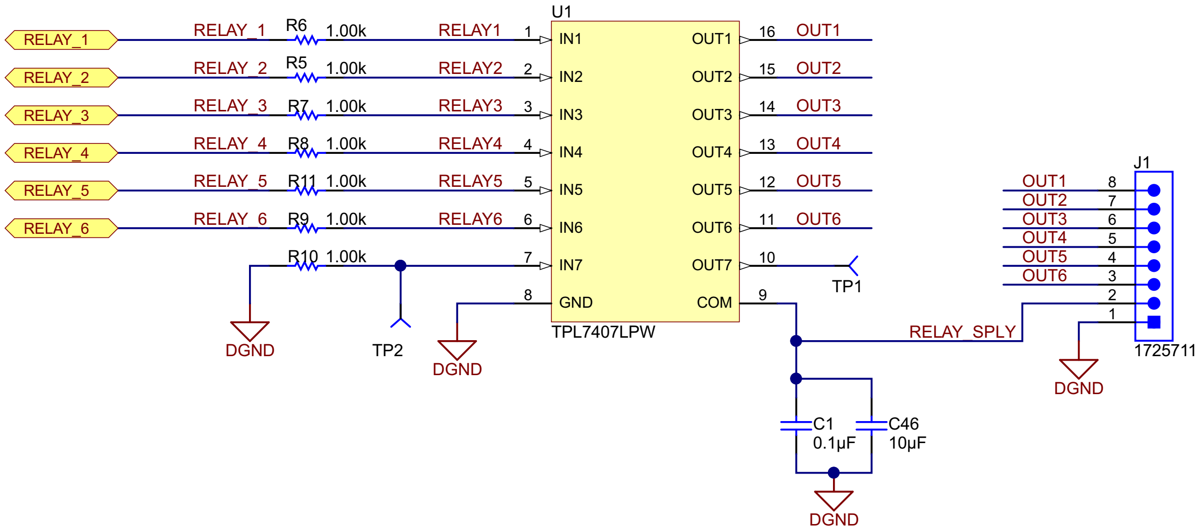

Figure 14. Digital Output Driver Circuit

2.4.4 MCU

2.4.4.1 MCU Interfacing

The TIDA-00454 design interfaces with the MSP430F67791A MCU. The user can interface three current and three voltage channels with the ΣΔ ADC of the MSP430F67791A device. The MSP430F67791A offers up to seven independent 24-bit ΣΔ ADCs with differential inputs and variable gain.

The MCU has a built-in segment liquid-crystal display (LCD) driver and scan interface. Figure 15 shows the MSP430F67791A MCU schematic.

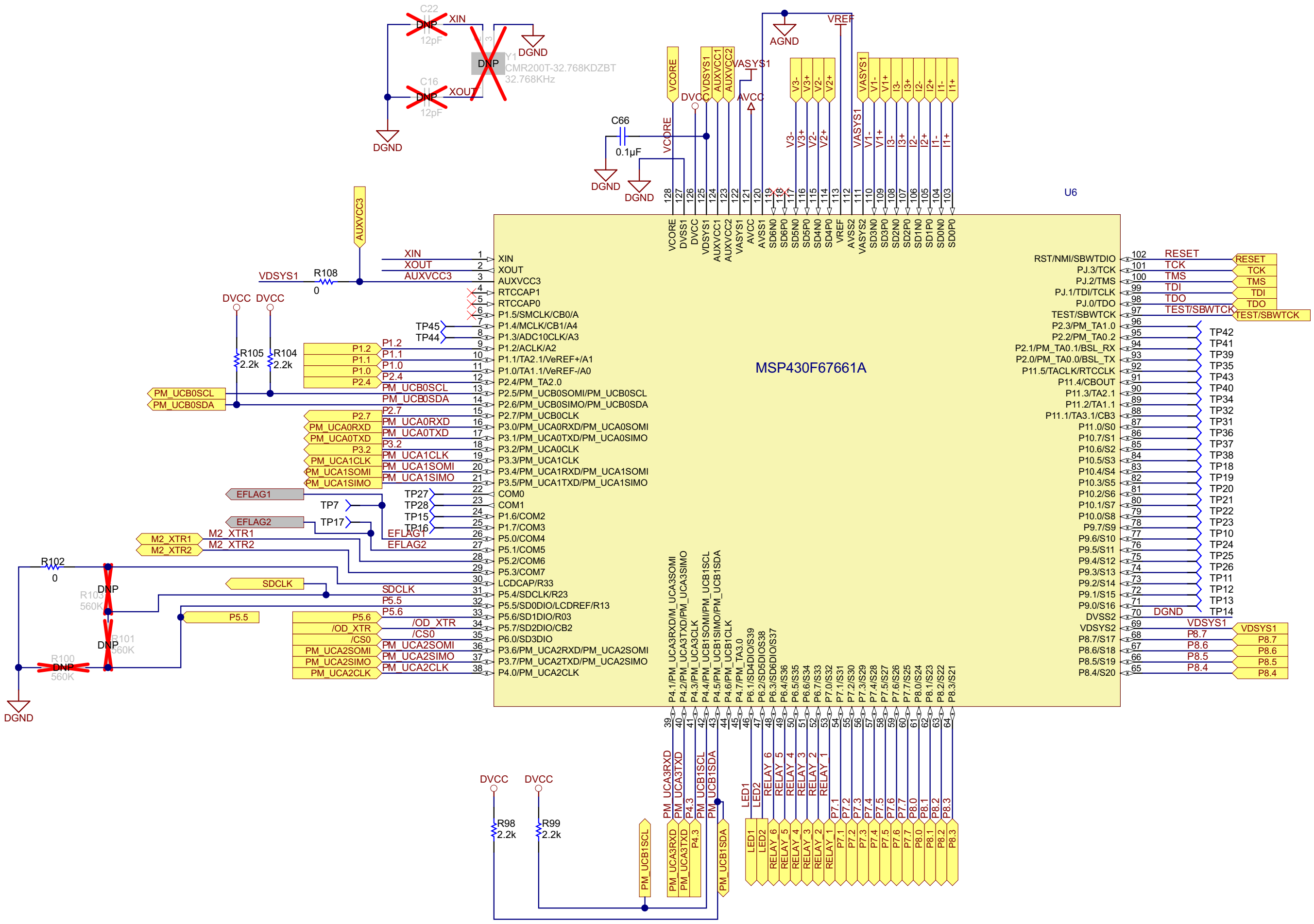

Figure 15. MSP430F67791A MCU Hardware Configuration Schematics

The following list details the different expansion options available in this design:

- SPI: SPI can be used for communication with a graphical user interface (GUI) or other communication unit.
- UART: Implement RS232 communication by connecting the RS232 chip externally to the UART.
- I^{2}C: This design may require to calibrate the inputs based on the accuracy of the sensing devices. In this case, an EEPROM can be connected to the I^{2}C interface to store the calibration values. This I^{2}C interface can be used to interface to the temperature sensor, RTC, or any other I^{2}C interface-based peripherals.
- GPIO: The GPIO inputs can be used as I/O, timer inputs, or pulse width modulation (PWM) outputs. Use these I/Os when feature enhancements are required. Alternatively, the user can use the GPIO for discrete (step) alarm setting. To generate the required steps, a BCD or HEX rotary switch can be used. The output of a BCD or HEX rotary switch can be connected with the GPIO of the MCU.
- ADC: Implement the analog alarm-setting feature by connecting a potentiometer output to the ADC pin of the MCU. The potentiometer output voltage variation must be within the acceptable input voltage range of the specified ADC.

The following Figure 16 shows the expansion interface connectors with the different expansion options discussed in the preceding list.

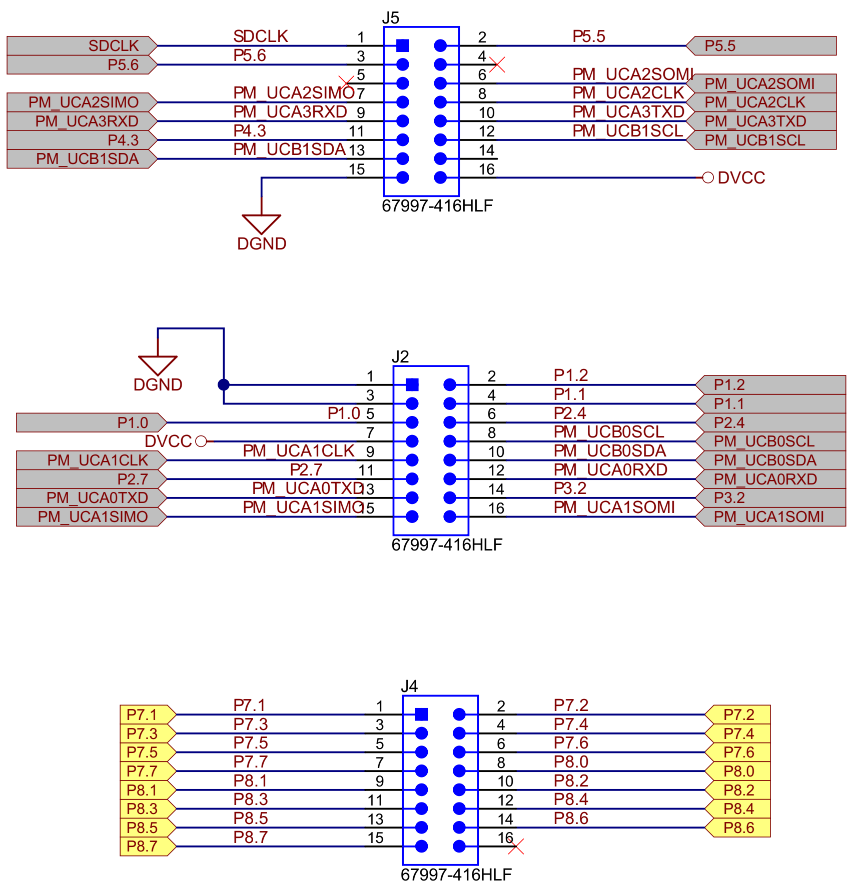

Figure 16. Expansion Interface Connectors

LED indication:

Two LEDs are available on the TIDA-00454 design board. The user can configure both LEDs based on the requirements (see Figure 17).

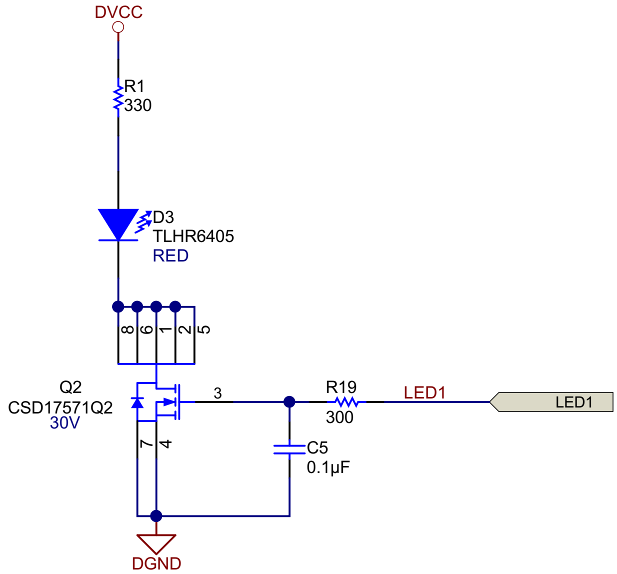

Figure 17. LED Driver Schematic

The LED functionality has been configured as follows:

LED1 – Turned ON when the error flag (EFLAG1) of analog output 0 is observed as low

LED2 – Turned ON when the error flag (EFLAG2) of analog output 1 is observed as low

NOTE: The error flag is active-low.

2.4.4.2 MCU Programming

The TI MSP430™ family of MCUs supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with the GPIO. The TEST/SBWTCK signal is used to enable the JTAG signals. In addition to these signals, the RESET signal is required to interface with the MSP430 development tools and device programmers. Figure 18 shows the JTAG programming connector. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools* User's Guide (SLAU278).

For a complete description of the features of the JTAG interface and its implementation, consult the *MSP430 Programming Via the JTAG Interface* User's Guide (SLAU320).

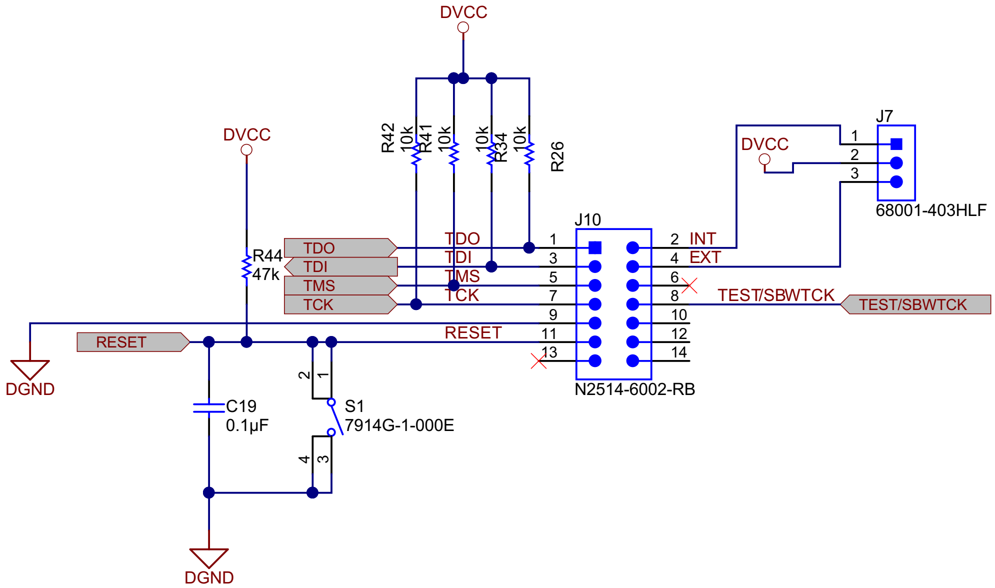

Figure 18. JTAG Programming Connector

2.4.5 Power Supply

2.4.5.1 Isolated Power Supply

The user must connect the external dc supplies 15 V and –15 V on the four-pin terminal block J14 to power the isolated section of the TIDA-00454 board (see Figure 19). The power supply is protected for reverse polarity and overvoltage.

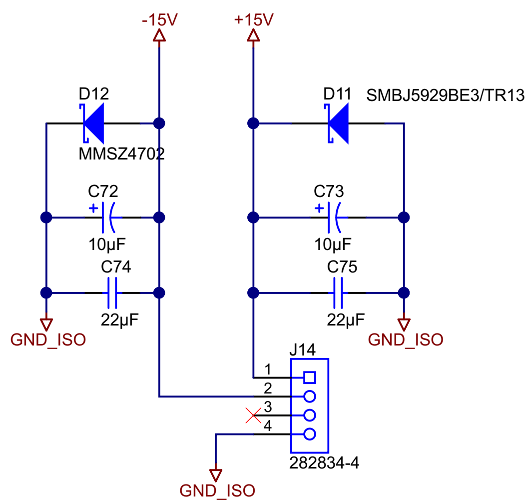

Figure 19. Input Connection for 15 V and –15 V

The DAC8563 requires a 5.5-V supply voltage. The TPS7A4201 LDO is used to step-down 15 V to 5.5 V. The following Figure 20 shows the LDO circuit diagram.

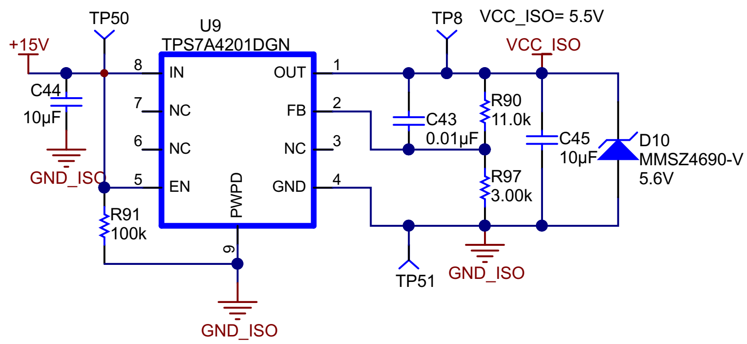

Figure 20. Regulator for DAC 5.5 V

2.4.5.2 *Non-Isolated Power Supply*

As Figure 21 shows, an external dc supply must be connected on a two-pin terminal block J8 to power the non-isolated section of the TIDA-00454 board. The TIDA-00454 design uses the TPS7A65-Q1 LDO. The DVCC for the MSP430F67791A device is 3.3 V. The power supply is protected for reverse polarity and overvoltage.

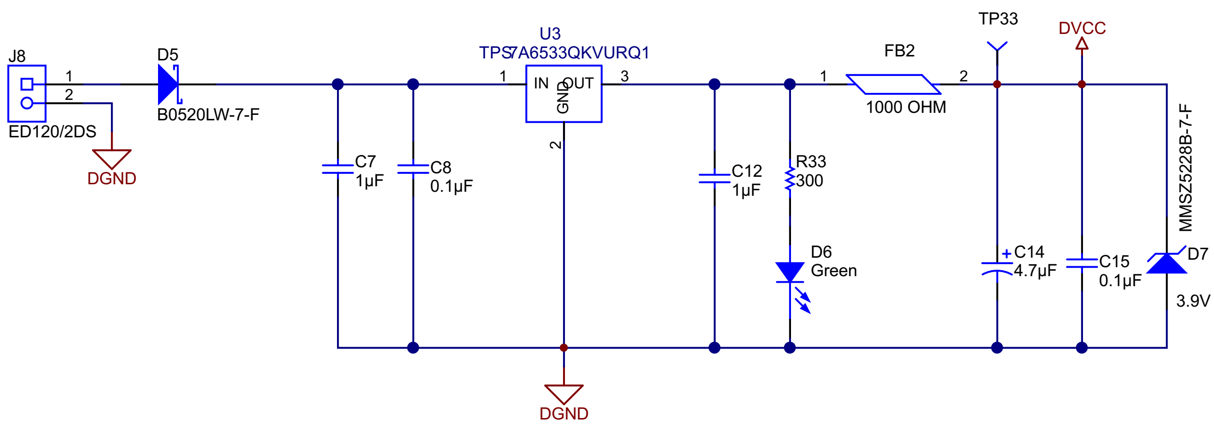

Figure 21. 3.3-V Power Supply

2.4.6 Need for Transducer

The addition of a number of distributed energy sources makes for increasingly complex electric power transmission and distribution systems. The expectations regarding the performance of these systems also continue to rise, such as operating at higher efficiency and reducing the time. Improving efficiency and reducing downtime is achievable by connecting additional devices to a centralized system for the purposes of monitoring. Implementing a protection relay or circuit breakers protects the critical, primary equipment. Monitoring most of the critical loads is another important factor to increasing the efficiency and reducing downtime. One simple way to monitor these loads is by using transducers. Transducers monitor different electrical parameters and report those parameters to a monitoring system digitally using an RS485 communication interface or by using dc analog outputs. The dc analog outputs can be current or voltage.

Transducers convert ac voltage or current into a standard output signal. An ac transducer measures a wide range of input current and voltage and has dc analog outputs, digital outputs, and light-emitting diodes (LEDs) to indicate the status. Transducers do not have self-contained displays and the inclusion of communication ports is optional.

Transducers have two types of standard dc outputs: dc analog voltage outputs (such as 0 V to 10 V) and dc analog current outputs (such as 4 mA to 20 mA).

Table 9 shows each output type and the associated advantages and limitations.

Table 9. Transducer Output Types

DC VOLTAGE OUTPUT	
ADVANTAGES	Easier to test for voltage Wide range of control interfaces
LIMITATIONS	Possible signal degradation with long cable runs More susceptible to noise
DC CURRENT OUTPUT	
ADVANTAGES	Accuracy of the signal is not affected by voltage drop from wire resistance Longer cable lengths have less signal degradation Good noise immunity
LIMITATIONS	An accurate and complex setup is required to test the current output

Power transducers that include ac voltage and current measurements are required to measure power and energy in both directions. The direction of energy is indicated by the current direction when the transducers are configured for this application and the bidirectional dc output indicates the amplitude and direction of the current being measured.

The following dc output voltage ranges are commonly used:

- ±10-V dc
- ±5-V dc
- 0- to 10-V dc
- 0- to 5-V dc

The following dc output current ranges are commonly used:

- ±20-mA dc with an over-range of ±24-mA dc
- 0- to 20-mA dc
- 4- to 20-mA dc

Transducers use 12- to 16-bit digital-to-analog converters (DACs). The number of bits can be selected based on transducer accuracy specification. Texas Instruments (TI) has a wide portfolio of precision DACs.

The transducer output connects to the data acquisition system. The common industry practice is to provide isolation whenever integrating two systems. Isolation can be provided using digital isolators. TI has a wide portfolio of digital isolators for such applications.

2.4.7 Digital Output

Transducers also offer digital outputs. This digital output uses an electromechanical relay to convey the status, event, or alarm of predefined conditions. Relay outputs can also provide power to auxiliary equipment. To drive electromechanical relays, a discrete bipolar junction transistor (BJT) or metal-oxide semiconductor field-effect transistor (MOSFET) is used along with a free-wheeling diode for inductive kickback protection. TI provides a single-chip solution that simplifies the process of driving relays.

2.4.8 TIDA-00454 Advantages

The TIDA-00454 TI Design demonstrates:

- Onboard input ac voltage sensing using a potential divider and current sensing using a current transformer (CT)
- Six 24-bit simultaneous $\Delta\Sigma$ analog-to-digital converters (ADCs) for measuring the wide range input with high accuracy

- Capability to measure three-phase voltages and currents
- Digital isolator for isolating DAC interface signals
- Two individually selectable, bidirectional dc analog outputs (voltage or current output)
- Flexibility for user to select any of the three phases for sending the measured parameters (voltage and current) through dc analog output
- Six open collector outputs for relay drive
- Universal asynchronous receiver and transmitter (UART) for serial communication (TTL Interface)

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The following section provides information on the different connectors used.

3.1.1.1 Connectors

Table 10. Connector Details

INPUT/OUTPUT TYPE	SPECIFICATION	CONNECTOR
INPUTS		
Voltage I/P	Channel 1	J11
	Channel 2	J12
	Channel 3	J13
OUTPUTS		
Analog Output	Analog Output 0 (AOUT0)	J9.3 – J9.4
	Analog Output 1 (AOUT1)	J9.1 – J9.2
Analog output parameter selection[1] (connect jumper between mentioned pins)	Phase 1 (AOUT0 = V1; AOUT1 = I1)	J4.1 – J4.2
	Phase 2 (AOUT0 = V2; AOUT1 = I2)	J4.3 – J4.4
	Phase 3 (AOUT0 = V3; AOUT1 = I3)	J4.5 – J4.6
Analog output type (voltage ±10 V or current ±24 mA) selection (connect jumper between mentioned pins)	AOUT0 = ±10-V voltage mode	J3.2 – J3.3
	AOUT0 = ±24-mA current mode	J4.7 – J4.8, J3.2 – J3.3
	AOUT1 = ±24-mA current mode	J3.2 – J3.3
	AOUT1 = ±10-V voltage mode	J4.9 – J4.10, J3.2 – J3.3
Digital (relay) output (connect 8.5 V or higher on J1.2 to J2.1 for operation of relay driver IC)	Channel 1	J1.8 – J1.1
	Channel 2	J1.7 – J1.1
	Channel 3	J1.6 – J1.1
	Channel 4	J1.5 – J1.1
	Channel 5	J1.4 – J1.1
	Channel 6	J1.3 – J1.1
POWER SUPPLY		
Non-isolated power supply input	12-V dc	J8.1 wrt J8.2
Isolated power supply input	15-V dc	J14.1 wrt J14.4
	–15-V dc	J14.2 wrt J14.4
MCU		
MCU programming	JTAG	J10
Expansion I/O interface	SPI, I^{2}C, UART, and GPIO	J5, J2, J4

[1] Analog output parameter selection: The appropriate phase jumper must be connected. The analog output is at mid-value and no data sends in the case that no jumper is connected for the phase selection. In the case where multiple jumpers are connected for phase selection, priority is given as per phase 1 > phase 2 > phase 3. For example, if phase 1 and phase 2 jumpers are connected, phase 1 receives priority and phase 1 data sends to the analog outputs.

The current input wires are taken through the current transformer and do not have connectors (see Figure 22). The wires are connected externally as flying leads. An external terminal block can be used to connect the current inputs.

Figure 22. Current Input Wire Through CT

Figure 23 shows the interface connectors for the TIDA-00454 board.

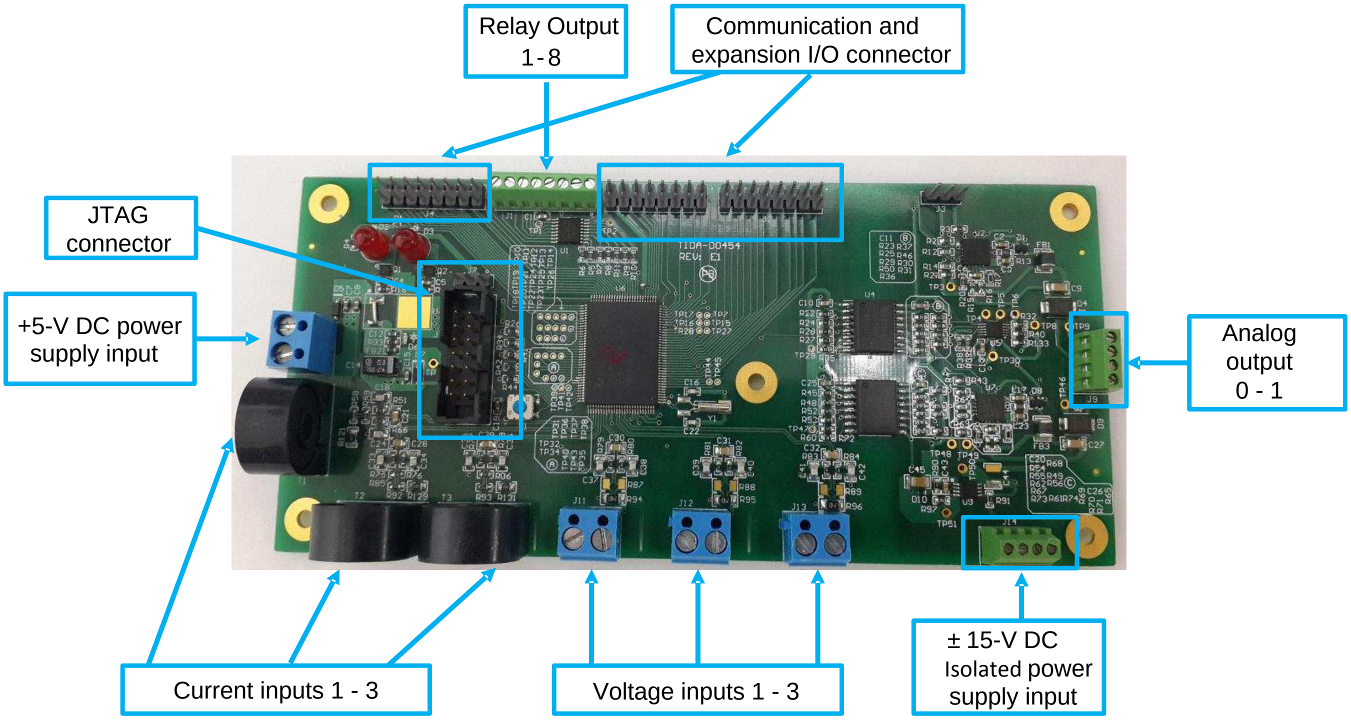

Figure 23. TIDA-00454 Interface Connectors

3.1.1.2 External DC Power Supply for Input Voltage Range

The power supply input is 5-V dc for the non-isolated section.

A 15-V dc and −15-V dc is required for the isolated section.

The initial inrush current is more and the user must take care if the power supply used has a set current limit.

3.1.1.3 AC Input Range

3.1.1.3.1 AC Current Input Range

The current input range for this design is 0.25- to 10-A ac with 20% overload.

3.1.1.3.2 AC Voltage Input Range

The ac voltage input range for this design is 23 V to 320 V.

3.1.1.4 DC Analog Output Range

3.1.1.4.1 DC Current Output Range

The dc current output is set to ±24 mA for both channels.

3.1.1.4.2 DC Voltage Output Range

The dc voltage output is set to ±10 V for both channels. The input ac parameters are converted to dc output parameters below.

Use the following scaling factors to calculate the expected output for the applied input.

AC input current conversion:

DC voltage output (V) = 0.9849 × input current (A)

DC current output (mA) = 2.01021 × input current (A)

AC input voltage conversion:

DC voltage output (V) = 0.031125 × input voltage (V)

DC current output (mA) = 0.075517 × Input Voltage (V)

3.1.1.4.3 Enhancements

The user can modify the current output range to 4 mA to 20 mA or 0 mA to 24 mA. See Section 2.4.2.2 for more details.

The user can modify the voltage output range to 0 V to 5 V, 0 V to 10 V, or ±5 V. See Section 2.4.2.2 for more details.

Testing with these settings has not been performed in this design.

3.1.2 Software

In this design, the software has three functional blocks (separated as projects):

- Mathematical routines
- Metrology computation
- Application wrapper that deals mainly with application-processor functionality and communication

The following subsections describe the software. The first subsection describes the setup of various peripherals of the MSP430 device. Subsequently, the entire metrology software is described as two major processes: the foreground process and background process. These subsections further detail the SPI, DAC, and XTR300 modules.

3.1.2.1 ΣΔ24 Initialization

The MSP430F6991A device has seven independent ΣΔ data converters (of which six are used). The clock to the ΣΔ24 (fM) derives from the system clock, which is configured to run at 25 MHz. The sampling frequency is defined as fs = fM / OSR. The OSR is chosen to be 256 and the modulation frequency (fM), is chosen as 1.048576 MHz, resulting in a sampling frequency of 4.096 Ksps. The ΣΔ24 is configured to generate regular interrupts for every sampling instance. The following are the ΣΔ channel associations:

- SD0P0 and SD0N0 Current 1
- SD1P0 and SD1N0 Current 2
- SD2P0 and SD2N0 Current 3
- SD3P0 and SD3N0 Voltage 1
- SD4P0 and SD4N0 Voltage 2
- SD5P0 and SD5N0 Voltage 3

3.1.2.2 Foreground Process (Analog Input)

The foreground process includes the initial setup of the MSP430 hardware and software immediately after a device RESET. The following Figure 24 shows the flowchart for this process.

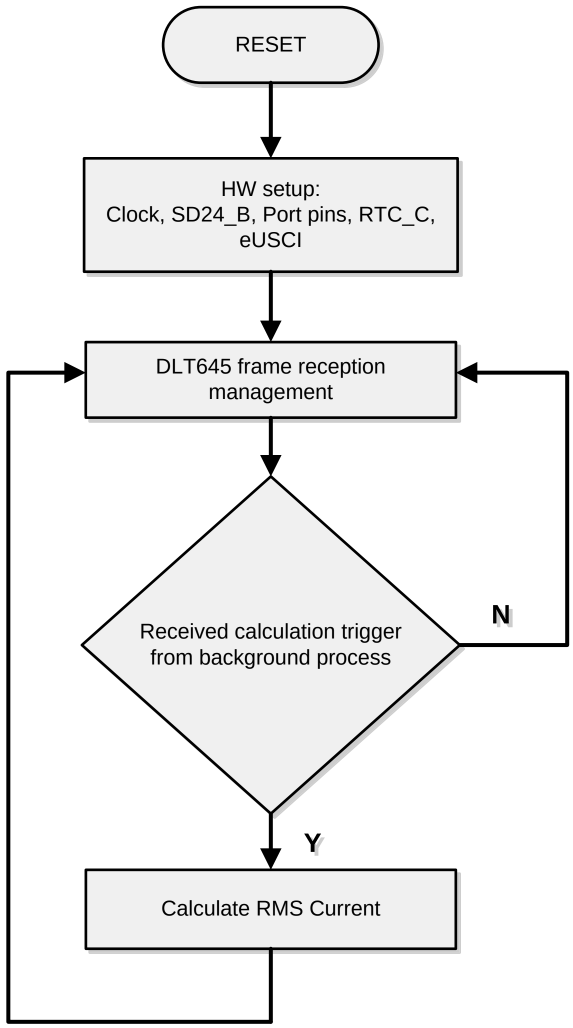

Figure 24. Foreground Process

The initialization routines involve the setup of the ADCs, clock system, GPIO (port) pins, RTC module for one-second interrupts and timekeeping, and the USCI_A0 for UART functionality. After setting up the hardware, any received frames from the GUI are processed. Subsequently, the foreground process checks whether the background process has notified it to calculate new metering parameters. This notification asserts a status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for one second in the background process. These dot products are used by the foreground process to calculate the corresponding RMS current in real-world units. Each processed current dot product is accumulated in separate 64-bit registers to further process and obtain the rms.

Equation 7 shows the formula used to calculate the RMS current:

$$V_{RMS,ch} = K_{v,ch} \times \frac{\sum_{n=1}^{\text{Sample count}} v_{ch}(n) \times v_{ch}(n)}{\text{Sample Count}} - v_{offset,ch}$$

$$I_{RMS,ch} = K_{i,ch} \times \frac{\sum_{n=1}^{\text{Sample count}} i_{ch}(n) \times i_{ch}(n)}{\text{Sample Count}} - i_{offset,ch}$$

where

- ch= Current channel whose parameters are being calculated [that is, Channel A(=1), Channel B(=2), Channel C(=3), Channel D(=4), Channel E(=5), Channel F(=6), or Channel G(=7)]
- $v_{ch}(n)$ = Voltage sample at a sample instant n (equal to the offset), which is used to subtract effects of the additive white Gaussian noise from the voltage converter
- $I_{ch}(n)$ = Each current sample of channel n at a sample instant n (equal to the offset), which is used to subtract effects of the additive white Gaussian noise from the current converter
- Sample count = Number of samples in one second
- $K_{i,ch}$ = Scaling factor for each current (7)

The power and energy are calculated for one frame of active and reactive energy samples. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate channel active and reactive powers by the formulas in Equation 8.

$$P_{ACT,ch} = K_{ACT,ch} \frac{\sum_{n=1}^{\text{Sample count}} v(n) \times i_{ch}(n)}{\text{Sample Count}} \qquad P_{REACT,ch} = K_{REACT,ch} \frac{\sum_{n=1}^{\text{Sample count}} v_{90}(n) \times i_{ch}(n)}{\text{Sample Count}}$$

where

- v_{90}ch (n) = Voltage sample at a sample instant n shifted by 90°
- $K_{ACT,ch}$ = Scaling factor for active power
- $K_{REACT,ch}$ = Scaling factor for reactive power (8)

After calculating the active and reactive power, the apparent power of each phase is calculated by the following formula in Equation 9:

$$P_{APP,ch} = \sqrt{P_{ACT,ch}^{2} + P_{REACT,ch}^{2}} \qquad (9)$$

3.1.2.3 Background Process (Analog Input)

The background function mainly deals with timing critical events in software. The background function uses the ΣΔ interrupt as a trigger to collect current samples. When the first sample of the current channel (converter 0) is ready, a ΣΔ interrupt is generated. When the interrupt for the first sample of the current channel is generated, the sample processing is done by the “per_sample_dsp()” function.

Figure 25 shows the flowchart for the per_sample_dsp() function. The per_sample_dsp() function is used to calculate the results of the intermediate current dot product, which are fed into the foreground process for the calculation of RMS current. Because 24-bit current samples are used, the current samples are processed and accumulated in dedicated 64-bit registers.

The output of each ΣΔ converter is a signed integer and any stray dc or offset value on these converters is removed using a DC-tracking filter. Separate dc estimates for all currents are obtained using the filter and current samples. These estimates are then subtracted from each current sample. The resulting instantaneous current samples are used to generate the intermediate RMS dot product. After accumulating a sufficient number of samples (approximately one second's worth), the foreground function is triggered to calculate the final I_{RMS} values.

In the software, there are two sets of dot products; at any given time, one set is used by the foreground for calculation and the other set is used as the working set by the background. After the background process has a sufficient number of samples, it swaps the two dot products so that the foreground uses the newly-acquired dot products that the background process has just calculated. The background process then uses a new empty set to calculate the next set of dot products.

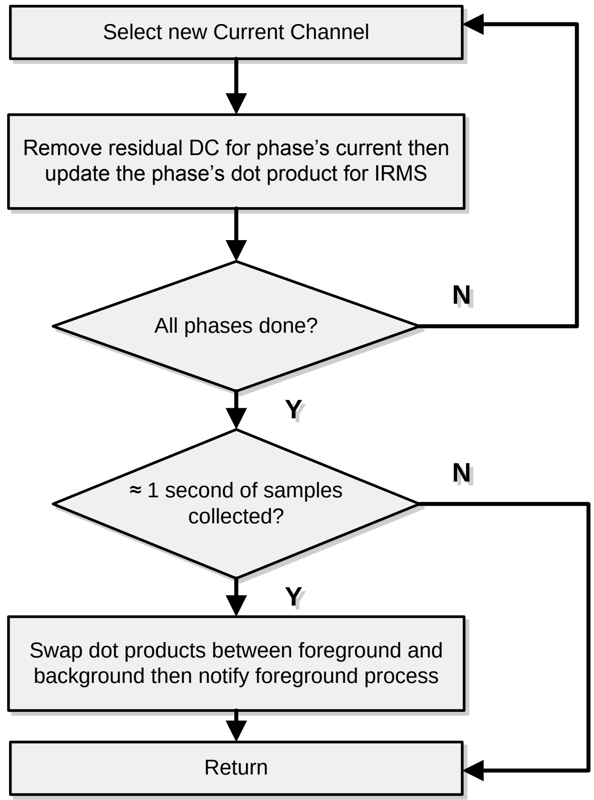

Figure 25. Per_sample_dsp() Function

3.1.2.4 SPI Initialization

The following steps outline the SPI initialization:

1. Initialize the pins P3.6, P3.7, and P4.0 as the SOMI, SIMO, and Clock.
2. Select P6.0 as the output; this pin function as /CS.
3. Reset the universal serial communication interface (USCI) module using register OFS_UCA2CTLW0 and clear all the other bits.
4. Set the SPI clock source as SMCLK (set OFS_UCA2CTLW0 bit 6 and bit 7).
5. Select the master mode using OFS_UCA2CTLW0 bit 11.
6. Select synchronous mode enable using OFS_UCA2CTLW0 bit 8.
7. Select the SPI mode as three-pin (OFS_UCA2CTLW0 bit 9 and bit 10 clear).
8. Set SPI speed to the desired rate (for example: 50 K, 1 Mbps) using register OFS_UCA2BRW (default: 50000 bps).
9. In the register OFS_UCA2CTLW0 , set bit 13 (MSB first option) and bit 15 (data captured on the first and changed on the next).
10. In the register OFS_UCA2CTLW0, set bit 14 (the SPI clock polarity as inactive to be high).
11. Enable the SPI module by clearing OFS_UCA2CTLW0 bit 0.
12. Clear interrupts using the UCA2IFG register.
13. Enable the SPI receive interrupt using the register UCA2IE bit 0.

3.1.2.5 DAC and XTR300 Initialization

Set P5.2, P5.3, and P5.5 as the outputs using register P5DIR.

Voltage or current selection

- Clear P5.2 using the P5OUT register to select the voltage output on XTR300 channel 0 (default). Setting P5.2 and the XTR300 channel 0 as the current channel is also possible.
- Set P5.3 using the P5OUT register to select the current output on XTR300 channel 1 (default). Clearing P5.3 and setting the XTR300 channel 1 as the voltage channel is also possible.

DAC internal reference

- Enable the DAC internal reference and gain as 2 using the SPI command {0x38, 0x00, 0x01}
- Allow the internal reference to settle with a few delay cycles

SPI data transmission

- Clear P6.0 to assert chip select
- When the transmit buffer is not busy, copy the data to the TX buffer UCA2TXBUF
- Allow a few cycles of delay to transmit the data and set P6.0

Command to DACA, DACB, or both

- To send data to both DACs, use command {0x17, data1, data2} where data1 and data2 are 8-bit data corresponding to 16-bit DAC data.
- To send data to DACA, use command {0x00, data1, data2} where data1 and data2 are 8-bit data corresponding to 16-bit DAC data.
- To send data to DACB, use command {0x01, data1, data2} where data1 and data2 are 8-bit data corresponding to 16-bit DAC data.
- To start with a DAC output of zero on both DAC channels, an initial SPI command is sent {0x17, 0x7F, and 0xFF}.

Jumper settings for ac input voltage selection

The jumper settings are read every time the ProcessDac() is called.

Ports P7 and P8 pins are used to read the jumper settings.

P7SEL0 is set to 0x00 to select the GPIO mode.

P7DIR is set to 0xAA (or 1010 1010b) to select inputs and output ports alternatively (0 is the input and 1 is the output).

Set P7REN to 0xFF for enabling the resistors.

P7OUT is set to 0xAA to make the outputs high.

When the jumper is connected and the output has been made high, the input port reads high (1). When the jumper is not connected, the input port reads low (0).

P8SEL0 is set to 0x00 to select GPIO mode

P8DIR is set to 0x02 (0000 0010b) to select bit 0 as the input and bit 1 as the output.

Set P8REN to 0xFF for enabling the resistors.

P8OUT is set to 0x02 to make the output high.

Input channel selection

When P7IN [bit 2] is set, select channel 1 as the DAC output.

When P7IN [bit 4] is set, select channel 2 as the DAC output.

When P7IN [bit 6] is set, select channel 3 the as DAC output.

When P7IN [bit 2, 4, and 6] are not set, no channel is selected and the DAC output is set to mid value.

XTR300 current- or voltage-mode selection

When P8IN [bit 0] is asserted high, P5OUT [bit 2] is set high (1) to enable current mode.

When P8IN [bit 0] is asserted low, P5OUT [bit 2] is set low (0) to enable voltage mode.

When P8IN [bit 2] is asserted high, P5OUT [bit 3] is set high (1) to enable voltage mode.

When P8IN [bit 2] is asserted low, P5OUT [bit 3] is set low (0) to enable current mode.

DACA and DACB values are updated every alternate second.

ProcessDac()

The function ProcessDac() is called once every second when the execution of the foreground task completes. Read the RMS current and voltage from input channels (0, 1, or 2). Input channel selection and XTR300 output-mode selection is based on the jumper settings.

The look-up table for current reading contains an entry for every 1 A between 0 A to 12 A. The look-up table for voltage reading contains an entry for every 25 V between 0 V to 320 V. The current and voltage readings are matched with a corresponding entry in the DAC data look-up table. The DAC data is derived by using the look-up table readings and interpolation for the intermediate data points. The DAC data is sent to the DAC through SPI and the result can be observed at the output of the XTR300 terminals.

Relay driver

1. Configure the relevant bits in P6SEL0 and P7SEL0 for the port functionality. Port functionality is selected by writing 0 to the specific bits.
2. Initialize the following ports as output P6.1, P6.2, P6.3, P6.4, P6.5, P6.6, P6.7 (using P6DIR), and P7.0 (using P7DIR).
3. The bits are configured as the output by writing 1 to the specific bits in the register.
4. A 1 is written to P6OUT and P7OUT to make the outputs high and vice versa. By default the relay outputs are off.
5. LEDs are used to indicate the driver errors of the dc analog output. If EFLAG1 (P5IN [bit 0]) is asserted low (0), P6OUT[bit 1] is set high (1) to illuminate LED1. If EFLAG2 (P5IN [bit 1]) is asserted low (0), P6OUT[bit 2] is set high (1) to illuminate LED2. LED1 and LED2 are turned off by default. Refer also to Section 2.4.4.1 (under *LED indication*).

3.1.2.6 GUI Setup

A GUI is provided with this TI Design for calibration purposes and to display the results. To run the GUI, the eUSCIA0 UART TX/RX pins must be connected to an isolated UART to RS-232 adapter, such as: http://www.ti.com/tool/TIDA-00163.

3.1.2.6.1 Viewing Results

To run the GUI:

1. Connect the measurement module to a PC through an RS-232 cable and connect the isolated UART to an RS-232 adapter.
2. Open the */Source/GUI* folder and open the *calibration-config.xml* in a text editor.
3. Change the "port name" field within the "meter" tag to the COM port connected to the meter (see Figure 26). In Step 4, this field changes to COM7.

```
            </correction>
          </phase>
          <temperature/>
          <rtc/>
        </cal-defaults>
        <meter position="1">
          <port name="com7" speed="9600"/>
        </meter>
        <reference-meter>
          <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
          <type id="chroma-66202"/>
          <log requests="on" responses="on"/>
          <scaling voltage="1.0" current="1.0"/>
        </reference-meter>
```

Figure 26. GUI Configuration File Changed to Communicate With Meter

4. Run the *calibrator.exe* in the */Source/GUI* folder. If the COM port in the *calibration-config.xml* has been changed in the previous Step 3 (the com port connected to the measurement module), the GUI opens (see the following Figure 27).
5. If the GUI connects properly to the measurement module, the top-left button is green (specified as “Comms”). If experiencing problems with connections, or if the code is not configured correctly, the button is red (see Figure 28).
6. Click the green button to view the results.

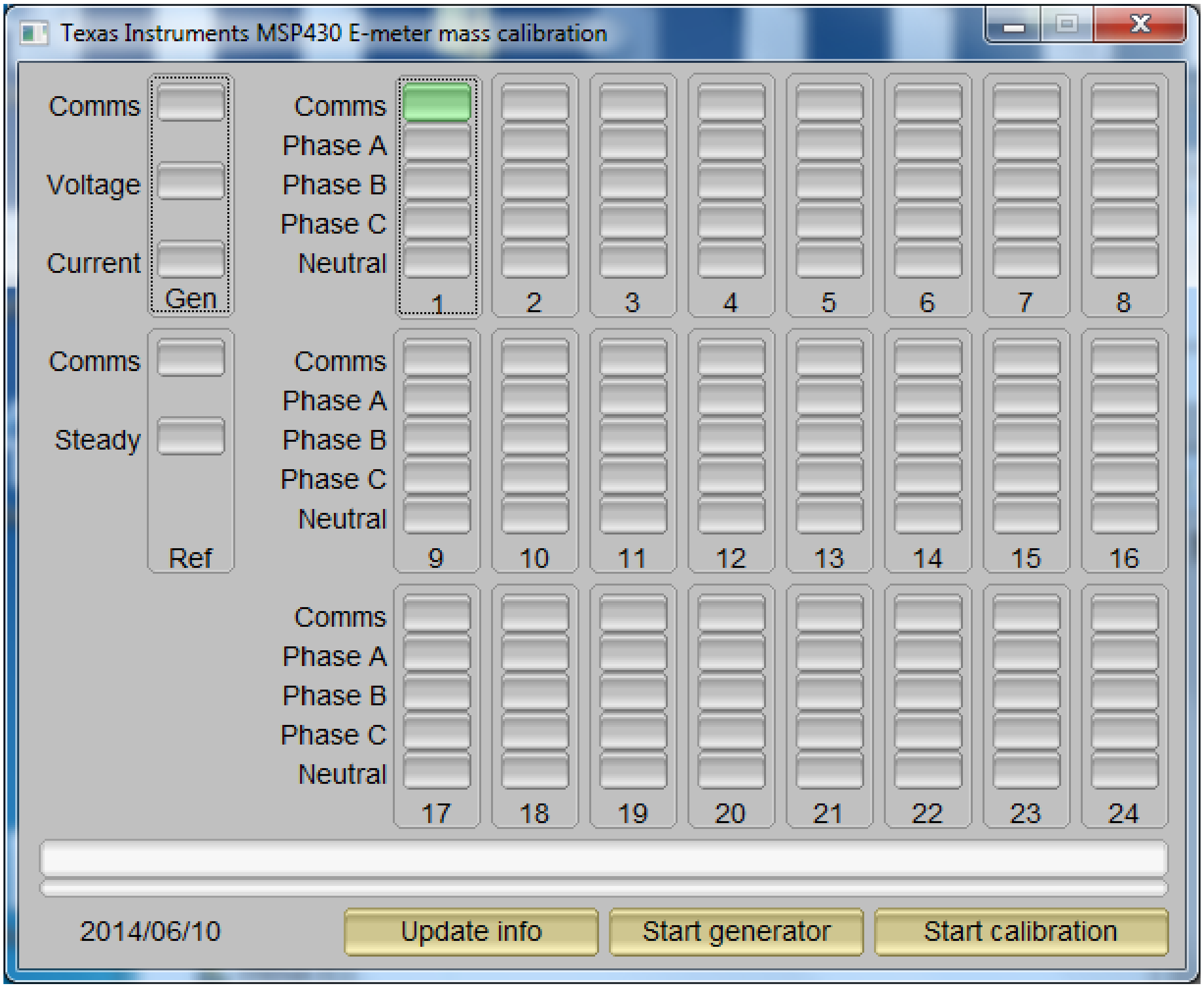

Figure 27. GUI Startup Window (Snapshot of GUI Screen)

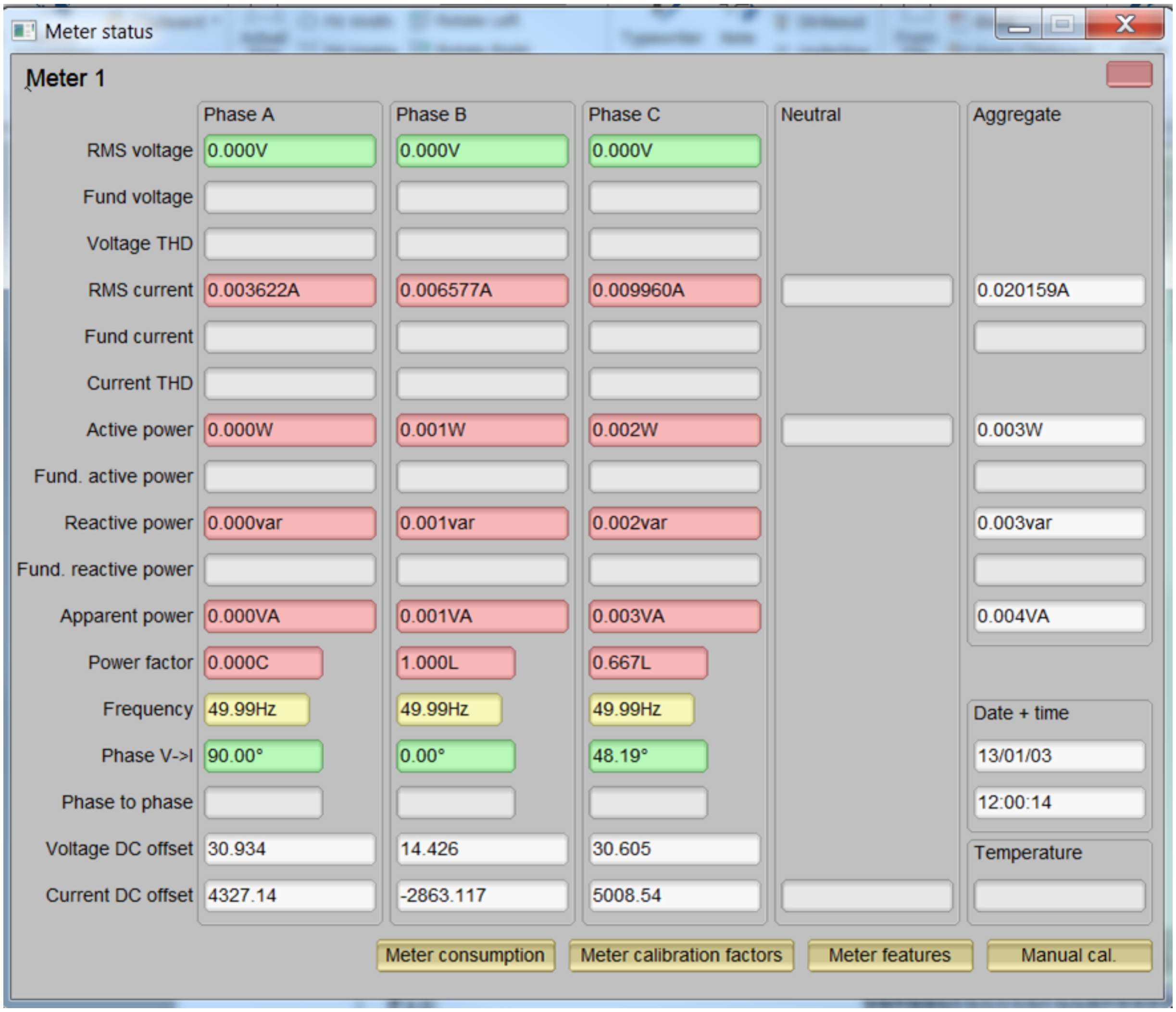

Figure 28. Results Window (Snapshot of GUI Screen)

3.2 Testing and Results

3.2.1 Test Setup

Figure 29. 5-V DC Source

Figure 30. Programmable Power Source

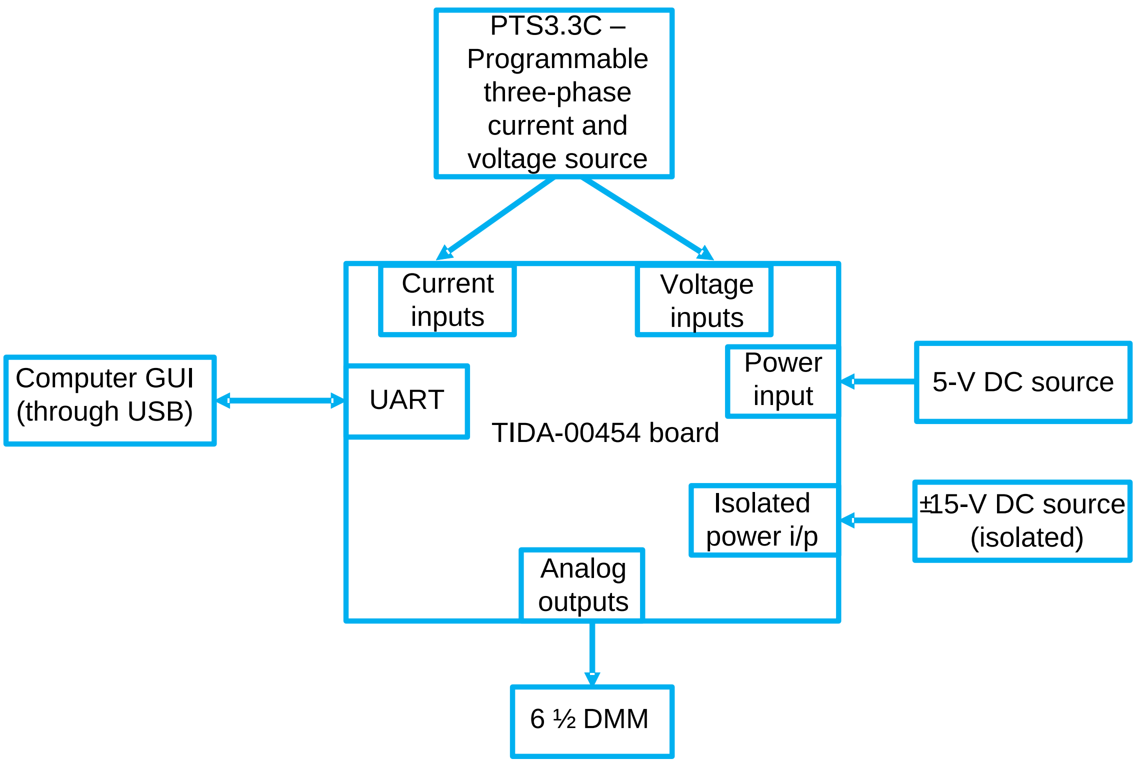

Figure 31. Test Setup for Connecting TIDA-00454 Board

3.2.2 Test Results

3.2.2.1 Functional Testing

Table 11. Functional Test Results

PARAMETERS	MEASURED PARAMETER	MEASURED VALUE
Non-isolated power supply	12-V dc input	11.998 V
	3.3 V	3.302 V
Isolated power supply	15-V dc input	15.008 V
	−15-V dc input	–15.003 V
	5.5 V	5.453 V

Digital output

An LED is connected to the digital output connector. The digital output is turned ON and OFF and the LED status is observed. The LED is used with a 10-mA current limiting resistor.

Table 12. Observation for Digital Output

	EXPECTED LED STATUS	OBSERVATION	EXPECTED LED STATUS	OBSERVATION
Digital output 1	ON	ON	OFF	OFF
Digital output 2	ON	ON	OFF	OFF
Digital output 3	ON	ON	OFF	OFF
Digital output 4	ON	ON	OFF	OFF
Digital output 5	ON	ON	OFF	OFF
Digital output 6	ON	ON	OFF	OFF

Input phase selection for dc analog output

For the analog output, one of the three phases are selected during the transducer operation. The required phase can be selected using the same jumper configurations, as the following Table 13 shows.

Table 13. Observation for Input Phase Selection

JUMPER SETTING	OBSERVATION
J4.1 – J4.2	Phase 1
J4.3 – J4.4	Phase 2
J4.5 – J4.6	Phase 3
J4.3 – J4.4 J4.5 – J4.6	Phase 2

DC analog output—current or voltage selection

For the phase selected using the preceding settings in Table 13, the dc output proportional to the input current and voltage measured are provided by AOUT0 and AOUT1.

The dc output type (current or voltage) required for AOUT0 and AOUT1 can be configured as the following Table 14 shows.

Table 14. Observation for DC Analog Output Type Selection

JUMPER SETTING	OBSERVATION
J3.2 – J3.3	AOUT0 = Voltage mode
J4.7 – J4.8 J3.2 – J3.3	AOUT0 = Current mode
J3.2 – J3.3	AOUT1 = Current mode
J4.9 – J4.10 J3.2 – J3.3	AOUT1 = Voltage mode

3.2.2.2 *Performance Testing*

The ac input frequency is 50 Hz unless otherwise specified. Please note the following before analyzing the accuracy performance results:

- Measured output voltage or current: This is the output voltage or current measured without applying gain and offset calibration.
- % Error: This is the output measurement error after applying offset and gain calibration.
- The dc offset is zero (not applicable) when no offset is mentioned.

NOTE: Be sure to consider the gain factor and offset when calculating.

3.2.2.2.1 *Accuracy Test—AC Input Voltage Measurement*

Table 15. Voltage Channel 1

INPUT AS % OF NOMINAL VOLTAGE (100% = 230 V)	MEASURED INPUT VOLTAGE (V)	MEASURED OUTPUT VOLTAGE (V)	ERROR (%)
120	276.117	276.693	–0.08
100	230.116	230.479	–0.13
90	207.117	207.388	–0.16
80	184.112	184.347	–0.16
70	161.113	161.264	–0.19
60	138.105	138.195	–0.22
50	115.1	115.155	–0.23
40	92.105	92.134	–0.25
30	69.1003	69.103	–0.27
20	46.0015	46.037	–0.18
10	23.0016	22.99	–0.26
8	18.4021	18.39	–0.26
6	13.8025	13.793	–0.22
4	9.20154	9.193	–0.18
2	4.60264	4.595	–0.03

The gain factor for voltage channel 1 is 0.997 and the offset is –0.020 V.

Table 16. Voltage Channel 2

INPUT AS % OF NOMINAL VOLTAGE (100% = 230 V)	MEASURED INPUT VOLTAGE (V)	MEASURED OUTPUT VOLTAGE (V)	ERROR (%)
120	276.117	276.726	–0.07
100	230.116	230.516	–0.12
90	207.117	207.416	–0.15
80	184.112	184.347	–0.16
70	161.113	161.279	–0.18
60	138.105	138.215	–0.21
50	115.1	115.171	–0.22
40	92.105	92.141	–0.24
30	69.1003	69.111	–0.26
20	46.0015	46.013	–0.23
10	23.0016	22.993	–0.25
8	18.4021	18.392	–0.25
6	13.8025	13.793	–0.22
4	9.20154	9.195	–0.15
2	4.60264	4.598	0.03

The gain factor for voltage channel 2 is 0.997 and the offset is –0.020 V.

Table 17. Voltage Channel 3

INPUT AS % OF NOMINAL VOLTAGE (100% = 230 V)	MEASURED INPUT VOLTAGE (V)	MEASURED OUTPUT VOLTAGE (V)	ERROR (%)
120	276.117	276.689	–0.09
100	230.116	230.499	–0.13
90	207.117	207.606	–0.05
80	184.112	184.34	–0.17
70	161.113	161.268	–0.19
60	138.105	138.201	–0.22
50	115.1	115.164	–0.23
40	92.105	92.133	–0.25
30	69.1003	69.107	–0.26
20	46.0015	46.002	–0.26
10	23.0016	22.991	–0.26
8	18.4021	18.39	–0.26
6	13.8025	13.792	–0.23
4	9.20154	9.193	–0.18
2	4.60264	4.596	–0.01

The gain factor for voltage channel 3 is 0.997 and the offset is –0.020 V. Figure 32 shows a plot of the voltage channel accuracy test for all three channels.

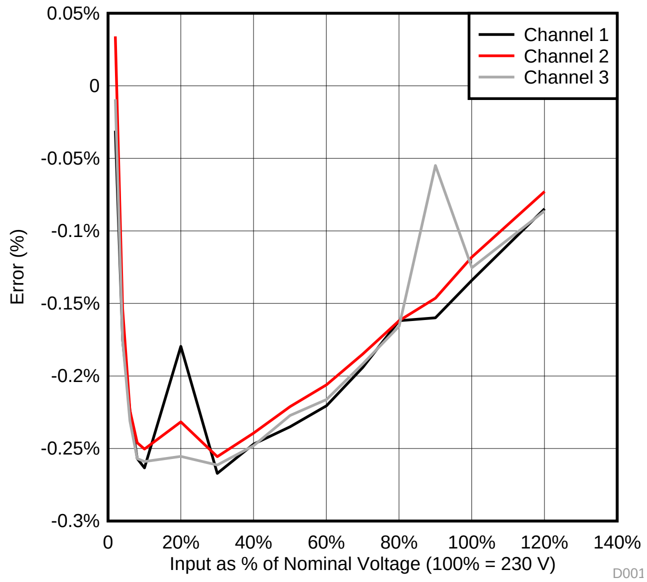

Figure 32. AC Input Voltage Accuracy Test

3.2.2.2.2 Accuracy Test —AC Input Current Measurement

The current accuracy has been measured for normal current (I in phase with V) and reverse current (I out of phase by 180º with respect to voltage).

Table 18. Current Channel 1

INPUT AS % OF NOMINAL CURRENT (100% = 5 A)	MEASURED INPUT CURRENT (A)	MEASURED OUTPUT CURRENT (A)	ERROR (%)
200	10.0048	10.0028	–0.02
175	8.75284	8.75523	0.03
150	7.50277	7.50843	0.08
120	6.003	6.00915	0.1
100	5.00162	4.9994	–0.04
90	4.5023	4.49955	–0.06
80	4.00247	3.99972	–0.07
70	3.50151	3.50199	0.01
60	3.00186	3.00101	–0.03
50	2.50166	2.50182	0.01
40	2.0021	2.00139	–0.04
30	1.50168	1.50143	–0.02
20	1.0001	1.00017	0.01
10	0.500147	0.500358	0.04
8	0.400185	0.40024	0.01
6	0.300242	0.300199	–0.01
4	0.200152	0.200194	0.02
2	0.100174	0.10017	0
–2	0.100171	0.100127	–0.04
–4	0.200165	0.200068	–0.05
–6	0.300185	0.300177	0
–8	0.40017	0.400196	0.01
–10	0.500192	0.500184	0
–20	1.00014	1.00067	0.05
–30	1.50175	1.50193	0.01
–40	2.00202	2.00201	0
–50	2.50204	2.50211	0
–60	3.00166	3.00224	0.02
–70	3.50209	3.50228	0.01
–80	4.00182	4.0024	0.01
–90	4.502	4.50203	0
–100	5.00213	5.00212	0
–120	6.00298	6.00042	–0.04
–150	7.50034	7.49938	–0.01
–175	8.75308	8.75068	–0.03
–200	10.001	10.0025	0.01

The gain factor for current channel 1 is 1.

Table 19. Current Channel 2

INPUT AS % OF NOMINAL CURRENT (100% = 5 A)	MEASURED INPUT CURRENT (A)	MEASURED OUTPUT CURRENT (A)	ERROR (%)
200	10.0048	9.99528	–0.1
175	8.75284	8.74436	–0.1
150	7.50277	7.49481	–0.11
120	6.003	5.9966	–0.11
100	5.00162	4.99553	–0.12
90	4.5023	4.49608	–0.14
80	4.00247	3.99696	–0.14
70	3.50151	3.49953	–0.06
60	3.00186	2.99866	–0.11
50	2.50166	2.5002	–0.06
40	2.0021	2.00015	–0.1
30	1.50168	1.50064	–0.07
20	1.0001	0.999972	–0.01
10	0.500147	0.499983	–0.03
8	0.400185	0.399992	–0.05
6	0.300242	0.300028	–0.07
4	0.200152	0.200054	–0.05
2	0.100174	0.100138	–0.04
–2	0.100171	0.1000094	–0.16
–4	0.200165	0.20003	–0.07
–6	0.300185	0.2999993	–0.06
–8	0.40017	0.399518	–0.16
–10	0.500192	0.499896	–0.06
–20	1.00014	1.00012	0
–30	1.50175	1.50096	–0.05
–40	2.00202	2.00079	–0.06
–50	2.50204	2.50052	–0.06
–60	3.00166	3.00028	–0.05
–70	3.50209	3.49997	–0.06
–80	4.00182	3.99944	–0.06
–90	4.502	4.49891	–0.07
–100	5.00213	4.999815	–0.05
–120	6.00298	5.99618	–0.11
–150	7.50034	7.49421	–0.08
–175	8.75308	8.74374	–0.11
–200	10.001	9.99462	–0.06

The gain factor for current channel 2 is 1.

Table 20. Current Channel 3

INPUT AS % OF NOMINAL CURRENT (100% = 5 A)	MEASURED INPUT CURRENT (A)	MEASURED OUTPUT CURRENT (A)	ERROR (%)
200	10.0048	9.99195	–0.13
175	8.75284	8.7446	–0.09
150	7.50277	7.4937	–0.12
120	6.003	5.9947	–0.14
100	5.00162	4.99637	–0.1
90	4.5023	4.497745	–0.1
80	4.00247	3.99781	–0.12
70	3.50151	3.49996	–0.04
60	3.00186	2.99827	–0.12
50	2.50166	2.50012	–0.06
40	2.0021	1.9992	–0.14
30	1.50168	1.50048	–0.08
20	1.0001	1.00031	0.02
10	0.500147	0.499675	–0.09
8	0.400185	0.399689	–0.12
6	0.300242	0.299981	–0.09
4	0.200152	0.200117	–0.02
2	0.100174	0.100161	–0.01
–2	0.100171	0.100112	–0.06
–4	0.200165	0.200034	–0.07
–6	0.300185	0.300046	–0.05
–8	0.40017	0.399762	–0.1
–10	0.500192	0.500007	–0.04
–20	1.00014	1.00013	0
–30	1.50175	1.50112	–0.04
–40	2.00202	2.00102	–0.05
–50	2.50204	2.50041	–0.07
–60	3.00166	3.00025	–0.05
–70	3.50209	3.49926	–0.08
–80	4.00182	4.00007	–0.04
–90	4.502	4.49915	–0.06
–100	5.00213	4.9988	–0.07
–120	6.00298	5.9989	–0.07
–150	7.50034	7.49265	–0.1
–175	8.75308	8.747	–0.07
–200	10.001	9.99219	–0.09

The gain factor for current channel 3 is 1. Figure 33 shows a plot of the current channel accuracy test for all three channels.

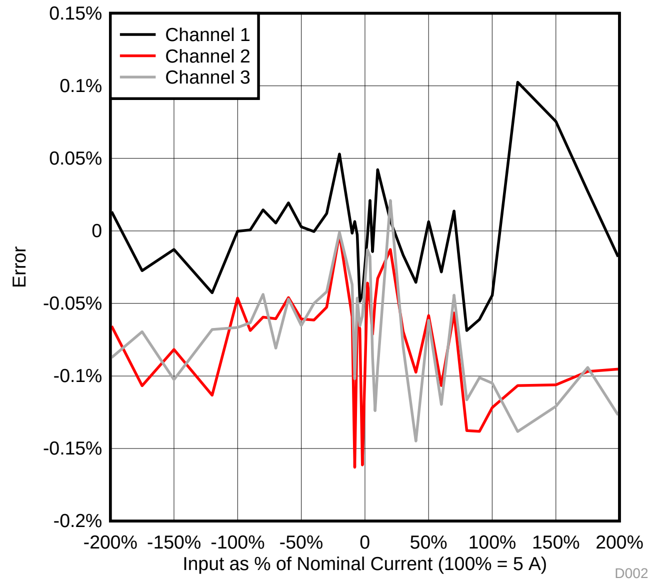

Figure 33. AC Input Current Accuracy Test

3.2.2.2.3 DAC Output Accuracy Test

Table 21. DAC8563 Output Accuracy Test

INPUT AS % OF NOMINAL CURRENT (100% = 5 A)	MEASURED INPUT CURRENT (A)	EXPECTED DAC OUTPUT VOLTAGE (V)	MEASURED DAC OUTPUT VOLTAGE (V)	ERROR (%)
240	12.0145	4.9609	4.957	–0.07
220	11.007	4.7546	4.7522	–0.04
200	10.0012	4.5486	4.5489	0.02
175	8.75188	4.2927	4.2932	0.02
150	7.50162	4.0366	4.0372	0.03
120	6.00183	3.7293	3.7285	–0.01
100	5.00152	3.5245	3.5242	0.01
90	4.50133	3.4220	3.4215	0
80	4.00189	3.3197	3.3193	0
70	3.50167	3.2172	3.2154	–0.04
60	3.00196	3.1149	3.1127	–0.05
50	2.50152	3.0124	3.0115	–0.01
40	2.00178	2.9100	2.9094	0
30	1.50174	2.8075	2.8067	–0.01
20	1.00015	2.7048	2.7044	0
10	0.500169	2.6024	2.6008	–0.04
8	0.400179	2.5819	2.5803	–0.04
6	0.300165	2.5614	2.5601	–0.03
4	0.200173	2.541	2.5404	0
2	0.100168	2.5204	2.5201	0.01
–2	–0.100167	2.4794	2.4792	0.01
–4	–0.200169	2.4589	2.4588	0.02
–6	–0.300152	2.4384	2.4384	0.02
–8	–0.400163	2.4179	2.4186	0.05
–10	–0.500163	2.3975	2.3983	0.06
–20	–1.00012	2.295	2.2948	0.01
–30	–1.50184	2.1922	2.1925	0.04
–40	–2.00187	2.0898	2.0898	0.02
–50	–2.50182	1.9875	1.9877	0.04
–60	–3.00181	1.885	1.8851	0.03
–70	–3.50165	1.7826	1.7836	0.08
–80	–4.00179	1.6801	1.6798	0.01
–90	–4.50168	1.5778	1.5776	0.02
–100	–5.00194	1.4753	1.4749	0.01
–120	–6.00154	1.2705	1.2706	0.05
–150	–7.50256	0.9631	0.9619	–0.07
–175	–8.75278	0.707	0.7058	–0.10
–200	–10.0002	0.4515	0.4507	–0.07
–220	–11.0044	0.2457	0.2453	0
–240	–12.02	0.0389	0.0383	–0.36

The gain factor for the DAC8563 accuracy test is 1 and the offset is –0.0005 V. Figure 34 shows a plot of the DAC8563 accuracy test.

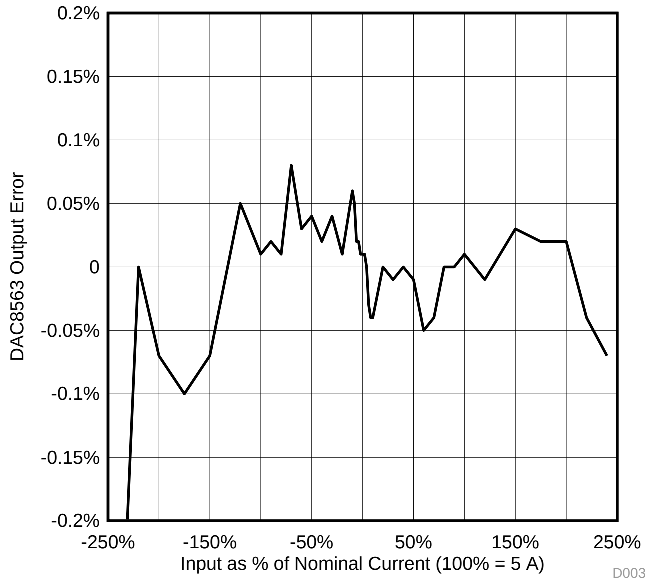

Figure 34. DAC8563 Output Accuracy Test

3.2.2.2.4 DC Analog Output Accuracy Test

3.2.2.2.4.1 DC Current Output Accuracy Test

The analog output is set as the bidirectional current output.

A 500-Ω precise, 0.1% resistor is connected to the analog output. This 500-Ω resistor is measured using the four-wire method with a 6½ digital multimeter (DMM).

$$R_{MEASURED} = 499.924\ \Omega \quad (10)$$

Measure the voltage drop across this resistor using a 6½ DMM. The output current is calculated by dividing the measured voltage by the measured resistance.

The full-scale range (FSR) error is also calculated for the dc current output. Calculate the FSR error using the following Equation 11:

$$\%Error_{FSR} = \text{(Measured current – Expected current) / Full scale current (Measured dc current at 200\% of input current))} \quad (11)$$

Table 22. DC Current Output Accuracy Test for AOUT1

INPUT AS % OF NOMINAL CURRENT (100% = 5 A)	MEASURED INPUT CURRENT (A)	EXPECTED DC CURRENT OUTPUT (mA)	MEASURED DC CURRENT OUTPUT (mA)	ERROR (%)	FULL SCALE ERROR - $ERROR_{FSR}$ (%)
240	12.0145	24.1162	24.0997	–0.07	–0.08
220	11.007	22.0946	22.083	–0.05	–0.06
200	10.0012	20.0752	20.1015	0.13	0.13
175	8.75188	17.5675	17.5941	0.15	0.13
150	7.50162	15.0577	15.0833	0.17	0.13
120	6.00183	12.0469	12.0568	0.08	0.05
100	5.00152	10.0394	10.0541	0.15	0.07
90	4.50133	9.0354	9.0476	0.14	0.06
80	4.00189	8.0328	8.0450	0.15	0.06
70	3.50167	7.0287	7.0267	–0.03	–0.01
60	3.00196	6.0253	6.0203	–0.08	–0.02
50	2.50152	5.0212	5.0282	0.14	0.03
40	2.00178	4.0179	4.0268	0.22	0.04
30	1.50174	3.0138	3.0203	0.22	0.03
20	1.00015	2.0074	2.0177	0.51	0.05
10	0.500169	1.0033	1.0014	–0.19	–0.01
8	0.400179	0.803	0.8004	–0.33	–0.01
6	0.300165	0.6019	0.6031	0.21	0.01
4	0.200173	0.4015	0.4099	2.08	0.04
2	0.100168	0.2004	0.2107	5.14	0.05
–2	–0.100167	–0.2019	–0.1899	–5.92	0.06
–4	–0.200169	–0.403	–0.3902	–3.18	0.06
–6	–0.300152	–0.6034	–0.5899	–2.23	0.07
–8	–0.400163	–0.8045	–0.7849	–2.44	0.1
–10	–0.500163	–1.0048	–0.9831	–2.16	0.11
–20	–1.00012	–2.0089	–1.9985	–0.52	0.05
–30	–1.50184	–3.016	–3.0019	–0.47	0.07
–40	–2.00187	–4.0194	–4.0094	–0.25	0.05
–50	–2.50182	–5.0227	–5.011	–0.23	0.06
–60	–3.00181	–6.0268	–6.0169	–0.16	0.05
–70	–3.50165	–7.0302	–7.0123	–0.25	0.09
–80	–4.00179	–8.0342	–8.0304	–0.05	0.02
–90	–4.50168	–9.0376	–9.0328	–0.05	0.02
–100	–5.00194	–10.0417	–10.0397	–0.02	0.01
–120	–6.00154	–12.0484	–12.044	–0.04	0.02
–150	–7.50256	–15.0614	–15.0715	0.07	–0.05
–175	–8.75278	–17.5705	–17.5829	0.07	–0.06
–200	–10.0002	–20.0744	–20.0867	0.06	–0.06
–220	–11.0044	–22.0908	–22.0895	–0.01	0.01
–240	–12.02	–24.1177	–24.2131	0.4	–0.48

The gain factor for the dc current output accuracy test is 1. Figure 35 shows a plot of the dc current output accuracy test.

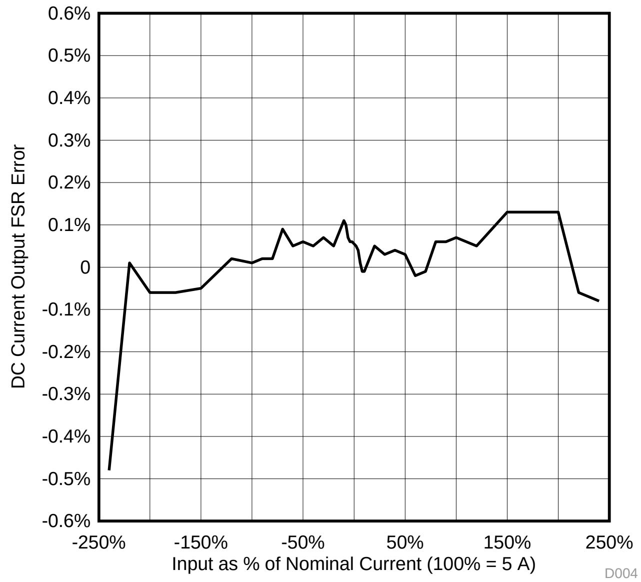

Figure 35. DC Current Output Accuracy Test for AOUT1

Table 23. DC Current Output Accuracy Test for AOUT0

INPUT AS % OF NOMINAL VOLTAGE (100% = 230 V)	MEASURED INPUT VOLTAGE (V)	EXPECTED DC CURRENT OUTPUT (mA)	MEASURED DC CURRENT OUTPUT(mA)	ERROR (%)	FULL SCALE ERROR - $ERROR_{FSR}$ (%)
10	23.0017	1.7370	1.7596	–0.01	0.00
50	115.002	8.6846	8.6935	–0.06	–0.02
100	230.014	17.3700	17.3620	–0.06	–0.04

3.2.2.2.4.2 Voltage Output Accuracy Test

The analog output is set as the bidirectional voltage output.

A 1.1-kΩ resistor is connected to the analog output. The voltage is measured using a 6½ DMM.

Table 24. DC Voltage Output Accuracy Test for AOUT0

INPUT AS % OF NOMINAL CURRENT (100% = 5 A)	MEASURED INPUT CURRENT (A)	EXPECTED DC VOLTAGE OUTPUT (V)	MEASURED DC VOLTAGE OUTPUT (V)	ERROR (%)	FULL SCALE ERROR - $ERROR_{FSR}$ (%)
200	9.9947	9.8438	9.9401	–0.13	–0.13
175	8.7449	8.6129	8.7043	–0.07	–0.06
150	7.4937	7.3805	7.4732	0.11	0.08
120	6.0026	5.912	5.9685	–0.22	–0.13
100	4.9974	4.9219	4.969	–0.26	–0.13
90	4.4998	4.4318	4.4806	–0.14	–0.06
80	3.9975	3.9371	3.9696	–0.44	–0.17
70	3.5004	3.4475	3.4811	–0.33	–0.11
60	2.9987	2.9534	2.9801	–0.44	–0.13
50	2.501	2.4633	2.487	–0.45	–0.11
40	2.0007	1.9705	1.9856	–0.75	–0.15
30	1.5006	1.478	1.4925	–0.71	–0.11
20	0.9998	0.9847	0.9909	–1.4	–0.14
10	0.4998	0.4923	0.4979	–1.9	–0.09
8	0.4	0.3940	0.3993	–2.19	–0.09
6	0.3002	0.2956	0.3012	–2.53	–0.08
4	0.2001	0.1971	0.2069	–1.13	–0.02
2	0.1001	0.0986	0.1036	–6.13	–0.06
–2	–0.1001	–0.0986	–0.0889	–0.60	0.01
–4	–0.2001	–0.197	–0.1823	–3.31	0.07
–6	–0.3	–0.2955	–0.2815	–2.32	0.07
–8	–0.4	–0.394	–0.3797	–2.04	0.08
–10	–0.5	–0.4924	–0.4783	–1.81	0.09
–20	–1.0002	–0.9851	–0.9713	–1.37	0.14
–30	–1.5008	–1.4781	–1.4778	–0.34	0.05
–40	–2.0006	–1.9703	–1.979	–0.06	0.01
–50	–2.5004	–2.4627	–2.4674	–0.41	0.1
–60	–3.0001	–2.9548	–2.9608	–0.46	0.14
–70	–3.4998	–3.4469	–3.4617	–0.28	0.1
–80	–3.9995	–3.9391	–3.9676	–0.03	0.01
–90	–4.4984	–4.4305	–4.4607	–0.1	0.04
–100	–4.9972	–4.9217	–4.9491	–0.25	0.12
–120	–5.9946	–5.9041	–5.9439	–0.16	0.1
–150	–7.4941	–7.3809	–7.4437	–0.02	0.02
–175	–8.7439	–8.6119	–8.6845	–0.05	0.04
–200	–9.995	–9.8441	–9.9208	–0.13	0.13

The gain factor for the dc voltage output accuracy test is 0.99 and the offset is 0.01 V. Figure 36 shows a plot of the dc voltage output accuracy test.

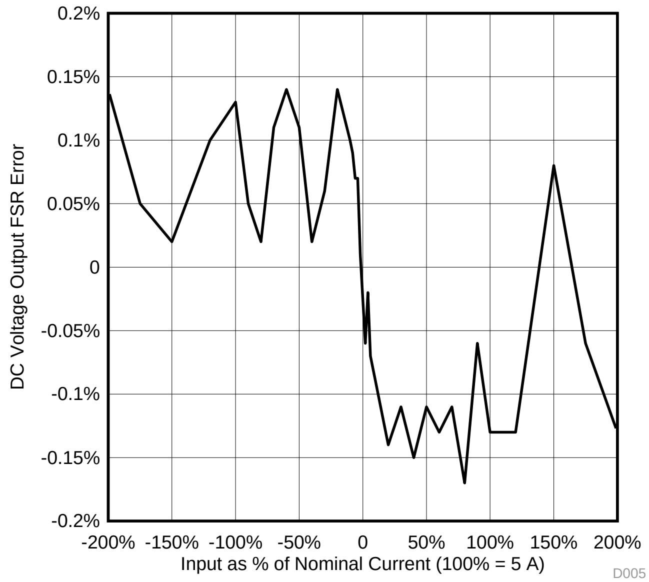

Figure 36. DC Voltage Output Accuracy Test for AOUT0

Table 25. DC Voltage Output Accuracy Test for AOUT1

INPUT AS % OF NOMINAL VOLTAGE (100% = 230 V)	MEASURED INPUT VOLTAGE (V)	EXPECTED DC VOLTAGE OUTPUT (V)	MEASURED DC VOLTAGE OUTPUT (V)	ERROR (%)	FULL SCALE ERROR – $ERROR_{FSR}$ (%)
10	23.0021	0.7159	0.7259	–0.05	0.06
50	115.001	3.5794	3.5845	–0.06	0.04
100	230.01	7.1591	7.1574	–0.08	0

The gain factor for the dc voltage output accuracy test is 1.001 and the offset is 0.011 V.

3.2.2.2.5 Analog Output Transient Response Test

The analog output is set to mid level (0 V). The command is sent through the MCU to change the output voltage level and another port pin is toggled to high (to capture the start time of the command) when the MCU command has been sent. This process captures the transient response of the DAC output and analog output in the CRO, along with the start of the command input (see Figure 37).

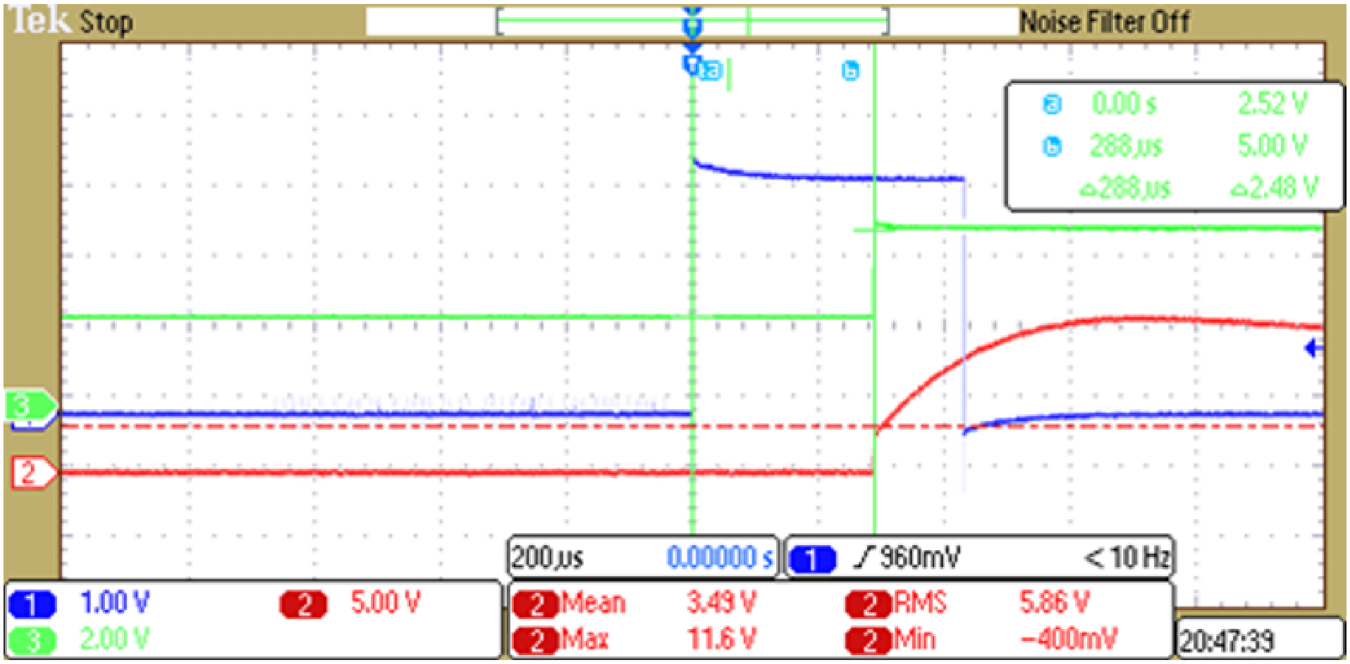

Figure 37. Transient Response (Blue = Port Pin, Green = DAC Output, Red = DC Analog Output)

3.2.2.2.6 Output Driver XTR300 Error Flag Test

The XTR300 device indicates fault conditions on the output and on the IA input in addition to the overtemperature conditions indicated by the error flags.

The EF_{LD} indicates fault conditions while driving voltage or current into the load. In voltage output mode, the EF_{LD} monitors the voltage limits of the output swing and the current limit condition caused from short- or low-load resistance. In current output mode, the EF_{LD} indicates a saturation into the supply rails from a high load resistance or open load.

The following Table 26 shows the testing for the error flag EF_{LD}.

Table 26. Load Error Flag Test (Active-Low)

SERIAL NUMBER	PARAMETERS	EXPECTED	OBSERVED
1	Current output mode: 500-Ω resistor connected	EF_{LD} = HIGH OFF)	EF_{LD} = VCC (OFF)
2	Current output mode: No (open) resistor connected	EF_{LD} = LOW (Active)	EF_{LD} = LOW (Active)
3	Voltage output mode: 1100-Ω resistor connected	EF_{LD} = HIGH (OFF)	EF_{LD} = VCC (OFF)
4	Voltage output mode:0-Ω (short) jumper connected	EF_{LD} = LOW (Active)	EF_{LD} = LOW Active)

3.2.2.2.7 AC Input Accuracy Testing at 60 Hz

3.2.2.2.7.1 Accuracy Test—Voltage Measurement

Table 27. Voltage Channel 1

INPUT AS % OF NOMINAL VOLTAGE (100% = 230 V)	MEASURED INPUT VOLTAGE (V)	MEASURED OUTPUT VOLTAGE (V)	ERROR (%)
10	22.9988	22.973	0.1
50	114.938	114.982	0.08
100	229.996	230.209	0.11

The gain factor for voltage channel 1 is 1 and the offset is –0.048 V.

Table 28. Voltage Channel 2

INPUT AS % OF NOMINAL VOLTAGE (100% = 230 V)	MEASURED INPUT VOLTAGE (V)	MEASURED OUTPUT VOLTAGE (V)	ERROR (%)
10	22.9988	22.976	0.11
50	114.938	114.996	0.09
100	229.996	230.236	0.13

The gain factor for voltage channel 2 is 1 and the offset is –0.048 V.

Table 29. Voltage Channel 3

INPUT AS % OF NOMINAL VOLTAGE (100% = 230 V)	MEASURED INPUT VOLTAGE (V)	MEASURED OUTPUT VOLTAGE (V)	ERROR (%)
10	22.9988	22.974	0.1
50	114.938	114.986	0.08
100	229.996	230.218	0.12

The gain factor for voltage channel 3 is 1 and the offset is –0.048 V.

3.2.2.2.7.2 Accuracy Test—Current Measurement

Table 30. Current Channel 1

INPUT AS % OF NOMINAL CURRENT (100% = 5 A)	MEASURED INPUT CURRENT (A)	MEASURED OUTPUT CURRENT (A)	ERROR (%)
10	0.500126	0.500039	–0.02
50	2.50136	2.50056	–0.03
100	5.00138	4.99763	–0.07

The gain factor for current channel 1 is 1.

Table 31. Current Channel 2

INPUT AS % OF NOMINAL CURRENT (100% = 5 A)	MEASURED INPUT CURRENT (A)	MEASURED OUTPUT CURRENT (A)	ERROR (%)
10	0.500126	0.499743	0.02
50	2.50136	2.49905	0.01
100	5.00138	4.99482	–0.03

The gain factor for current channel 2 is 1.001.

Table 32. Current Channel 3

INPUT AS % OF NOMINAL CURRENT (100% = 5 A)	MEASURED INPUT CURRENT (A)	MEASURED OUTPUT CURRENT (A)	ERROR (%)
10	0.500126	0.499624	0
50	2.50136	2.49887	0
100	5.00138	4.99172	–0.09

The gain factor for current channel 3 is 1.001.

3.2.2.3 Summary of Test Results

Table 33. Test Results

SERIAL NUMBER	PARAMETERS	RESULT
1	Isolated power supply output 5.5 V	Ok
2	Non-Isolated power supply output 3.3 V	Ok
3	Digital output	Ok
4	Input phase selection for dc analog output	Ok
5	DC analog output—current or voltage selection	Ok
6	AC input voltage measurement accuracy	Ok
7	AC input current measurement accuracy	Ok
8	DAC output accuracy	Ok
9	DC analog output accuracy	Ok
10	DC analog output transient response	Ok
11	DC analog output error flag test	Ok

4 Design Files

4.1 Schematics

To download the schematics for each board, see the design files at TIDA-00454.

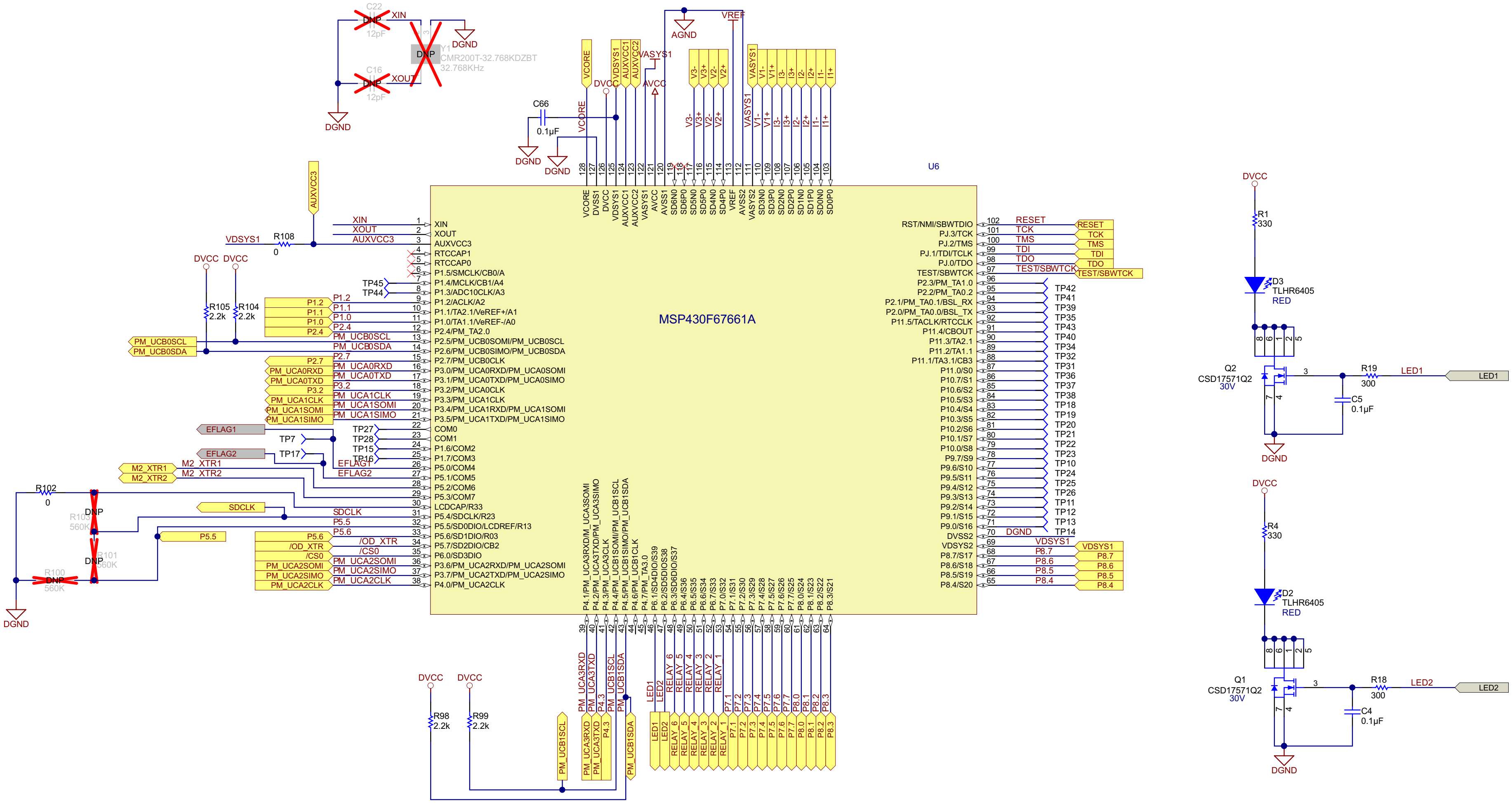

Figure 38. TIDA-00454 Schematic Page 1

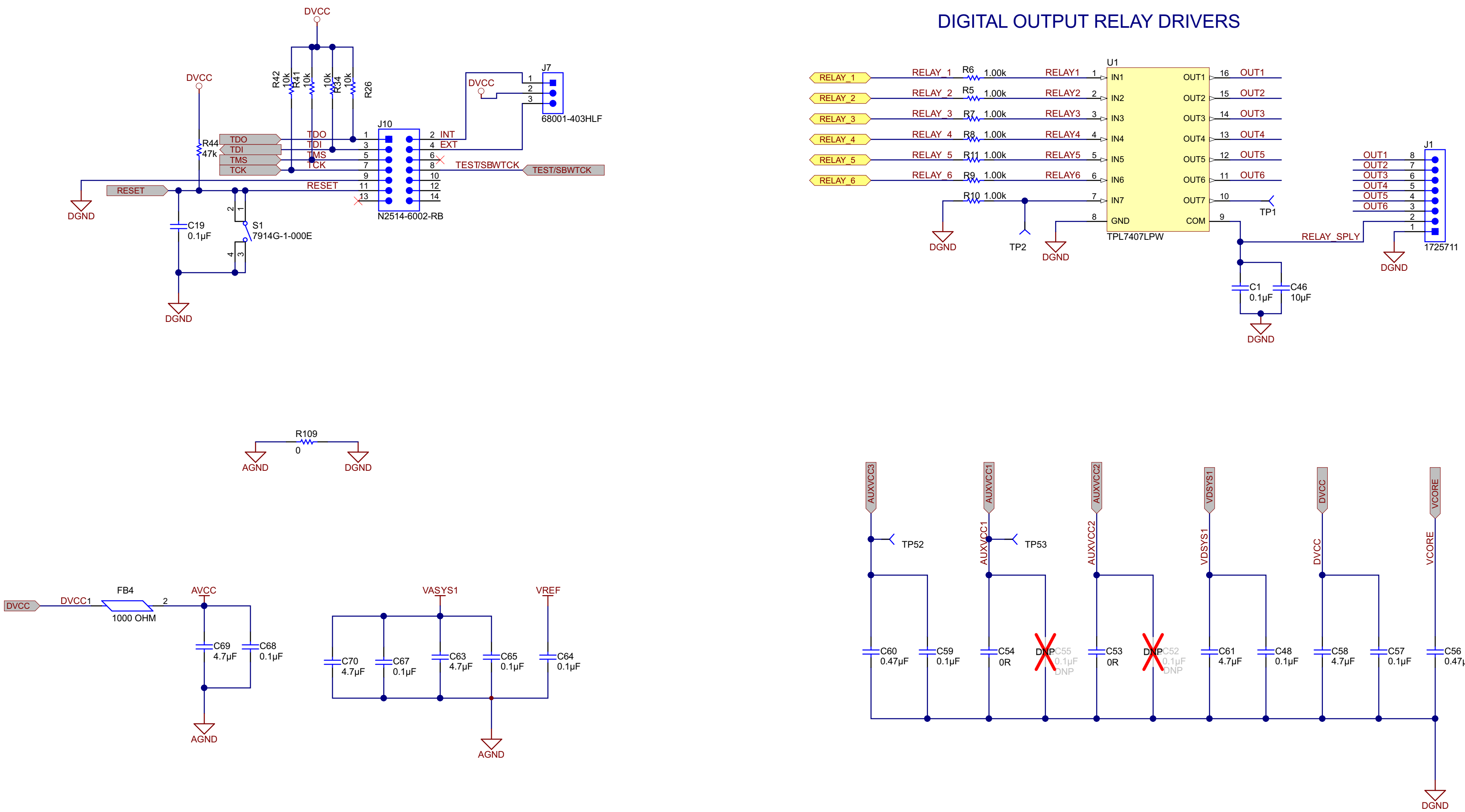

Figure 39. TIDA-00454 Schematic Page 2

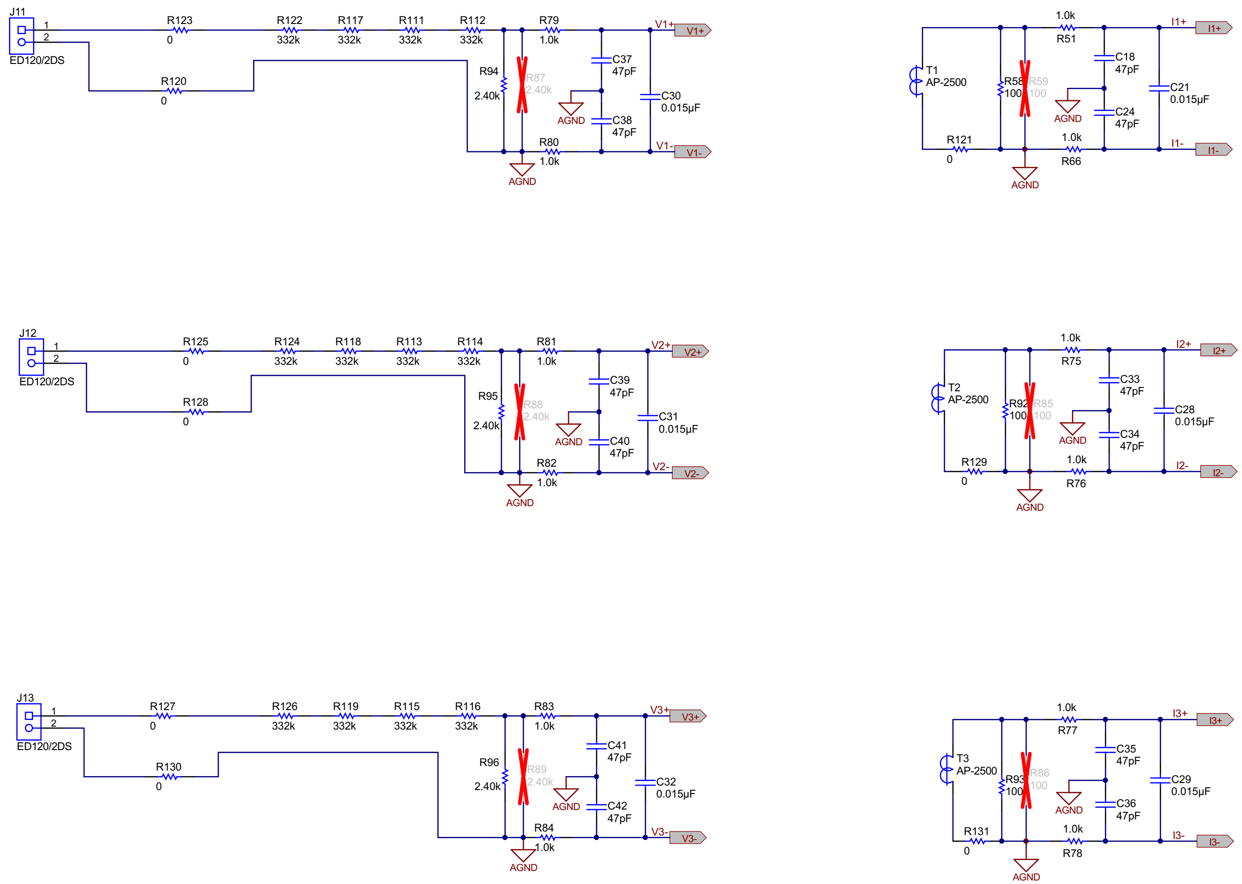

Figure 40. TIDA-00454 Schematic Page 3

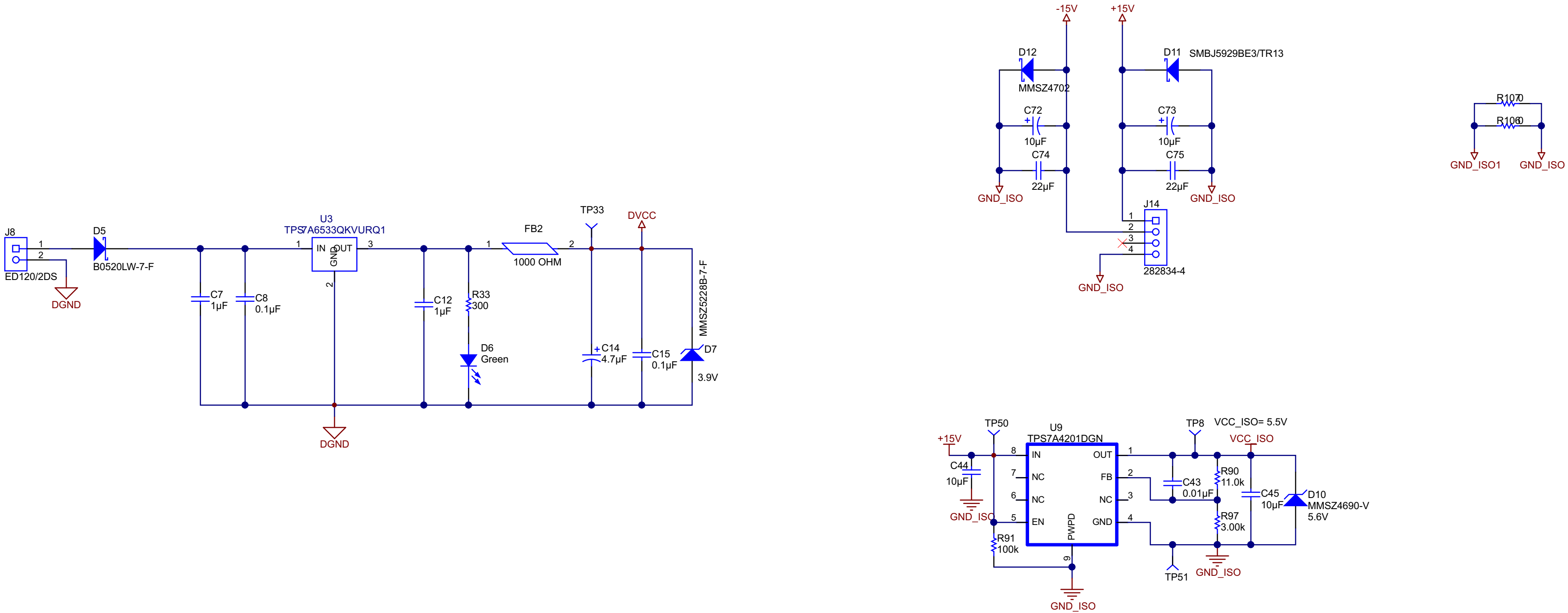

Figure 41. TIDA-00454 Schematic Page 4

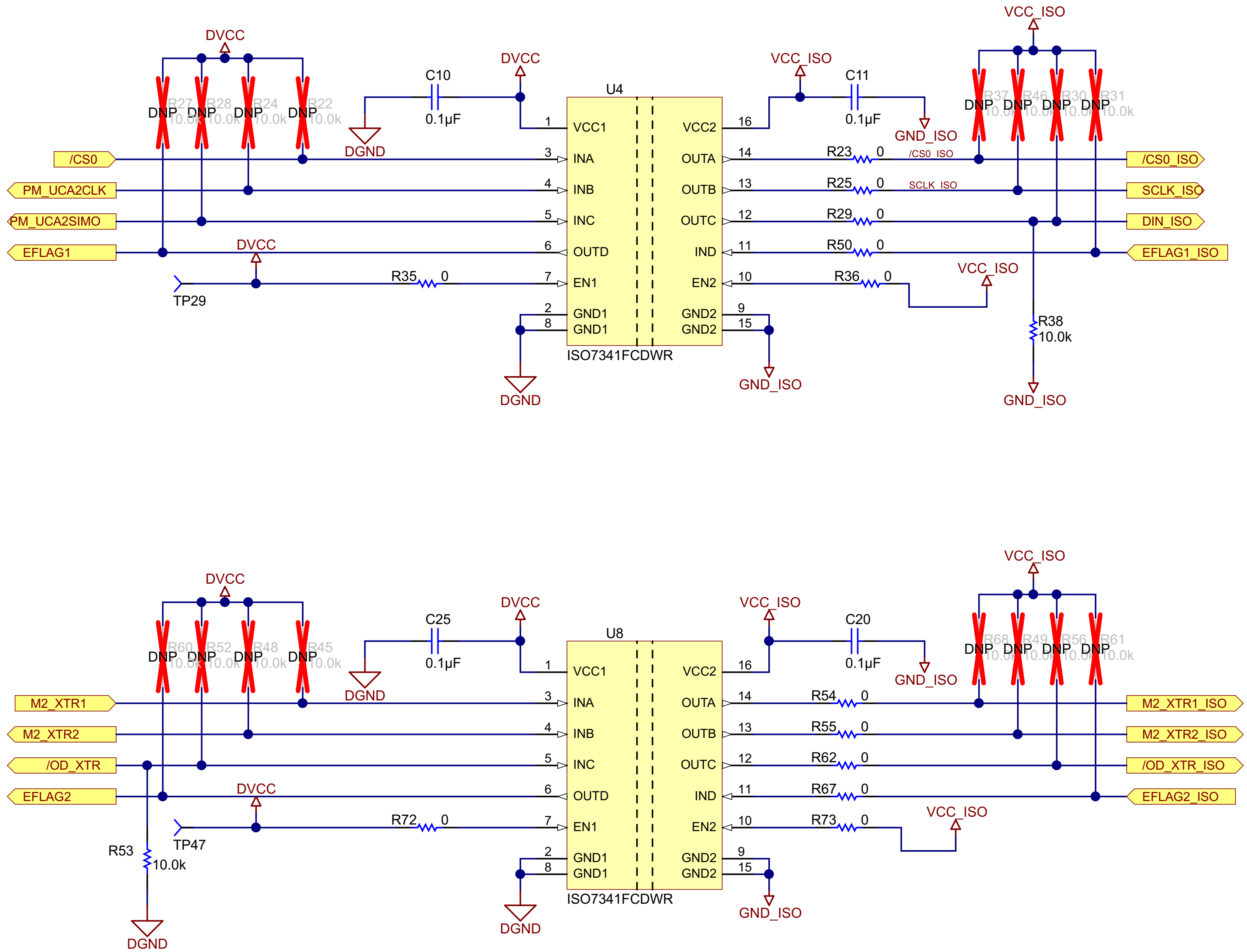

Figure 42. TIDA-00454 Schematic Page 5

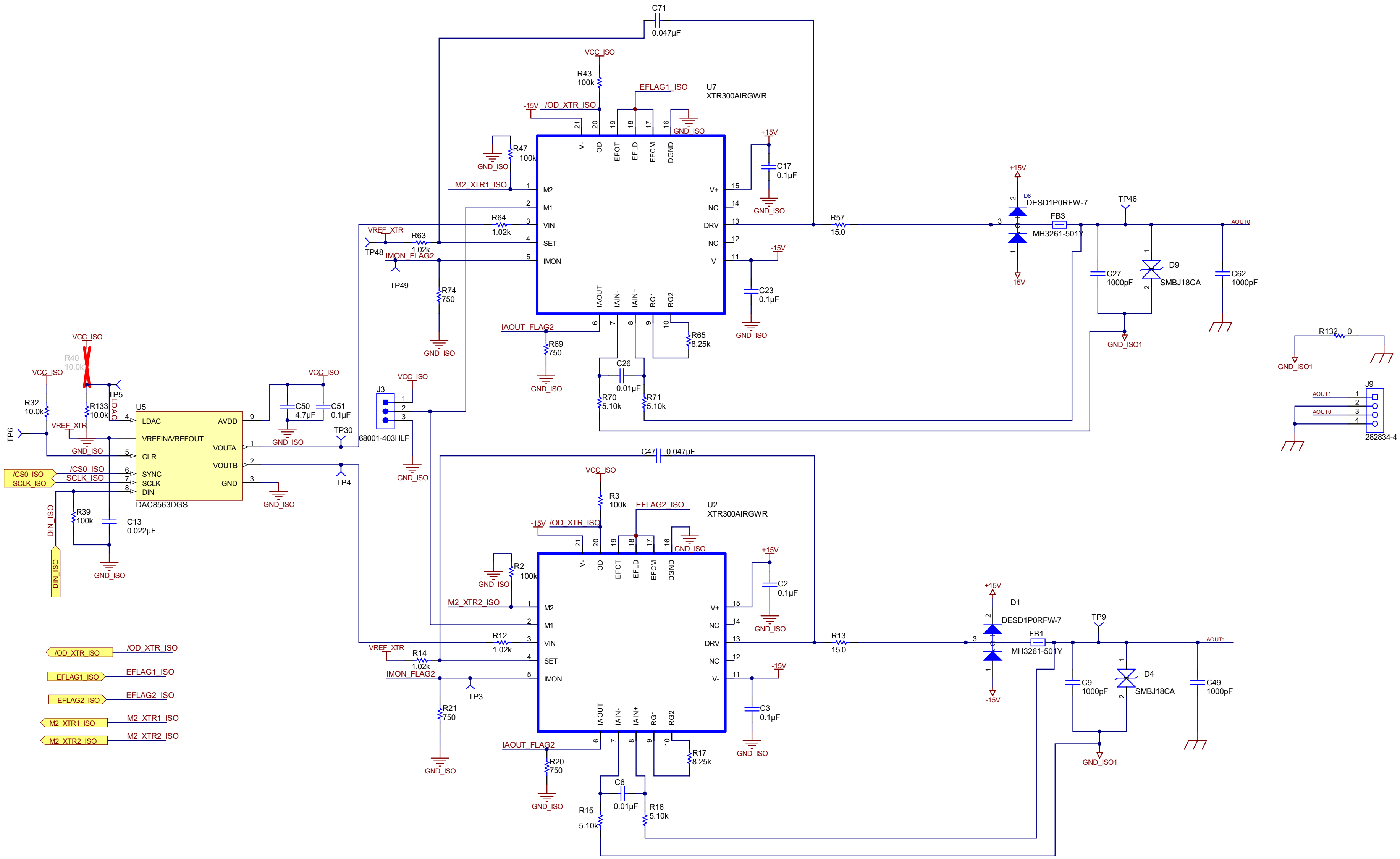

Figure 43. TIDA-00454 Schematic Page 6

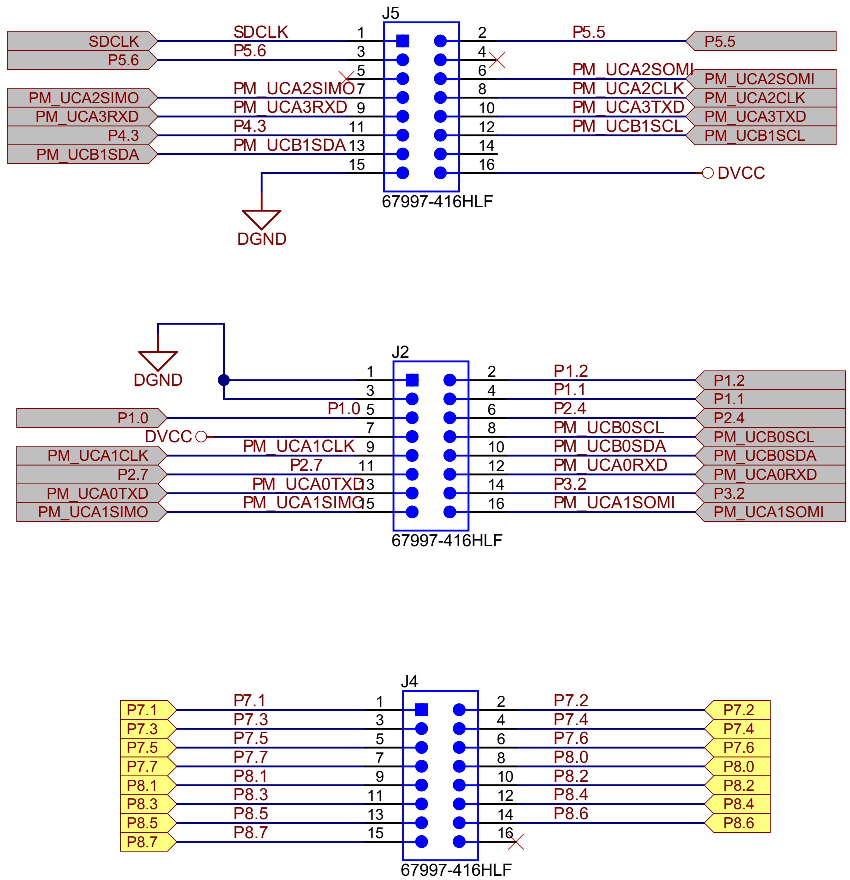

Figure 44. TIDA-00454 Schematic Page 7

4.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-00454.

4.3 PCB Layout Recommendations

To download the layout prints for each board, see the design files at TIDA-00454 .

4.4 Altium Project

To download the Altium Designer® project files for each board, see the design files at TIDA-00454.

4.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00454.

4.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-00454.

5 Software Files

To download the software files, see the design files at TIDA-00454.

6 Related Documentation

- *Two - Channel Source/Sink Combined Voltage & Current Output, Isolated, EMC/EMI Tested Reference Design*
- *WEBENCH® Design Center*
- *TI E2E Community*

6.1 Trademarks

Altium Designer is a registered trademark of Altium LLC or its affiliated companies.

7 Terminology

CT— Current transformer

FSR— Full-scale range

ADC— Analog-to-digital converter

DAC— Digital-to-analog converter

8 About the Authors

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2015) to A Revision **Page**

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