TI Designs

Reference Design of an Efficient High V_I AMOLED Supply for Consumer Display Applications

Description

Currently, all AMOLED display supply devices from TI are restricted to an input voltage of lower than 5 V. However, the demand rises up to supply these panels directly from the input supply in notebook PC or tablet PC applications where the input voltage ranges between 6 and 21 V or even more. This reference design offers a solution for such applications by using the AMOLED bias device TPS65635 and an additional pre-regulator (buck-converter), the TPS54302. The optional enable logic ensures low shutdown current.

Resources

PMP9800	Design Folder
TPS65635	Product Folder
TPS54302	Product Folder
SN74LVC2G132	Product Folder
SN74LVC1G104	Product Folder
PMP9782	Tools Folder

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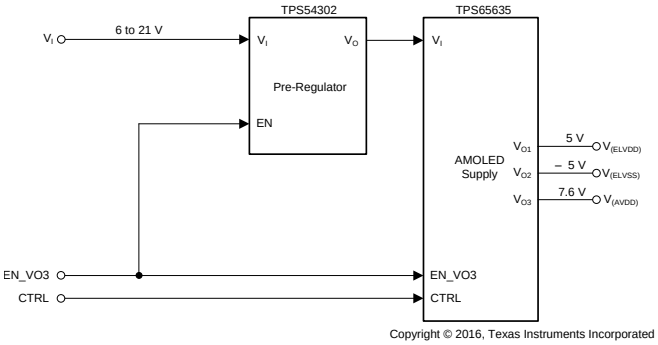
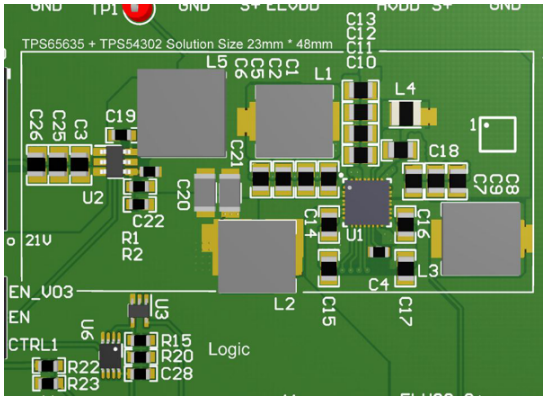
Features

- High Efficiency > 90 %
- Input Voltage From 6 to 21 V
- Small Solution Size
- High Output Current Capability (up to 1.4 A)
- Cost Reduction
- Enable Logic for Power Sequencing
- Improved EMI Performance

Applications

- Notebook PCs (NBPCs)
- Tablets





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1 System Overview

1.1 System Description

To support higher input voltages, it is necessary to add a pre-regulator in front of the TPS65635. For highest efficiency, the TPS54302 device is suggested. This converter is configured to generate an output voltage of 4.7 V, which is the supply voltage for the TPS65635. The implementation is based on the TPS54302 user's guide (SLVUAP9). For a detailed design description, see the TPS54302 datasheet (SLVSDG6).

In some applications, a charge-pump in the source driver generates $V_{(AVDD)}$. Therefore, $V_{(AVDD)}$ is not used and only $V_{(ELVSS)}$ has to be programmed. In this case, see Figure 2. The enable circuitry is required to filter out the program pulses of the CTRL signal with the advantage that the CTRL signal can be used to enable the pre-regulator.

1.1.1 TPS65635

The TPS65635 integrates a boost converter for the $V_{(AVDD)}$ rail, a boost converter for the $V_{(ELVDD)}$ rail, and an inverting buck-boost converter to provide $V_{(ELVSS)}$. As this device is originally designed to supply battery operated products the input voltage ranges from 2.9 to 4.7 V.

1.1.2 TPS54302

The TPS54302 device is a 3-A synchronous buck converter and focuses on high efficiency. The device includes two integrated switching MOSFET's and an internal loop compensation. The device requires only eight additional external components. As the MOSFETs are integrated and employs a SOT-23 package, the TPS54302 achieves high power density and offers a small footprint on the PCB.

Additionally, the device introduces a frequency spread spectrum operation and therefore improves the EMI performance.

1.2 Key System Specifications

The key system specification from the TPS65635 plus the TPS54302 are set as the following:

- Input supply voltage V_I of 6 to 21 V
- Output voltage of the TPS54302 device of 4.7 V
- Output voltages of the TPS65635:
  - A positive supply voltage $V_{(AVDD)}$ for the display source driver of 7.6 V at up to 90 mA
  - A positive supply voltage $V_{(ELVDD)}$ for the OLEDs of 5 V at up to 1.4 A
  - A negative supply voltage $V_{(ELVSS)}$ for the OLEDs of −5 V at up to 1.4 A

This TI Design operates with a wide range of input supply voltages. Table 1 shows the input supply voltages typically used by the target applications.

Table 1. Typical Input Supply Voltage Ranges

APPLICATION	INPUT VOLTAGE RANGE
NBPC	2s Li-Ion battery + mains adapter: 6 V < V_I < 21 V
	3s Li-Ion battery + mains adapter: 9 V < V_I < 21 V
Tablet	2s Li-Ion battery: 6 V < V_I < 12 V

1.3 Block Diagram

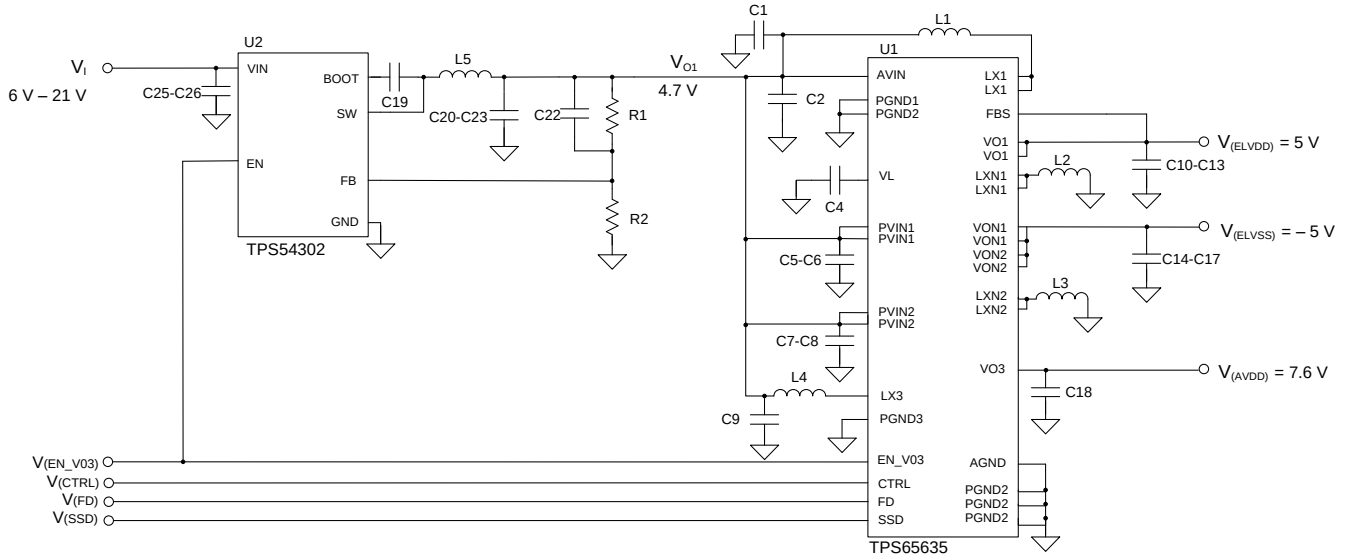

Figure 1. Schematic Overview Configuration With AVDD Required

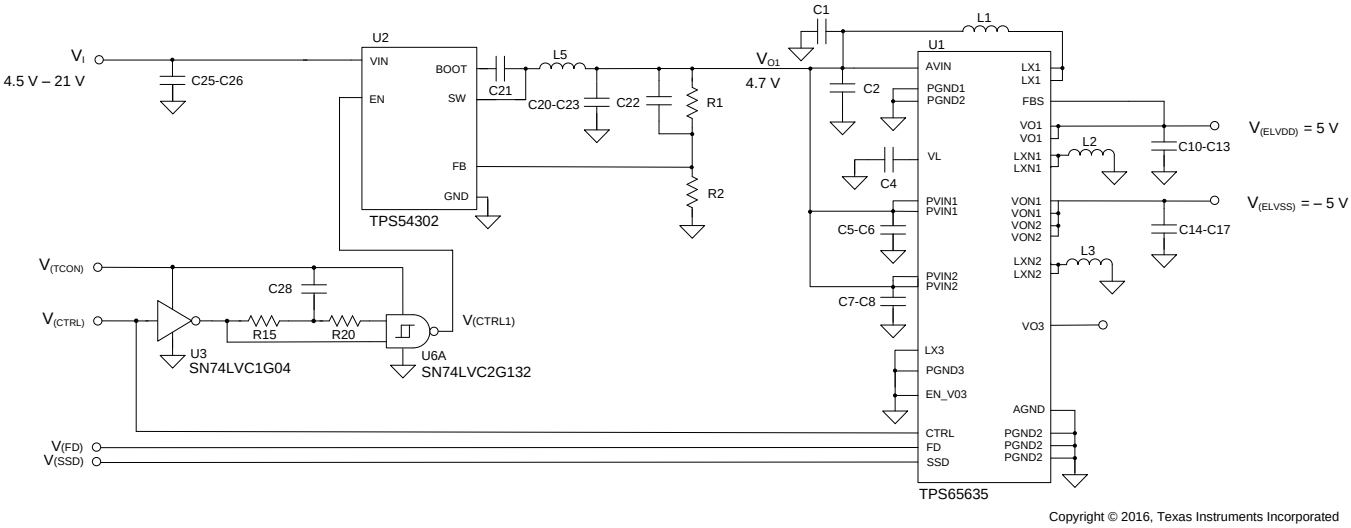

Figure 2. Schematic Overview Configuration Without AVDD Required With Enable Logic

1.4 Highlighted Products

The reference design for AMOLED display applications that are supplied by high input voltages of up to 21 V features the following devices.

1.4.1 TPS65635

- Triple output AMOLED bias supply device
- Output current capability of up to 1.4 A

1.4.2 TPS54302

- Synchronous buck converter with integrated switching FETs
- EMI friendly due to frequency spread spectrum

1.4.3 SN74LVC2G132

- Dual 2-input NAND gate with Schmitt-trigger inputs
- NanoFree package available

1.4.4 SN74LVC1G04

- Single inverter gate
- Ultra-small DPW package available

2 Testing and Results

2.1 Test Setup

This section describes how to set up the proposed design correctly. This refers to Figure 3.

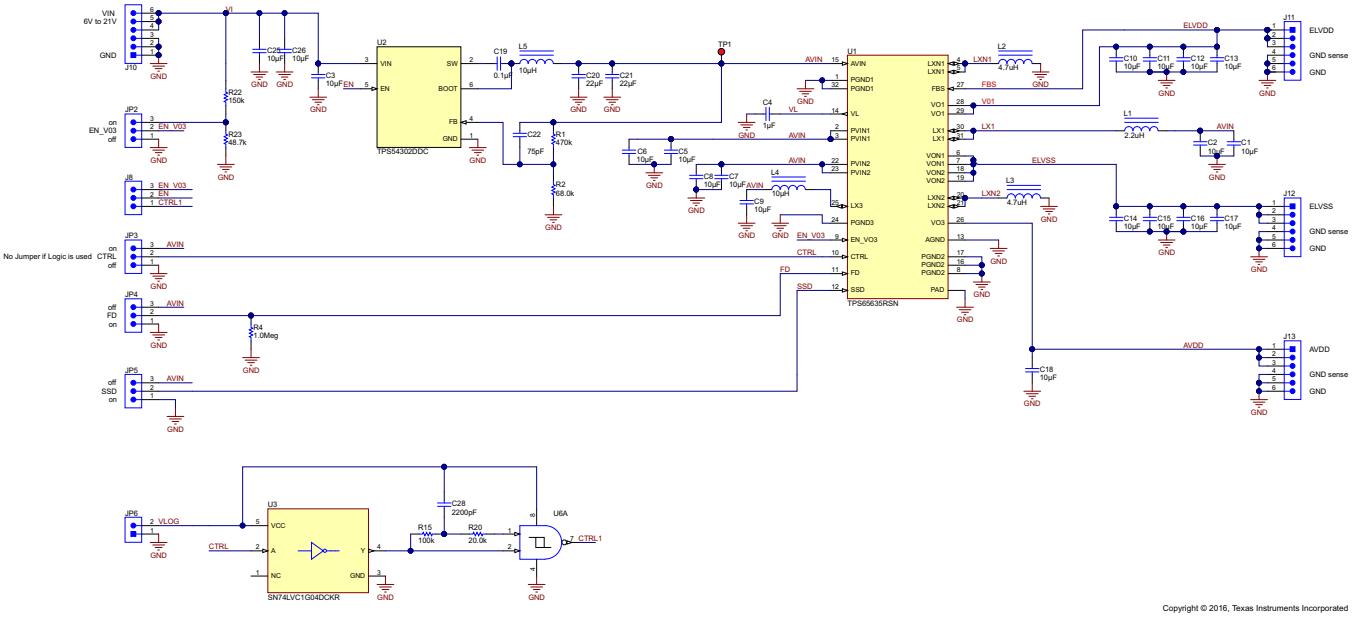

Figure 3. Schematic PMP9800 AMOLED Supply

2.1.1 Power Supply

Connect the power supply between pin 1, 2, 3 and pin 4, 5, 6 of jumper J10. For an accurate operation use a four-terminal connection. To minimize the parasitic inductance, TI recommends to use a short cable (less than 20 cm), twist the power (pin 1, 2, 3) and the return (pin 4, 5, 6) conductors together.

2.1.1.1 Load Condition

The connection of the loads of the AMOLED device must only be connected when the power supply has been switched on and the converters TPS54302 and TPS65635 are in regulation. To verify whether they are in regulation, measure the pre-regulator output voltage of test point TP1 and on Jumper J11, J12 and J13 for the output voltages of the AMOLED part.

It is crucial that both converters are in regulation before you can program the TPS65635. After confirming that both converters are in regulation, add the load:

- For $V_{(ELVDD)}$ between pin 1, 2, 3 and 4, 5, 6 of Jumper J11.
- For $V_{(ELVSS)}$ between pin 1, 2, 3 and 4, 5, 6 of Jumper J12
- For $V_{(AVDD)}$ between pin 1, 2, 3 and 4, 5, 6 of Jumper J13

2.1.2 Jumper Settings

There are few jumpers on the proposed schematic that can be set according to the application requirement. The main different application requirements and the according jumper settings are listed in Table 2:

Table 2. Jumper Settings

REQUIREMENT	ENABLE SIGNAL	JUMPER SETTING	REMARKS
$V_{(AVDD)}$ required	External signal EN_V03 controls the TPS54302 and the $V_{(AVDD)}$ rail of the TPS65635	J8: EN = External EN_V03	Connect a jumper between pin 3 and pin 2 of jumper J8.
		JP2: Not connected	Do not connect a jumper on jumper JP2.
		JP3: As required	Use JP3 as standard enable jumper or connect an external signal CTRL on pin 2.
	Input supply controls the TPS54302 and the $V_{(AVDD)}$ rail of the TPS65635	J8: EN = EN_V03	Connect a jumper between pin 3 and pin 2 of jumper J8.
		JP2: EN_V03 = on	Connect a jumper between pin 3 and pin 2 of jumper JP2.
		JP3: As required	Use JP3 as standard enable jumper or connect an external signal CTRL on pin 2.
$V_{(AVDD)}$ not required	Program signal controls the TPS54302 and the $V_{(ELVDD)}$ or $V_{(ELVSS)}$ rail of the TPS65635[1]	J8: EN = CTLR1	Connect a jumper between pin 2 and pin 1 of jumper J8.
		JP2: EN_V03 = off	Connect a jumper between pin 2 and pin 1 of jumper JP2.
		JP3: CTRL = external	To program, connect the program signal on pin 2 of jumper JP3.
		JP6: VLOG = 3.3 V – 5 V	Connect a power supply 3.3-V on pin 2 and GND on pin 1 of jumper JP6.
Fast discharge	—	JP4: FD = off	If fast discharge is not required, connect a jumper between pin 3 and pin 2 of jumper JP4.
		JP4: FD = on	If fast discharge is required, connect a jumper between pin 2 and pin 1 of jumper JP4.
Start-up short detection	—	JP5: SSD = off	If start-up short detection is not required, connect a jumper between pin 3 and pin 2 of jumper JP4.
		JP5: SSD = on	If fast discharge is required, connect a jumper between pin 2 and pin 1 of jumper JP4.

(1) If programming is not needed, the CTRL pin can be used as a standard enable pin. In this case, connect a jumper between pin 3 and pin 2 or between pin 1 and pin 2 to enable or disable the output voltages $V_{(ELVDD)}$ and $V_{(ELVSS)}$.

2.1.3 Programming

The TPS65635 can be programmed according to the device's datasheet on (SLVSCI9). The programming is necessary to:

- Change the output voltage of $V_{(AVDD)}$ or $V_{(ELVSS)}$
- Change the overcurrent detection value

2.1.4 Power Sequencing

The output of the pre-regulator and the outputs of the AMOLED supply have external enable pins that needs to be set accordingly. This TI Design offers an enable logic where the user can omit one unnecessary signal that is the enable signal for the pre-regulator. The following subsections describe the power sequence possibilities for different cases.

2.1.4.1 $V_{(AVDD)}$ Required: EN = EN_VO3

If the application does require the $V_{(AVDD)}$ rail, then there are two choices to power on the system. The first choice is to use the dedicated enable signal EN_VO3 to enable the pre-regulator that sequentially powers-on the $V_{(AVDD)}$ rail of the AMOLED device when the interrail voltage V_{O1} of 4.7 V has been achieved. To use this setting:

1. Connect a jumper between pin 3 and pin 2 of jumper J8.
2. Do not connect a jumper on jumper JP2.
3. Connect the external EN_VO3 signal on pin 2 of Jumper JP2.
4. Use jumper JP3 either as a standard enable pin or connect an external signal on pin 2 to program the TPS65635 device.

The $V_{(ELVDD)}$ and $V_{(ELVSS)}$ rails need to be enabled separately by the CTRL signal. For reliable operation, keep the CTRL pin low for about 5 ms until the output voltage of the pre-regulator and the $V_{(AVDD)}$ rail of the TPS65635 is in regulation. The first rising edge of the CTRL signal will start the power-on sequence of $V_{(ELVDD)}$ and $V_{(ELVSS)}$. The $V_{(ELVSS)}$ inverting buck-boost converter begins with –5 V default value 10 ms after the CTRL pin goes high.

If the EN_V03 signal is set to low, it takes about 11 ms until the $V_{(AVDD)}$ rail is powered off. Disable the $V_{(ELVDD)}$ and $V_{(ELVSS)}$ rail after this.

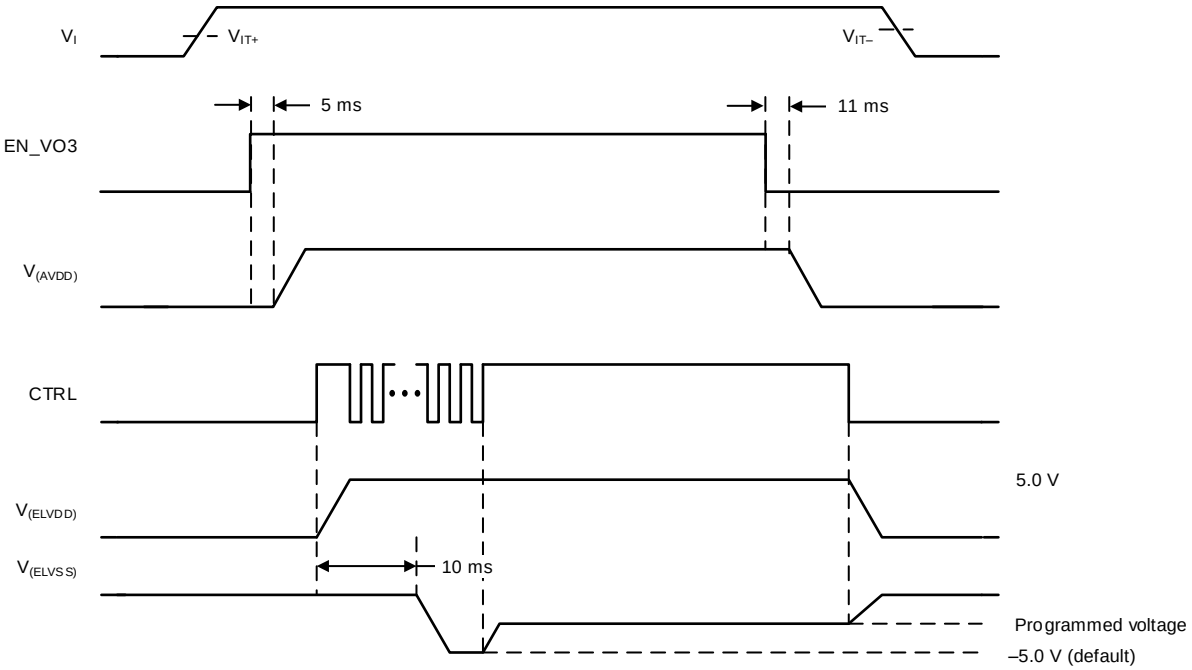

Figure 4. Power-On and Power-Off Sequence With Dedicated EN_V03 Signal

The second choice is to use the input voltage V_I and automatically enable the power-on sequence. To use this setting:

1. Connect a jumper between pin 3 and pin 2 of jumper JP2.
2. Connect a jumper between pin 3 and pin 2 of jumper J8.
3. Use jumper JP3 either as a standard enable pin or connect an external signal on pin 2 to program the TPS65635 device.

The controlling of the $V_{(ELVDD)}$ and $V_{(ELVSS)}$ rails have to be handled the same way as in the first choice setting.

If the application requires $V_{(AVDD)}$, the enable logic is not needed. This means the user do not need to connect a supply voltage $V_{(LOG)}$ on JP6. Short out CTLR1 to CTRL by connecting pin 1 of Jumper J8 to pin 2 of jumper JP3 to power on the pre-regulator and sequentially the AMOLED bias device.

2.1.4.2 $V_{(AVDD)}$ Not Required: EN = CTRL1

If the application does not require the $V_{(AVDD)}$ rail, then use the CTRL signal as an enable signal to power on and power off the system. In this case, the enable circuit is required to filter out the program pulses of the CTRL signal. To use this setting:

1. Connect a jumper between pin 2 and pin 1 of jumper J8.
2. Do not connect a jumper on jumper JP2.
3. Connect the program signal CTRL on pin 2 of Jumper JP2.
4. Connect a supply voltage $V_{(LOG)}$ on pin 2 of jumper JP6 and GND on pin 1.

If CTRL pin goes high, it takes about 5 ms until the output voltage of the pre-regulator and the $V_{(ELVDD)}$ rails of the TPS65635 is in regulation. The $V_{(ELVSS)}$ inverting buck-boost converter begins with the –5 V default value 15 ms after the CTRL pin goes high. When the CTRL pin goes low, the output voltages of the TPS65635 will shut down immediately.

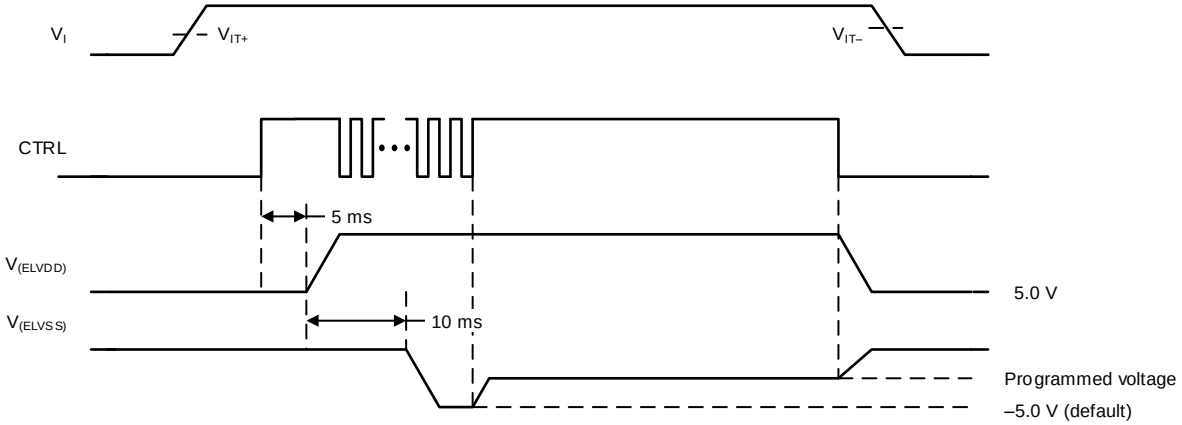

Figure 5. Power-On and Power-Off Sequence With Dedicated CTRL Signal

shows a circuit that enables the pre-regulator with the program signal CTRL. For a detailed description of this circuit, see the application report *A Wide-VI AMOLED Supply for NBPC, Tablet and Automotive Display Applications* (SLVA731).

2.2 Test Data

The application circuit of the AMOLED bias supply device TPS65635 and the pre-regulator TPS54302 were evaluated. The following graphs show the efficiency, the different power-on and power-off sequences, the line and load transient performance, and the output voltage ripple of the AMOLED bias rails.

2.2.1 Efficiency

The following curves show the efficiency of the circuit in case $V_{(AVDD)}$ is not required (see Section 2.1.4.2). The load during this evaluation is connected between $V_{(ELVDD)}$ and $V_{(ELVSS)}$.

In some applications it appears that there is a strict height constraint for the components. The limiting parameter for these requirements is the inductor for the pre-regulator. It needs to be considered that smaller (thinner) inductors comes with higher DC resistance and therefore with lower efficiency. The following figures show the efficiency of three different solution sizes. The chosen inductors are:

Table 3. Inductor Selection for Efficiency Measurement

SUPPLIER	PART NUMBER	INDUCTANCE	PACKAGE SIZE (L × H × W)	DCR (TYP)
Wurth Elektronik	7447714100	10 µH	10 × 5 × 10 mm	23 mΩ
Coilcraft	XAL7030-102ME	10 µH	6.5 × 3.1 × 6.5 mm	57 mΩ
Cyntec	HBELE061E-100MS-11	10 µH	6.1 × 1.5 × 6.1 mm	114 mΩ

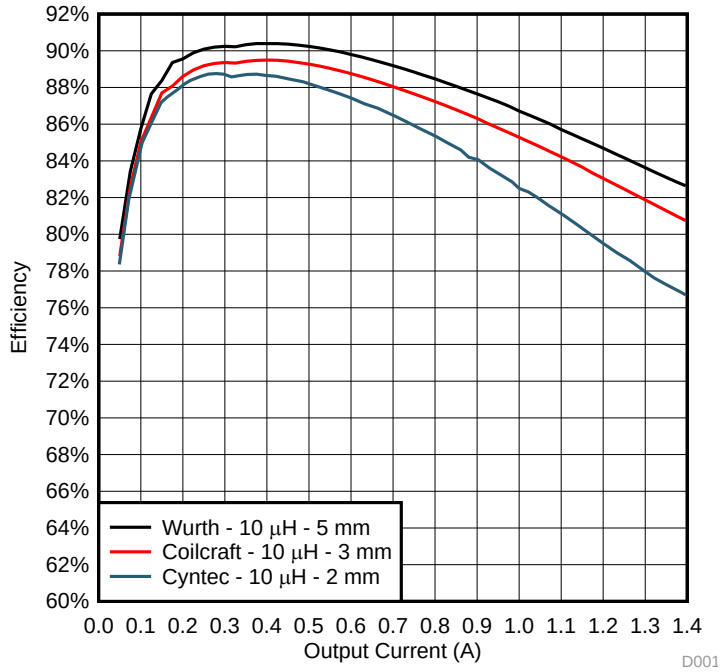

Figure 6. Efficiency versus Output Current

NOTE: V_I = 12 V, No load on $V_{(AVDD)}$, $V_{(ELVDD)}$ = 5 V, $V_{(ELVSS)}$ = – 5 V, FD = SSD = ON, T_A = 25 °C

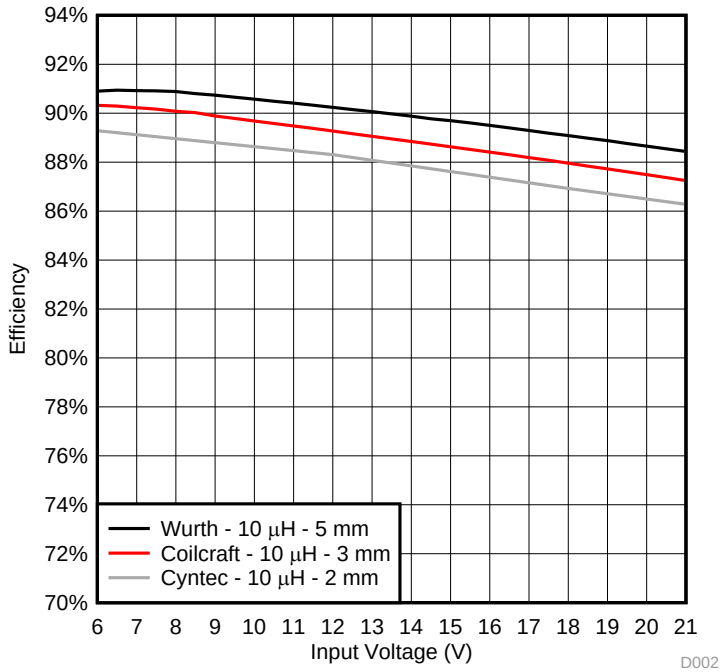

Figure 7. Efficiency versus Input Voltage

NOTE: $I_{(ELVDD-ELVSS)}$ = 500 mA, No load on $V_{(AVDD)}$, $V_{(ELVDD)}$ = 5 V, $V_{(ELVSS)}$ = – 5 V, FD = SSD = ON, T_A = 25 °C

2.2.2 Power Sequencing

As described in Section 2.1.4, the enable signal of the pre-regulator can be controlled either by the enable signal for the $V_{(AVDD)}$ rail or by the program signal for the $V_{(ELVDD)}$ and $V_{(ELVSS)}$ rails. Figure 8 and Figure 9 show the power-on and power-off sequences of these cases.

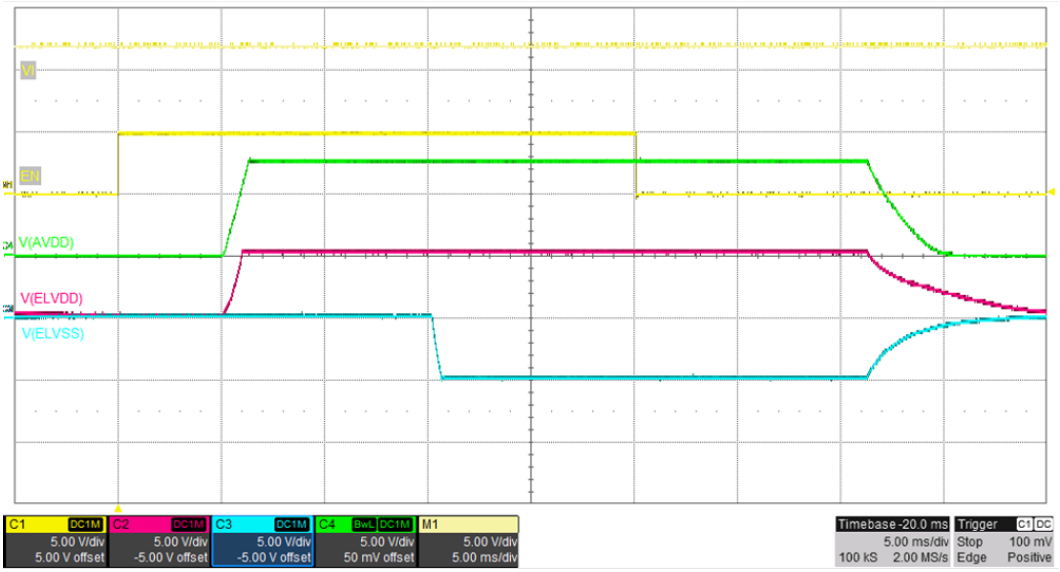

Figure 8. Power-On and Power-Off Sequence With $V_{(AVDD)}$

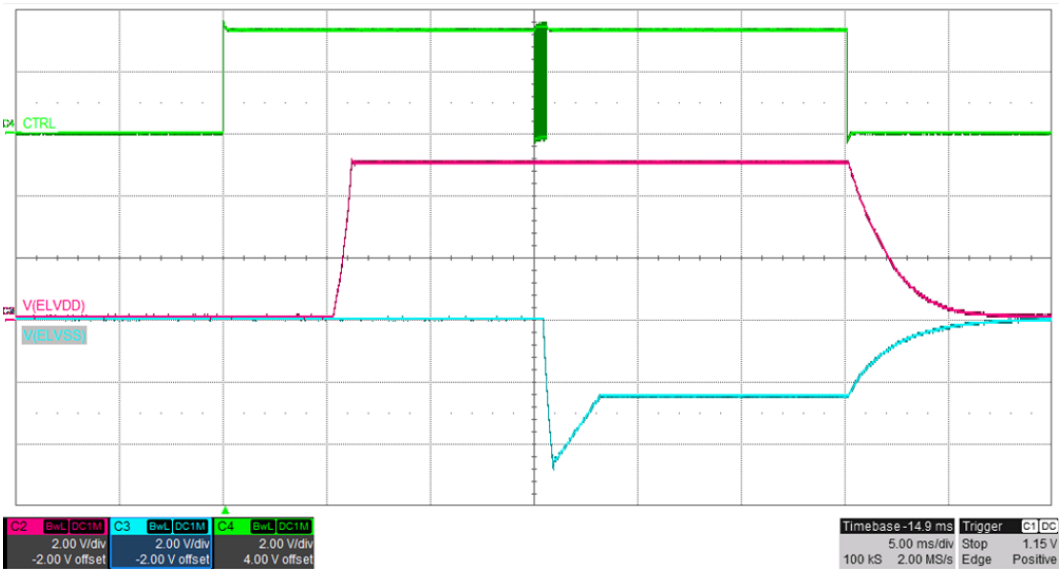

Figure 9. Power-On and Power-Off Sequence Without $V_{(AVDD)}$

NOTE: This power-up sequence shows an example when $V_{(ELVSS)}$ is programmed at the time when the inverting buck-boost converter starts to regulate. As soon as the CTRL pin goes high the converter regulates to its default output voltage of –5 V and only after that the programmed value of 2.4 V will be set.

2.2.3 Line Transient Response

Figure 10 show the line transient response of the circuit under the given condition.

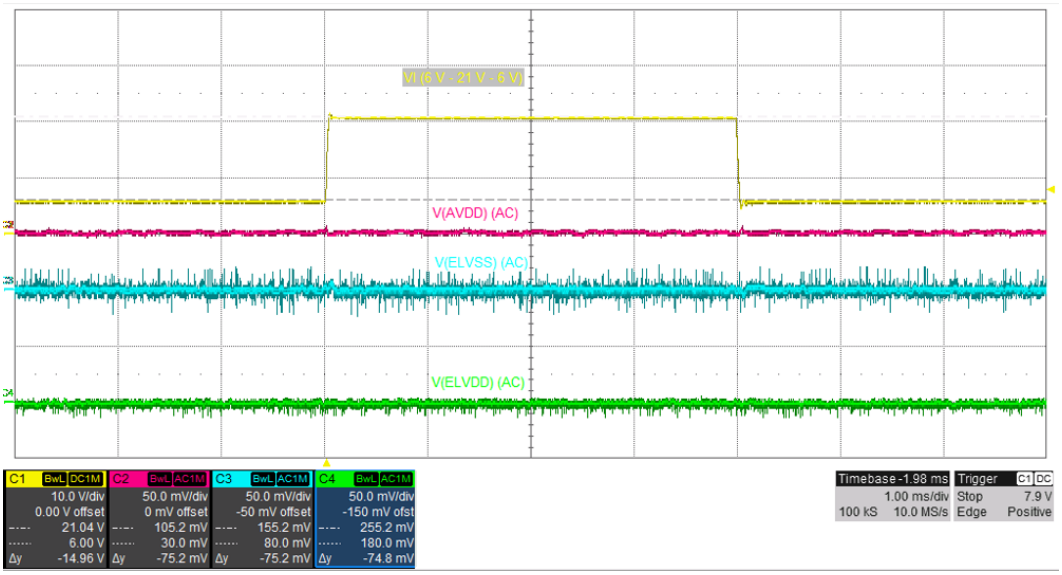

Figure 10. Line Transient Response

NOTE: $I_{(ELVDD-ELVSS)}$ = 500 mA, $I_{(AVDD)}$ = 50 mA, V_I = 6 to 21 V, $t_{r(VI)}$ = $t_{f(VI)}$ = 30 µs

2.2.4 Load Transient Response

Figure 11 through Figure 14 show the load transient response of the circuit under the given condition.

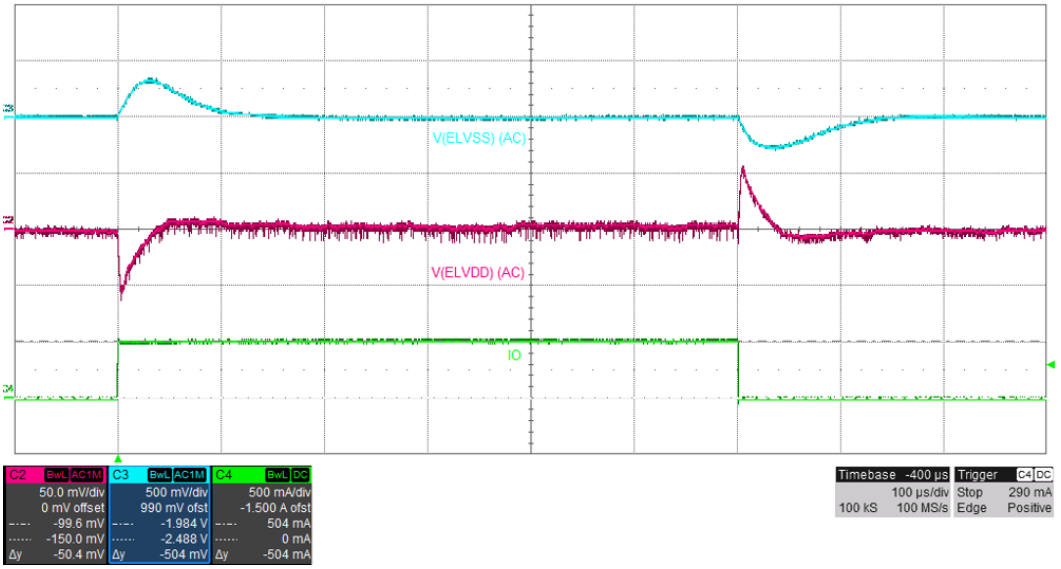

Figure 11. Load Transient Response of $V_{(ELVDD)}$ and $V_{(ELVSS)}$

NOTE: V_I = 12 V, $I_{(ELVDD-ELVSS)}$ = 0 to 500 mA, $t_{r(VI)}$ = $t_{f(VI)}$ = 1 µs

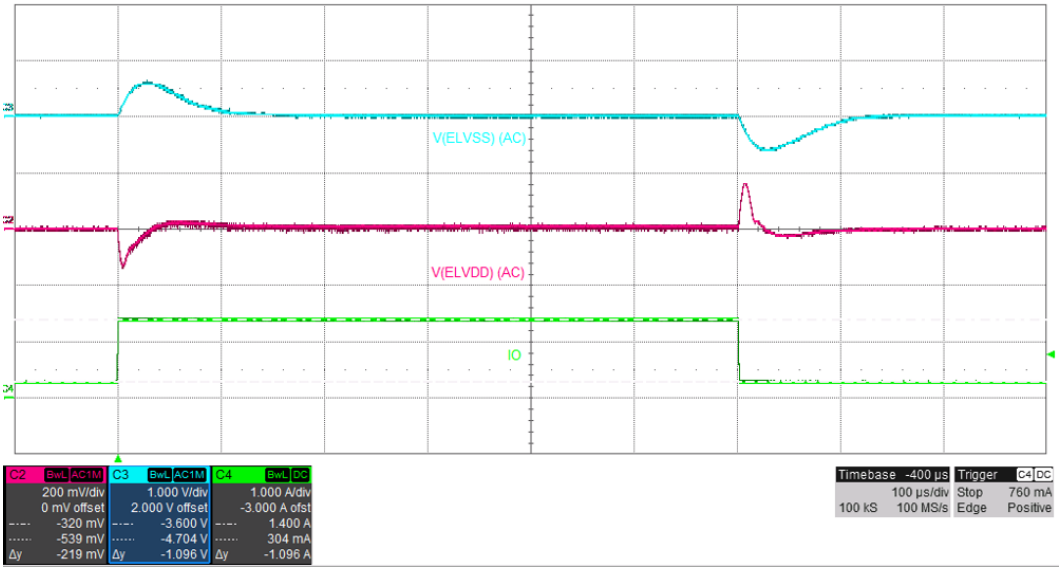

Figure 12. Load Transient Response of $V_{(ELVDD)}$ and $V_{(ELVSS)}$

NOTE: V_I = 12 V, $I_{(ELVDD-ELVSS)}$ = 300 to 1400 mA, $t_{r(VI)} = t_{f(VI)}$ = 1 µs

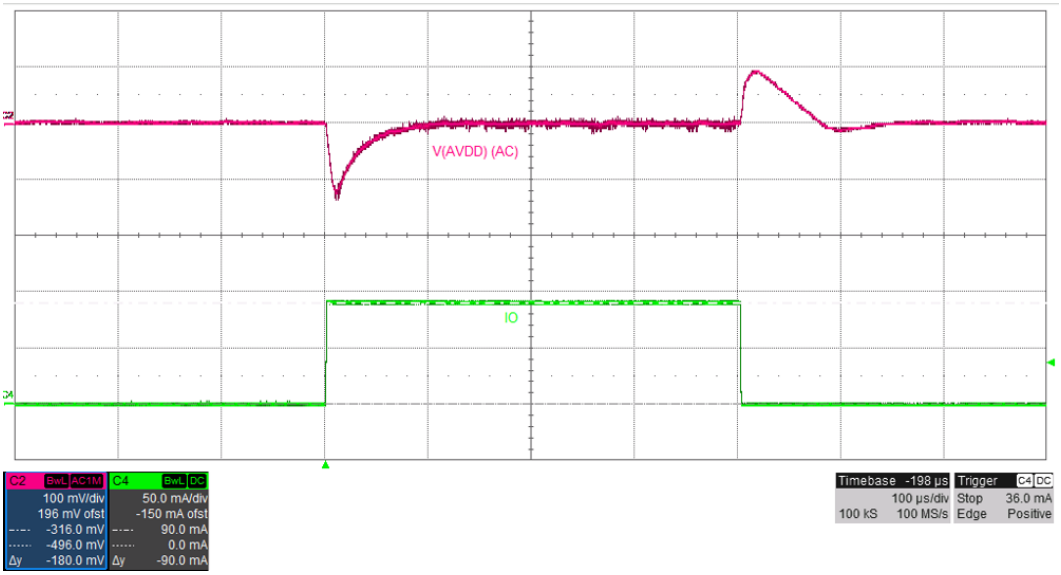

Figure 13. Load Transient Response of $V_{(AVDD)}$

NOTE: V_I = 12 V, $I_{(AVDD)}$ = 0 to 90 mA, $t_{r(VI)} = t_{f(VI)}$ = 1 µs

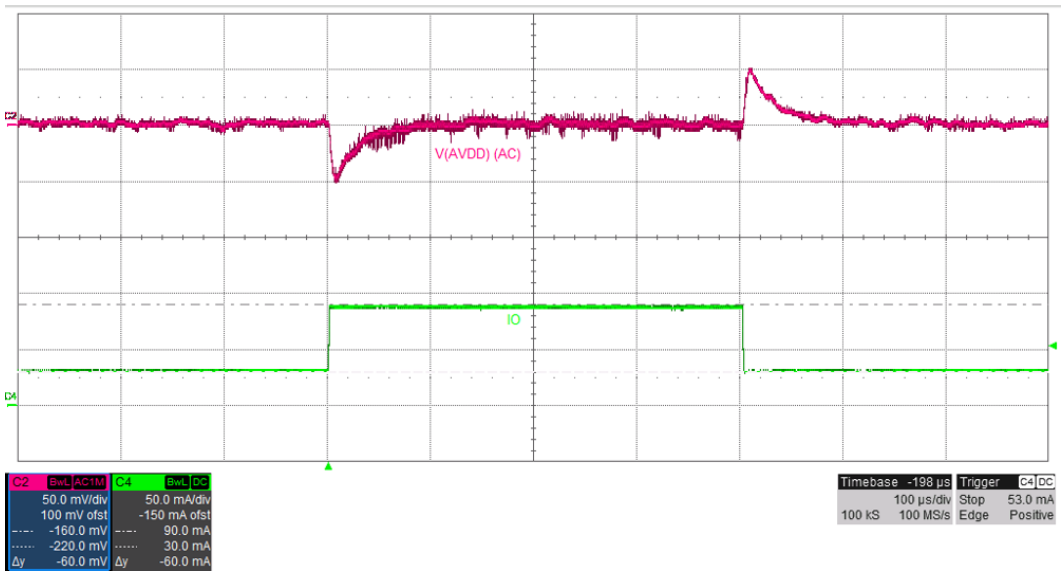

Figure 14. Load Transient Response of $V_{(AVDD)}$

NOTE: V_I = 12 V, $I_{(AVDD)}$ = 30 to 90 mA, $t_{r(VI)} = t_{f(VI)}$ = 1 µs

3 Design Files

3.1 Schematics

To download the schematics, send a request to display_power_evm@list.ti.com.

3.2 Bill of Materials

To download the bill of materials (BOM), send a request to display_power_evm@list.ti.com.

3.3 PCB Layout Recommendations

3.3.1 Layout Prints

To download the layer plots, send a request to display_power_evm@list.ti.com.

3.4 Altium Project

To download the Altium project files, send a request to display_power_evm@list.ti.com.

3.5 Gerber Files

To download the Gerber files, send a request to display_power_evm@list.ti.com.

3.6 Assembly Drawings

To download the assembly drawings, send a request to display_power_evm@list.ti.com.

4 Software Files

To download the software files, send a request to display_power_evm@list.ti.com.

5 References

1. Texas Instruments, *A Wide-Vi AMOLED Supply for NBPC, Tablet and Automotive Display Applications*, Application Report (SLVA731)
2. Texas Instruments, WEBENCH® Design Center (http://www.ti.com/webench)

6 About the Author

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