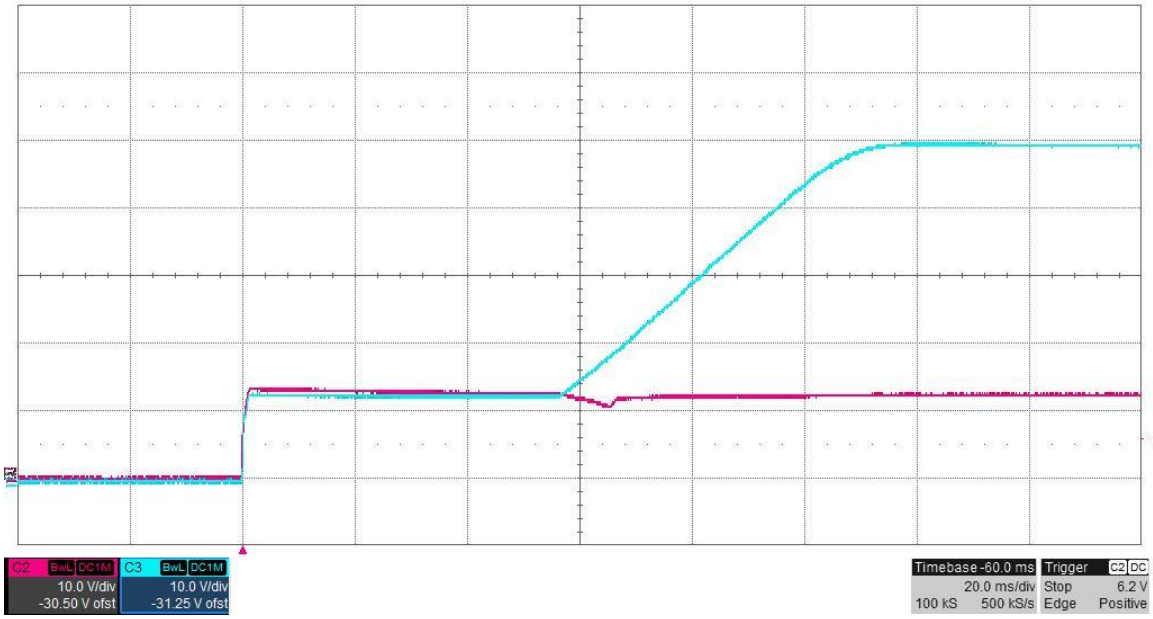
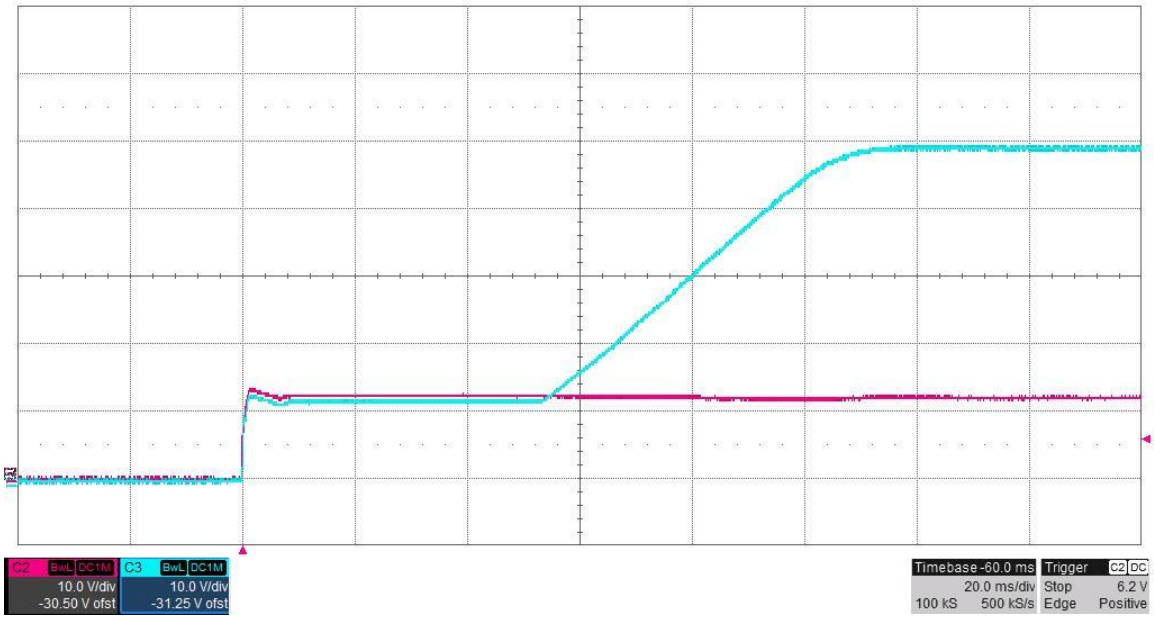
1 Startup

The photo below shows the output voltage startup waveform after the application of 12V in. The 50V output was loaded to 0A. (10V/DIV, 20mS/DIV)

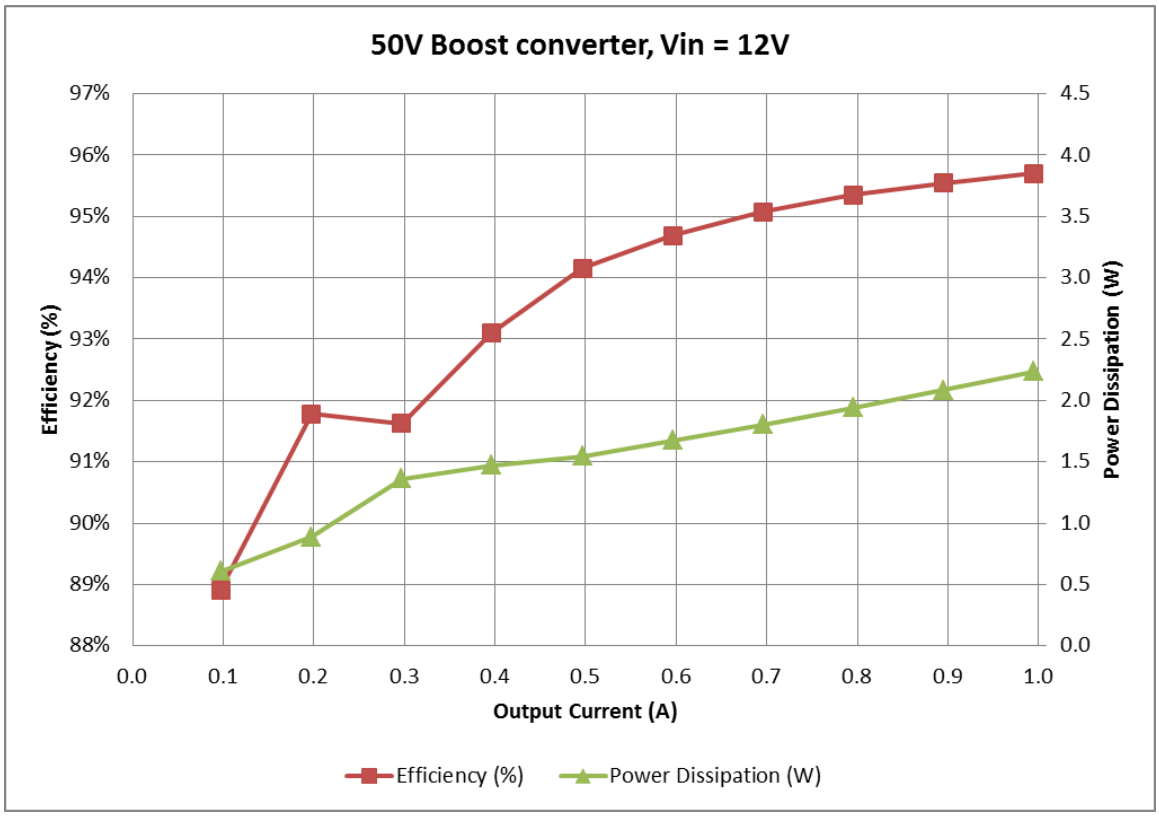


The photo below shows the output voltage startup waveform after the application of 12V in. The 50V output was loaded to 1A. (10V/DIV, 20mS/DIV)



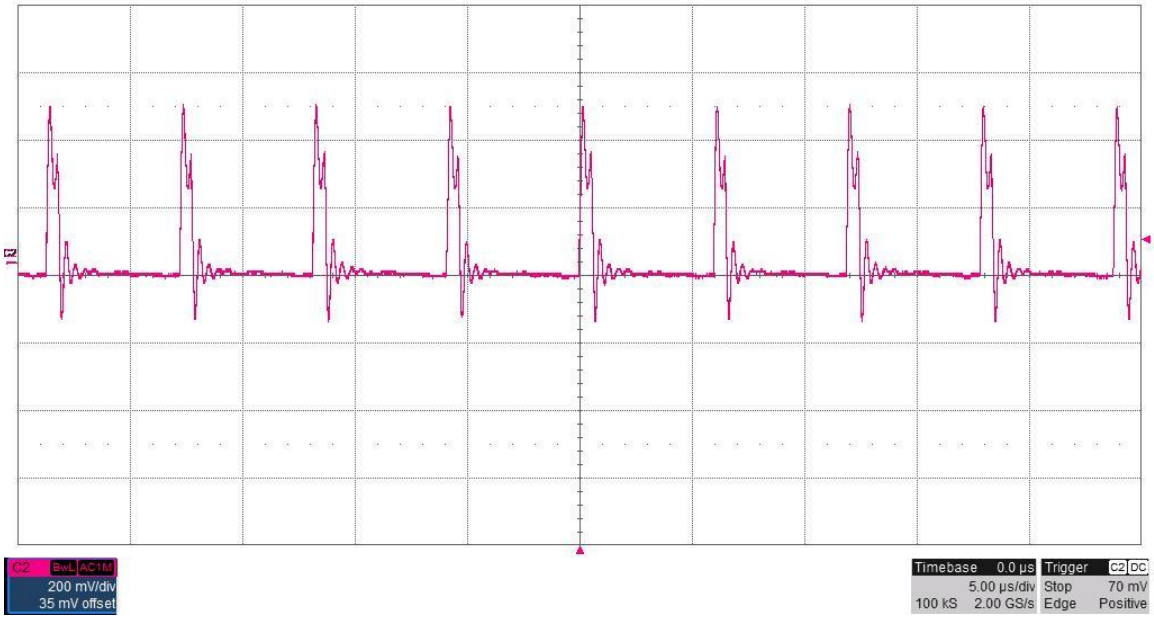
2 Efficiency

The boost converter efficiency is shown below for Vin = 12V and Vout = 50V.

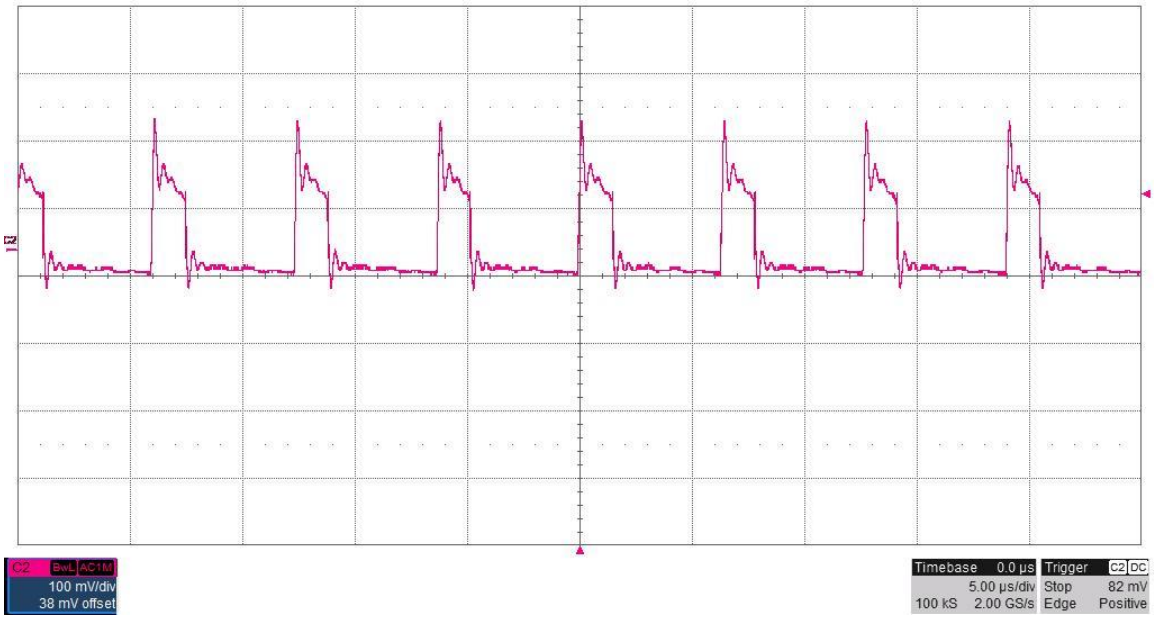


3 Output Ripple Voltage

The 50V output ripple voltage (AC coupled) is shown in the figure below. The image was taken with the output loaded to 1A. The input voltage is set to 5V. (200mV/DIV, 5uS/DIV)

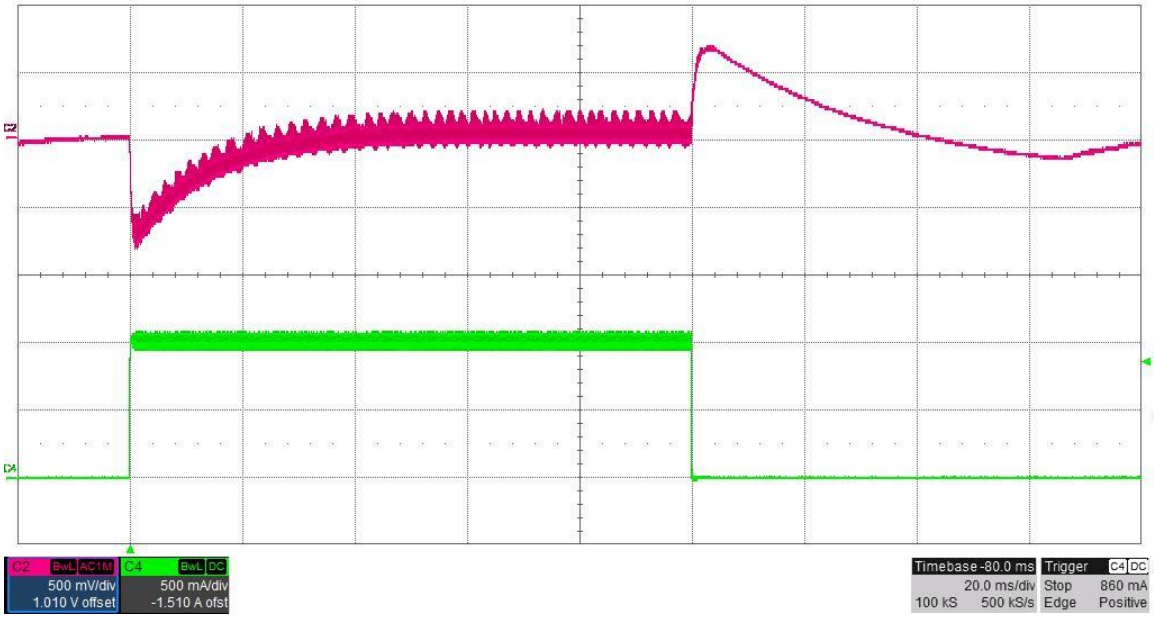


The 50V output ripple voltage (AC coupled) is shown in the figure below. The image was taken with the output loaded to 1A. The input voltage is set to 12V. (100mV/DIV, 5uS/DIV)

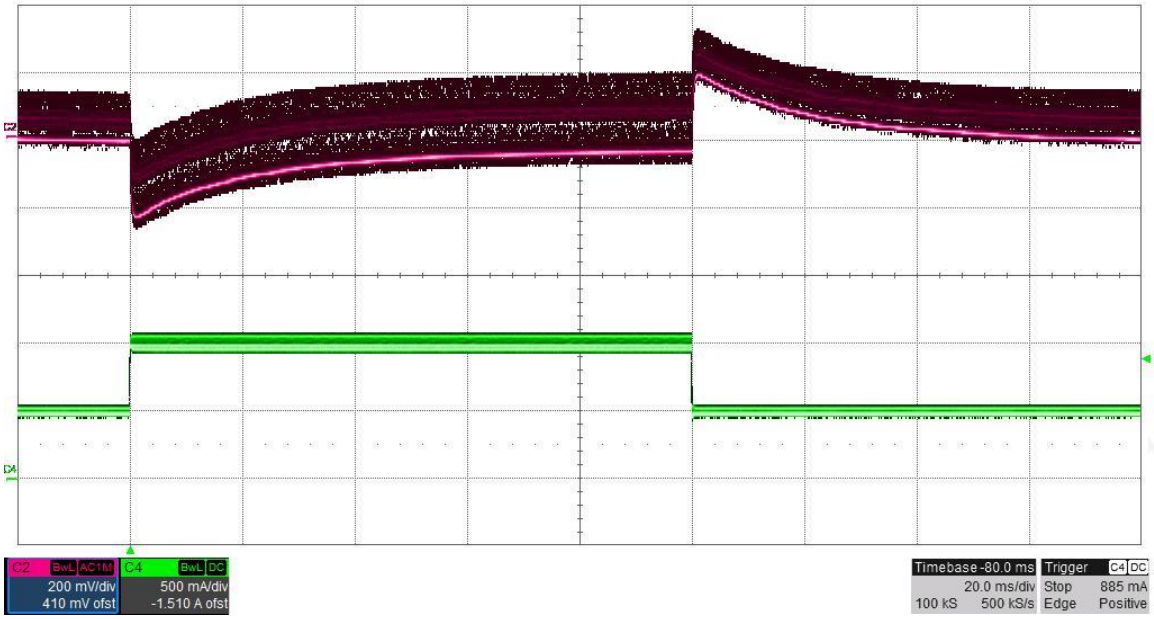


4 Load Transients

The photo below shows the 50V output voltage (ac coupled) when the load current is stepped between 0A and 1A. Vin = 12V. (500mV/DIV, 500mA/DIV, 20mS/DIV)

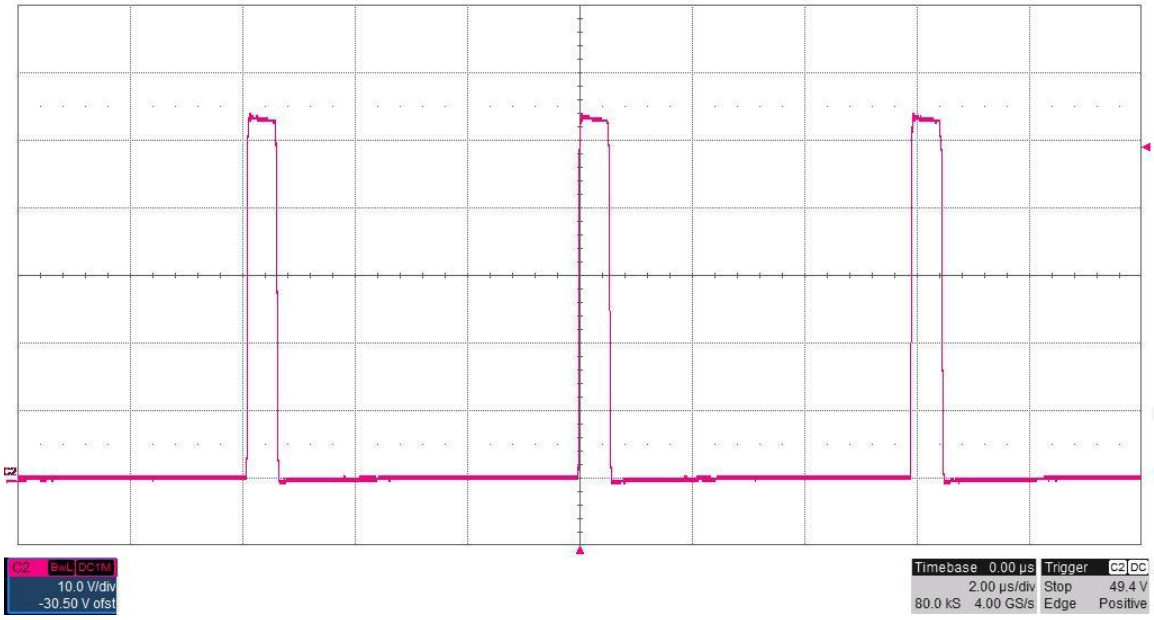


The photo below shows the 50V output voltage (ac coupled) when the load current is stepped between 0.5A and 1A. Vin = 12V. (200mV/DIV, 500mA/DIV, 20mS/DIV)

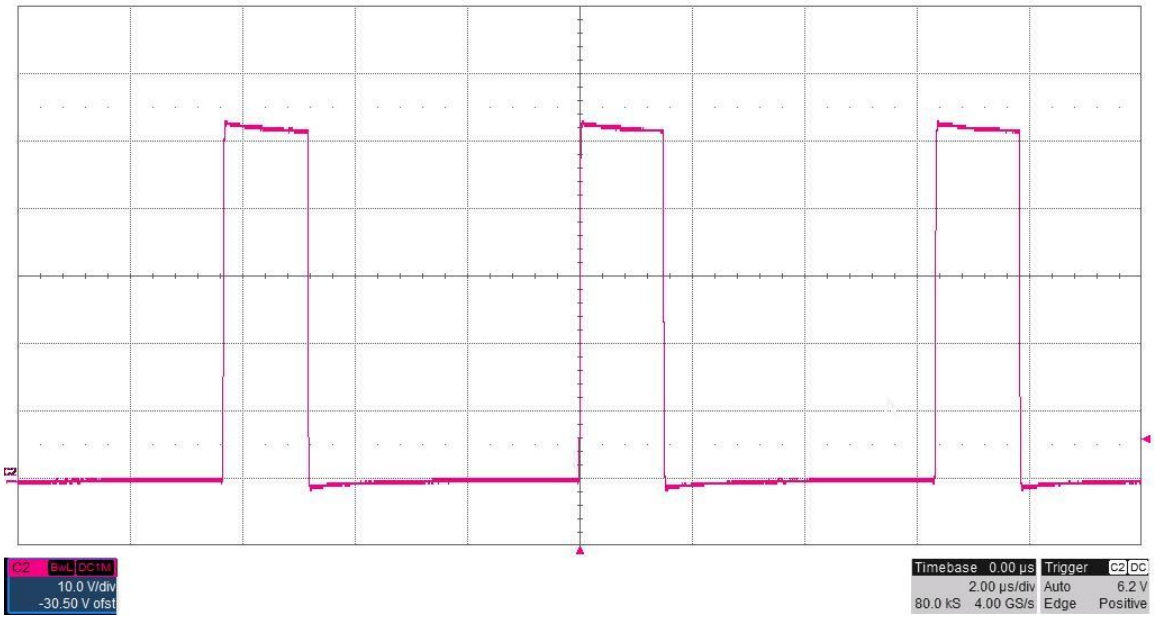


5 Switch Node Waveforms

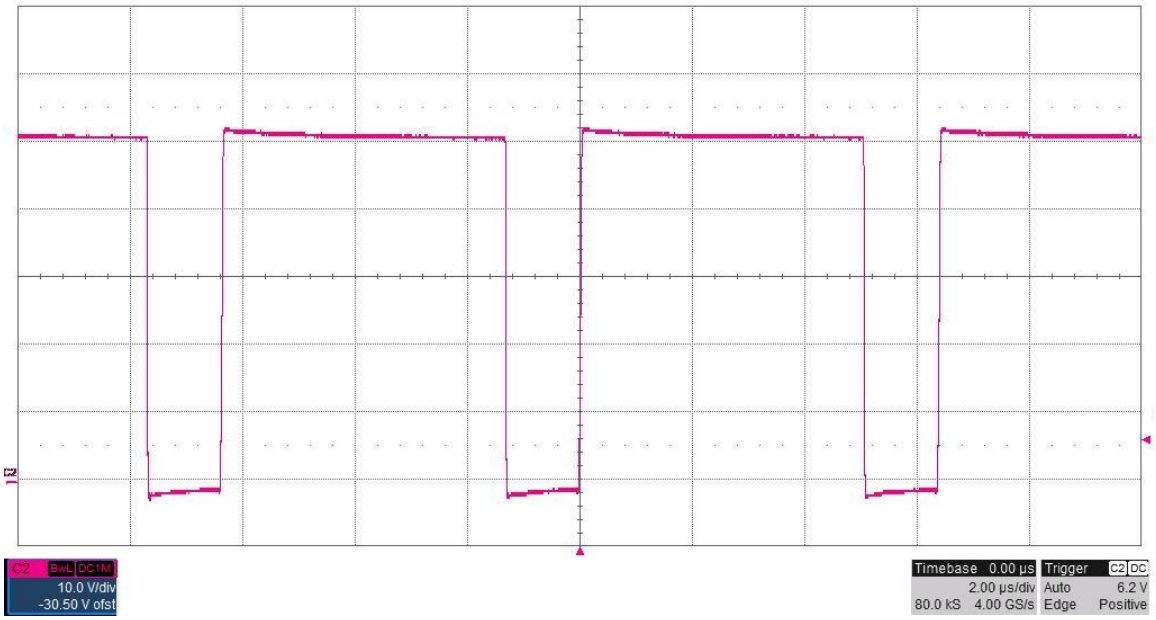
The photo below shows the FET switching voltage (TP2) for an input voltage of 5V and a 1A load. (10V/DIV, 2uS/DIV)



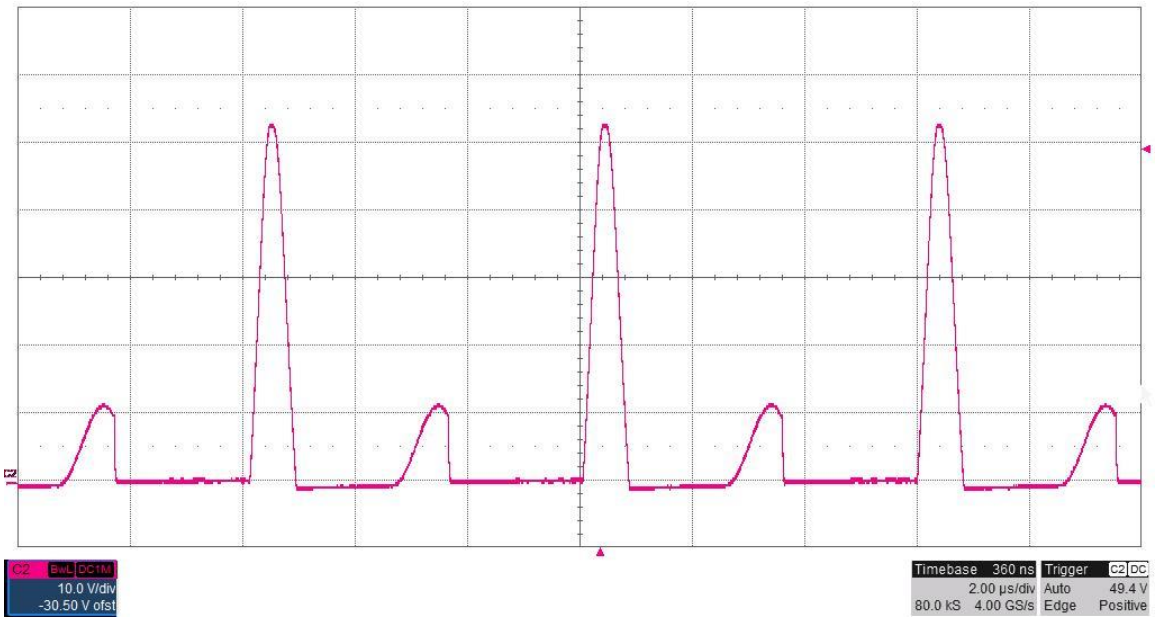
The photo below shows the FET switching voltage (TP2) for an input voltage of 12V and a 1A load. (10V/DIV, 2uS/DIV)



The photo below shows the FET switching voltage (TP2) for an input voltage of 40V and a 1A load. (10V/DIV, 2uS/DIV)

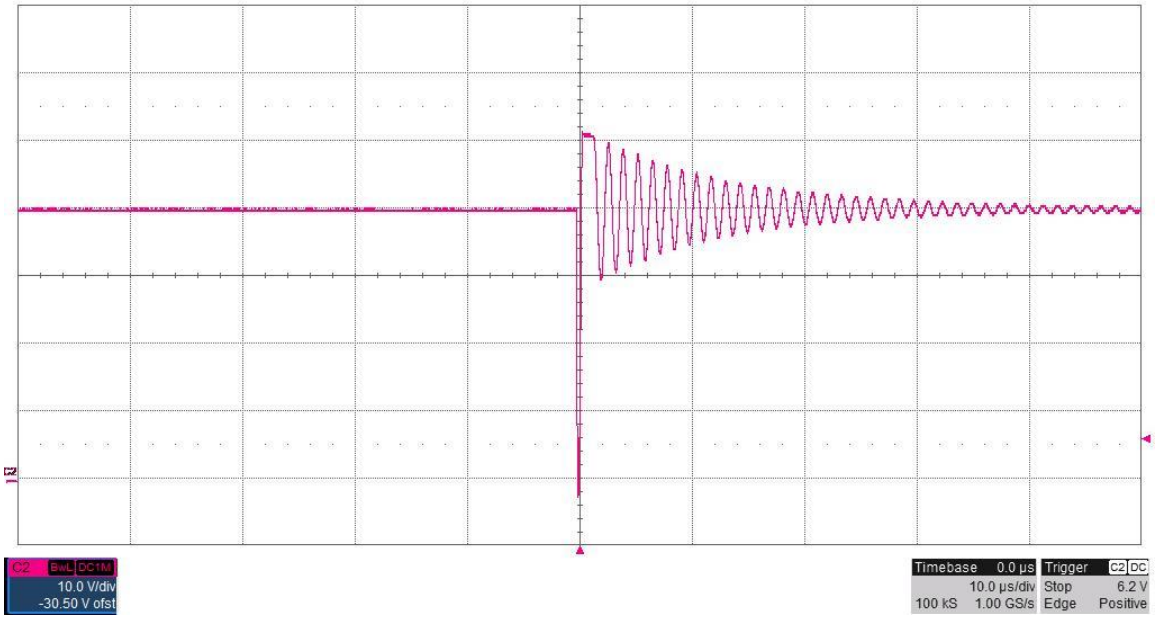


The photo below shows the FET switching voltage (TP2) for an input voltage of 5V and a 0A load. (10V/DIV, 2uS/DIV)



The photo below shows the FET switching voltage (TP2) for an input voltage of 12V and a 0A load. (10V/DIV, 2uS/DIV)

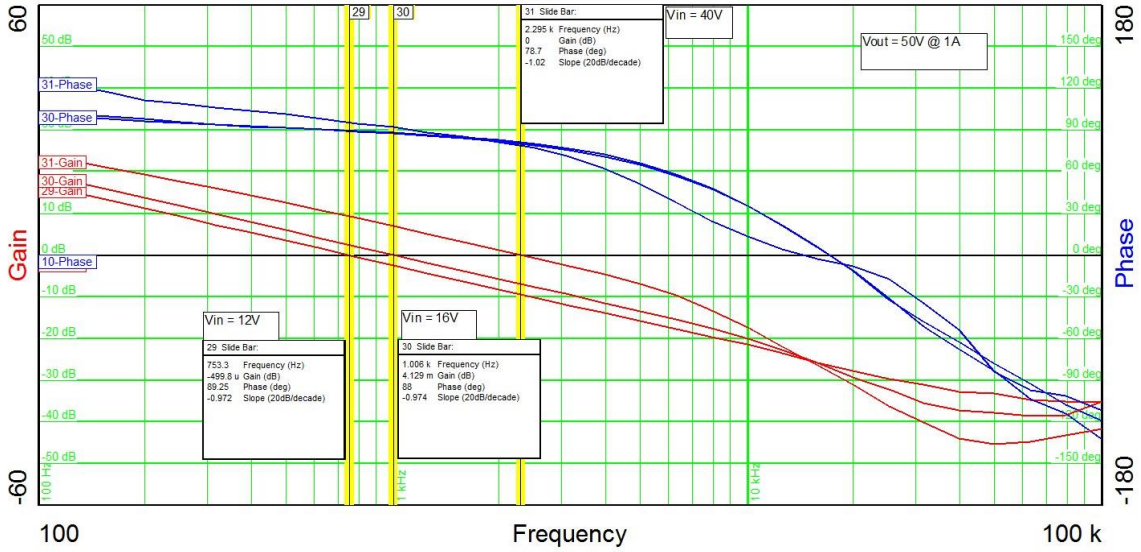
The photo below shows the FET switching voltage (TP2) for an input voltage of 40V and a 0A load. (10V/DIV, 10uS/DIV)



6 Loop Gain

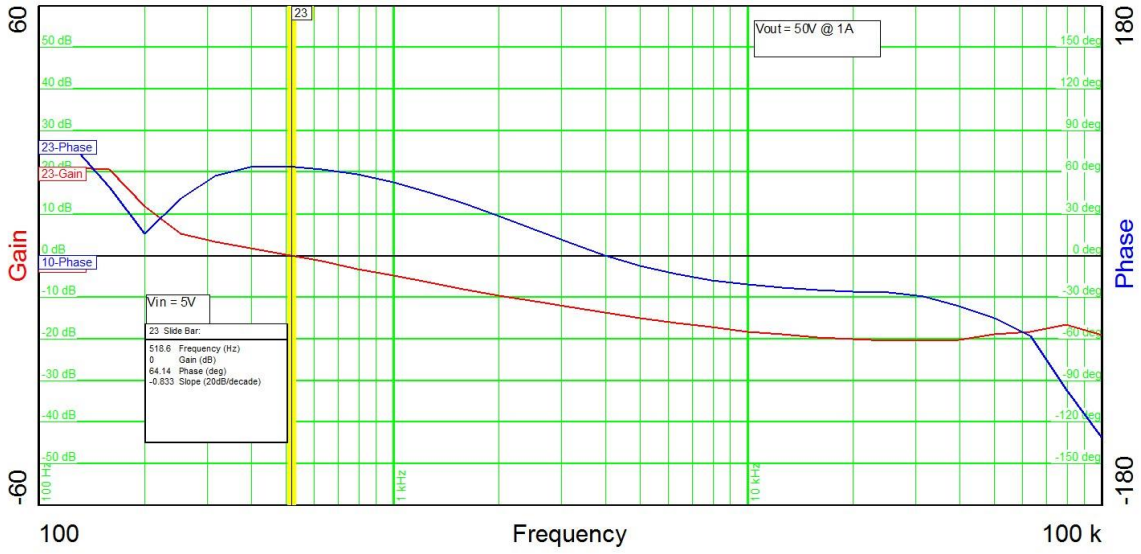
The plot below shows the loop gain for various input voltages and the output set to 1A.

Loop Gain (Vin = 12V)	BW: 753Hz	PM: 89 degrees
Loop Gain (Vin = 16V)	BW: 1.01KHz	PM: 88 degrees
Loop Gain (Vin = 40V)	BW: 2.30KHz	PM: 79 degrees



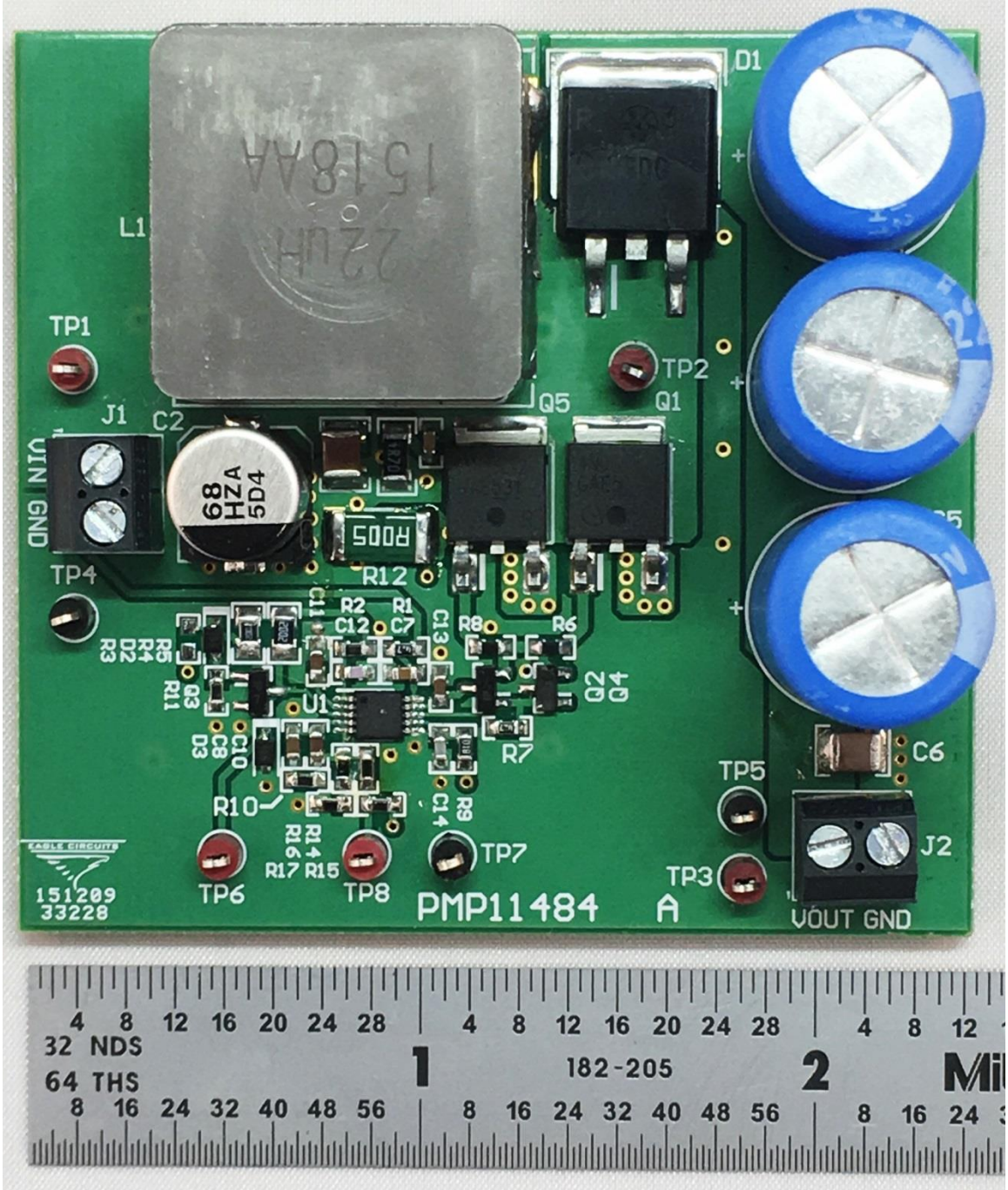
The plot below shows the loop gain at 5V input and the output set to 1A. A 1200uF/63V aluminum capacitor added to the input to reduce the cabling source impedance.

Loop Gain (Vin = 5V)	BW: 519Hz	PM: 64 degrees



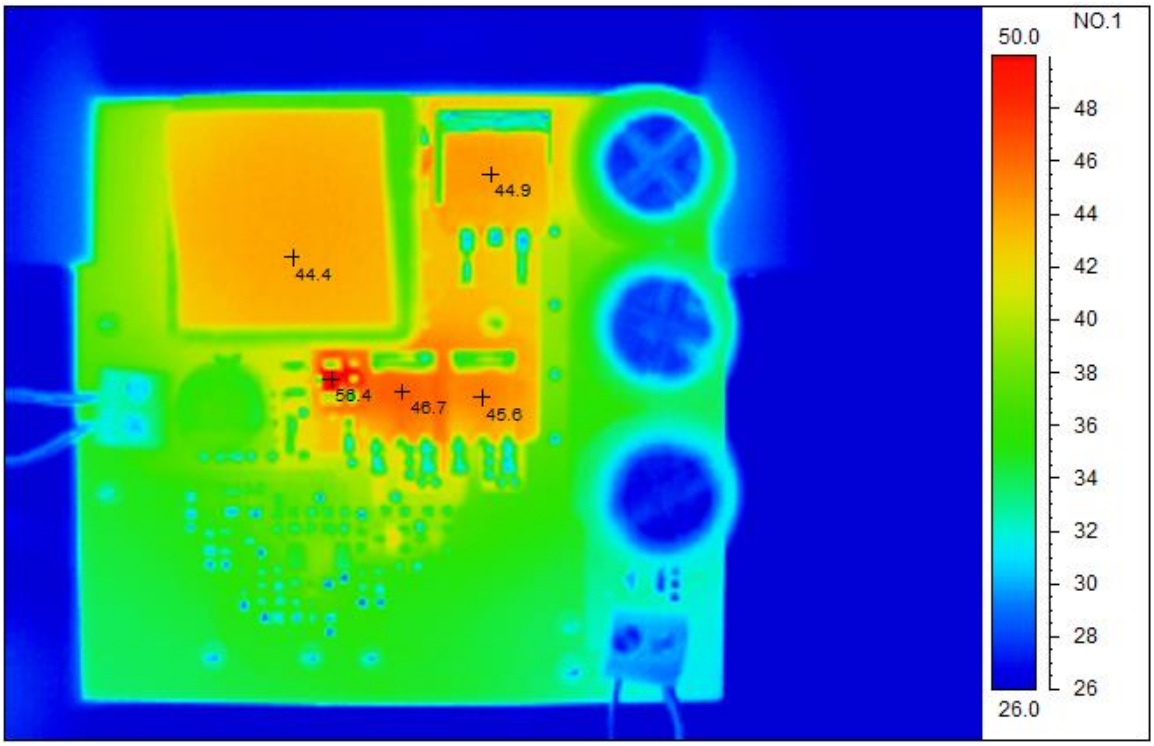
7 Photo

The photo below shows the PMP11484 REVB assy.



8 Thermal Image

A thermal image is shown below operating at 12V input and 50V@1A output (room temp, no airflow).



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