TI Designs
TPS7B4253-Q1 High-Accuracy Power Supply Reference Design

Description

This TI Design is a high-accuracy power supply solution for automotive, achieving a maximum of 0.3% high-accuracy power supply for an analog-to-digital converter (ADC) without a high accuracy low dropout (LDO) in the system.

Resources

TIDA-00981	Design Folder
TPS7B4253-Q1	Product Folder
REF5050A-Q1	Product Folder
TPS79801-Q1	Product Folder

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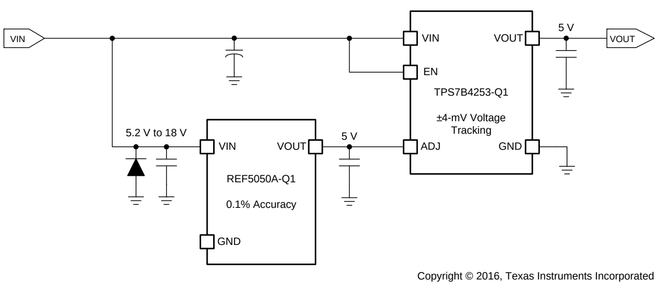
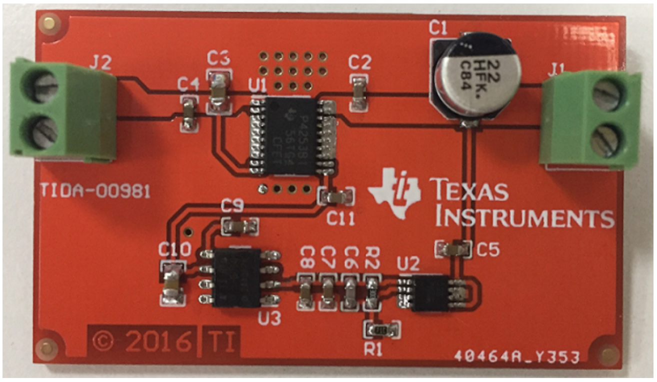
Features

- Automotive Battery Direct Connection
- 0.3% Output Voltage Accuracy
- ±4-mV Line and Load Regulation
- Reverse Polarity Protection
- Reverse Current and Short to Battery Protection

Applications

- Data Acquisition Systems
- Automotive Body Control Module
- Industrial Process Control
- Precision Instrumentation





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1 System Overview

1.1 System Description

The TIDA-00981 TI Design is for high-accuracy power supply requirements with connecting a battery directly to an application. It is easy to achieve a 0.3% accuracy with 300-mA current capacity to power the ADC in the system. In this TI Design, the TPS79801-Q1 device works as the power supply for the REF5050A-Q1 device. The REF5050A-Q1 device generates a 0.2% reference voltage from –40°C to +125°C and connects to the TPS7B4253-Q1 ADJ pin, then the TPS7B4253-Q1 device works as a battery direct-connect LDO with an output voltage of 5 V ±0.3%.

1.2 Key System Specifications

Table 1. Key Design Parameters

PARAMETERS	SPECIFICATIONS
Input voltage range	6 V to 40 V
Output voltage	5 V
Maximum output current	300 mA
Output voltage accuracy	0.3%

1.3 Block Diagram

Figure 1 shows the TIDA-00981 system block diagram.

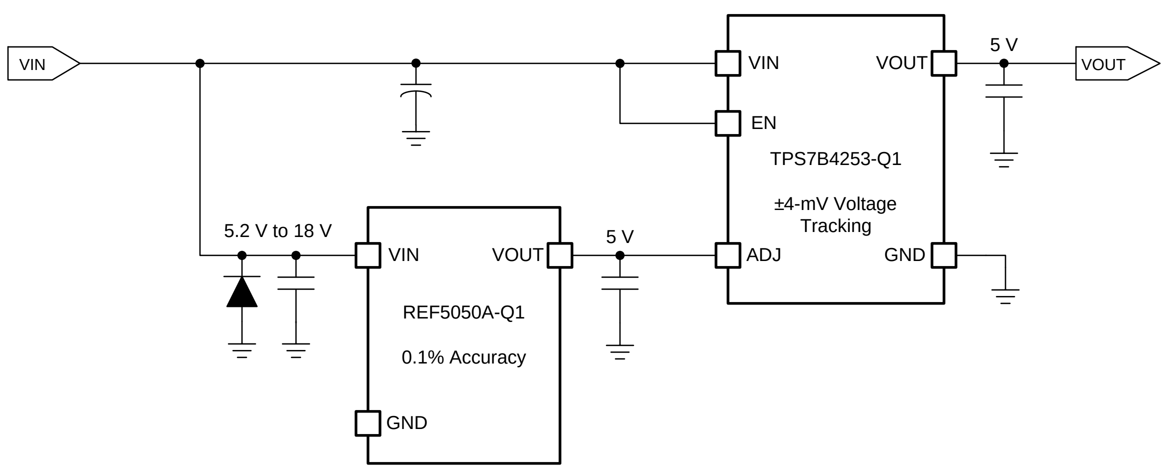

Figure 1. TIDA-00981 Block Diagram

1.4 Highlighted Products

The key features for selecting the highlighted devices for this TI Design are outlined in the following subsections. Refer to the complete details of the highlighted devices in the respective product data sheets.

1.4.1 TPS7B4253-Q1 — 300-mA, 40-V LDO Tracking

The TPS7B4253-Q1 device is designed for automotive applications with a 45-V load dump. The device can be used as a one tracking LDO regulator or a voltage tracker to build one closed power loop for off-board sensors with an onboard main supply. The output of the device is accurately regulated by a reference voltage at the ADJ pin. To provide an accurate power supply to the off-board modules, the device offers a 4-mV ultra-low tracking tolerance between the ADJ and FB pins across the full temperature range.

The back-to-back PMOS (positive-channel metal-oxide semiconductor) topology eliminates the need for an external diode under reverse polarity condition. The TPS7B4253-Q1 device also includes thermal shutdown, inductive clamp, overload, and short-to-battery protection to prevent damage to onboard components during extreme conditions. The TPS7B4253-Q1 device offers high-current capability with tracking for the REF5050A-Q1 reference voltage.

1.4.2 REF5050A-Q1 — Low Noise, Low Drift, Precision Voltage Reference

The REF5050A-Q1 device is used as a high precision reference for the TPS7B4253-Q1 ADJ pin. The REF50xxA-Q1 family of devices is low-noise, low-drift, and very-high precision-voltage reference. These reference devices are capable of sinking and sourcing and are robust with regard to line and load changes. Excellent temperature drift (8 ppm/°C maximum) and high accuracy (0.1% maximum) are achieved using proprietary design techniques. These features, combined with very low noise, make the REF50xxA-Q1 family of devices ideal for use in high-precision data acquisition systems.

1.4.3 TPS79801-Q1 — 50-mA, 3-V to 50-V, LDO Linear Regulator

The TPS79801-Q1 device is used as the power supply for the REF5050A-Q1 device. The TPS798xx-Q1 is the first device in a line of 50-V, high-voltage, micropowered LDO linear regulators. This device is capable of supplying 50 mA of output current with a dropout voltage of only 300 mV. Designed for high-voltage (50 V) applications with a low quiescent current, 40-µA operating, and 1 µA in shutdown makes the TPS798xx-Q1 an ideal choice for battery-powered or high-voltage systems. Quiescent current is also well-controlled in dropout.

2 System Design Theory

This TI Design uses one pcs REF5050A-Q1 to generate the high-precision voltage reference as the input for the TPS7B4253-Q1 ADJ pin. The TPS7B4253-Q1 device connects to a battery directly, outputs accurate regulated voltage (the same as the ADJ pin voltage), and works as power stage with 300-mA current capability. The TPS79801-Q1 device offers 6-V to power the REF5050A-Q1 device.

2.1 Tracking LDO Design

For this TI Design, use the parameters shown in Table 2.

Table 2. Design Parameters

PARAMETERS	SPECIFICATIONS
Input voltage range	6 V to 40 V
Output voltage	5 V ±0.3%
ADJ voltage	5 V ±0.3%
Output capacitor	10 µF to 500 µF
Output capacitor ESR range	0.001 Ω to 20 Ω

2.1.1 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Reference voltage
- Output current
- Current limit

2.1.2 Input Capacitor

The TPS7B4253-Q1 device requires an input decoupling capacitor (the value depends on the application). The typical recommended value for the decoupling capacitor is 2.2 μF. The voltage rating must be greater than the maximum input voltage.

2.1.3 Output Capacitor

To ensure the stability of the TPS7B4253-Q1 device, the device requires an output capacitor with a value in the range from 10 μF to 500 μF, and an ESR range from 0.001 Ω to 20 Ω when the FB pin is directly connected to the OUT pin. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response

When multiple capacitors (two or more) are connected in parallel at the OUT pin, the ESR range of each output capacitor must be from 0.001 Ω to 3 Ω for loop stability.

2.1.4 ADJ Pin Voltage

The ADJ pin voltage is from the REF5050A-Q1 device; the accuracy is 0.2% at 5 V. Figure 2 shows the tracking LDO schematic.

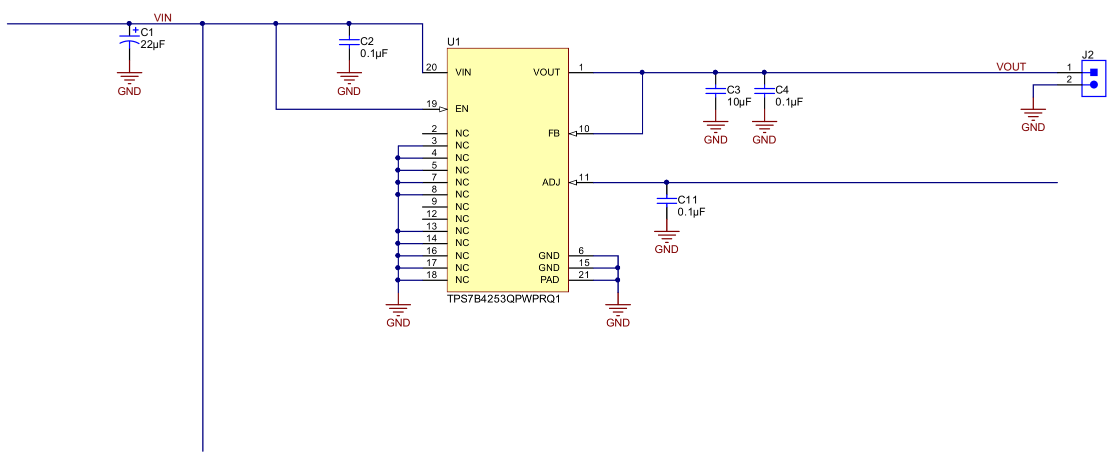

Figure 2. Tracking LDO Schematic

2.2 REF5050A-Q1 Design

The REF5050A-Q1 device is selected to output a 5-V reference voltage.

A supply bypass capacitor with a value between 1 μF to 10 μF is recommended. A 1-μF to 50-μF, low-ESR output capacitor (CL) must be connected from VOUT to GND. The ESR value must be less than or equal to 1.5 Ω. The ESR minimizes gain peaking of the internal 1.2-V reference and thus reduces noise at the VOUT pin.

The device section in the data sheet specifies the typical voltage noise at 0.1 Hz to 10 Hz for each member of the REF50xxA-Q1 family of devices. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care must be taken to ensure the output impedance does not degrade performance.

For additional information about how to minimize noise and maximize performance in mixed-signal applications, such as data converters, refer to [1], [2], and [3].

Figure 3 shows the reference voltage schematic.

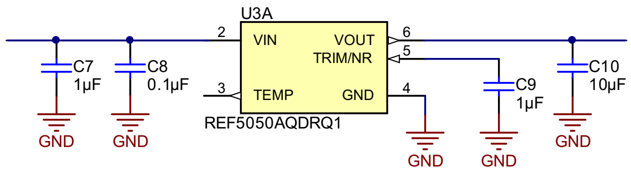

Figure 3. Reference Voltage Schematic

2.3 *TPS79801-Q1*

For this TI Design, use the parameters shown in Table 3.

Table 3. Design Parameters

PARAMETERS	SPECIFICATIONS
Input voltage range	6 V to 40 V
6 V	6 V
Output current rating	50 mA
Output capacitor	1 µF to 100 µF

2.3.1 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Output capacitor

2.3.2 FB Resistor

The TPS79801-Q1 device has an output voltage range of 1.275 V to 28 V. The output voltage is set by the ratio of two external resistors, shown in Figure 4. The feedback loop monitors the output to maintain the voltage at the adjust (FB) pin at 1.275 V referenced to ground. The current in resistor R1 = 1.275 V / R1, and the current in R2 is the current in R1 plus the FB pin bias current.

The FB pin bias current (0.2 µA at 25°C) flows through R2 into the FB pin. Use Equation 1 to calculate the output voltage. The value of R1 must be less than 250 kΩ to minimize errors in the output voltage caused by the FB pin bias current.

NOTE: In shutdown, the output is turned off and the divider current is zero.

A 100-pF capacitor (C1) placed in parallel with the top resistor (R2) of the output divider is necessary for stability and transient performance of the adjustable TPS798xx-Q1. The impedance of C1 at 10 kHz must be less than the value of R2.

The adjustable device is tested and specified with the FB pin tied to the OUT pin and a 1-mA DC load (unless otherwise specified) for an output voltage of 1.275 V. Specifications for output voltages greater than 1.275 V are proportional to the ratio of the desired output voltage to 1.275 V (VOUT / 1.275 V). For example, load regulation for an output current change of 1 mA to 50 mA is –10 mV (typical) at VOUT = 1.275 V.

$$V_{OUT} = 1.275\left(1 + \frac{R2}{R1}\right) + I_{FB}R2 \quad (1)$$

Select R1 = 53.6 K, and select R2 = 200 K.

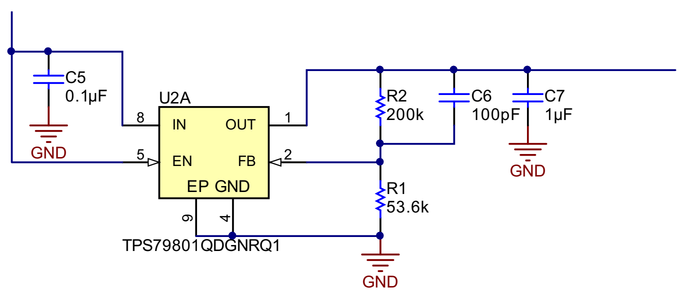

Figure 4. Power Supply Schematic of REF5050A-Q1

3 Getting Started Hardware

Connecting a 12-V DC supply to the onboard input connector (J1) turns on the circuit.

4 Testing and Results

Figure 5 shows the load regulation at V_{IN} = 14 V, Figure 6 shows the line regulation at load = 10 mA, and Figure 7 shows the line regulation at load = 100 mA.

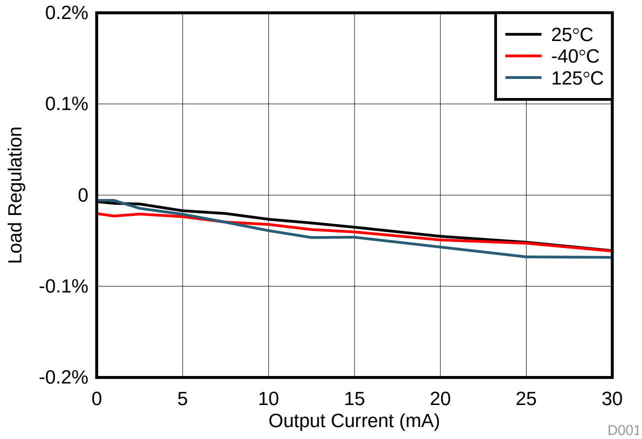

Figure 5. Load Regulation — V_{IN} = 14 V

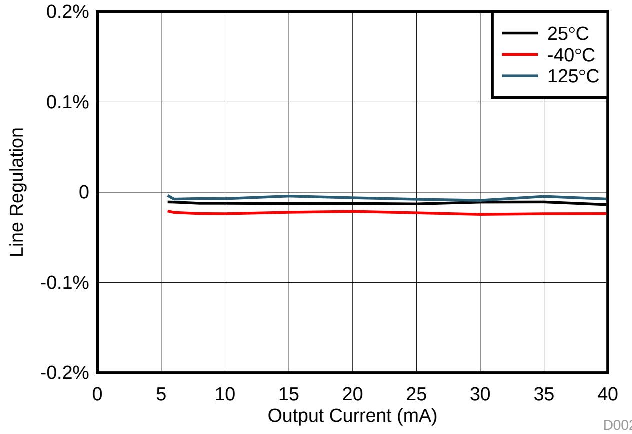

Figure 6. Line Regulation — Load = 10 mA

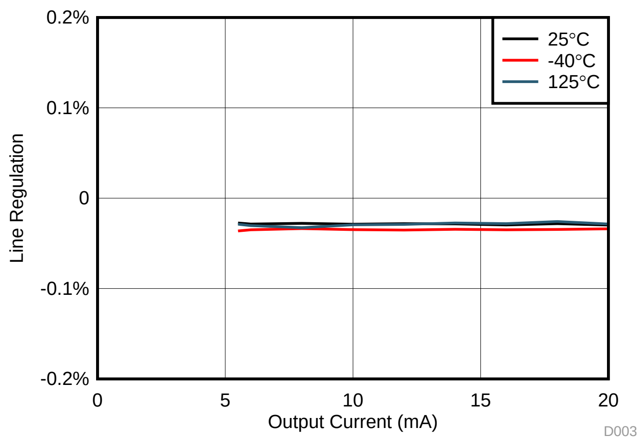

Figure 7. Line Regulation — Load = 100 mA

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00981.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00981.

5.3 PCB Layout Recommendations

The layout process is an important step for the use of a high-precision voltage reference and LDO. If the layout is not carefully designed, this will impact the voltage accuracy because of noise, and the driver may not deliver enough output current because of the thermal limitation.

For the REF5050A-Q1 layout, connect low-ESR, 0.1-μF ceramic bypass capacitors at the VIN and VOUT pins. Decouple other active devices in the system per the device specifications. Use a solid ground plane to help distribute heat and reduce electromagnetic-interference (EMI) noise pickup. Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring. Minimize trace length between the reference and bias connections to the end device to reduce noise pickup. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible and only make perpendicular crossings when absolutely necessary.

For the LDO layout, to improve the thermal performance of the device and maximize the current output at high ambient temperatures, TI recommends spreading the thermal pad as large as possible and placing a sufficient number of thermal vias on the thermal pad. Minimize equivalent series inductance (ESL) and ESR to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces for the path between the output capacitor and the OUT pins because vias can negatively impact system performance and even cause instability.

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00981.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00981.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00981.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00981.

6 Related Documentation

1. *How the voltage reference affects ADC performance, Part 1*, (SLYT331)
2. *How the voltage reference affects ADC performance, Part 2*, (SLYT339)
3. *How the voltage reference affects ADC performance, Part 3*, (SLYT335)
4. *TPS7B4253-Q1 300-mA 40-V Low-Dropout Voltage-Tracking LDO With 4-mV Tracking Tolerance*, (SLVSCP3)
5. *REF50xxA-Q1 Low-Noise, Very Low Drift, Precision Voltage Reference*, (SBOS456)
6. *TPS798xx-Q1 50 mA, 3 V to 50 V, Micropower, Low-Dropout Linear Regulator*, (SLVS822)

6.1 Trademarks

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7 About the Author

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