

TI Designs: TIDA-01350

High-Speed, Linear Transimpedance Amplifier Reference Design



Description

This transimpedance amplifier design is a high-speed, linear, two-stage transimpedance amplifier (TIA) application which uses the LMH5401 fully differential amplifier (FDA). Included in the reference design is a photo diode with integrated fiber pigtail. The provided photo diode allows for ease of testing as it represents a nearly ideal current source.

Resources

TIDA-01350	Design Folder
LMH5401	Product Folder
TINA-TI™	Tools Folder

Features

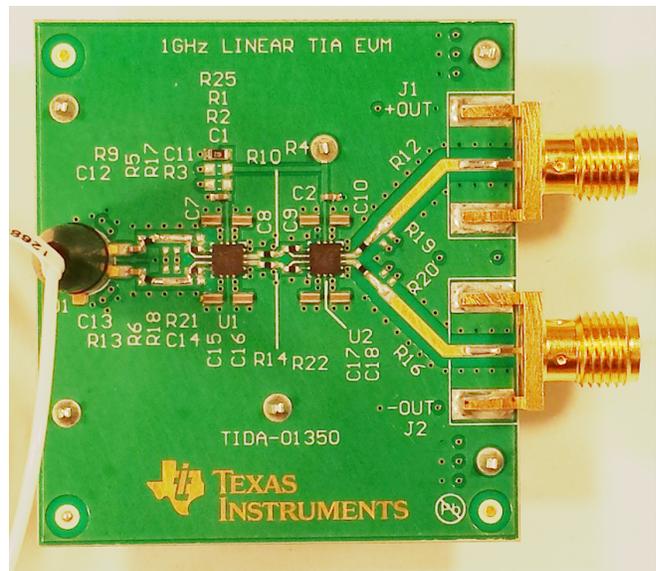
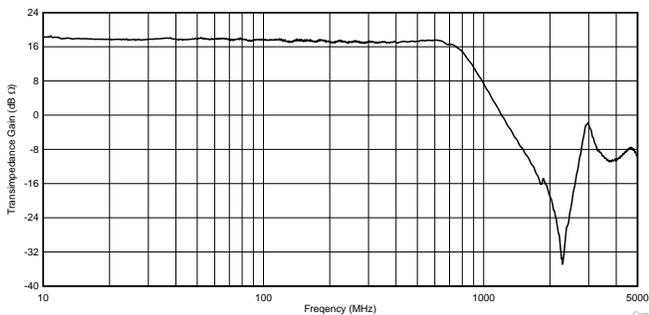
- Bandwidth > 500 MHz
- Convert Current to Voltage
- Photo Diode Included
- Two Stages for Increased Gain

Applications

- [Linear Optical Receiver](#)
- [Machine Vision](#)
- [Proximity Detector](#)



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1 System Description

The TIDA-01350 TI Design is a fixed-gain, high-bandwidth, fully-differential, current-to-voltage conversion circuit designed for high-speed applications. This reference design includes the full optical-to-electrical conversion gain circuit, including two stages of electrical gain for improved sensitivity and bandwidth.

Optical proximity detectors use a photodiode receiver to measure the return time of an optical pulse. The TIDA-01350 has a very-high-speed response and the sufficient level of sensitivity required to measure a reflected light pulse.

Machine vision applications, such as linear measurement or edge detection, require high-speed optical power measurements. The TIDA-01350 enables high-speed optical power detection.

Multi-bit modulation patterns such as PAM-4 or QPSK require receiver circuits with a linear response. The TIDA-01350 has very-high-fidelity linearity performance, which allows high-order modulation schemes that enable more data to be sent in the same bandwidth.

1.1 Key System Specifications

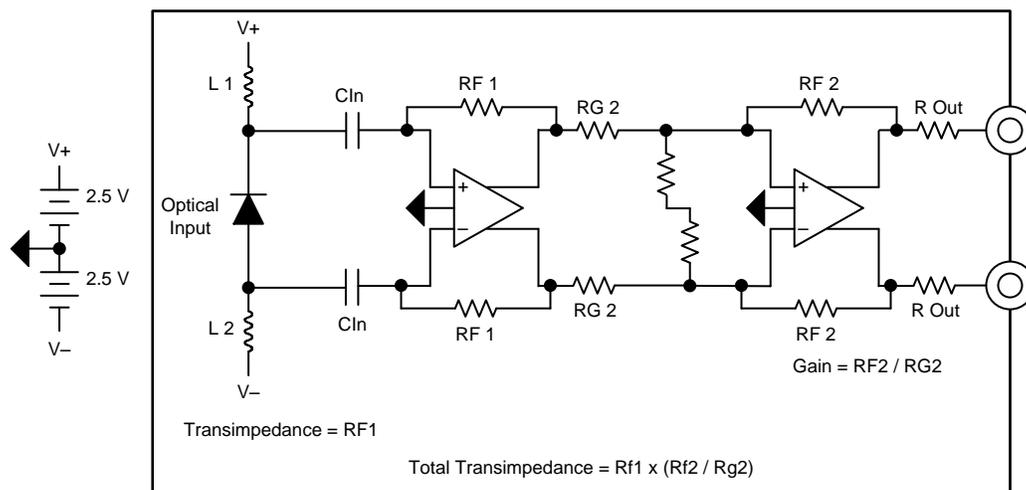
Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Supply voltage	5- V external supply
Current-to-voltage gain	500 Ω to 10000 Ω
Differential-output common-mode voltage	0 V
Target bandwidth	> 500 MHz
Onboard photo diode	AC Photonics PTD0075A2211
Fiber connector	FC/APC

2 System Overview

2.1 Block Diagram

Figure 1 shows a block diagram of the system. The main portion of the design is two fully-differential amplifiers (FDAs). An onboard photo diode is provided to facilitate high-speed testing. The board is populated for a transimpedance of 10000 Ω by default.



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Figure 1. System Block Diagram

2.2 Highlighted Products

2.2.1 THS4131

The TIDA-01350 design features the [LMH5401](#) fully differential amplifier (FDA).

The LMH5401 is a very-high-performance differential amplifier optimized for radio frequency (RF), intermediate frequency (IF), or high-speed, DC-coupled, time-domain applications. The device is ideal for DC- or AC-coupled applications that may require a single-ended-to-differential (SE-DE) conversion when driving an analog-to-digital converter (ADC). The LMH5401 generates very low levels of second- and third-order distortion when operating in SE-DE or differential-to-differential (DE-DE) mode.

The amplifier is optimized for use in both SE-DE and DE-DE systems. The device has unprecedented usable bandwidth from DC to 2 GHz. The LMH5401 can be used for SE-DE conversions in the signal chain without external baluns in a wide range of applications such as test and measurement, broadband communications, and high-speed data acquisition. [Figure 2](#) shows the LMH5401 block diagram.

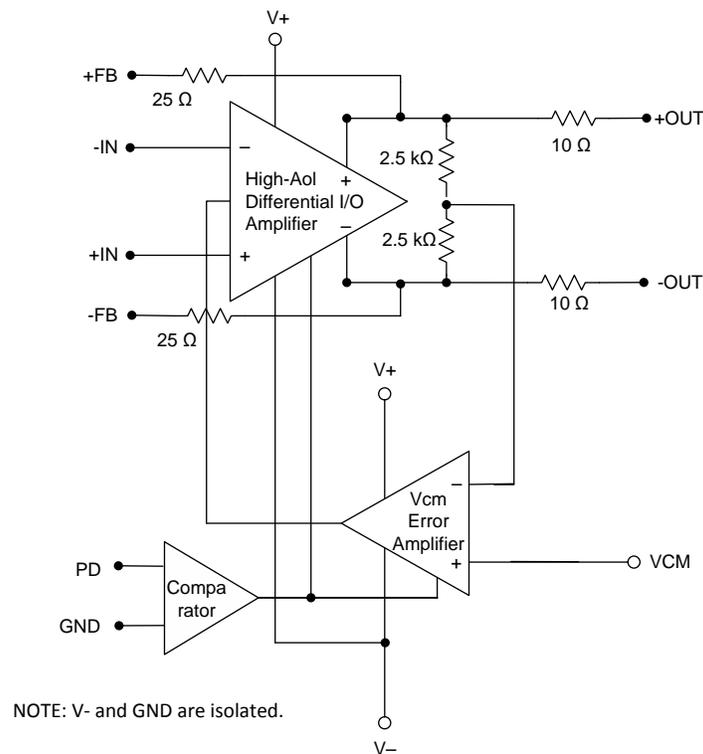
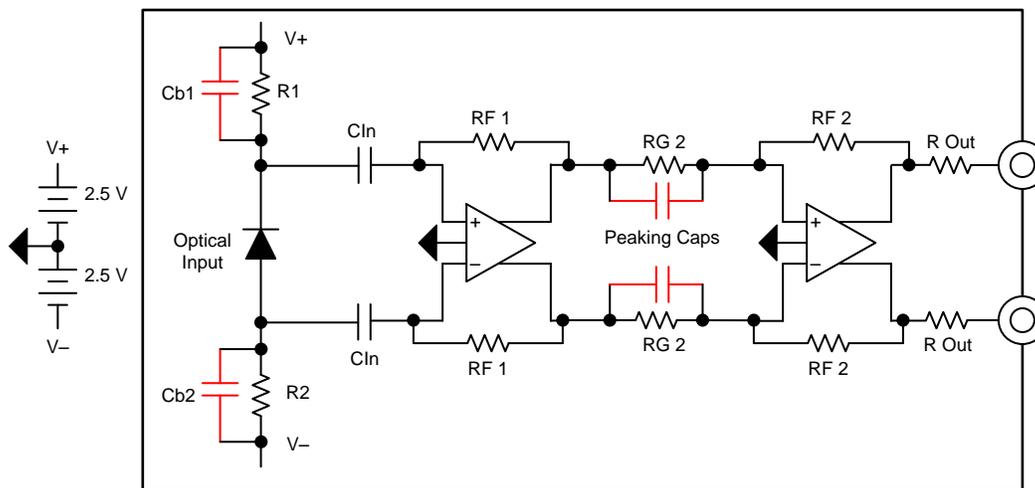


Figure 2. LMH5401 Functional Block Diagram

2.3 System Design Theory

The TIDA-01350 is a linear, high-speed transimpedance amplifier (TIA) reference design. Figure 3 shows the system block diagram. TIAs are very sensitive to input diode capacitance. As diode capacitance increases, the bandwidth of the circuit decreases. In the same manner, increasing the value of the feedback resistor decreases the bandwidth of the amplifier. Weighing both the required gain and bandwidth is very important because there is a gain bandwidth relationship in TIAs. Two stages are used in this reference design to achieve high gain as well as high bandwidth.

The other key component of the reference design is the photo diode. The PTD0075A2211 diode has been chosen for two primary specifications. The first key specification is the junction capacitance of 0.6 pF and the second key specification is the reverse bias voltage of 5 V. The 5-V bias voltage is chosen to keep the system design very simple because the amplifiers and the diode operate from the same supply voltage. The diode is specified for a 1550-nm optical wavelength but it operates very well at the 1310-nm test frequency, as well. The sensitivity of the diode is 0.9 A/W, which means for every watt of illumination power the diode allows 0.9 A of current to flow. This design has been tested at power levels of 5 mW and below.



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Figure 3. Frequency Shaping Components Shown in Red

3 Design Options

3.1 Diode Bias

There are two ways to apply the bias voltage to the photo diode. This first option is the use of inductors. The benefit of inductors is that the voltage applied to the diode is independent of the diode current. The drawback of using bias inductors is that inductors short out low-frequency optical currents. Inductors are also more expensive than resistors, which are the other option for diode bias.

In [Figure 1](#), inductors L1 and L2 are used to provide reverse bias to the photo diode. The diode used in TIDA-01350 is designed for a 5-V bias voltage, which is also the recommended supply voltage for the LMH5401 amplifier, so the bias inductors connect to the same supplies that are used for the amplifiers. Key parameters to consider when choosing the bias inductors are the inductance, parasitic capacitance, and series resistance. This design uses 1- μ H inductors, which provide a good balance of high impedance at low frequencies while maintaining low parasitic resistance. A larger value inductor improves the low-frequency response.

The photo diode can also be biased with resistors, as the previous [Figure 3](#) shows. If resistors are desired for providing the diode bias, make sure that the diode DC current does not reduce the DC bias voltage to the point that the diode performance suffers. Note that the diode junction capacitance increases as the bias voltage on the diode decreases. This increase in diode junction capacitance causes a decrease in system bandwidth.

Given a diode sensitivity of 0.9 A/W and an average illumination power of 1 mW, the average diode current is 0.9 mA. With two 1-k bias resistors, the diode bias voltage is reduced by $2 \times (0.0009 \times 1000) = 1.8$ V, which leaves a bias voltage of 5 V $-$ 1.8 V = 3.2 V.

Even though many electrical signals are zero-referenced, it is rare for optical signals to be fully modulated. Typically, a modulated optical signal only has modulation which is specified as an extinction ratio (ER). The ER is defined as the ratio of the one power to the zero power and is usually specified in dB. For example, if the one power is 1 mW and the zero power is 0.5 mW, the ER is $10 \times \log(1 / 0.5) = 3.0$ dB. A fully-modulated signal where the zero level is 0 mW would have an infinite ER.

The standing bias current required by the photo diode is determined by both the modulation current and the ER of the diode. The current consumed by the diode in the zero logic state is basically waste current. When using inductive bias, this waste current does not dissipate nearly as much power. In contrast, when using a resistive bias, the waste current contributes to voltage loss in the bias resistors. Using small-value bias resistors keeps this loss low, but then the signal current is diverted from the TIA and into the bias resistors. This dilemma makes selection of the bias resistor value difficult. A high-value resistor is desired for maximum system gain, so if possible, use a high ER modulator for the signal source.

3.2 AC Coupling and Stability

The capacitors labeled C_{IN} are required to isolate the bias voltage from the amplifier inputs. These capacitors are not optional if a reverse-biased diode is used. While it is possible to use a photo diode with no reverse bias, that application is not addressed in this reference design.

TIAs can be unstable when the input capacitance is too large. Place capacitors in parallel with the feedback resistors to stabilize the circuit. These capacitors are shown as CF1. These resistors are not required for the chosen photo diode, as discovered during characterization of the circuit.

The second-stage amplifier is a voltage amplifier. The LMH5401 device is specified for a minimum stable gain of 3 V/V. The unmarked resistors at the input of stage 2 are used to add gain to stage 2 for stability. These resistors are not required for any of the configurations detailed in this reference design.

[Section 5.1.1](#) provides further detail on the capacitors labeled as C_{b1}, C_{b2}, and Peaking Caps.

4 Getting Started Hardware

The performance of the TIDA-01350 has been evaluated using TINA-TI™ simulation software as well as in the lab using an optical-to-electrical vector network analyzer. Figure 4 shows the hardware setup diagram for evaluating the reference design frequency response. The optical unit is capable of -2 -dBm to 5 -dBm laser power. Use optical attenuators to test smaller input signals and reduce the optical power to the desired level.

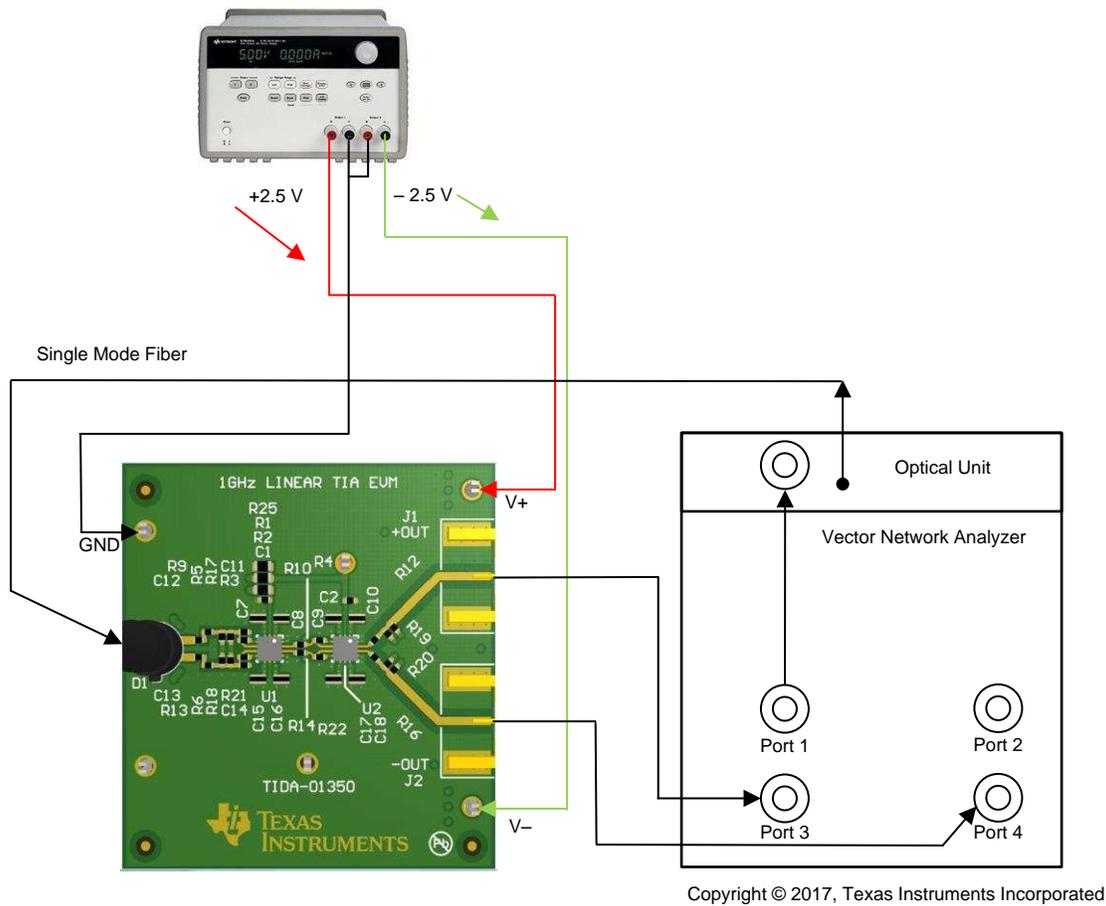


Figure 4. Hardware Setup Diagram

4.1 Applying Power and Basic Setup

The following subsections cover the two main test configurations for the TIDA-01350 reference design. The first configuration is for frequency response (see [Figure 4](#)). The second configuration is for time domain testing (see [Figure 9](#)).

4.1.1 Board Power Supply Setup

The TIDA-01350 reference design supports a supply voltage range of 4.5 V to 5.25 V. The recommended supply voltages are +2.5 V and -2.5 V with the output common-mode voltages set to 0 V. The setup procedure is as follows:

1. With the supplies disconnected, set the voltage on the DC power supply (capable of sourcing 300-mA current) between 4.5 V to 5.25 V. Also, set the current compliance limit to approximately 200 mA on the DC power supply.
2. Keeping the supplies turned OFF, connect the positive supply lead of the DC power supply to the red V+ test point.
3. Connect the negative power supply lead to the yellow V- test point.
4. When using split-supply supplies, connect the black GND connector to the supply common. When using single supplies, connect the black GND connector to V-.
5. When using single supplies, the Vcm pin must be set to an appropriate voltage as detailed in [Section 4.2](#). See [LMH5401 8-GHz, Low-Noise, Low-Power, Fully-Differential Amplifier](#) (SBOS710) for the voltage limits of this pin.
6. Enable the power supplies. The supply current must be approximately 120 mA.

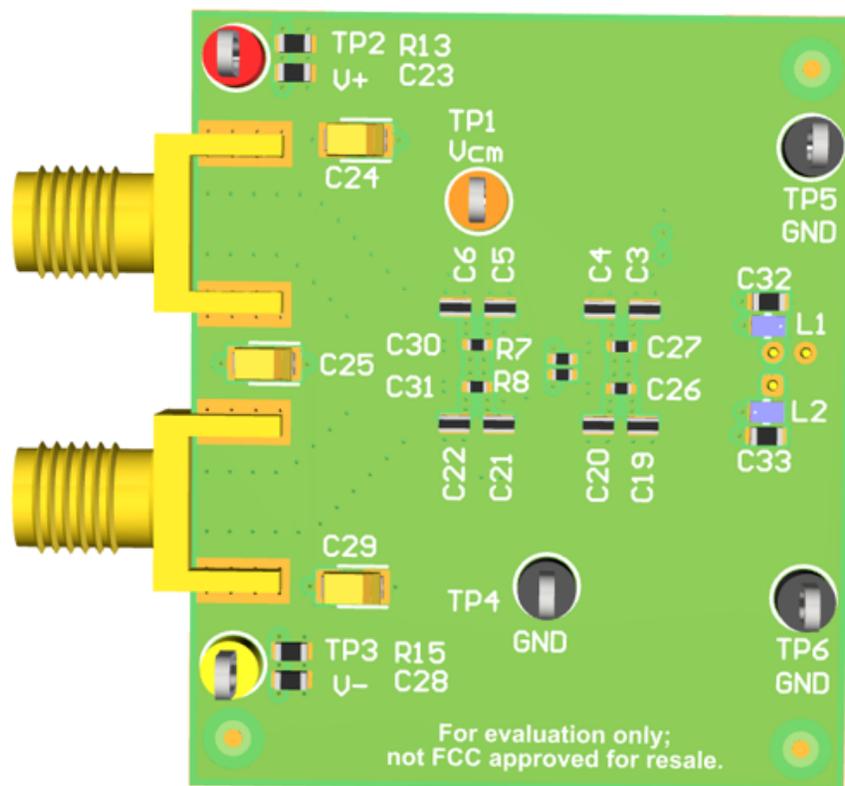


Figure 5. Board Layout Bottom Showing Supply Connections

4.1.2 Connecting Optical Input

1. Make sure the optical source is disabled.
2. The photodiode has an attached fiber optic cable with an angled physical contact (APC) connector. APC connectors are typically green in color. Check the owner's manual to determine what kind of connector the test equipment uses by default.
3. Connect the diode optical fiber to the optical source.
4. Enable the optical source.

4.1.3 Connecting AC Test Equipment

1. The +OUT and –OUT connectors (J1 and J2) are 50-Ω SMA connectors. Use a 50-Ω cable to connect these two connectors to test equipment that supports differential signaling, or use math as detailed in the following steps to extract the proper signal.
2. For differential signal measurement, an oscilloscope should be set to CHA – CHB to show a differential signal when +OUT and –OUT are connected to CHA and CHB, respectively.
3. For common-mode signal measurement, an oscilloscope should be set to (CHA + CHB) / 2 to show a differential signal when +OUT and –OUT are connected to CHA and CHB, respectively.

4.2 Output Common-Mode Voltage Option

The LMH5401 amplifier features an output common-mode control pin. This pin allows a small amount of voltage adjustment in the amplifier output common-mode voltage ($V_{ocm} = (+OUT - -OUT) / 2$). For small output voltage levels ($2 V_{pp}$ or lower), the amplifier output common-mode can be offset from mid supply by 0.5 V. For large output signals, the amplifier output common-mode must be set exactly to mid supply.

By default, the TIDA-01350 board has a 1-kΩ resistor from the Vcm test point to ground. This configuration is appropriate for split supplies that are symmetrical about ground. All testing for this design guide has been performed using split 2.5-V power supplies and $V_{ocm} = 0$ V.

Two options are available for single supplies or for supply voltages that are not symmetrical. The first option is to connect a bench power supply with the desired Vcm voltage to the Vcm test point. With a 1-kΩ resistor to ground, it is very easy to overdrive this pin to the desired voltage with no changes to the board. The second option is to remove R14 and use resistors R1 and R2 to set a voltage divider to set the proper Vcm voltage using the existing supplies. This option does not require an additional bench supply, but does require board modifications.

5 Testing and Results

5.1 Frequency Response

Figure 4 details the setup procedure for frequency response testing. Figure 6 shows the frequency response for several input optical power levels. This graph covers signals from -2 dBm to -27 dBm. The ER is approximately 5 dB.

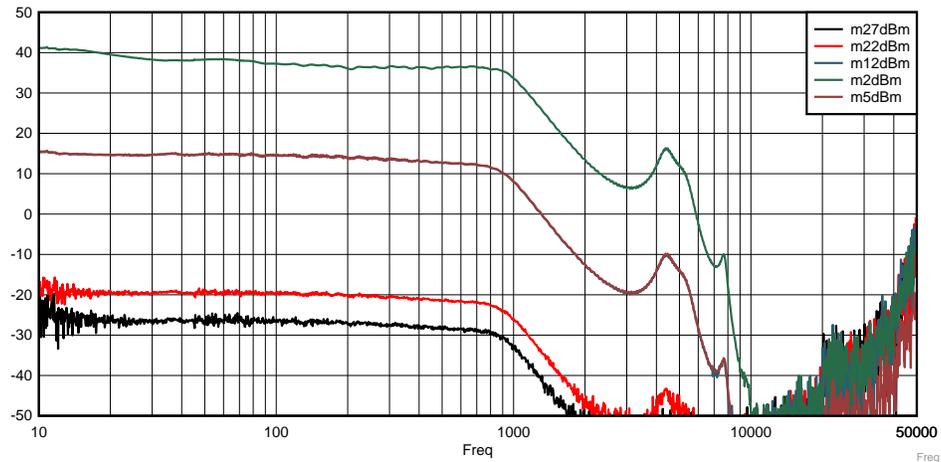


Figure 6. Optical Input Frequency Response

Note that in Figure 6 the gain shown includes losses in the optical modulator, so the gain is not directly correlated to the board gain. Table 2 lists the calculations for board gain.

5.1.1 Shaping Frequency Response

The addition of a few components enables the user to shape the frequency response to eliminate the gradual amplitude loss shown in the previous Section 5.1. The response in Figure 7 is flat out to 600 MHz. Figure 8 shows the additional components used to generate this frequency response. The trade-off for the increased flat-band response is a faster drop of amplitude above the flat-band frequency.

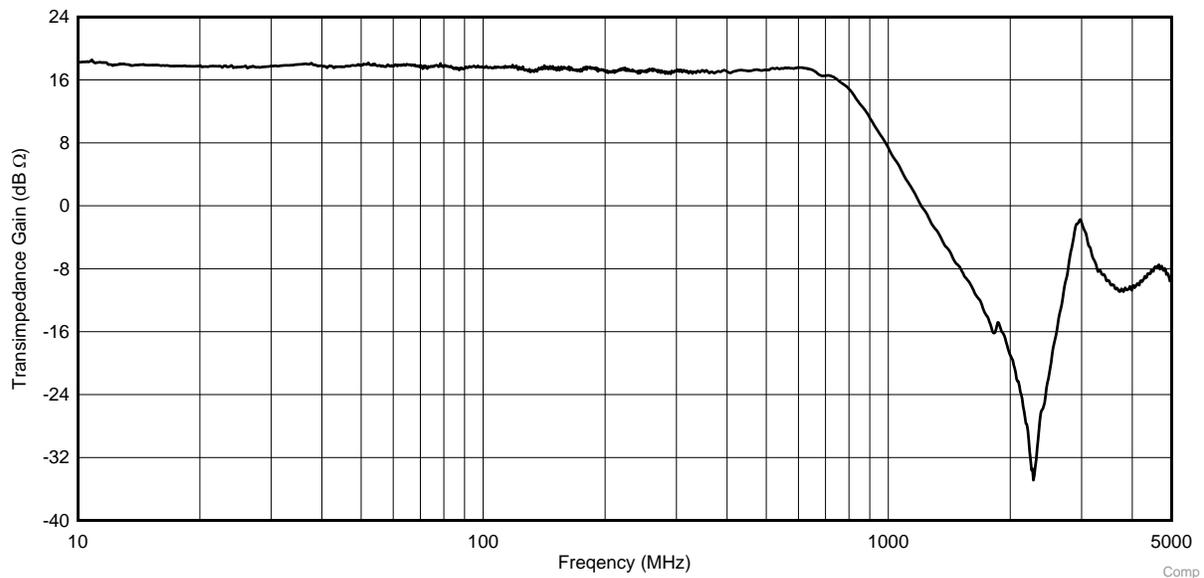
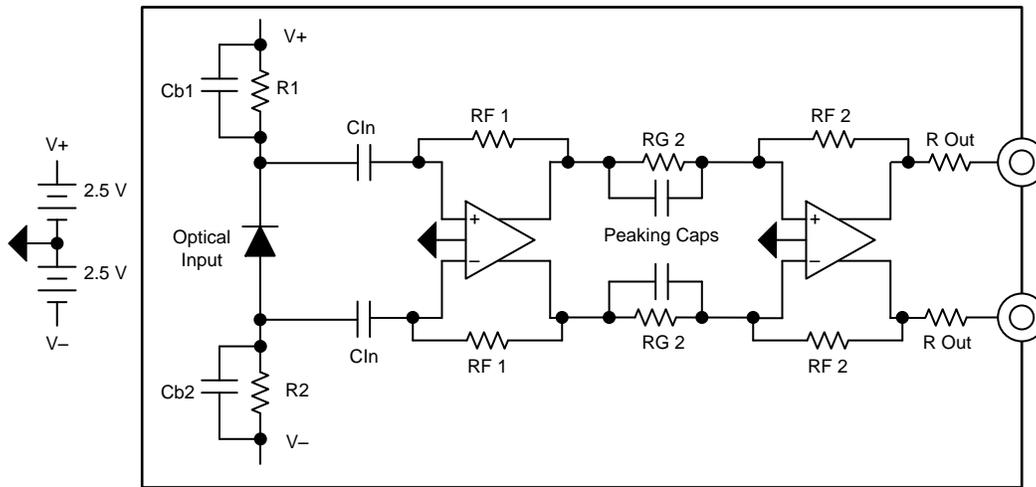


Figure 7. Frequency Response With Frequency Shaping

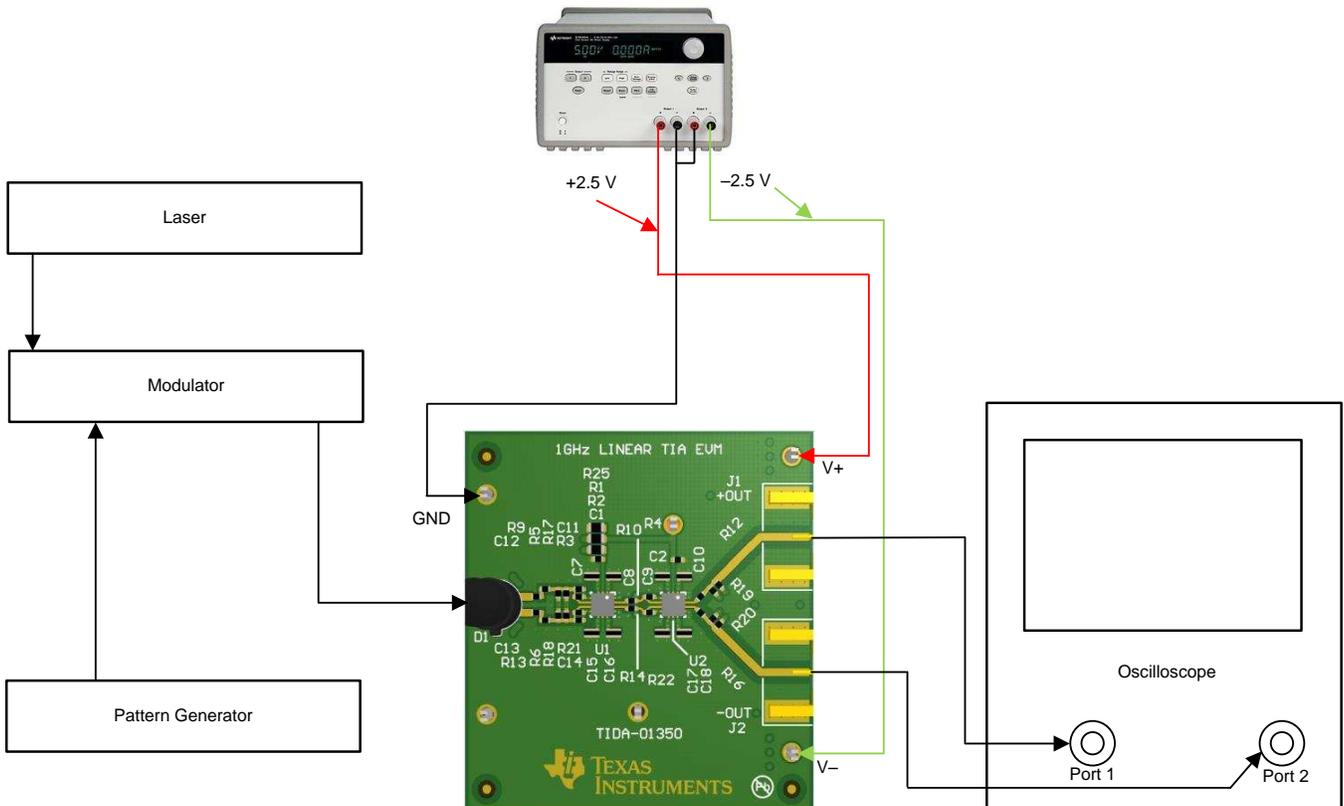


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Figure 8. Schematic Showing Frequency-Shaping Capacitors

5.2 Digital Data Testing

Figure 9 shows the hardware configuration for the digital data testing.



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Figure 9. Test Setup for Digital Testing

Figure 10 and Figure 11 show the results of the time domain measurements.

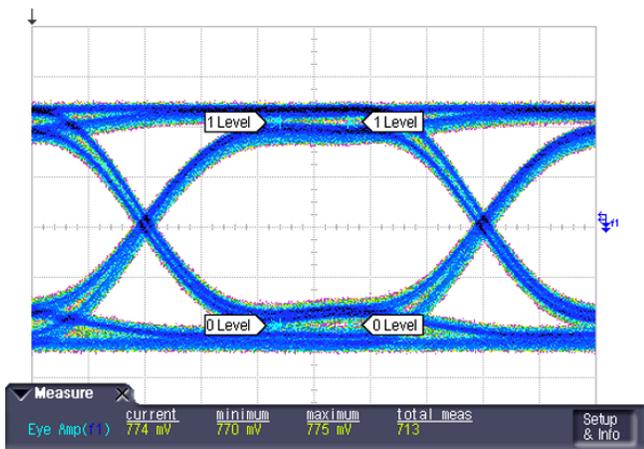


Figure 10. Small Signal Response: f = 700 MHz

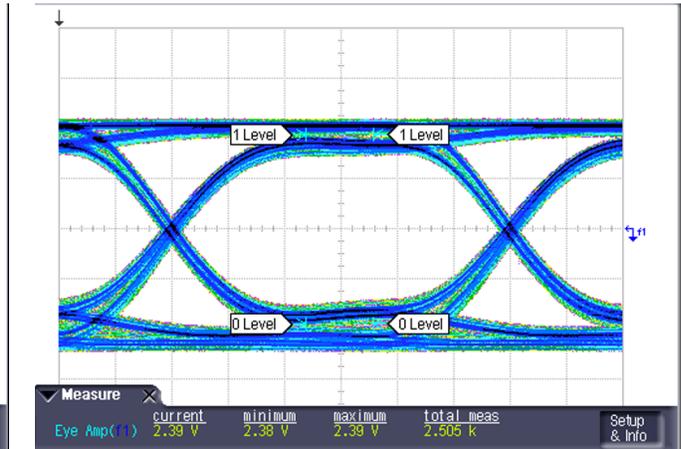


Figure 11. Large Signal Response: f = 700 MHz

5.3 Overall Transimpedance Gain

For high-speed circuits, the capacitance of the photo diode together with the gain of the amplifier limits the bandwidth. Reducing the diode capacitance increases bandwidth and reducing the TIA gain also increases bandwidth. Obtaining the desired bandwidth in one stage may not be possible for a given diode and gain. The TIDA-01350 reference design uses two stages of LMH5401 amplifiers to achieve bandwidths approaching 1 GHz along with transimpedances of 1 k Ω or higher. Table 2 lists the component selections for a variety of gain configurations. Note the 10 Ω in the interstage and output termination resistor columns. This occurrence is to indicate that there is an addition to the Ω of resistance internal to the LMH5410 device. This resistance must be included in the gain calculations.

Table 2. Transimpedance Gain for Various Resistor Values⁽¹⁾

STAGE 1 FEEDBACK RESISTORS	INTERSTAGE RESISTANCE	STAGE 2 FEEDBACK RESISTORS	OUTPUT TERMINATION RESISTORS	TOTAL SYSTEM TRANSIMPEDANCE GAIN
499 Ω	24.9 Ω + 10 Ω	499 V	40 Ω + 10 Ω	3567 Ω
300 Ω	24.9 Ω + 10 Ω	499 V	40 Ω + 10 Ω	2144 Ω
300 Ω	24.9 Ω + 10 Ω	300 V	40 Ω + 10 Ω	1289 Ω
200 Ω	24.9 Ω + 10 Ω	300 V	40 Ω + 10 Ω	859 Ω

⁽¹⁾ Transimpedance gain = $RF1 \times (RF2 / RG2) / 2$

Figure 12 shows the relationship between gain and bandwidth. Similarly, Figure 13 shows the gain for both a single-stage- and two-stage circuit. The performance gained by using two stages is clear.

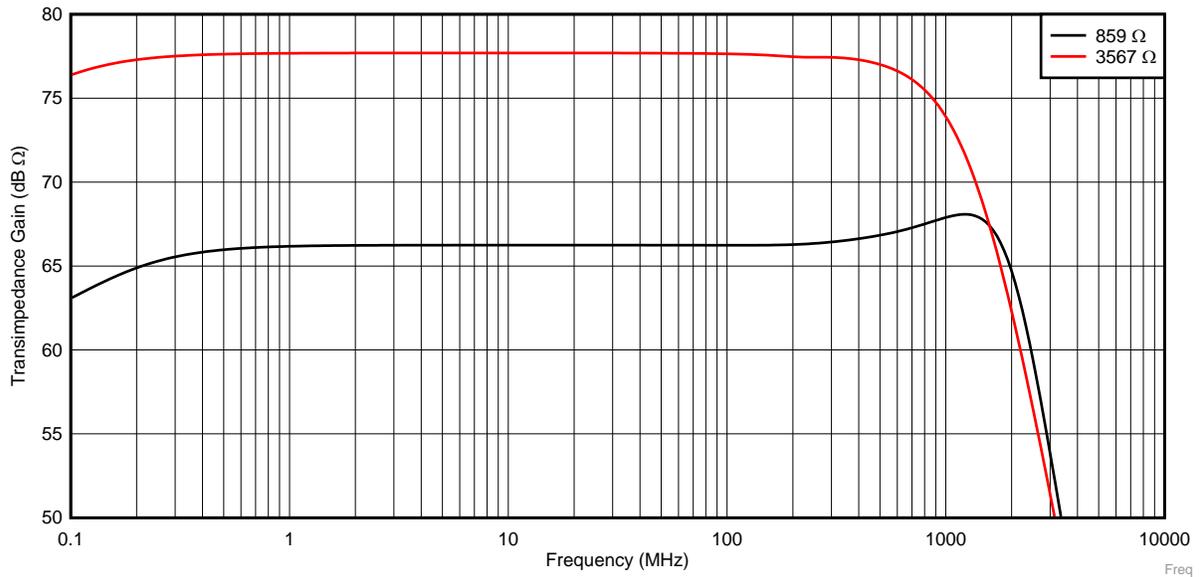


Figure 12. Bandwidth versus Gain for 3567 Ω and 859 Ω

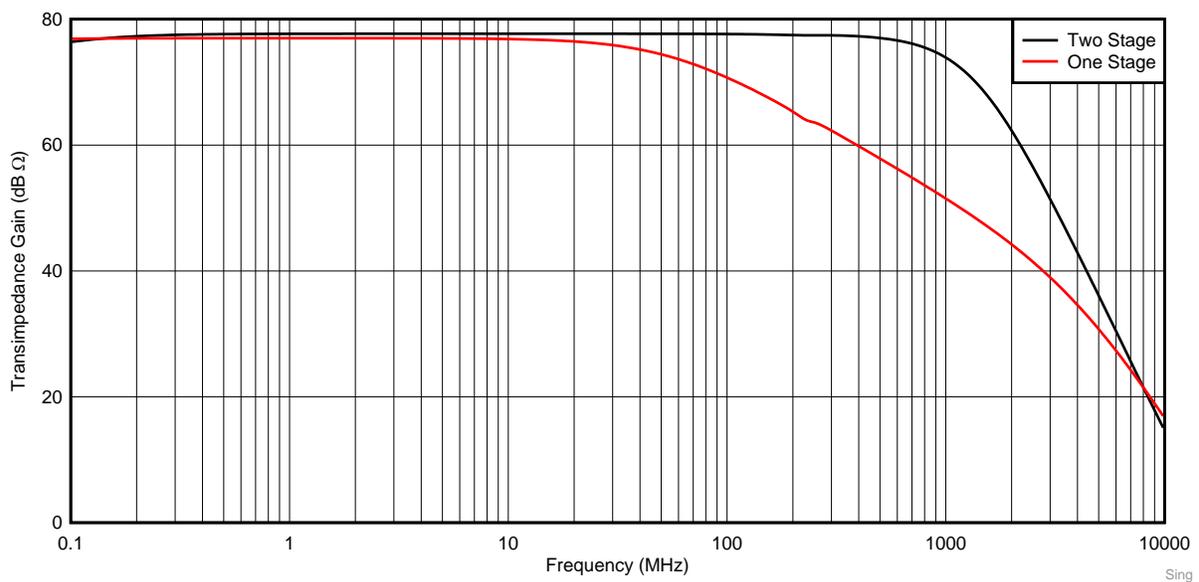


Figure 13. Bandwidth One Stage versus Two Stage

5.4 Noise

Table 3 lists the primary amplifier noise terms. See [Analysis of fully differential amplifiers](#) for a full explanation of amplifier error terms. For this reference design, the noise of the first stage is amplified by the second stage, so the first stage noise dominates. Using a 500-Ω feedback resistor for the first stage, the voltage noise and current noise are both significant. The voltage noise is 1.25 nV/√Hz and the current noise multiplied by the transimpedance gain is 1.75 nV/√Hz. These two noise sources are uncorrelated, so add in a root sum of squares (RSS) manner. The RSS sum of these sources are, in turn, added to the second-stage noise terms. Unlike the first stage, where the voltage and current noise are both significant, only the voltage noise is significant in the second stage. As it turns out, the total system noise is significantly higher than the amplifier contributions. Figure 14 shows the output noise for two different diode bias circuits.

Table 3. Input Referred Error Terms

PARAMETER	VOLTAGE NOISE	CURRENT NOISE
Stage 1 input noise	1.25 nV/√Hz	3.5 pA/√Hz
Stage 1 output noise, R _{F1} = 499	1.25 nV/√Hz	3.5 pA/√Hz × 500 = 1.75 nV/√Hz
Stage 2 input noise (at 100 MHz)	2.66 nV/√Hz	3.5 pA/√Hz × (500 34.9) = 0.122 nV/√Hz
Stage 2 output noise R _{F2} = 499, R _{G2} = 34.9	19 nV/√Hz	—

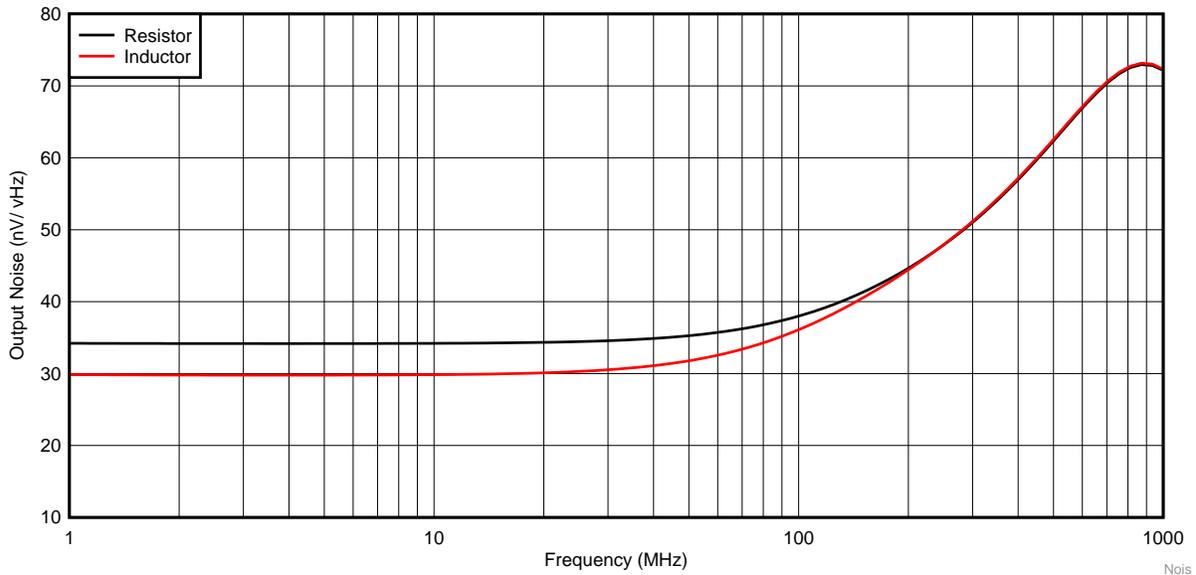


Figure 14. Output Referred Noise

The graph of output voltage noise in Figure 14 shows curves for both inductive bias and resistive bias (1-kΩ resistors) circuits. As expected, the inductive bias provides slightly lower noise because an inductor is ideally noiseless. The reason that the curves converge at higher frequencies is due to the amplifier voltage noise and the diode capacitance. Equation 1 shows the equation for the amplifier noise gain. Notice that the amplifier noise gain is a function of the input capacitance, the feedback resistor, and frequency. What is unique for a TIA is that there is no R_G or gain set resistor, which is a key attribute of the TIA applications. At higher frequencies, the amplifier noise gain grows larger; and so at high frequencies, this noise term dominates the other terms. The rolloff in noise that starts at 900 MHz is due to the frequency-shaping capacitors C_{b1} and C_{b2}.

$$\sqrt{1 + (2\pi f \times C_{IN} \times R_f)^2} \tag{1}$$

One important thing to note about high-frequency circuits is that there are no ideal components. As previously noted, there is no discrete or schematic value for R_G . Employing a careful PCB design to minimize parasitic resistance is essential to obtaining a reasonably accurate value for R_G . This task is especially important at high frequencies because of the RF skin effect, which causes resistance of circuit components to increase with increasing frequency. Likewise, the parasitic capacitance and inductance of the circuit elements can be large enough to cause performance changes. For example, this reference design does not use a feedback capacitor; however, the capacitance of the PCB traces is enough to provide sufficient capacitance on the feedback resistor to ensure stability. Due to this reason, [Equation 1](#) is only accurate at frequencies up to approximately 1.5 GHz.

6 Design Files

6.1 Schematics

To download the schematics, see the design files at [TIDA-01350](#).

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01350](#).

6.3 PCB Layout Recommendations

6.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01350](#).

6.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01350](#).

6.5 Layout Guidelines

Figure 15 shows the layout guidelines for this reference design. The design features a six-layer board with a Rogers RO4350 dielectric under the top layer. Note that the signal path is confined to the top layer. The other layers of the printed-circuit board (PCB) use standard FR406 dielectric. The other layers include ground and power planes. To maximize the interplane capacitance, the positive and negative power supply planes are adjacent on layers 3 and 4, respectively. The overall stack up is: Signal, Ground, V+, V-, Ground, and back.

See the layout section in [LMH5401 8-GHz, Low-Noise, Low-Power, Fully-Differential Amplifier](#) for layout guidelines related to the LMH5401.

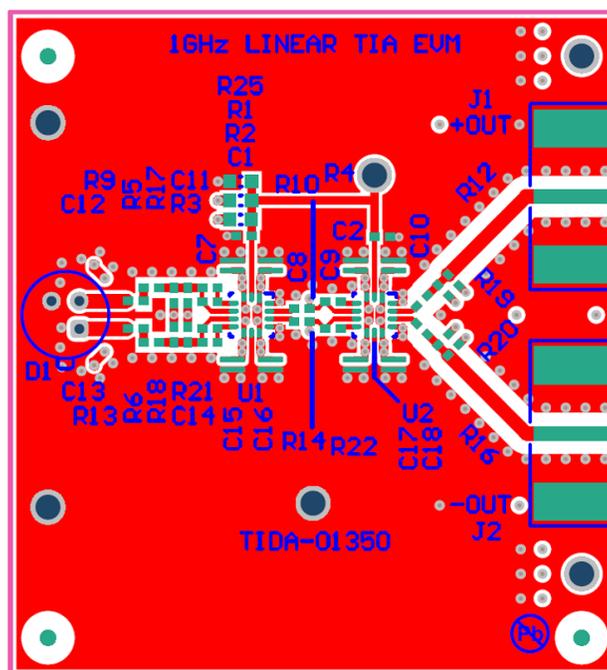


Figure 15. Example Layout (Top Layer)

6.6 Gerber Files

To download the Gerber files, see the design files at [TIDA-01350](#).

6.7 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01350](#).

7 Related Documentation

1. Texas Instruments, [LMH5401 8-GHz, Low-Noise, Low-Power, Fully-Differential Amplifier](#),
2. Texas Instruments, [Analysis of fully differential amplifiers](#)
3. Texas Instruments, [Op amp stability and input capacitance](#)

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8 About the Author

LOREN SIEBERT is an applications engineer with TI in the High-Speed Amplifier division in Fort Collins, Colorado. He supports high speed amplifier applications ranging from 4G and 5G radio base stations to Optical Networking.

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