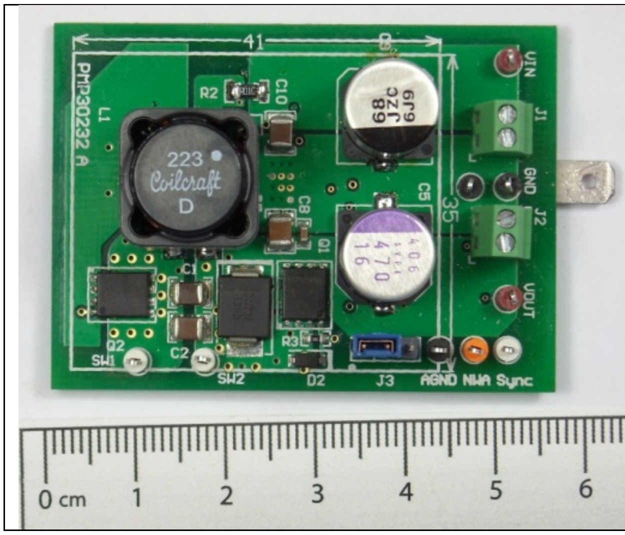
PMP30232RevB Test Results

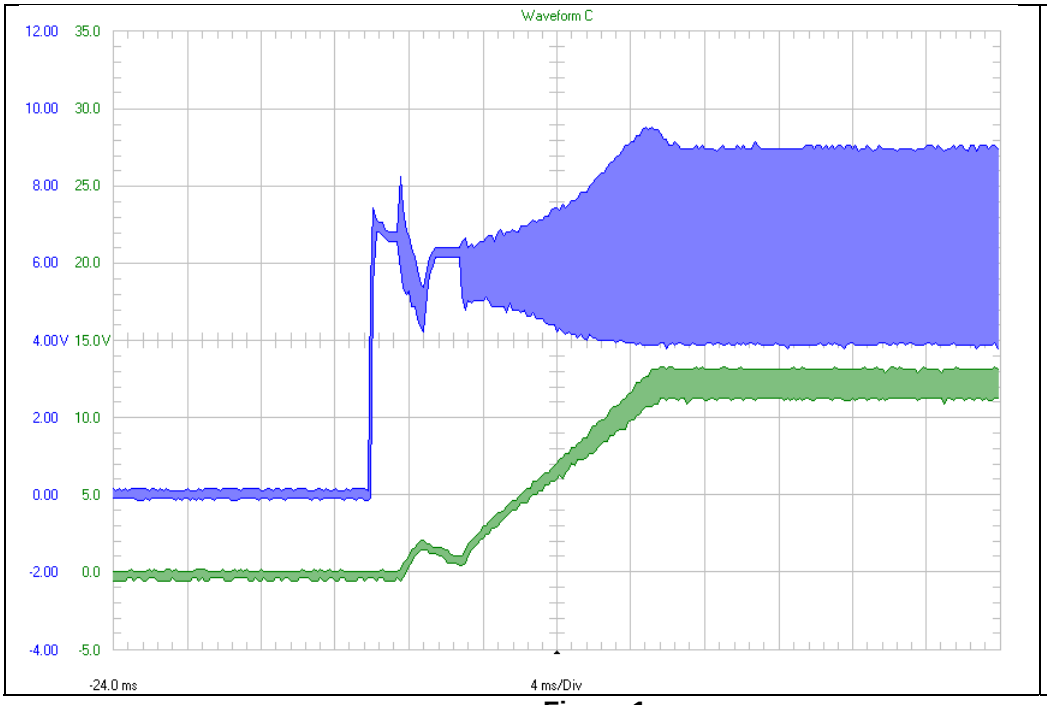
Topology: SEPIC
Device: LM5122
Switching frequency approx. 150kHz, measured here 158kHz
On 6.01V
Off 3.81V
(measured at 120mA load)

Unless otherwise mentioned the output current was set to 2A (with variable resistor)and the mode was set to forced PWM


41
PMP30232 A
L1
R2
C10
223
Coilcraft
D
VIN
J1
GND
J2
VOUT
C5
C8
35
Q1
C1
Q2
SW1
C2
SW2
R3
D2
J3
AGND
NWA
Sync
0 cm
1
2
3
4
5
6

1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set to 6V, with 2A load (resistor) at the output.



Ch1=> input voltage 2V/div

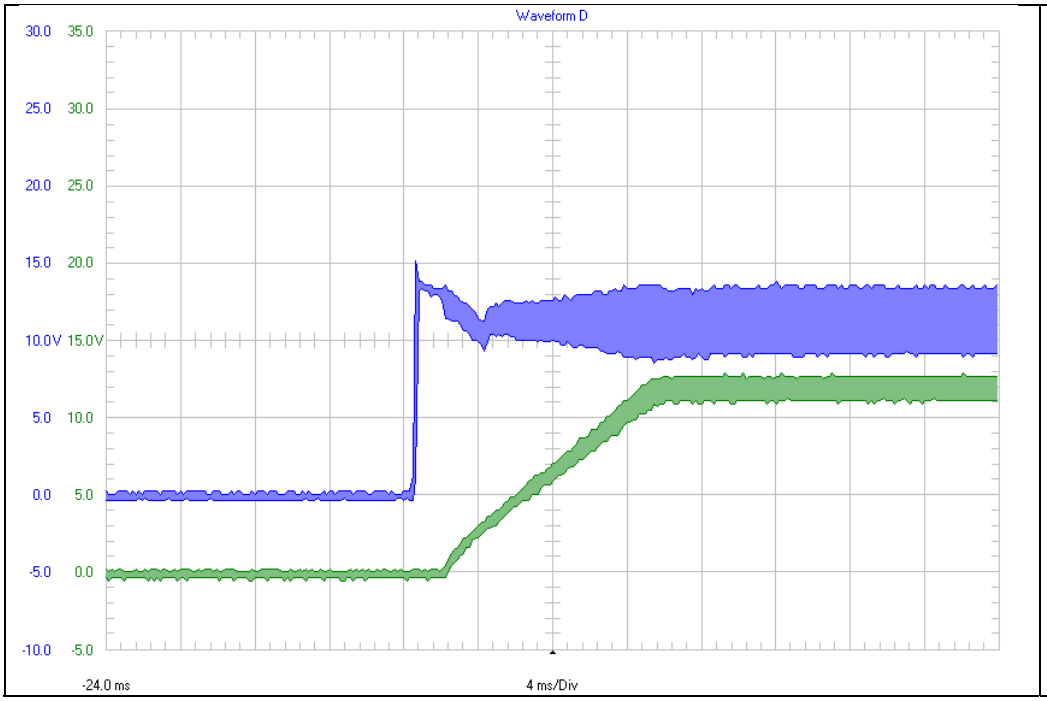
Ch2=> output voltage 5V/div

4ms/div

20MHz bw

Figure 1

The startup waveform is shown in the Figure 2. The input voltage was set to 12V, with 2A load at the output.



Ch1=> input voltage 5V/div

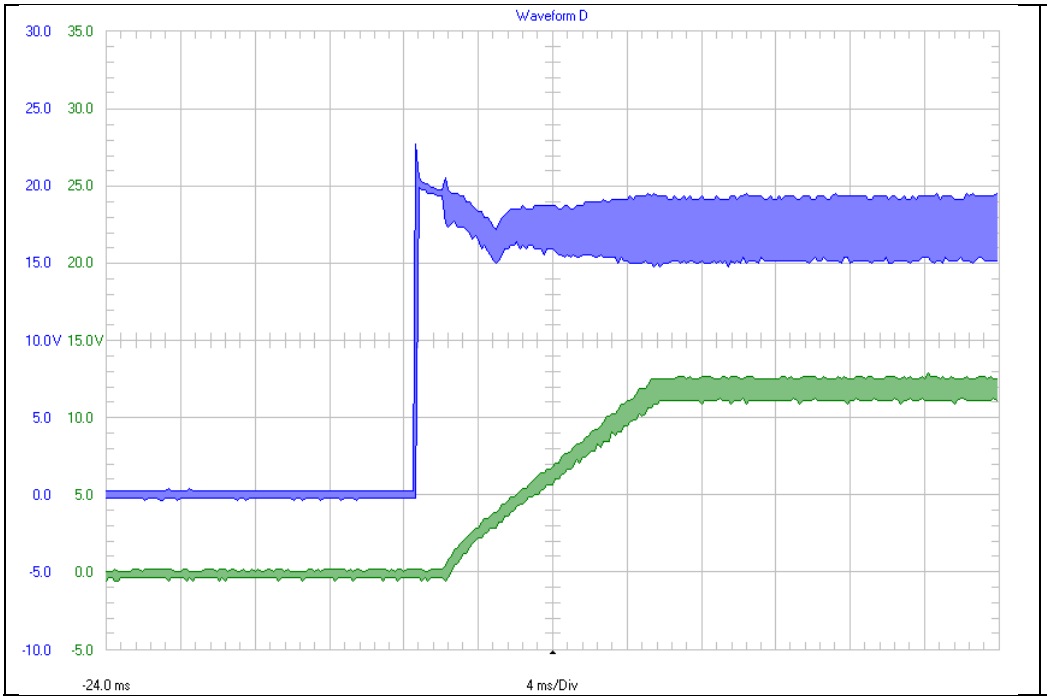
Ch2=> output voltage 5V/div

4ms/div

20MHz bw

Figure 2

The startup waveform is shown in the Figure 3. The input voltage was set to 18V, with 2A load at the output.



Ch1=> input voltage 5V/div

Ch2=> output voltage 5V/div

4ms/div

20MHz bw

Figure 3

2 Shutdown

The shutdown waveform is shown in the Figure 4. The input voltage was set to 6 V, with 2A load on the output. The power supply was disconnected**.**

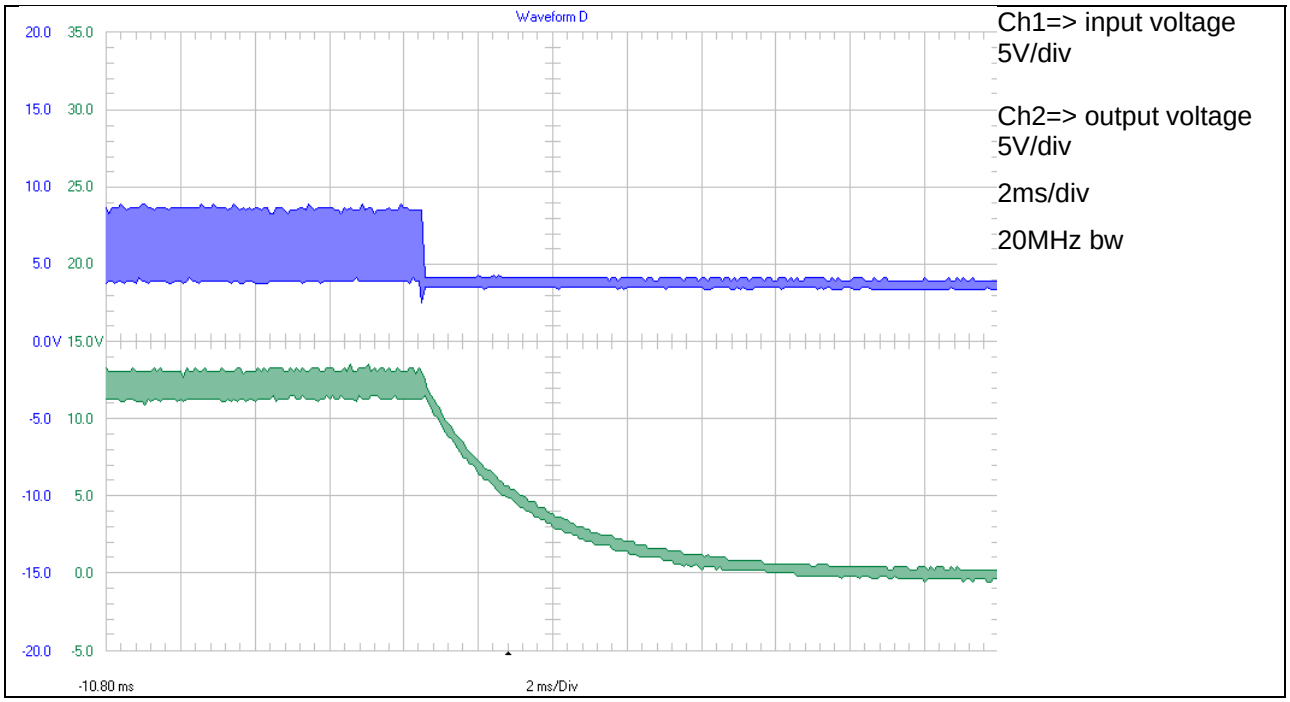


Figure 4

The shutdown waveform is shown in the Figure 5. The input voltage was set to 12V, with 2A load on the output. The power supply was disconnected.

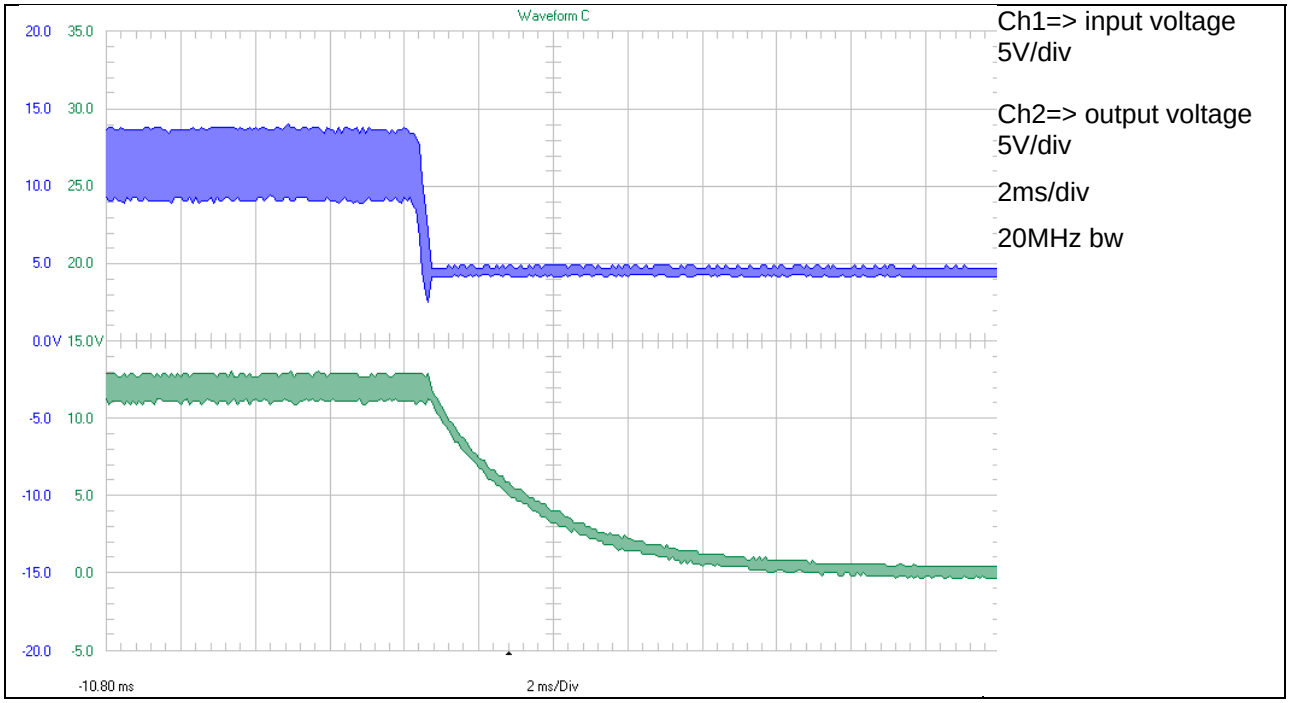


Figure 5

The shutdown waveform is shown in the Figure 6. The input voltage was set to 18V, with 1A load on the output. The power supply was disconnected.

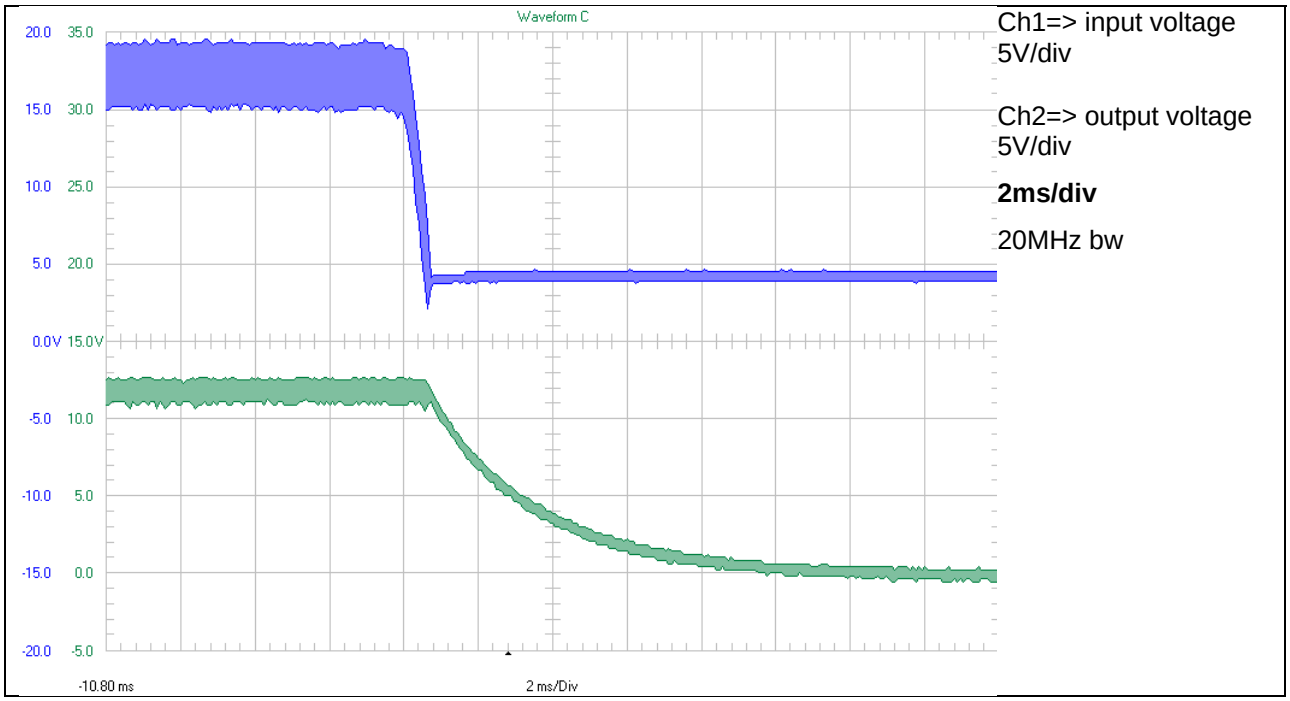


Figure 6

3 Efficiency

3.1 Forced PWM

The efficiency and loss (PIN-POUT) is shown in the Figure 7 below. The input voltage was set to 6V, 12V and 18V. The mode was set to **forced PWM**.

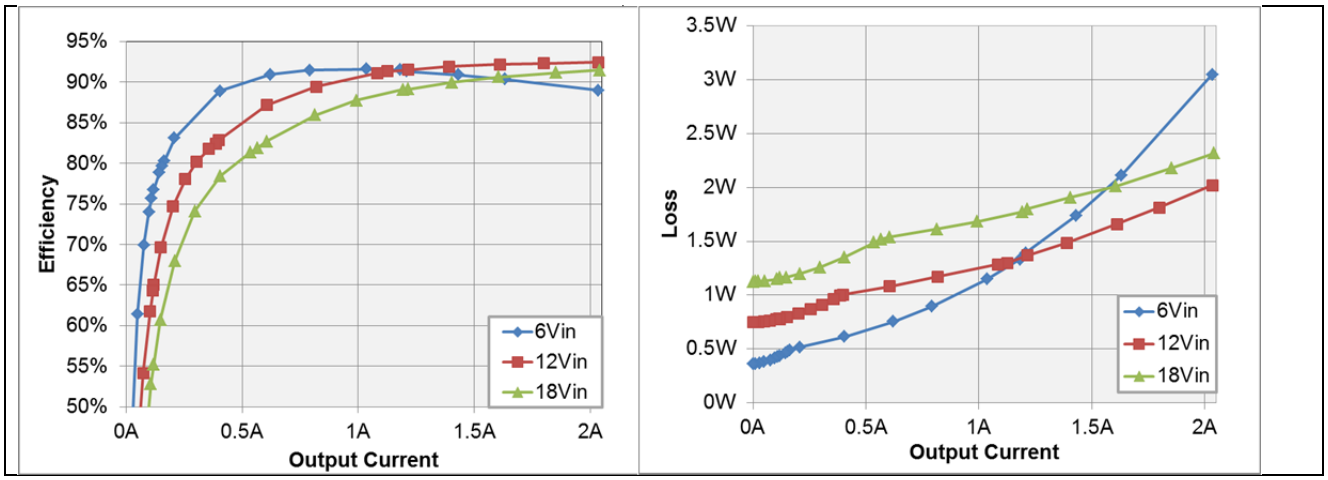


Figure 7

3.2 Diode Emulation

The efficiency and loss (PIN-POUT) is shown in the Figure 8 below. The input voltage was set to 6V, 12V and 18V. The mode was set to **diode Emulation**.

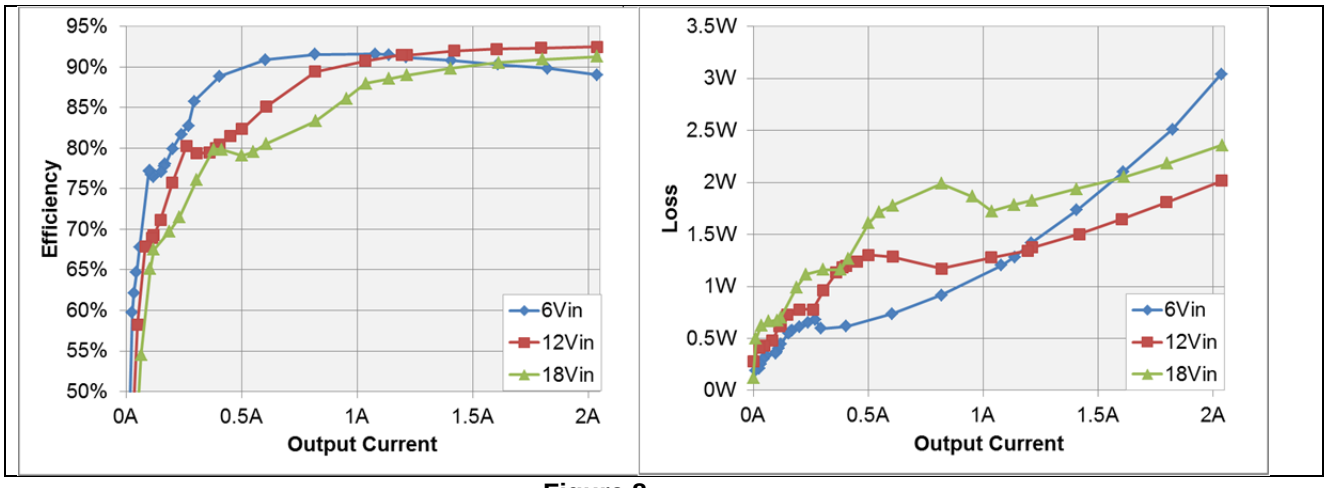
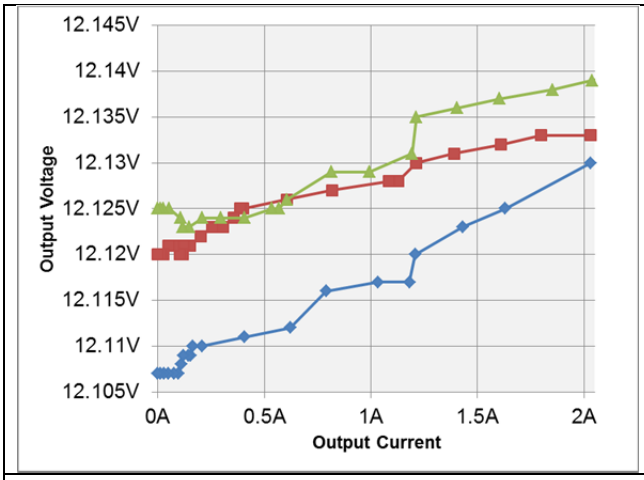


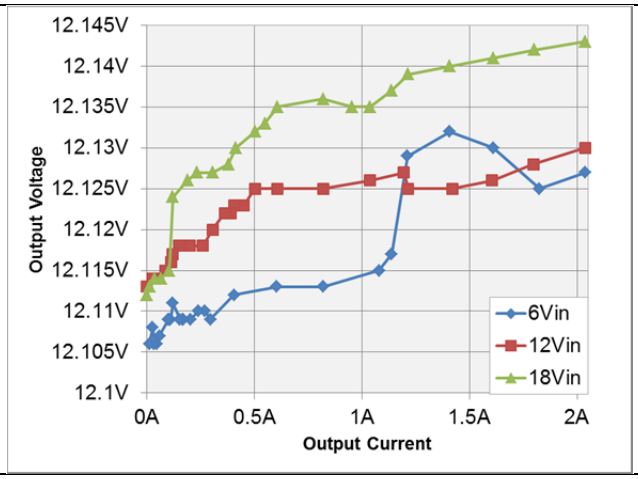
Figure 8

4 Load Regulation

The load regulation of the output is shown in the Figure 9 below. The input voltage was set to 6V, 12V and 18V.



forced PWM



diode emulation

Figure 9

Variable resistors were used (1k, 100R, 10R). The changes took place at 120mA and 1.2A.

5 Line Regulation

The line regulation is shown in Figure 10. The output current was set about 2A.

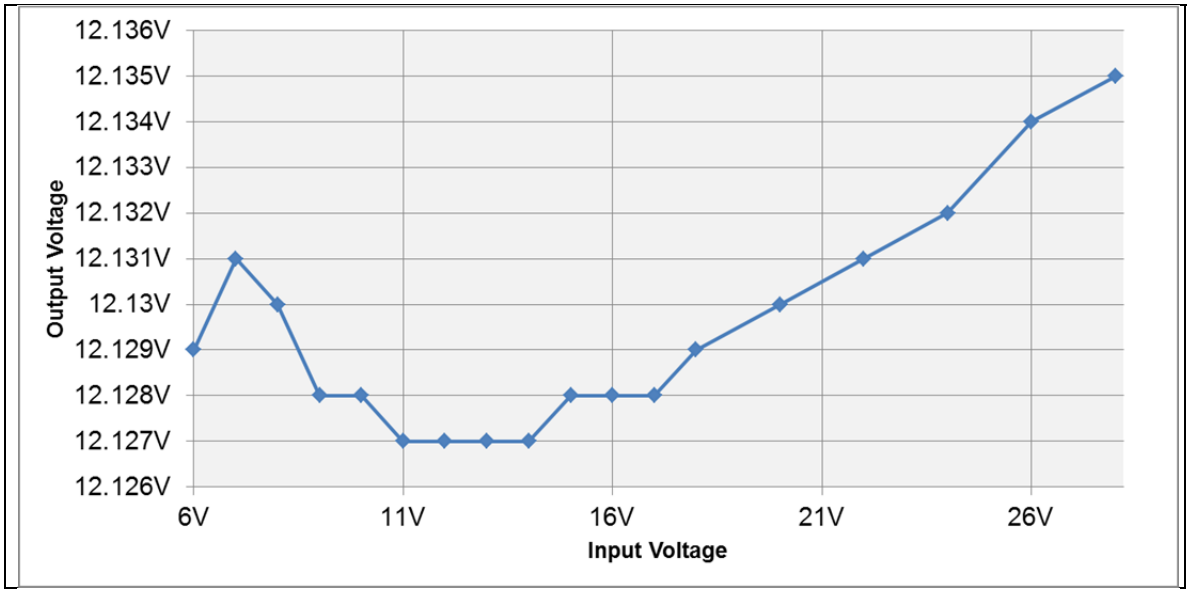


Figure 10

With the same setup efficiencies and losses were calculated. This is shown in Figure 11

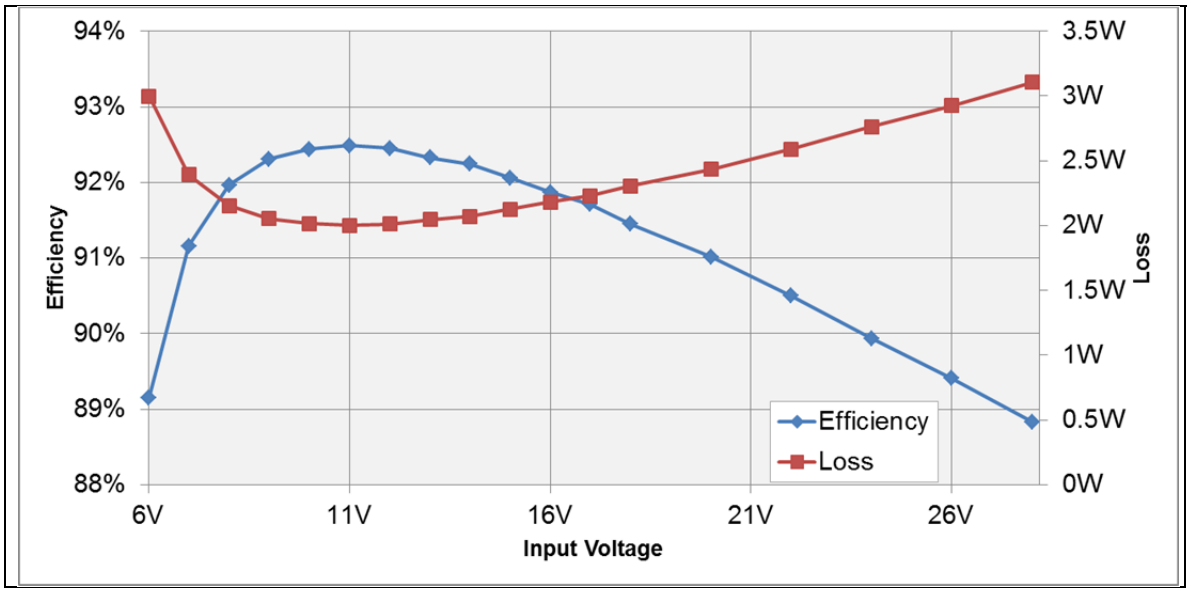
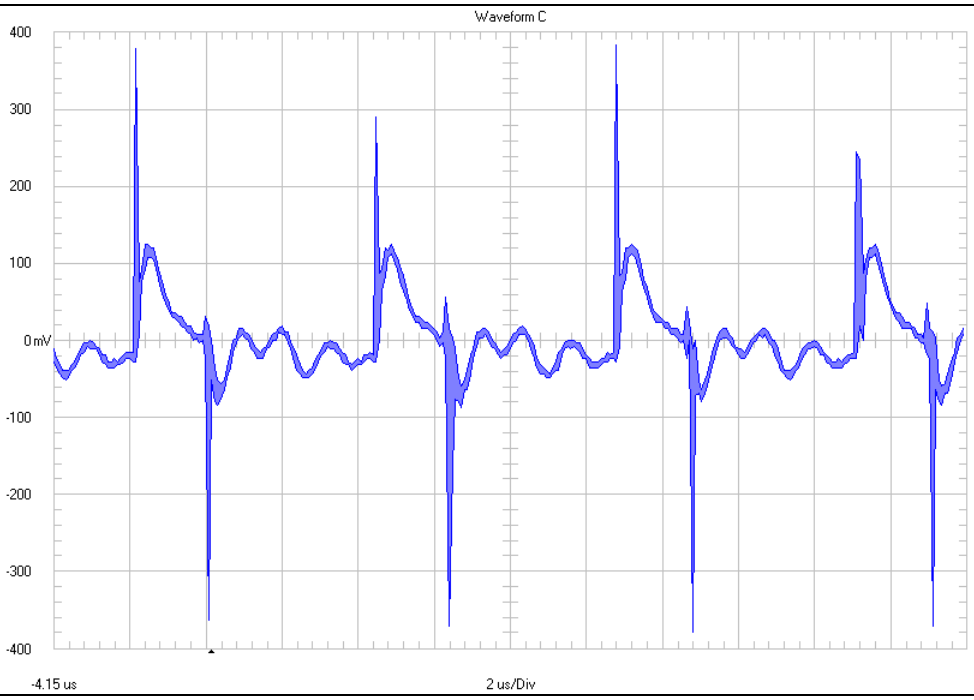


Figure 11

6 Output Ripple Voltage

The output ripple voltage is shown in Figure 12. Input voltage was set to 6V



Ch1 => output ripple

100mV/div

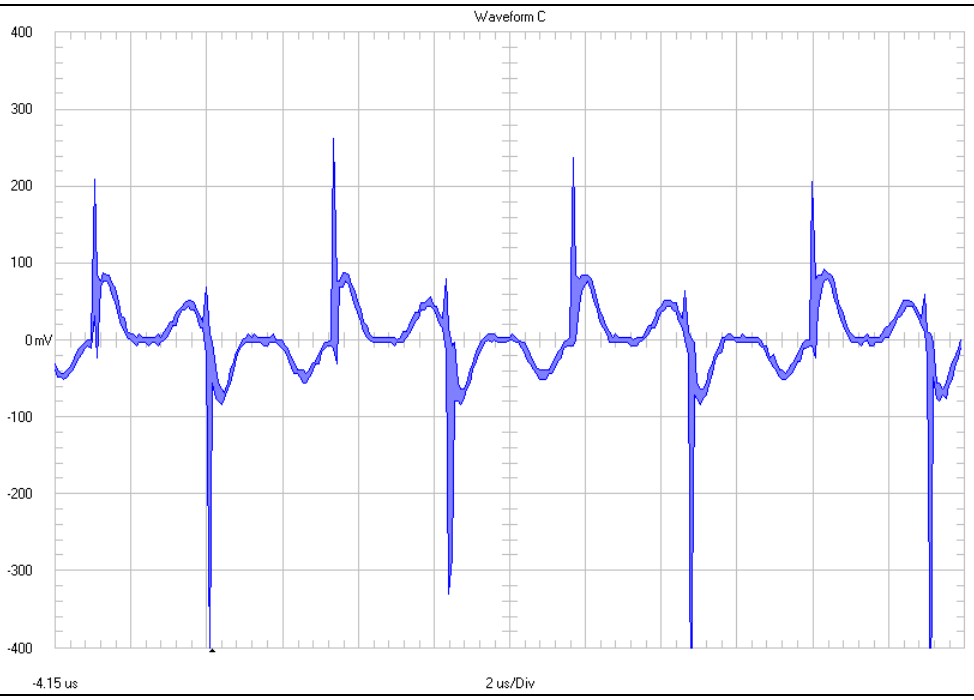
AC coupled

20MHz bw

2µs/div

Figure 12

The output ripple voltage is shown in Figure 13. Input voltage was set to 12V



Ch1 => output ripple

100mV/div

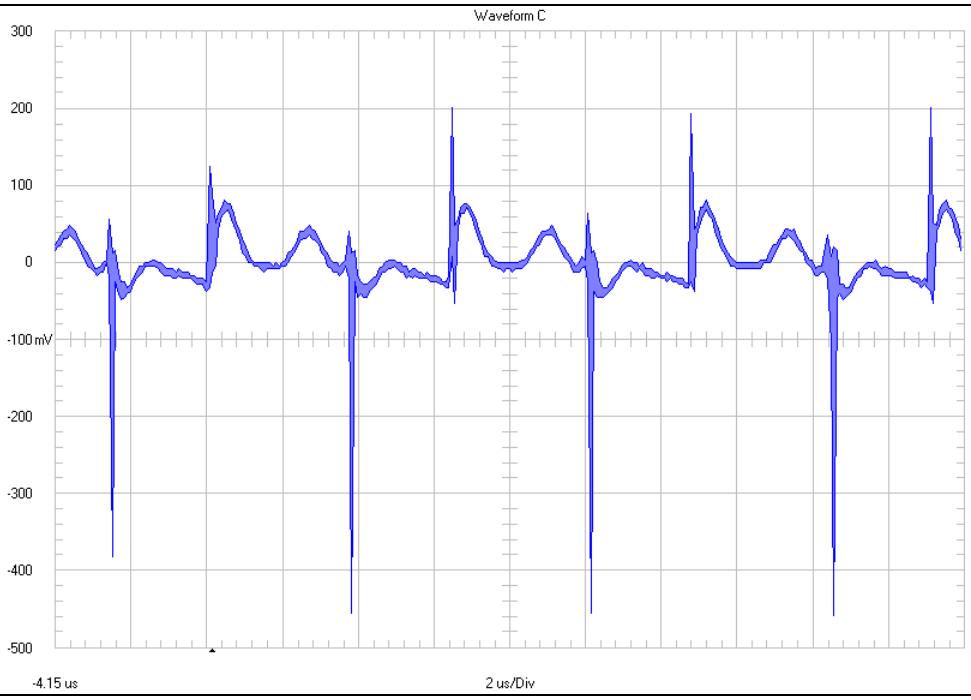
AC coupled

20MHz bw

2µs/div

Figure 13

The output ripple voltage is shown in Figure 14. Input voltage was set to 18V.



Ch1 => output ripple

100mV/div

AC coupled

20MHz bw

2µs/div

Figure 14

7 Input Ripple Voltage

The input ripple voltage is shown in Figure 15.

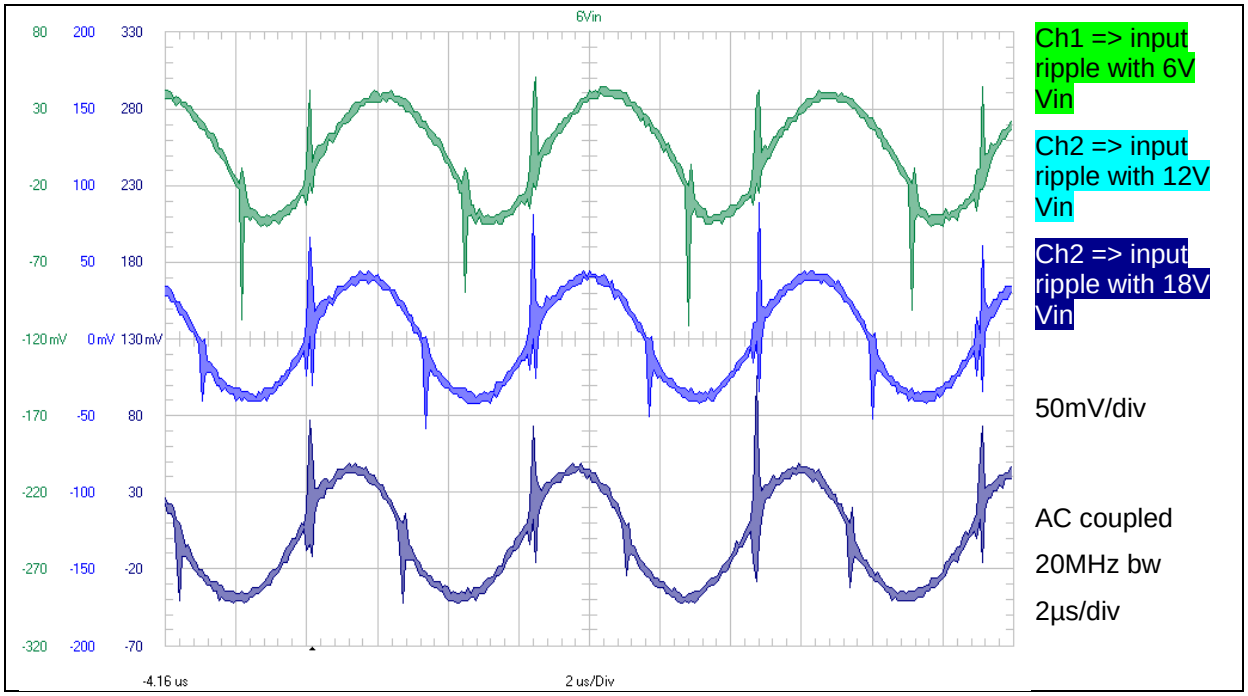


Figure 15

8 Load Transients

The Figure 16 shows the response to load transients for 6V input voltage. The load is switching from 1A to 2A (100Hz)
Electronic load was used

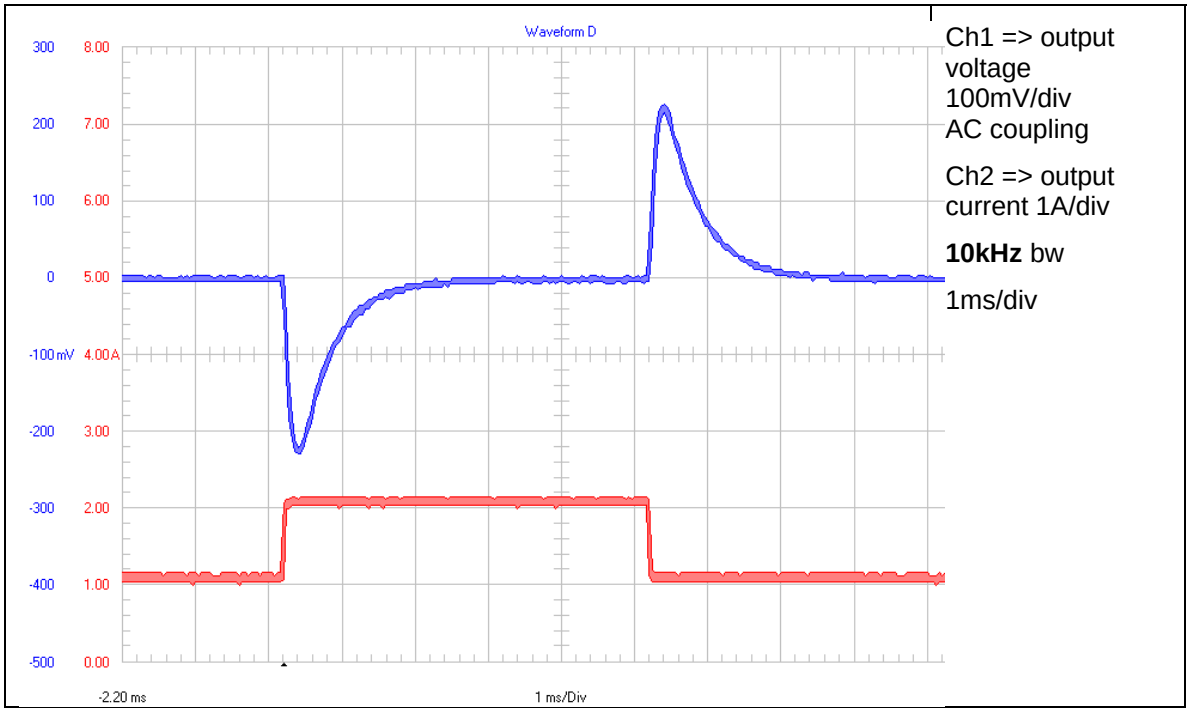


Figure 16

The Figure 17 shows the response to load transients for 12V input voltage. The load is switching from 1A to 2A,
Electronic load was used

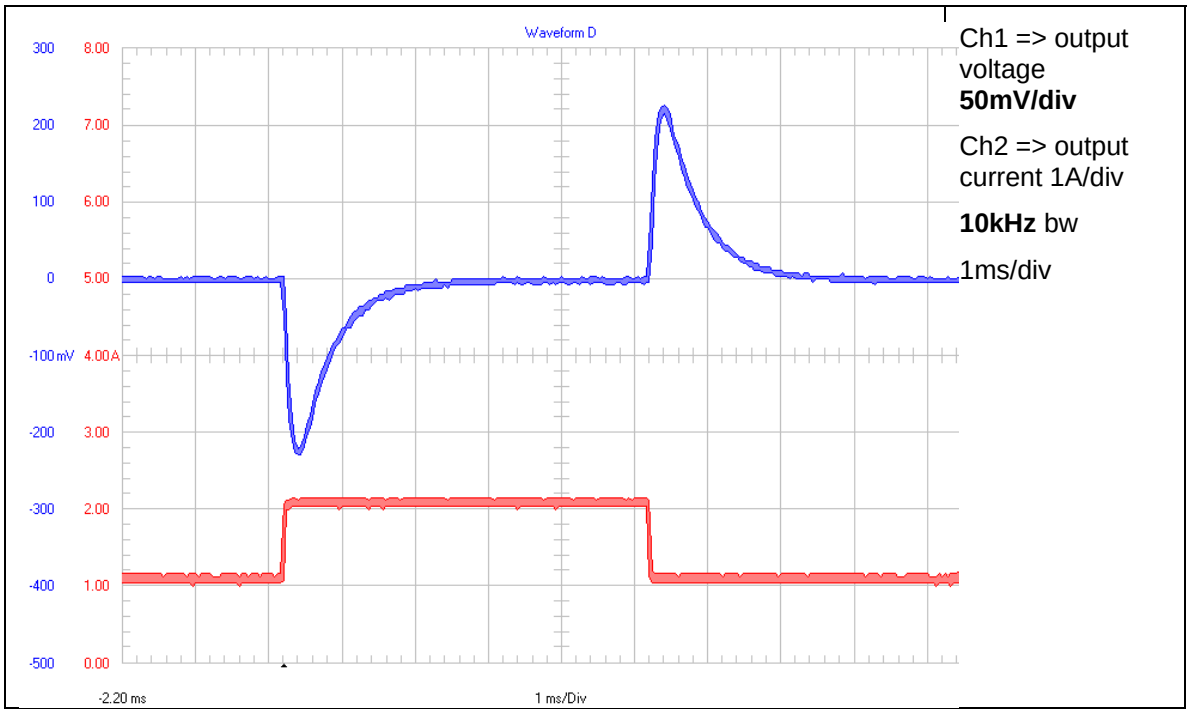


Figure 17

The Figure 18 shows the response to load transients for 18V input voltage. The load is switching from 1A to 2A,
Electronic load was used

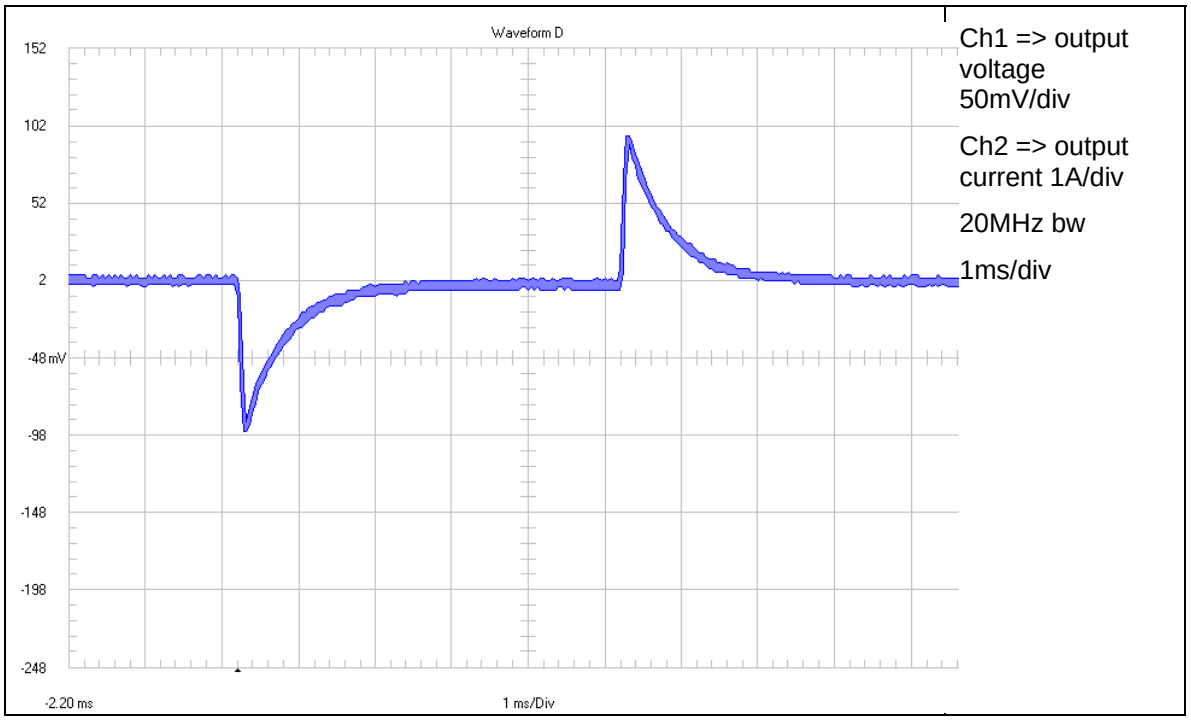


Figure 18

9 Control Loop Frequency Response

Figure 19 shows the loop response for 6V. Load is 2A (resistor).

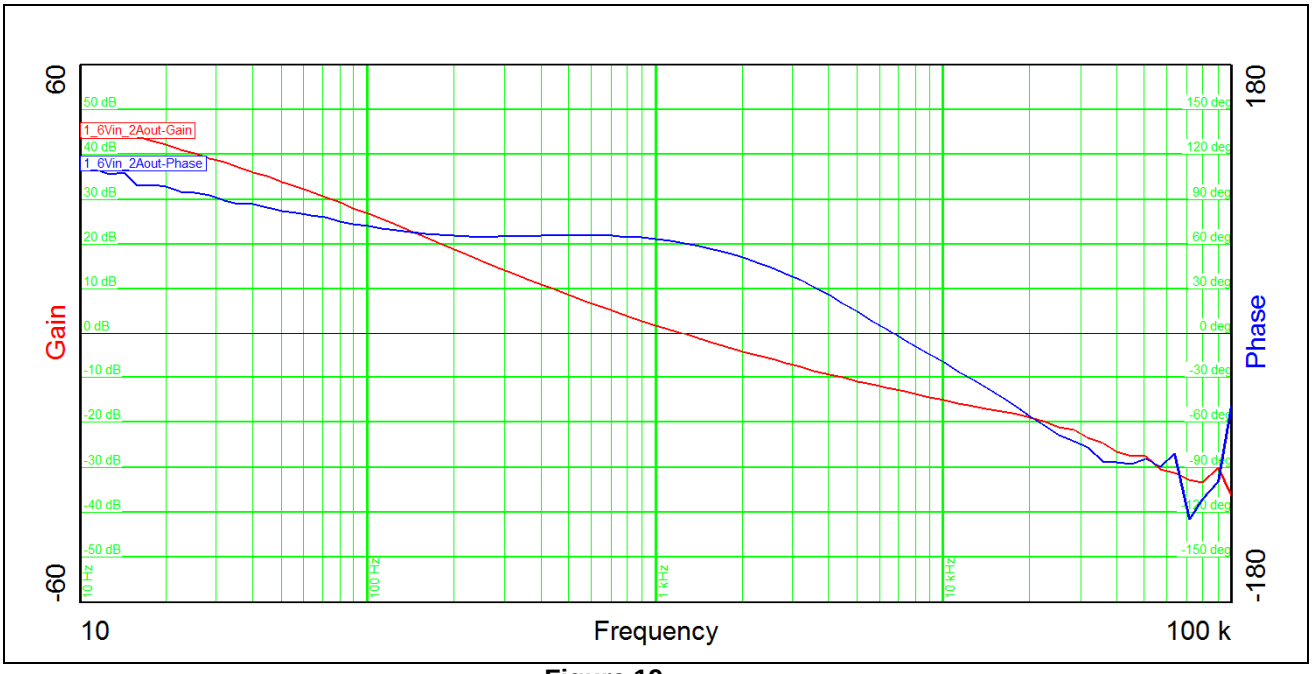


Figure 19

Figure 20 shows the loop response for 12V. Load is 2A.

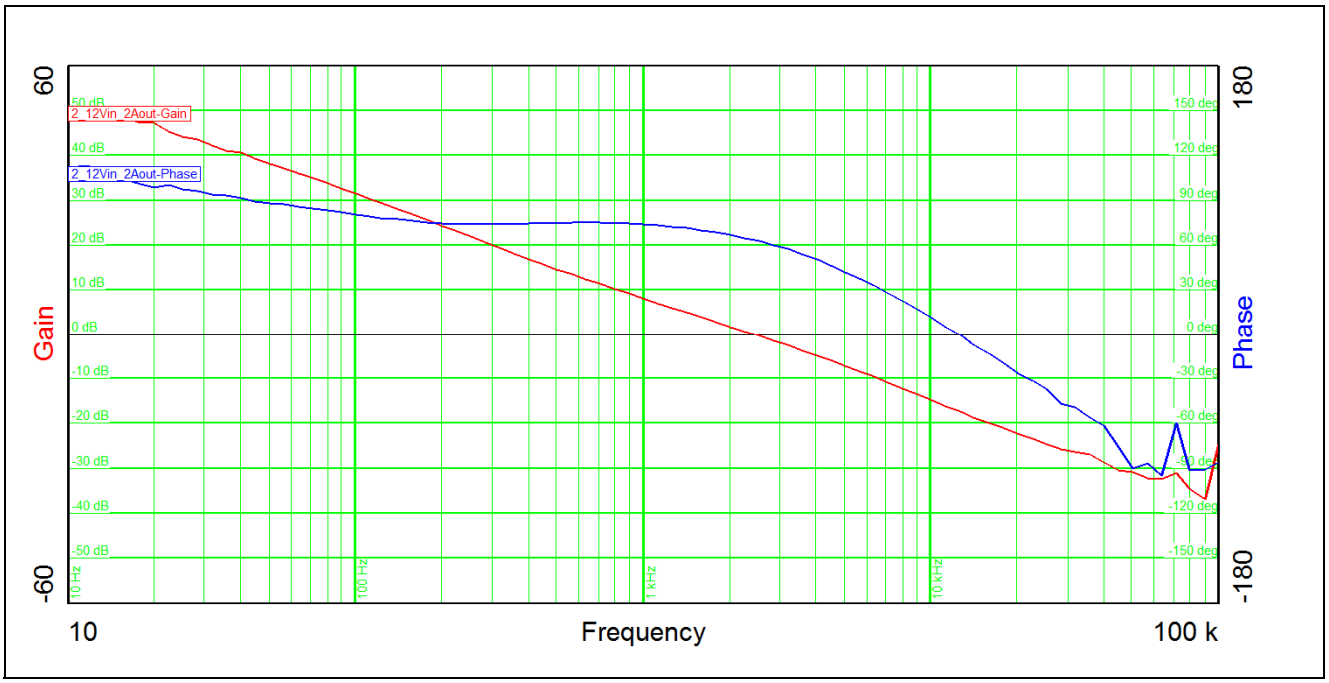


Figure 20

Figure 21 shows the loop response for 18V. Load is 2A.

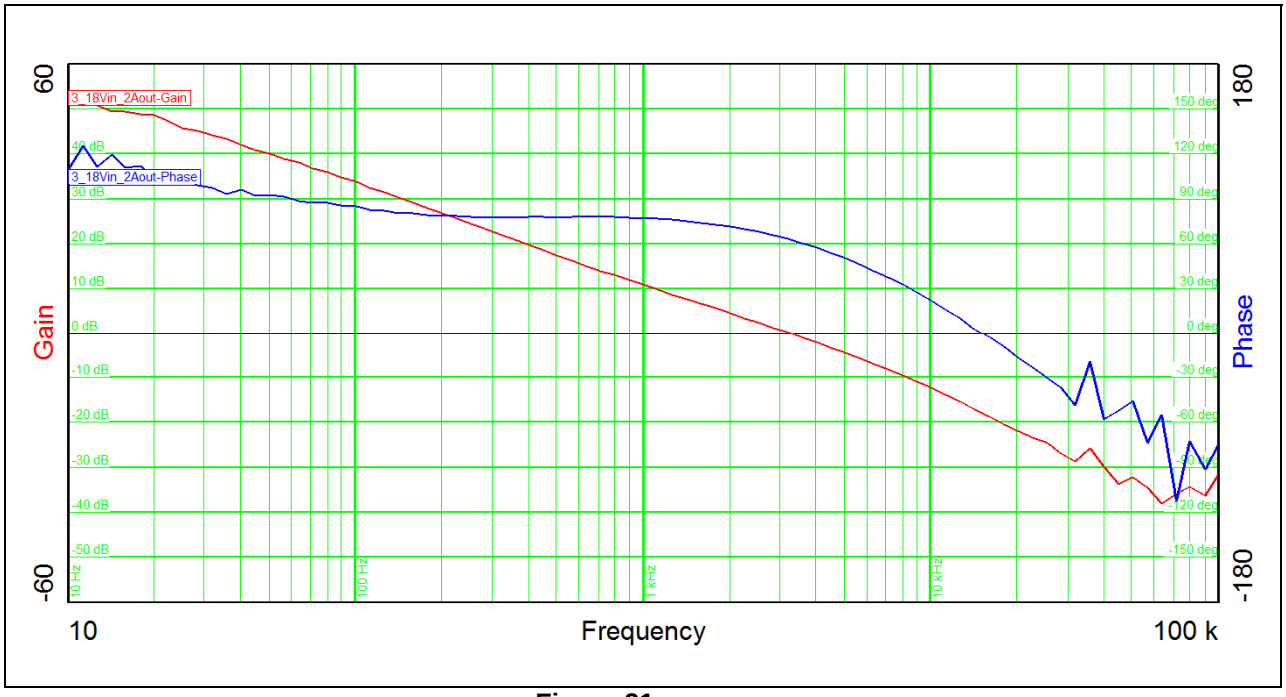


Figure 21

Table 1 summarizes the results of the above measurements

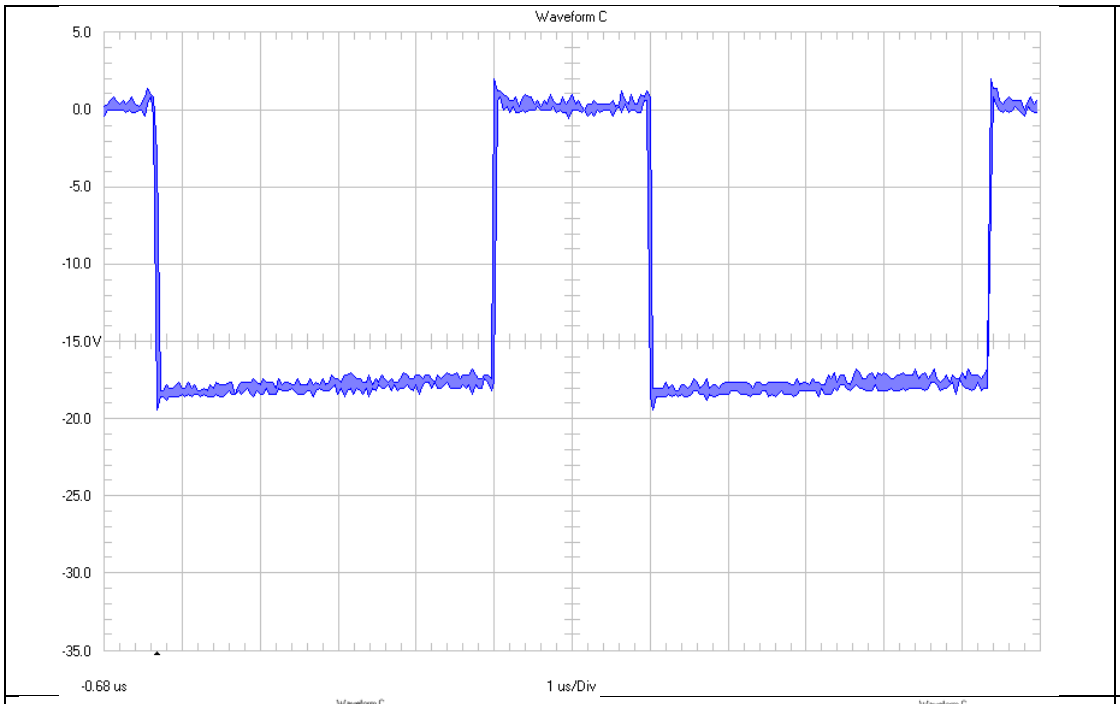
Vin	6V	12V	18V
Bandwidth (Hz)	1234	2431	3247
Phase margin	61°	63°	63°
slope (20dB/decade)	-1	-1.1	-1.1
gain margin (dB)	-12.6	-17.2	-17.9
slope (20dB/decade)	-0.7	-1.2	-1.6
freq (kHz)	6.7	12.6	15.2

Table 1

10 Miscellaneous Waveforms

10.1 Q1 Switch Node (source-VOUT)

The waveform of the voltage on switchnode is shown in Figure 22. Input voltage was set to 6V.



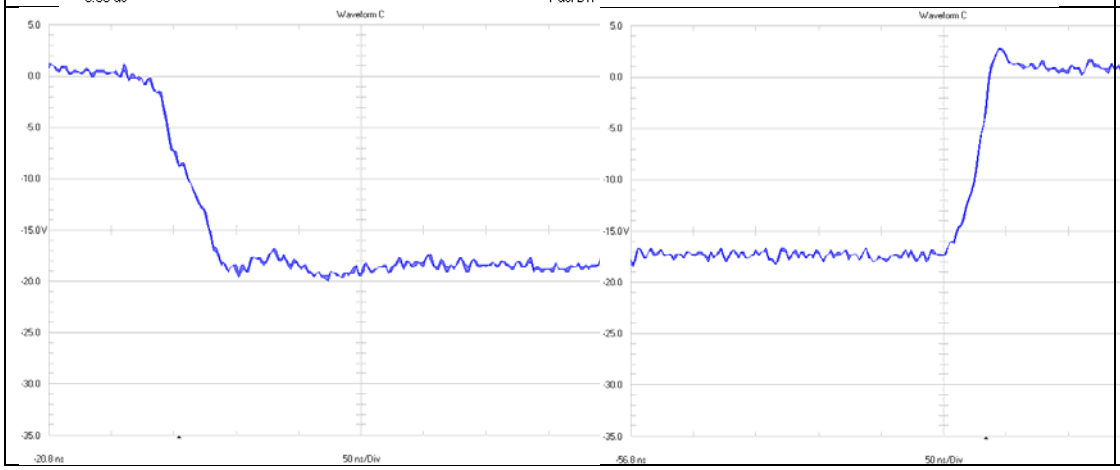
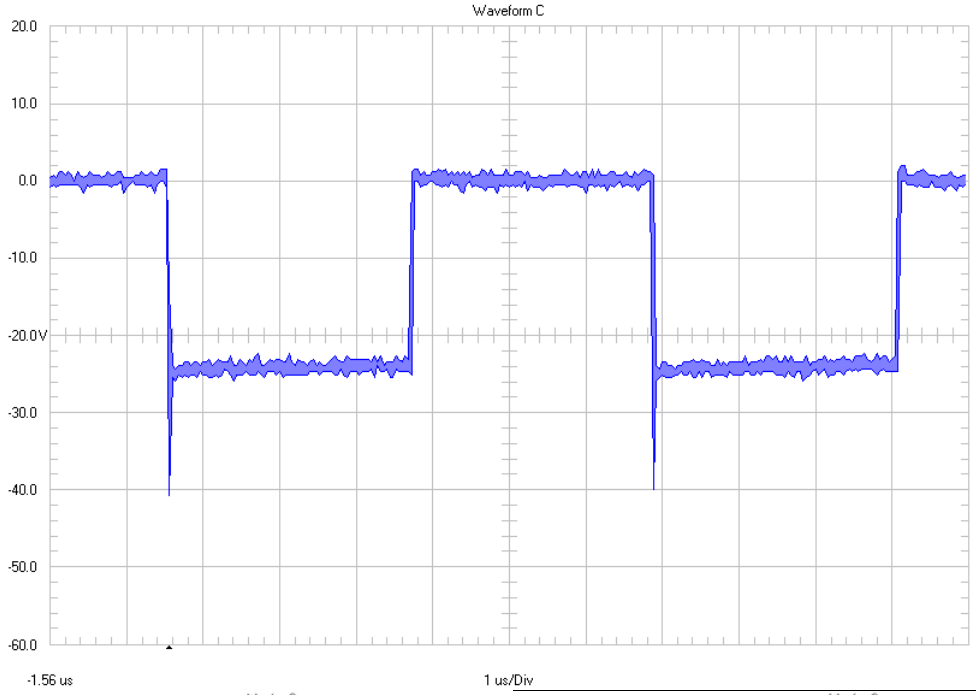


Figure 22

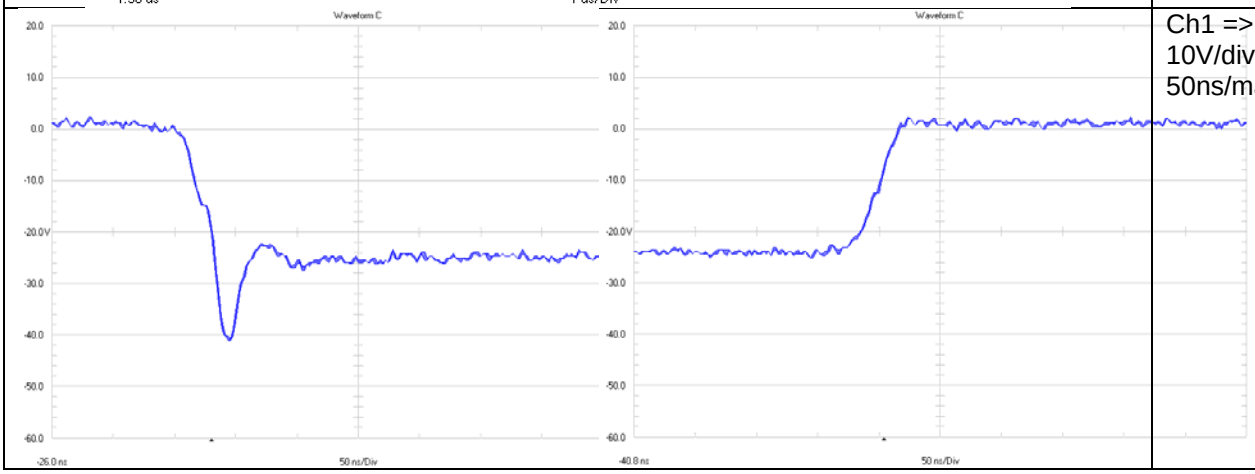
The waveform of the voltage on the switchnode is shown in Figure 23. Input voltage was set to 12V.



Ch1 =>
10V/div

1µs/div

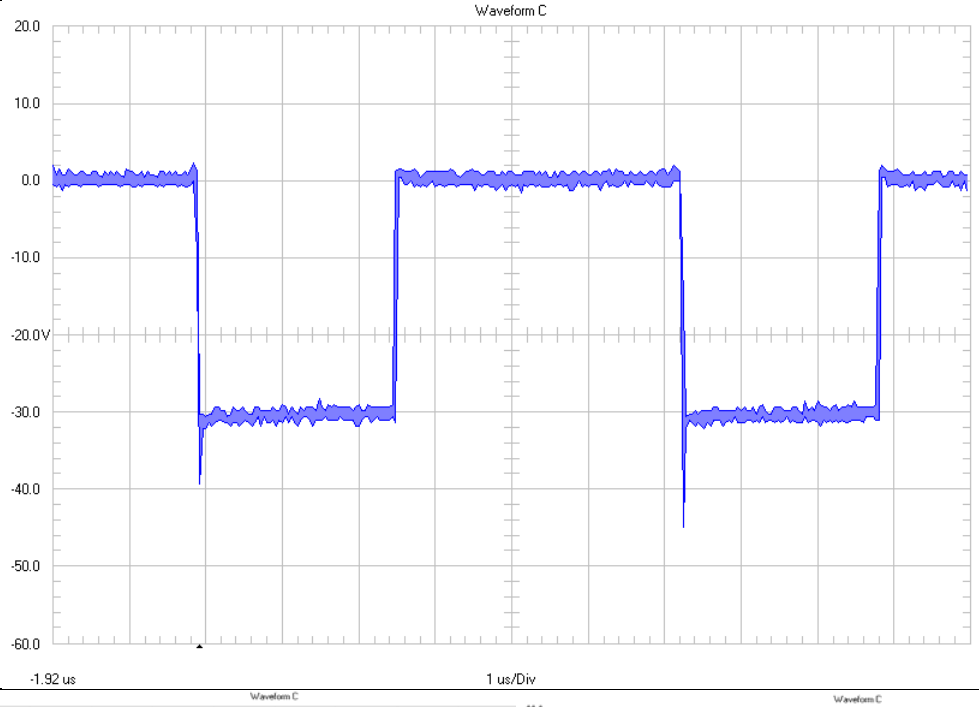
full bandwidth



Ch1 =>
10V/div
50ns/major div

Figure 23

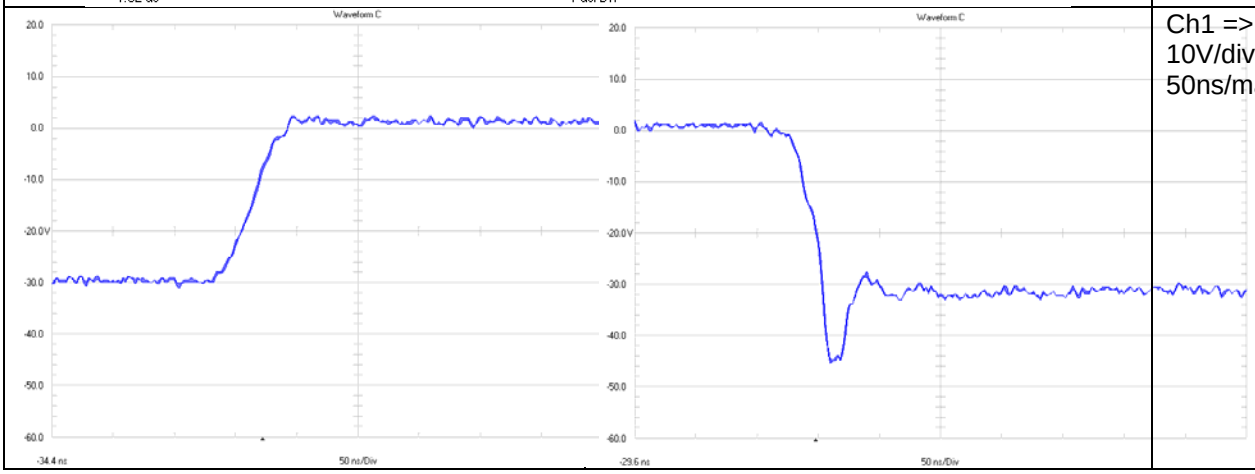
The waveform of the voltage on the switchnode is shown in Figure 24. Input voltage was set to 18V.



Ch1 =>
10V/div

1µs/div

full bandwidth

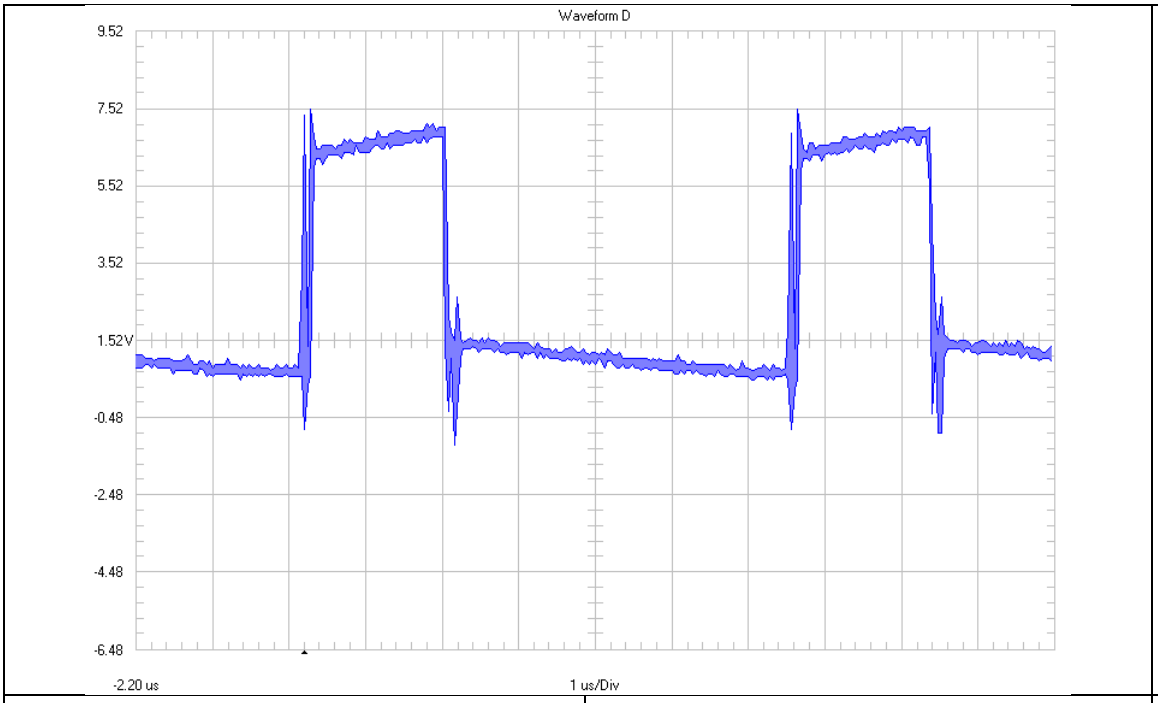


Ch1 =>
10V/div
50ns/major div

Figure 24

10.2 Q1 Gate – Source

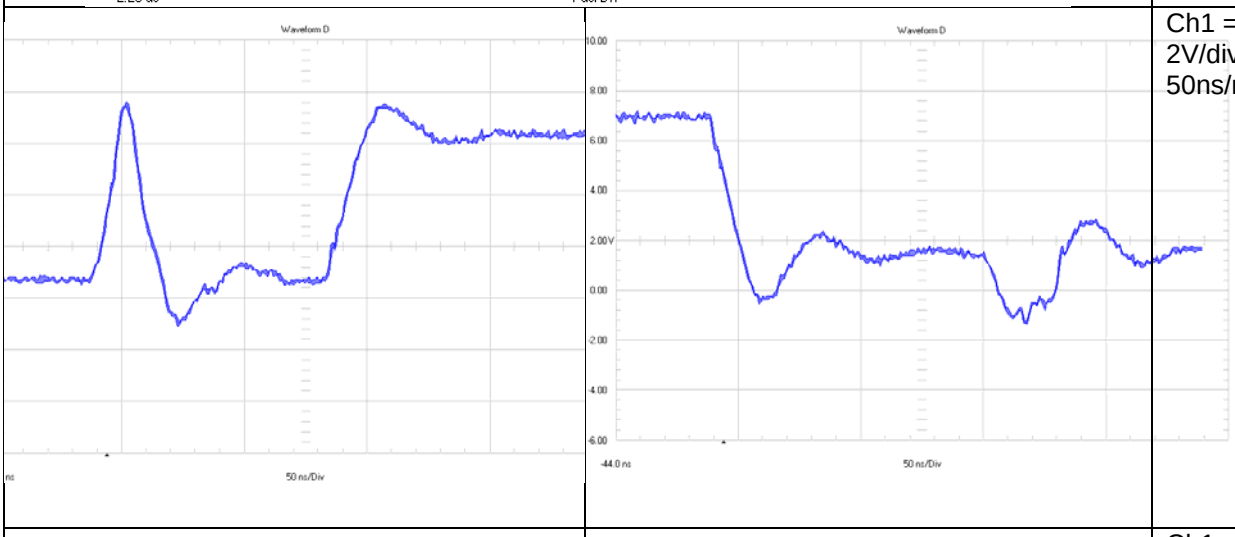
The waveform of the voltage on gate to source is shown in Figure 25. Input voltage was set to 6V.



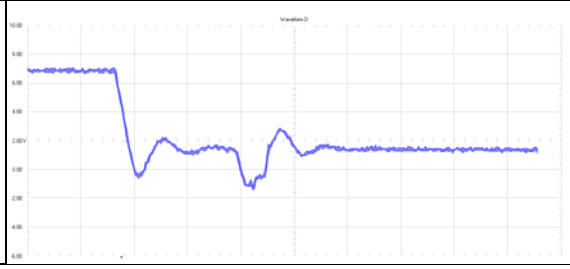
Ch1 =>
2V/div

1µs/div

full bandwidth



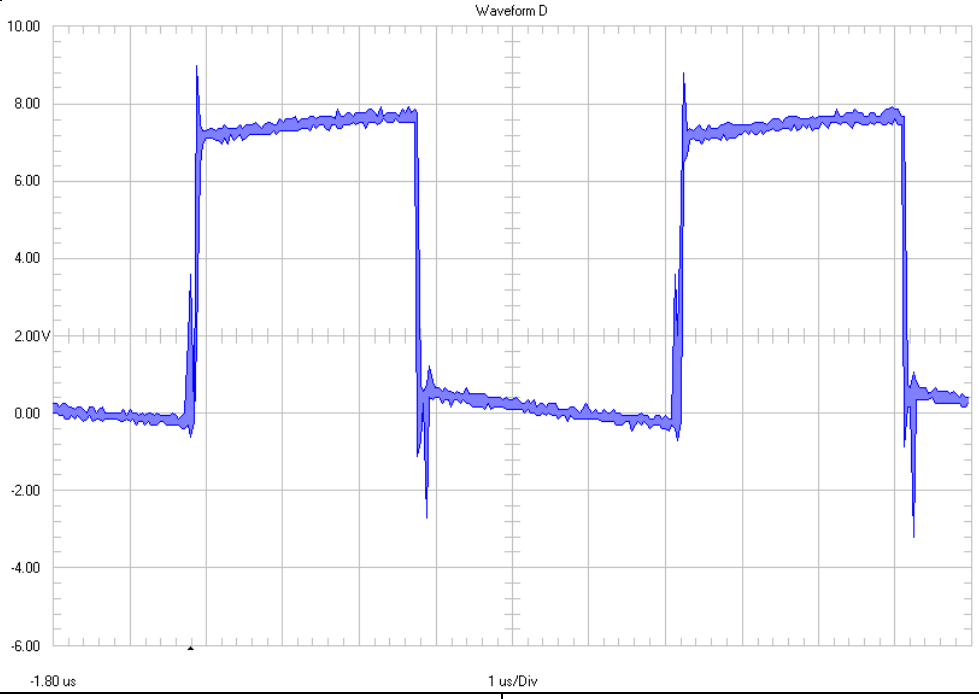
Ch1 =>
2V/div
50ns/major div



Ch1 =>
2V/div
50ns/**major** div

Figure 25

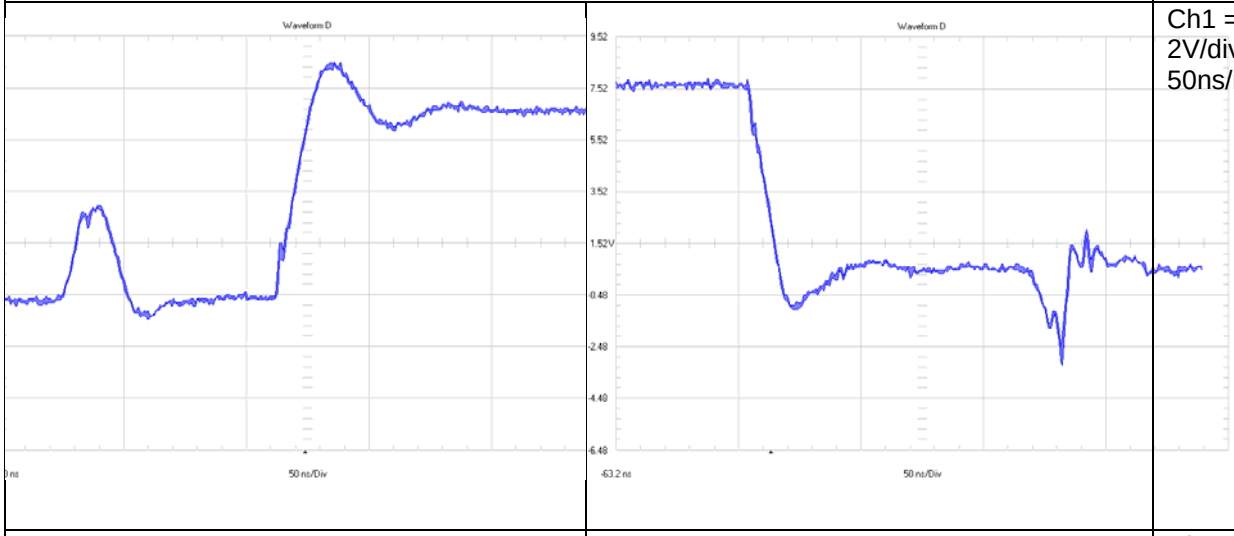
The waveform of the voltage on gate to source is shown in Figure 26. Input voltage was set to 12V.



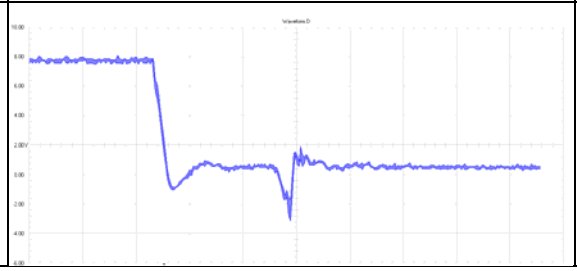
Ch1 =>
2V/div

1µs/div

full bandwidth



Ch1 =>
2V/div
50ns/major div



Ch1 =>
2V/div
50ns/major div

Figure 26

The waveform of the voltage on gate to source is shown in Figure 27. Input voltage was set to 18V.

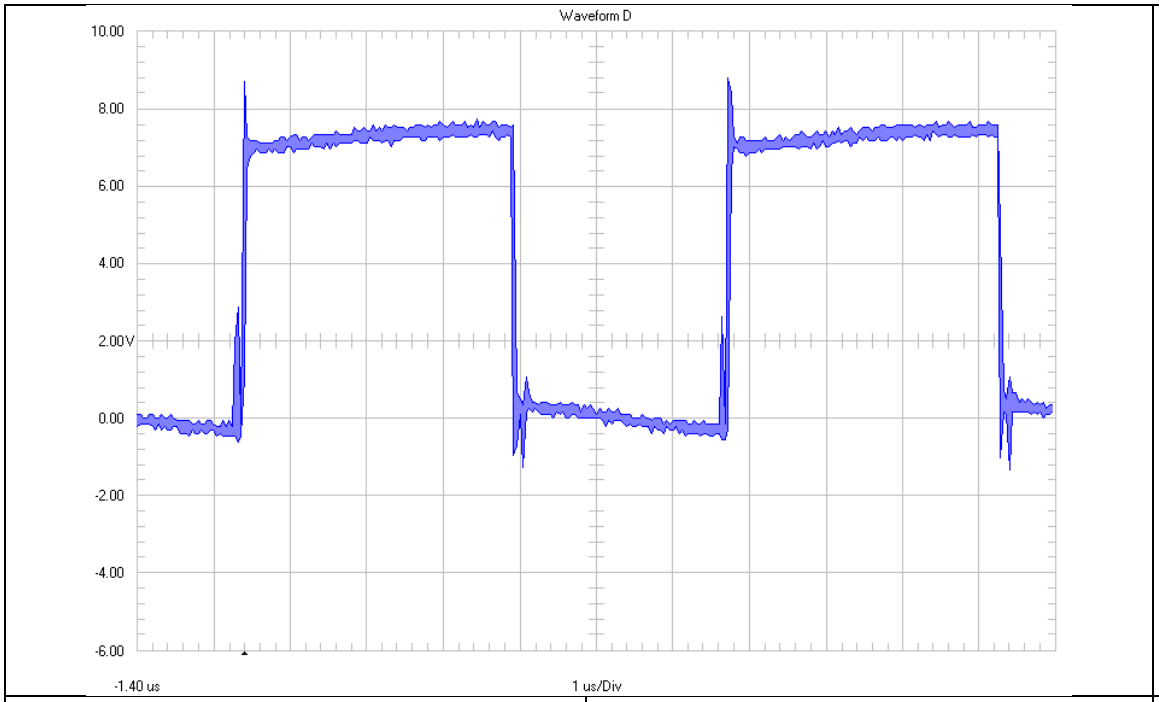
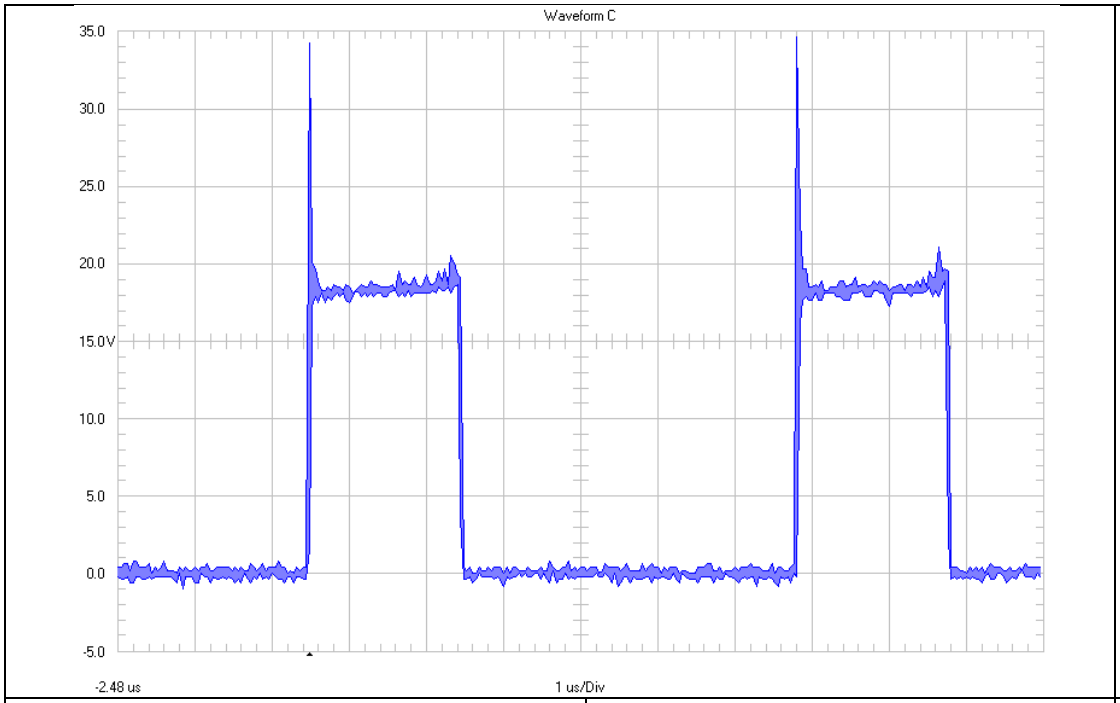


Figure 27

10.3 Q2 switchnode (drain-GND)

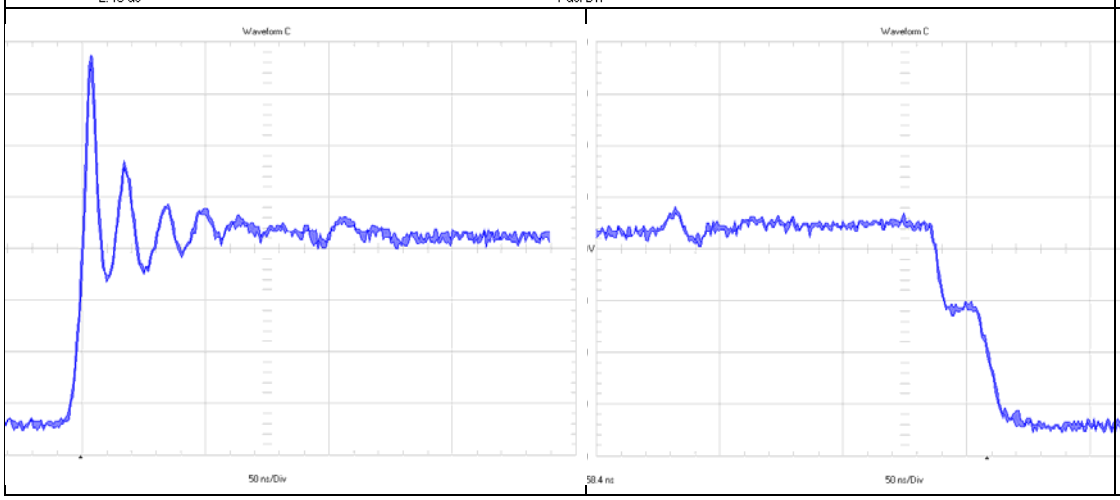
The waveform of the voltage is shown in Figure 28. Input voltage was set to 6V.



Ch1 =>
5V/div

1µs/div

full bandwidth



Ch1 =>
5V/div
50ns/major div

Figure 28

The waveform of the voltage is shown in Figure 29. Input voltage was set to 12V.

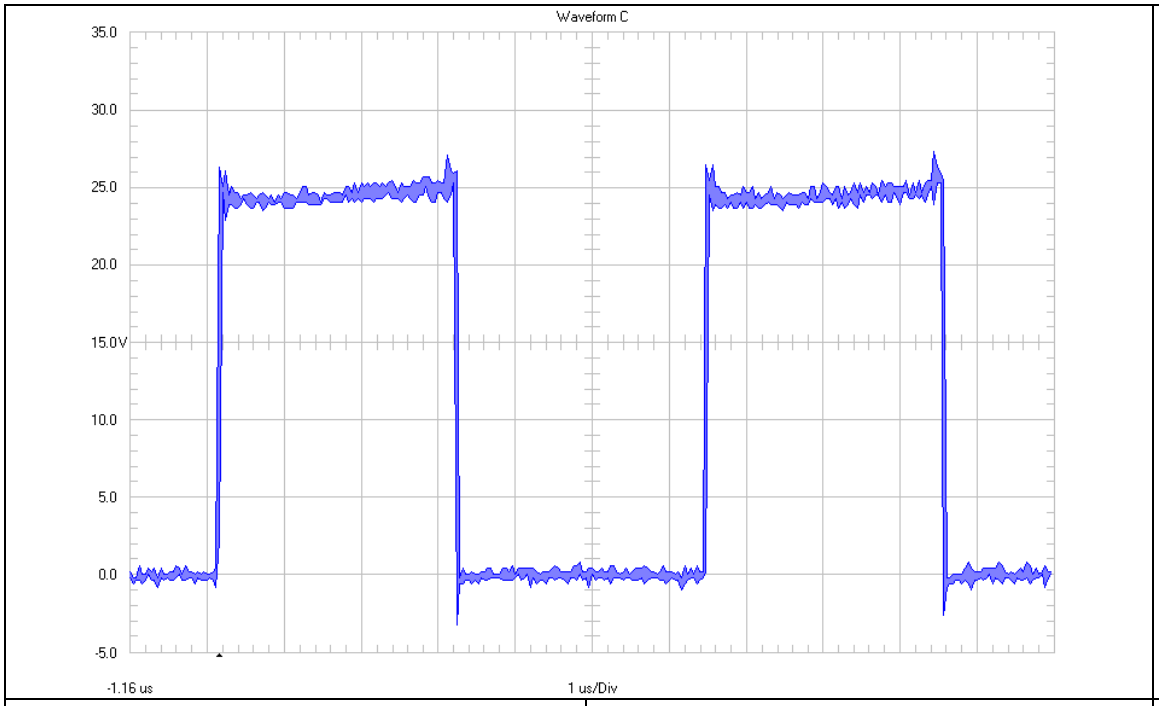


Figure 29

The waveform of the voltage is shown in Figure 30. Input voltage was set to 18V.

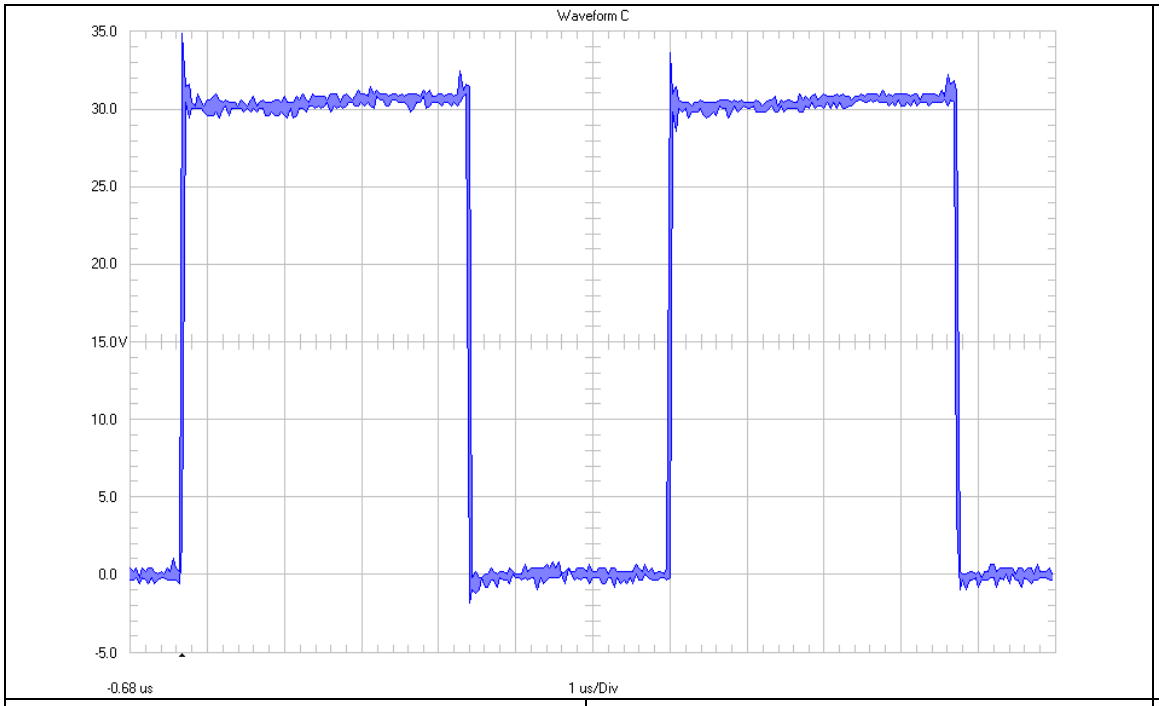
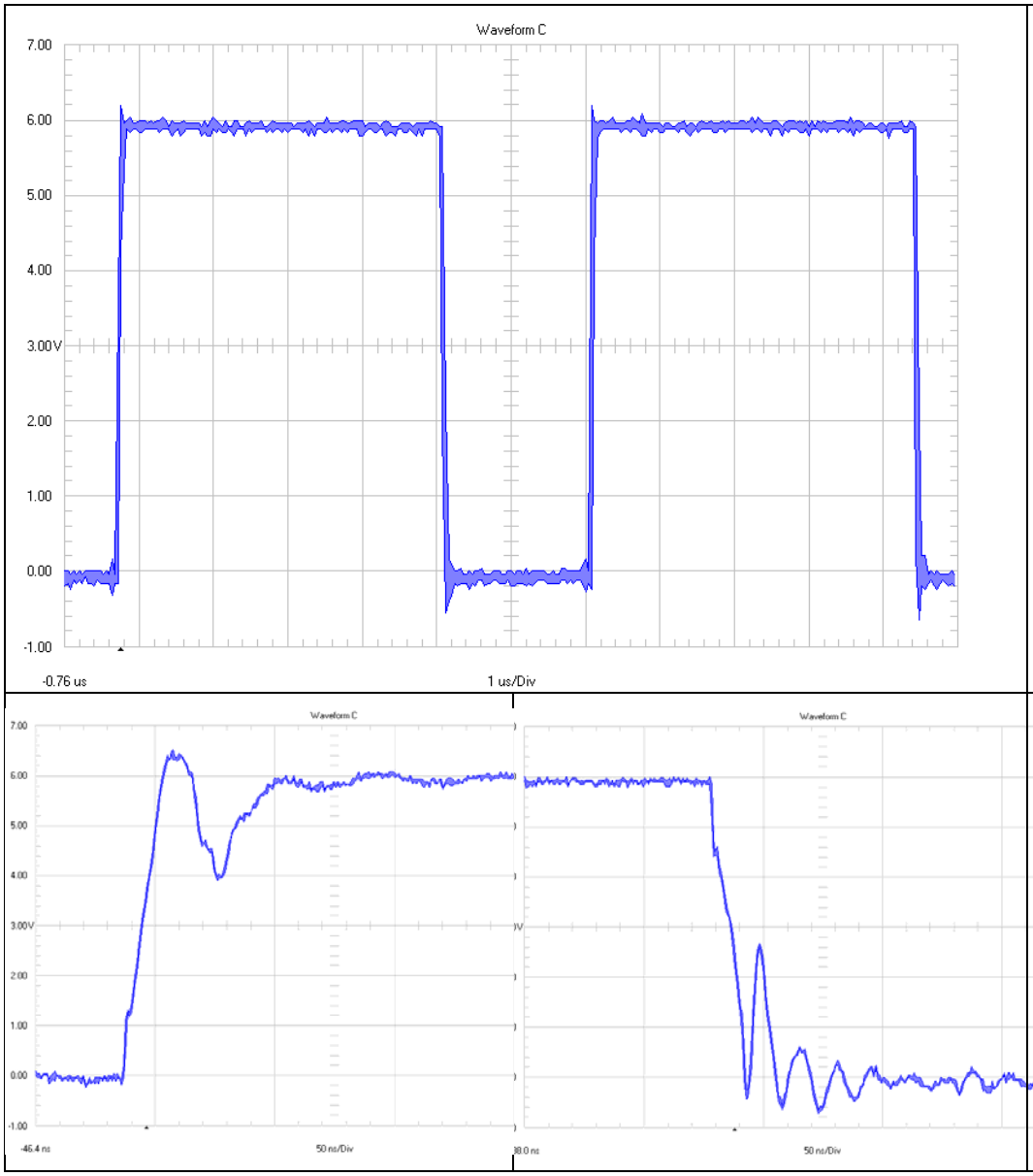


Figure 30

10.4 Q2 Gate-GND

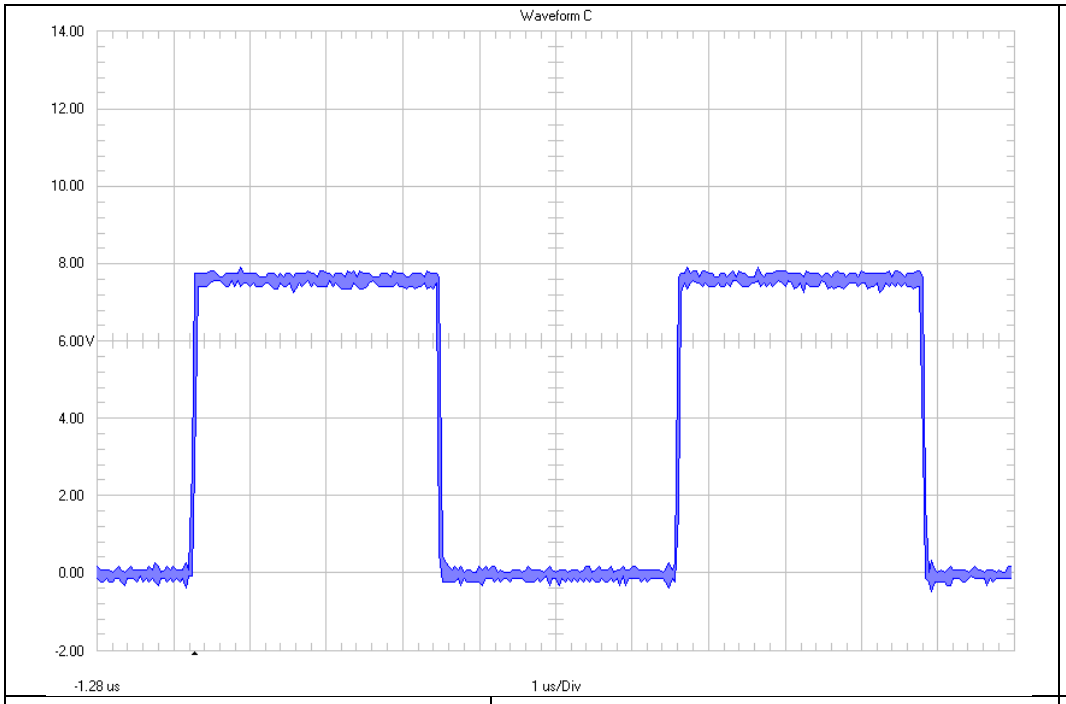
The waveform of the voltage is shown in Figure 31. Input voltage was set to 6V.



	Ch1 => **1V/div** 1µs/div full bandwidth
	Ch1 => 1V/div 50ns/major div

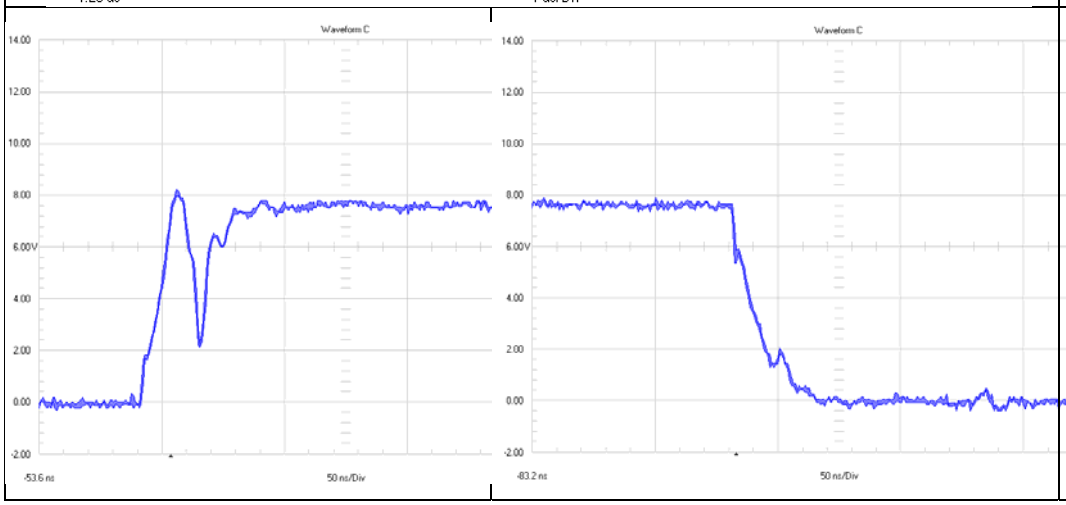
Figure 31

The waveform of the voltage is shown in Figure 32. Input voltage was set to 12V.



Ch1 =>
2V/div

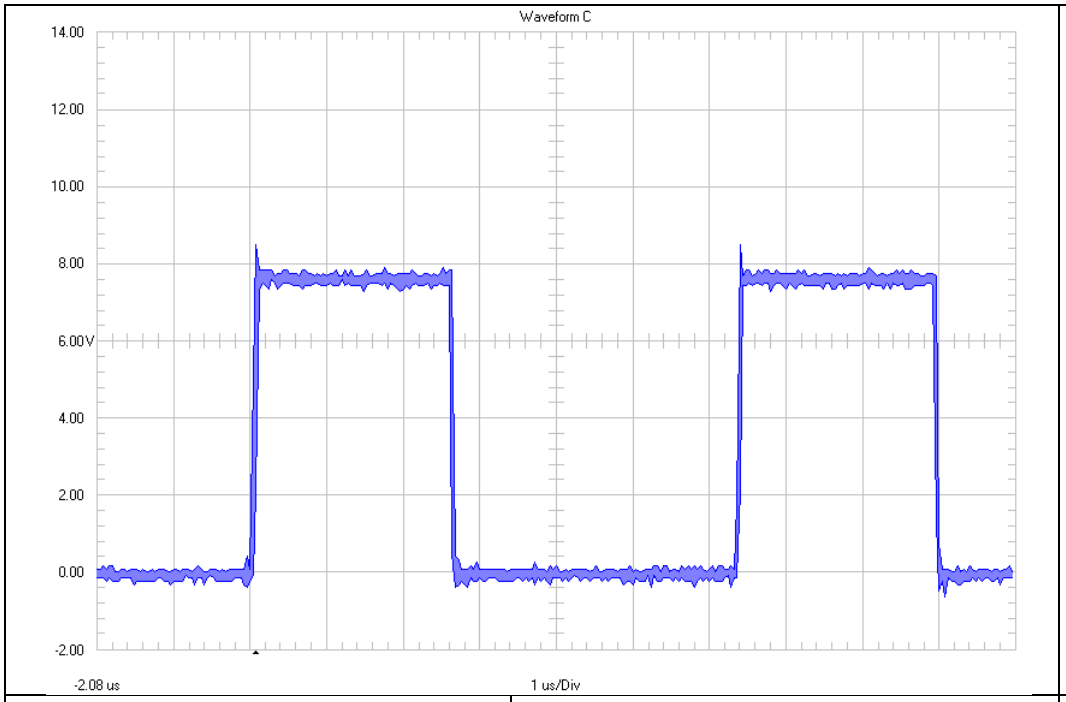
1µs/div
full bandwidth



Ch1 =>
2V/div
50ns/major div

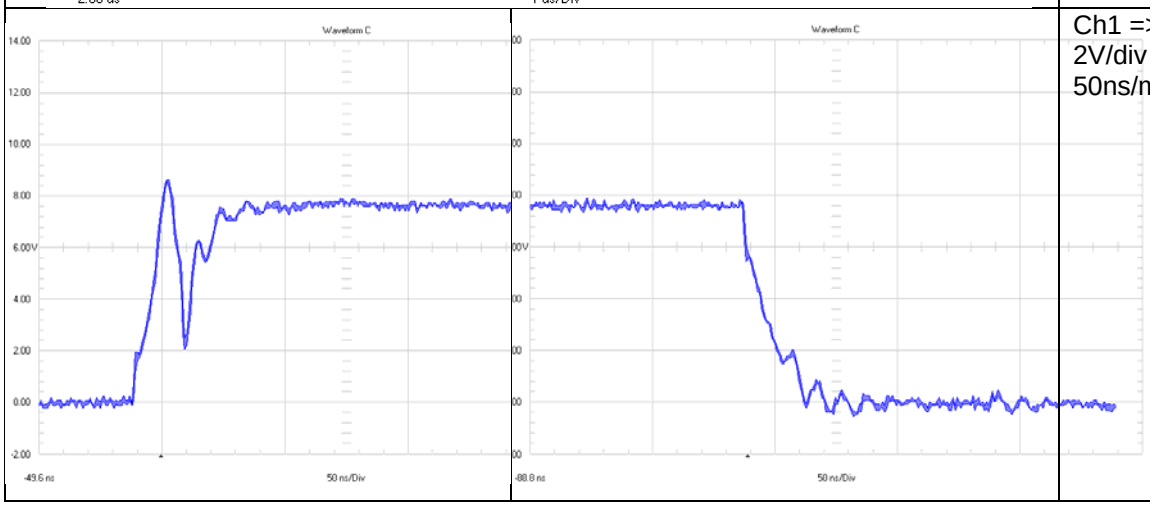
Figure 32

The waveform of the voltage is shown in Figure 33. Input voltage was set to 18V.



Ch1 =>
2V/div

1µs/div
full bandwidth



Ch1 =>
2V/div
50ns/major div

Figure 33

11 Thermal Image

Figure 34 shows the thermal image at 12V input voltage and 1A output current.

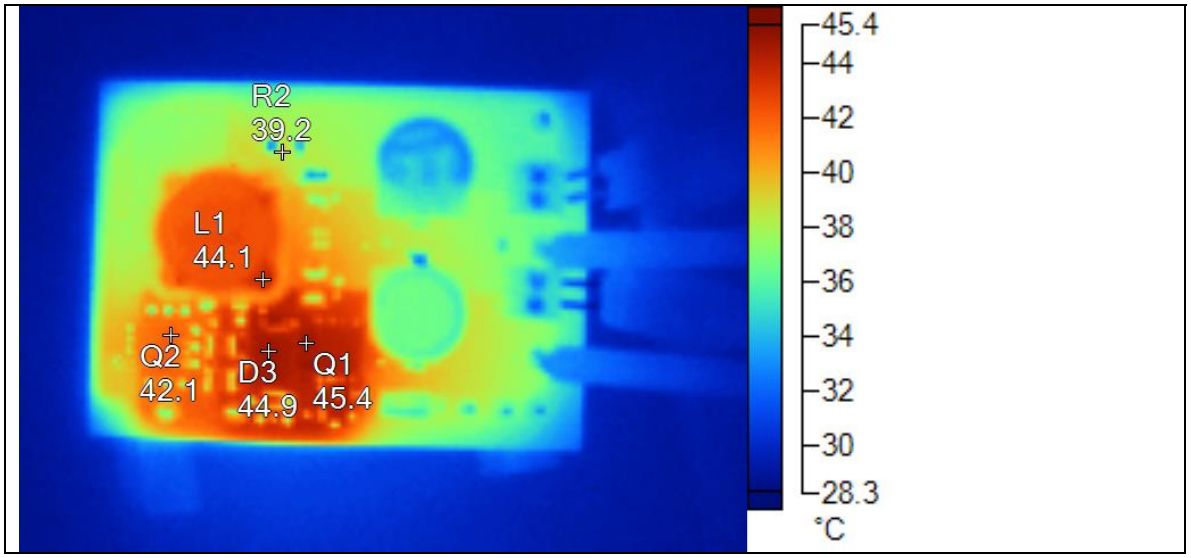


Figure 34

Name	Temperature
Q1	45.4°C
L1	44.1°C
D3	44.9°C
Q2	42.1°C
R2	39.2°C

Figure 35 shows the thermal image at 12V input voltage and 1.5A output current.

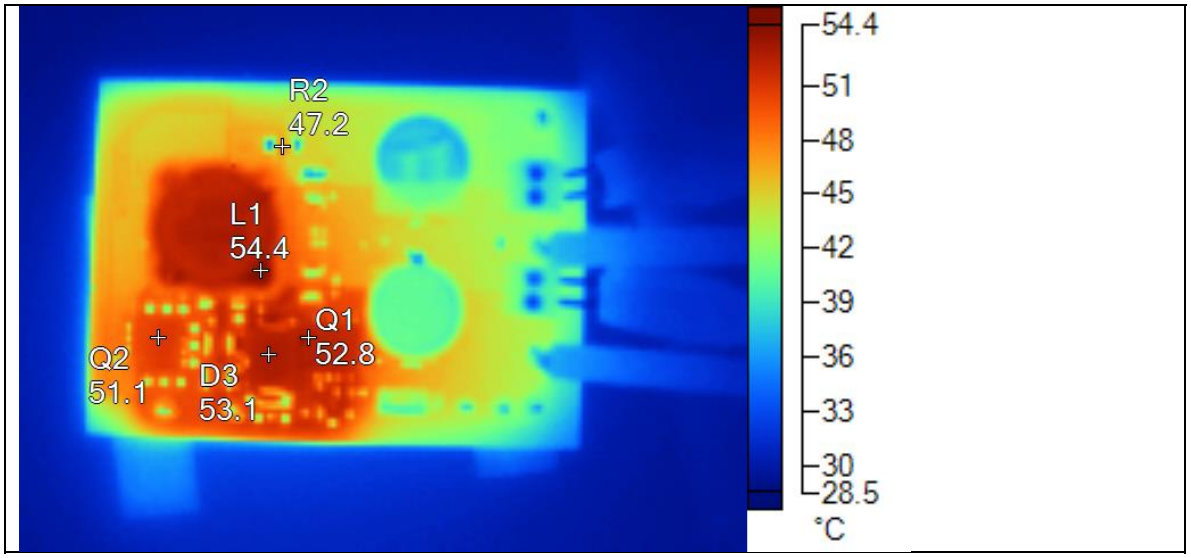


Figure 35

Name	Temperature
L1	54.4°C
Q1	52.8°C
D3	53.1°C
Q2	51.1°C
R2	47.2°C

Figure 36 shows the thermal image at 12V input voltage and 2A output current.

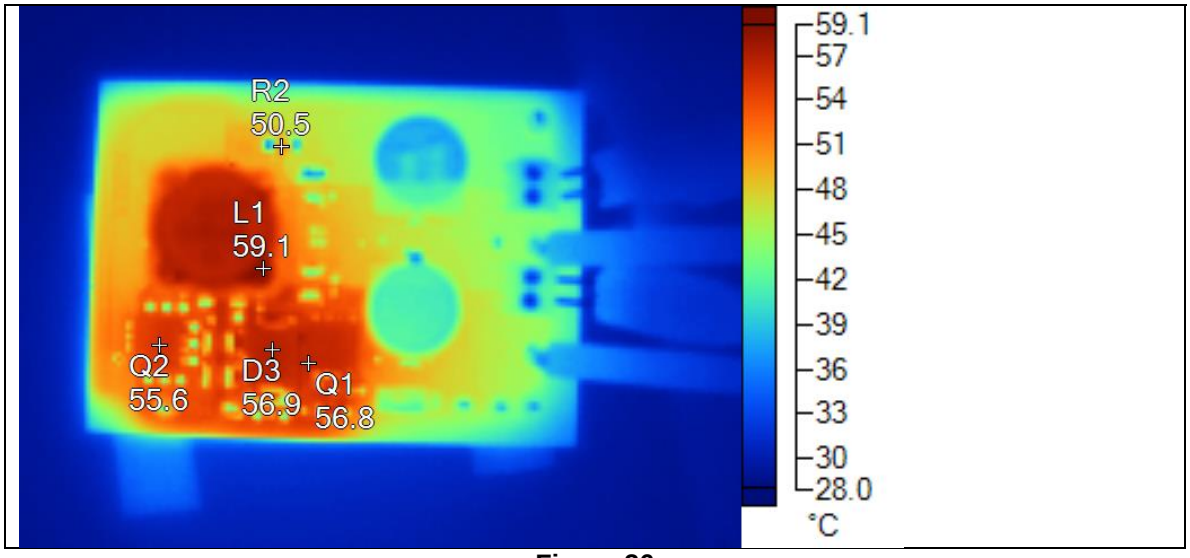


Figure 36

Name	Temperature
L1	59.1°C
Q1	56.8°C
D3	56.9°C
Q2	55.6°C
R2	50.5°C

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