TI Designs: TIDA-01583

Ultra-Low-Noise, Programmable Bias, and Power Supply Reference Design for Thermal Image Sensor

Description

This reference design demonstrates how to generate accurate and ultra-low noise, programmable bias voltages, and power supplies for thermal image sensors required for their operation. Such requirements cannot be directly met by switching power supplies, LDOs, or DAC outputs. This reference design is enabled by Texas Instruments' precision DAC, low-noise precision amplifier, and high PSRR, low-noise LDO.

Resources

TIDA-01583	Design Folder
TINA-TI™	SPICE Simulator
DAC80508	Product Folder
OPA2192	Product Folder
TPS71750	Product Folder
TPS71733	Product Folder

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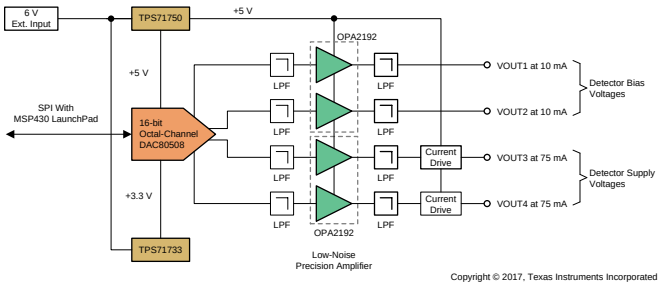
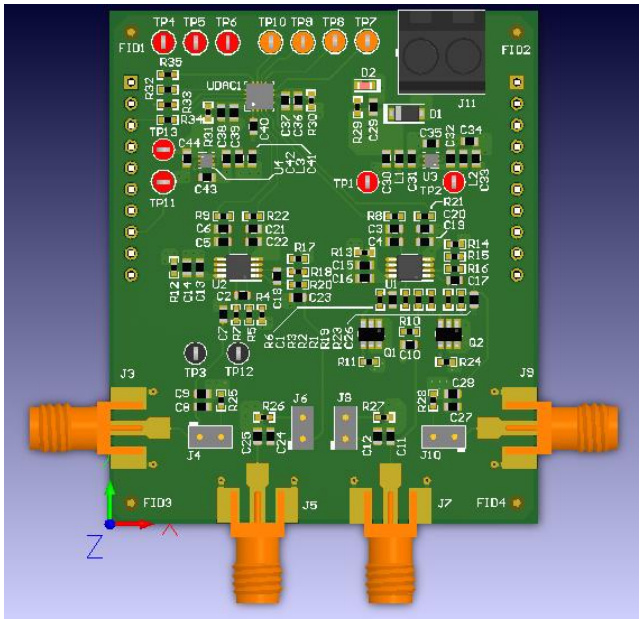
Features

- Total Integrated Noise < 4 μV_{RMS} From 0.1 Hz to 1 MHz
- Voltage Accuracy Better than ±10mV
- True 16-Bit DAC With Buffered Rail-to-Rail Voltage Output
- Programmable Voltage Outputs Allow On-The-Fly Compensation and Cater to Different Sensor Requirements
- Voltage Ranges: 0 V to 5 V
- Output Current Capability:
  - For Bias Voltage Circuit ≤ 10 mA (Without BJT)
  - For Power Supply Circuit ≤ 75 mA (With External BJT)

Applications

- Security and Surveillance: Thermal Imaging IP Camera
- Medical Imaging
- Test and Measurement
- Automotive Night Vision





1 System Description

Thermal imaging cameras are primarily designed and developed for military applications. In the past, most efforts were spent on cooled Infrared (IR) detector technology where the main focus was on improving the performance with less attention on cost-down to target civilian applications. Due to technology advancements and improved manufacturing processes, the emergence of uncooled microbolometer focal plane array (FPA) detectors has found its way into both military and high-volume commercial applications because of their small size, light weight, less power consumption, and affordable price while still delivering adequate image performance.

Today, uncooled microbolometer detectors are available in many different resolutions from sub-QQVGA to XGA. Any object in the universe at a temperature other than absolute zero emits the infrared radiation in long-wave Infrared (LWIR) band, even icebergs emit Infrared radiation. Thermal imaging cameras use radiation energy in the LWIR band (7.5-µm to 14-µm wavelength) to produce a clear monochrome image in different challenging environments like complete darkness, fog, smoke, light rain, and snow. Uncooled microbolometer detectors require bias voltages that are accurate with ultra-low noise to operate. Such requirements cannot be simply met by switching power supplies, low-dropout regulators (LDOs), or digital-to-analog converter (DAC) outputs. This demand careful design while maintaining high thermal sensitivity and lower noise to capture finest image details and temperature difference information.

Enabled by Texas Instruments' precision DAC, low-noise precision amplifier, and high-PSRR, low-noise LDO, this reference design demonstrates how to generate accurate and programmable bias voltages and power supplies with ultra-low noise for uncooled microbolometer detectors at a low cost. This design guide addresses component selection, design theory, and test results of the reference design system. The scope of this design guide gives system designers a head start in integrating TI's precision amplifier, precision DAC, and power management devices into their end-equipment systems. This reference design provides a complete set of downloadable documents such as a comprehensive design guide, schematic, Altium PCB layout files, bill of materials (BOM), test results, and Gerber files that help system designers in the design and development of their end-equipment systems. The following subsections describe the various blocks within the reference design system and what characteristics are most critical to best implement the corresponding function.

1.1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION
DAC resolution	True 16-bit DAC80508 in 16-pin QFN package (3 mm × 3 mm)
Number of outputs	Four outputs; DAC80508 is an octal channel DAC. Populate the remaining, if more channels are needed.
Voltage output range	0 V to 5 V, The design can be easily modified to support higher voltage outputs as the OPAx192 supports up to 36-V supply.
Output current	For Bias Voltage Circuit: ≤10 mA; For Power Supply Circuit: ≤ 75 mA
Integration bandwidth	0.1 Hz to 1 MHz
Integrated noise	Less than 4 μV_{RMS}
Accuracy	±10 mV

2 System Overview

2.1 Block Diagram

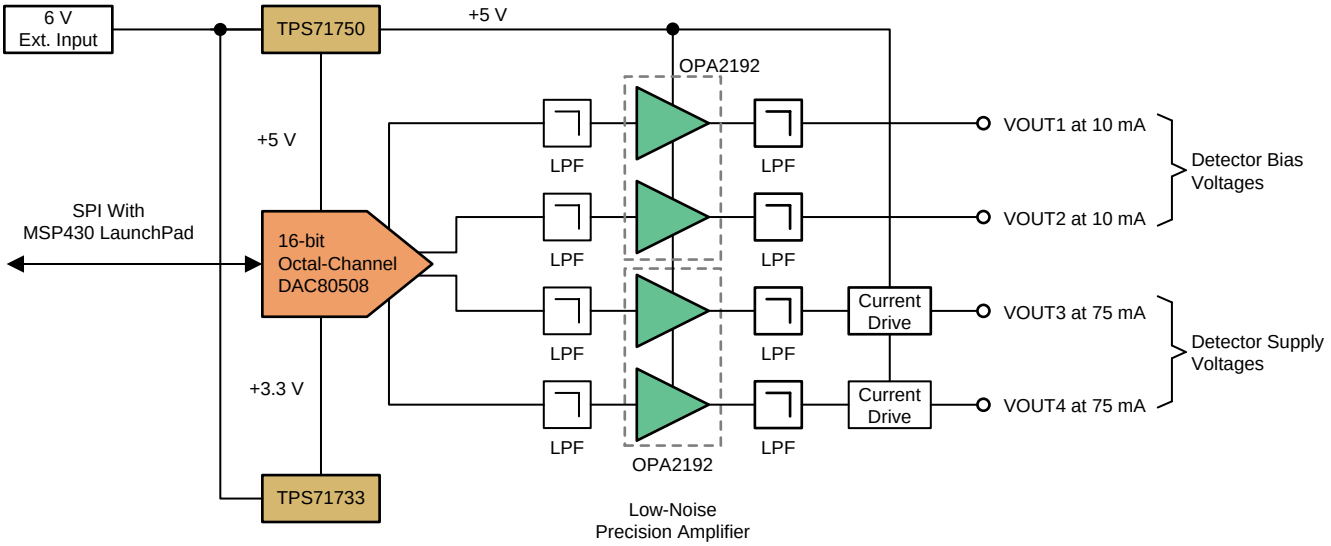


Figure 1. Block Diagram of TIDA-01583

2.2 Highlighted Products

This reference design features the following devices:

- DAC80508: 8-Channel, True 16-Bit, SPI, Voltage-Output DAC with Precision Internal Reference
- OPA2192: 36-V, Precision, RRIO, Low Offset Voltage, Low Input Bias Current Op Amp With e-trim™
- TPS71750 and TPS71733: 150-mA, High PSRR, Low Quiescent Current, Low Noise LDO

For more information on each of these devices, see their respective product folders at TI.com.

2.2.1 DAC80508

The DAC80508 device is a low-power, octal-channel, buffered voltage-output, DAC with a 16-bit resolution. This device includes a 2.5-V, 5-ppm/°C internal reference, eliminating the need for an external precision reference in most applications. A user-selectable gain configuration provides full-scale output voltages of 1.25 V (gain = ½), 2.5 V (gain = 1), or 5 V (gain = 2). This device operates from a single 2.7-V to 5.5-V supply, is specified monotonic, and provides high linearity of ±1 LSB INL.

Communication to the DAC80508 is performed through a four-wire serial interface that operates at clock rates of up to 50 MHz. The VIO pin enables serial interface operation from 1.7 V to 5.5 V. The flexible interface of the DAC80508 enables operation with a wide range of industry-standard microprocessors and microcontrollers.

The DAC80508 incorporates a power-on-reset circuit that powers up and maintains the DAC outputs at either zero scale or midscale until a valid code is written to the device. This device consumes low current of 0.7 mA/channel at 5.5 V, making it suitable for battery-operated equipment. A per-channel power-down feature reduces the device current consumption to 15 µA.

The features of the DAC80508 device are as follows:

- Performance:
  - INL: ±1 LSB maximum at 16-bit resolution
  - TUE: ±0.1% of FSR maximum
- Integrated 2.5-V precision internal reference:
  - Initial accuracy: 5 mV, maximum

  - Low drift: 5 ppm/°C, typical
- High drive capability: 20 mA with 0.5 V from supply rails
- Flexible output configuration:
  - User selectable gain: 2, 1 or ½
  - Reset to zero scale or midscale
- Wide operating range:
  - Power supply: 2.7 V to 5.5 V
  - Temperature: –40˚C to +125˚C
- 50-MHz, SPI-compatible serial interface:
  - 4-wire mode, 1.7-V to 5.5-V operation
  - Daisy-chain operation
  - CRC error check
- Low power: 0.7 mA/channel at 5.5 V
- Small package: 3-mm × 3-mm, 16-pin WQFN

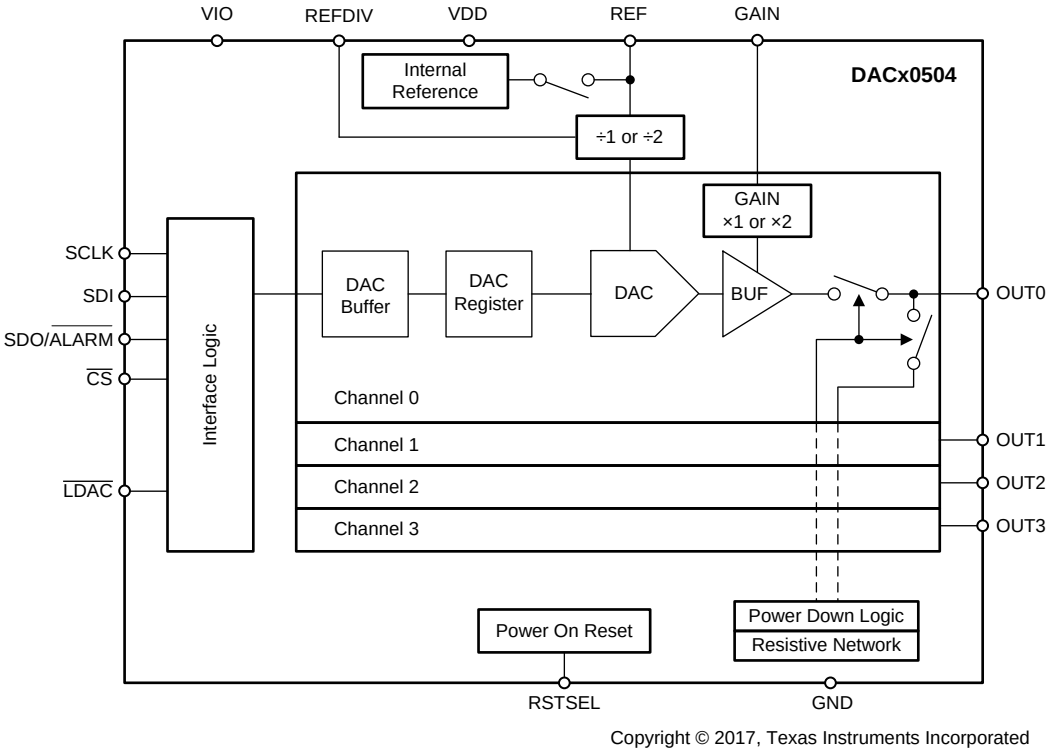


Figure 2. Simplified Block Diagram of DAC80508

2.2.2 OPA2192

The OPA2192 device is part of a new generation of 36-V, e-trim operational amplifiers (op amps). These devices offer outstanding DC precision and AC performance, including rail-to-rail input/output, low offset (±5 µV, typ), low offset drift (±0.2 µV/°C, typ), and 10-MHz bandwidth.

Unique features such as differential input-voltage range to the supply rail, high output current (±65 mA) high capacitive load drive of up to 1 nF, and high slew rate (20 V/µs) make the OPA2192 a robust, high-performance op amp for high-voltage industrial applications. The OPA2192 op amp is available in standard packages and is specified from –40°C to +125°C.

The features of the OPA2192 device are as follows:

- Low offset voltage: ±5 µV
- Low offset voltage drift: ±0.2 µV/°C
- Low noise: 5.5 nV/√Hz at 1 kHz
- High common-mode rejection: 140 dB
- Low bias current: ±5 pA
- Rail-to-rail input and output
- Wide bandwidth: 10-MHz GBW
- High slew rate: 20 V/µs
- Low quiescent current: 1 mA per amplifier
- Wide supply: ±2.25 V to ±18 V, 4.5 V to 36 V
- EMI and RFI filtered inputs
- Differential input voltage range to supply rail
- High capacitive load drive capability: 1 nF
- Industry standard packages:
  - Single in SOIC-8, SOT-23-5, and VSSOP-8
  - Dual in SOIC-8 and VSSOP-8
  - Quad in SOIC-14 and TSSOP-14

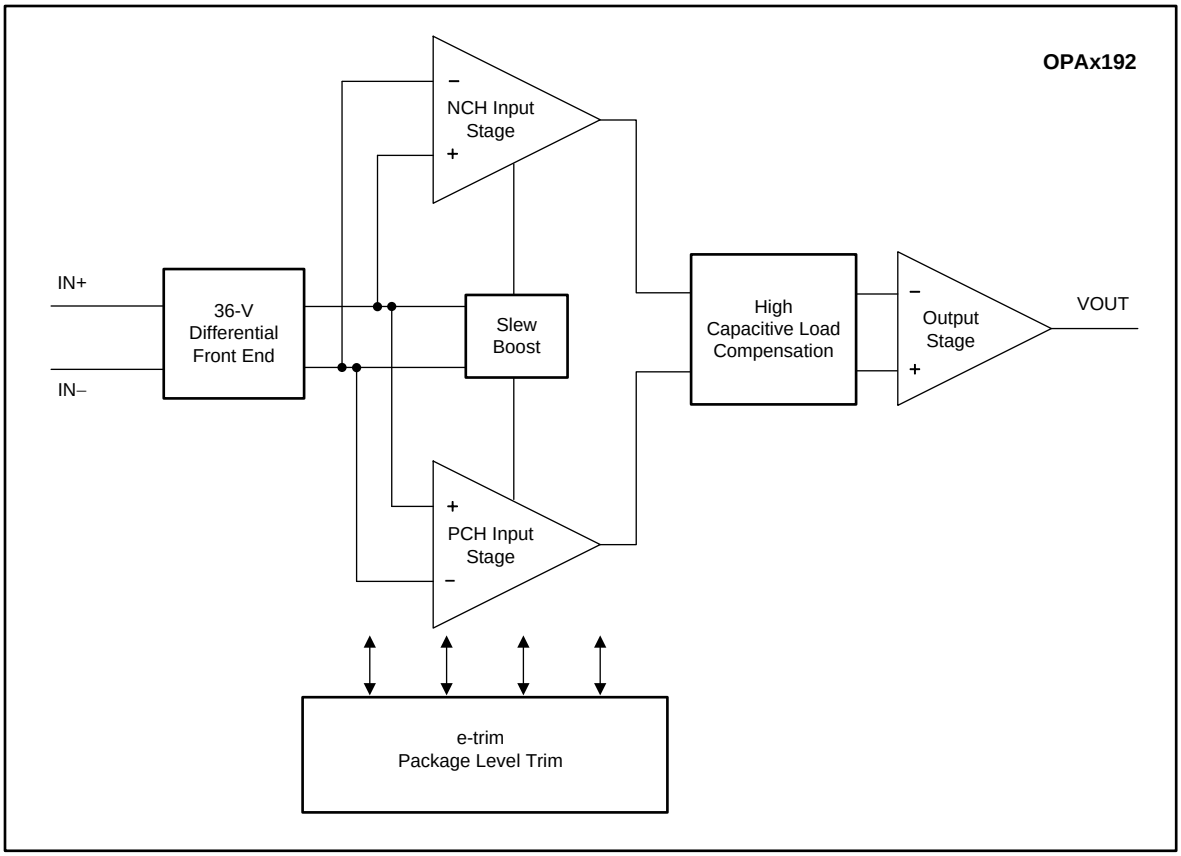


Figure 3. Functional Block Diagram of OPA2182

2.2.3 TPS717xx Series LDO: TPS71750 and TPS71733

The TPS717 family of LDO, low-power linear regulators offers very high power-supply rejection (PSRR) while maintaining very low 45-μA ground current in an ultra-small, five-pin SOT package. The family uses an advanced BiCMOS process and a PMOS pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The TPS717 is stable with a 1-μF ceramic output capacitor and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations. The device family is fully specified from T_J = –40°C to +125°C and is offered in a small SOT (SC70-5) package, a 2-mm × 2-mm WSON-6 package with a thermal pad, and a 1.5-mm × 1.5-mm WSON-6 package, which are ideal for small form factor portable equipment (such as wireless handsets and PDAs).

The features of OPA2192 are as follows:

- Input voltage: 2.5 V to 6.5 V
- Available in multiple output versions:
  - Fixed output with voltages from 0.9 V to 5 V
  - Adjustable output voltage from 0.9 V to 6.2 V
- Ultra-high PSRR: 70 dB at 1 kHz, 67 dB at 100 kHz, and 45 dB at 1 MHz
- Excellent load and line transient response
- Very low dropout: 170 mV typical at 150 mA
- Low noise: 30 μV_{RMS} typical (100 Hz to 100 kHz)
- Small 5-pin SC-70, 2-mm × 2-mm WSON-6, and 1.5-mm × 1.5-mm WSON-6 packages

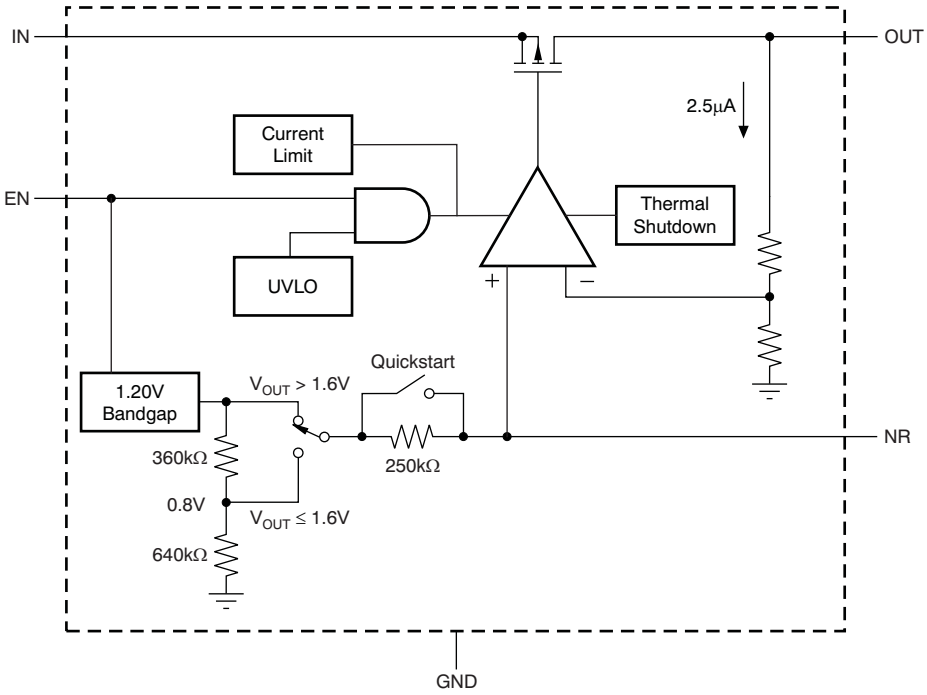


Figure 4. Functional Block Diagram of TPS717xx Fixed Output Voltage

2.3 System Design Theory

2.3.1 Theory of Operation

A bolometer is a temperature-sensitive electrical resistor that consists of an IR absorbing material, reflector, insulator, and CMOS read-out integrated circuit (ROIC). Absorption of incident IR radiation ultimately changes the resistance of bolometer elements. The information of this new resistance is electrically transferred to ROIC for further processing. Uncooled microbolometer detectors require a set of excitation voltages to produce an electrical output as shown in Figure 5. The change in resistance of the IR absorbing material causes the output voltage to change. These excitation voltages (bias voltages and power supplies) have very stringent accuracy and noise requirements to achieve high-quality image performance at the end.

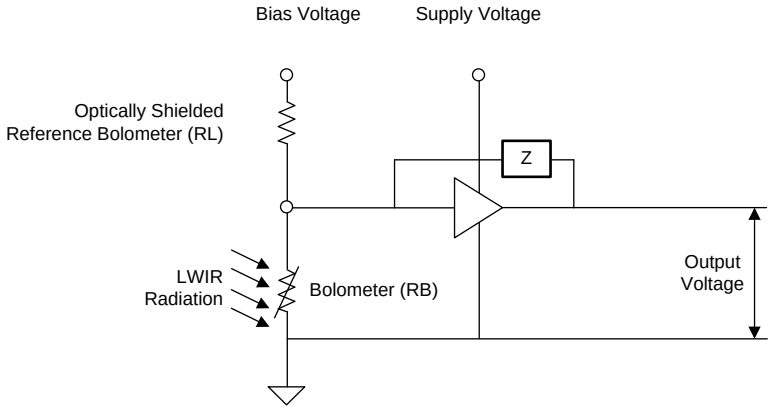


Figure 5. Simplified Diagram of Bolometer and Readout Circuit

Bias voltage and power supply circuits are generally placed near the respective pins of the detector and must be small in size. The bias voltages can be either fixed or tunable in nature depending upon focal plane array (FPA) temperature to adjust the dynamic range of analog video output. A bolometer demands very low current from bias voltage. A low biasing current also allows in achieving small self-heating. Whereas, detector power supplies are always fixed delivering few tens of mA current to the analog and digital blocks within the detector.

The architecture chosen to generate bias voltage and power supply for the detector is based on a true 16-bit buffered voltage output DAC combined with a low-noise amplifier and filters to achieve high accuracy and ultra-low noise performance. DAC output is adjusted through SPI with an MCU or FPGA to get the desired final voltage. The DAC output voltage is noisy and, therefore, heavily filtered by a simple first-order RC filter, rejecting any high-frequency noise. The filtered DAC voltage is then fed to the low noise buffer amplifier stage that isolates filter output from the load. The current driver only applies to the power supply circuit for the detector and consists of a bipolar transistor working in linear region, controlled by the output of the amplifier as shown on Figure 6.

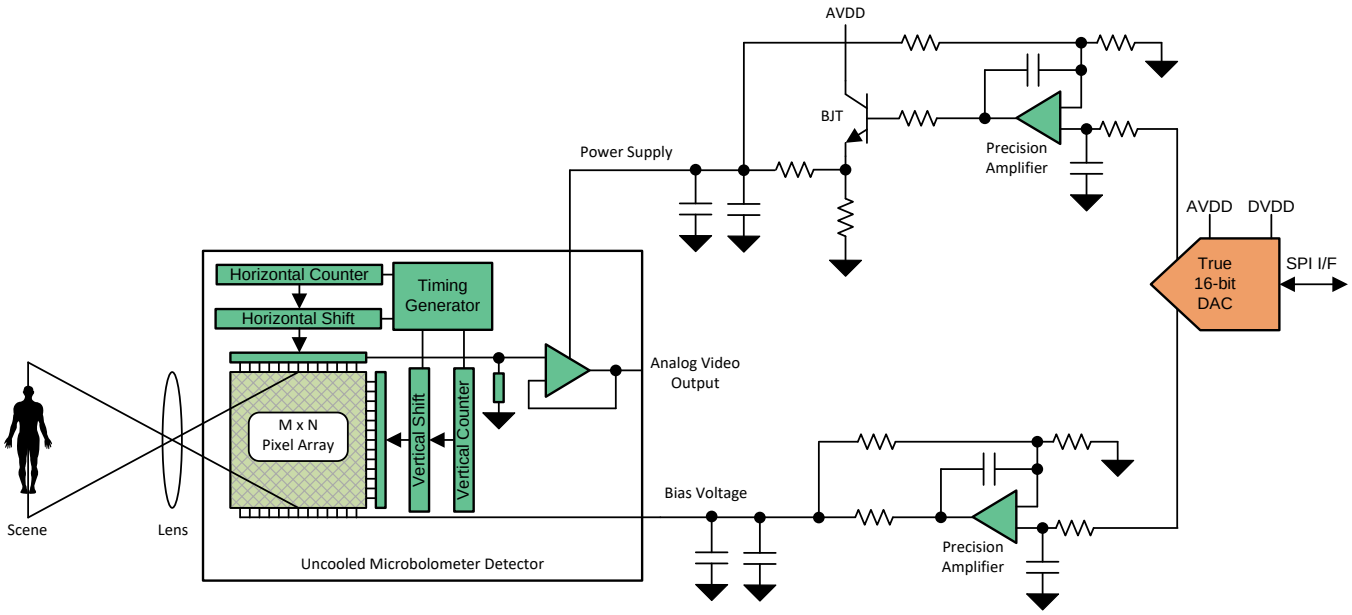


Figure 6. Bias Supply Generation Diagram

2.3.2 Component Selection

Before starting the circuit design and layout of the actual system, this reference design carefully examines all the captured system level requirements and features. Then, the design uses a top-down approach to translate these system level requirements into subsystem or component level requirements that helps in selecting the right set of devices. The following subsections describe some of the subsystem or component level requirements.

2.3.2.1 Selecting a DAC

From a system level standpoint, the DAC must satisfy the following requirements:

- Target resolution of 10 times lower than the overall voltage accuracy of 10 mV
- Quad or octal channels
- Buffered voltage output
- Internal reference
- Low output noise
- Rail-to-rail output
- Different analog (5.0 V nominal) and digital (3.3 V nominal) supply pins
- SPI
- Smaller package: Preferable 3-mm × 3-mm QFN

To see a list of eligible DACs from TI, go to TI Home → Data Converters → Digital-to-Analog Converters (DACs) → Precision DACs (=<10MSPS)

Refine the search by setting the filters according to the aforementioned requirements. Figure 7 shows the search results. The DAC80504/DAC80508 family is based on the R/2R core, the most suitable architecture to achieve lower noise than a string DAC and also has excellent INL and DNL performance. The DAC80504/DAC80508 family enables more integration, a lower cost, and higher performance for this application. The DAC80504 device is a quad-channel DAC whereas the DAC80508 is an octal-channel DAC.

Compare	Part Number	Resolution (Bits)	DAC Architecture	DAC Channels	Interface	INL (Max) (+/- LSB)	Output Range Min. (mA/V)	Output Range Max. (mA/V)	Settling Time (µs)	Output Type	Reference: Type	Rating	Operating Temperature Range (C)	Package Group	Package Size: mm2:W x L (PKG)	Approx. Price (US$)	Power Consumption (Typ) (mW)
	Filter by part number																
☐	DAC80504 - 4-Channel, True 16-Bit, SPI, Voltage-Output DAC With Precision Internal Reference - New	16	R-2R	4	SPI	1			4	Buffered Voltage	Int	Catalog	-40 to 125	WQFN	9 mm2: 3 x 3(WQFN)	10.34 | 1ku	15
☐	DAC80508 - 8-Channel, True 16-Bit, SPI, Voltage-Output DAC With Precision Internal Reference - New	16	R-2R	8	SPI	1			4	Buffered Voltage	Int	Catalog	-40 to 125	WQFN	9 mm2: 3 x 3(WQFN)	11.49 | 1ku	30

Figure 7. Selection of Precision DACs

To best demonstrate the performance of this reference design subsystem, the DAC80508 best satisfies these requirements. However, integrating the technology demonstrated in this reference design into an end-equipment system may necessitate a different DAC to suit the conditions of the actual system (see the Data Converters overview page).

2.3.2.2 Selecting a Precision Op Amp

From a system level standpoint, the precision op amp must satisfy the following requirements:

- Low offset voltage and offset drift for excellent DC performance
- Low input bias and offset currents (A large series resistor is used on the amplifier input to make a heavy filter. The voltage drop across the series filter resistor must be less than 0.5 LSB of the selected DAC. Amplifiers with a CMOS input stage generally have a low bias and offset currents than those with a bipolar input transistor.)
- Low noise
- Low I_Q (preferably less than 2.5 mA)
- High output current (> 20 mA)
- RRIO
- Wide single-supply operation for a detector that might require higher supply voltages
- High capacitive load driving capability
- Single- or dual-amplifier package options
- Smaller package (preferable 3-mm × 3-mm for a single amplifier)

To see a list of eligible precision op amps from TI, go to TI Home → Amplifiers → Operational Amplifiers (Op Amps) → Precision Op Amps (=<10MSPS)

Refine the search by setting the filter according the aforementioned requirements. Figure 8 shows the search results. The top results are OPA388, OPA192, OPA320, LMP7707, OPA197, and OPA322.

Compare	Part Number	Number of Channels (#)	Total Supply Voltage (Min) (+5V=5, +/-5V=10)	Total Supply Voltage (Max) (+5V=5, +/-5V=10)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/us)	Rail-to-Rail	Vos (Offset Voltage @ 25C) (Max) (mV)	Offset Drift (Typ) (uV/C)	Iq per channel (Typ) (mA)	Vn at 1kHz (Typ) (nV/rtHz)	CMRR (Typ) (dB)	Rating	Operating Temperature Range (C)	Package Group	Approx. Price (US$)	Package Size: mm2:W x L (PKG)	Input Bias Current (Max) (pA)	Output Current (Typ) (mA)	Architecture
☐	OPA388 - 10MHz, CMOS, Zero-Drift, Zero-Crossover, True RRIO Precision Operational Amplifier	1	2.5	5.5	10	5	In, Out	0.005	0.005	1.7	7	138	Catalog	-40 to 125	SOIC, SOT-23, VSSOP	0.98 | 1ku	29 mm2: 6 x 4.9(SOIC), 8 mm2: 2.8 x 2.9(SOT-23), 15 mm2: 4.9 x 3(VSSOP)	350	60	CMOS
☐	OPA192 - High-Voltage, Rail-to-Rail Input/Output, 5μV, 0.2μV/°C, Precision Operational Amplifier	1	4.5	36	10	20	In, Out	0.025	0.15	1	5.5	120	Catalog	-40 to 125	SOIC, SOT-23, VSSOP	1.15 | 1ku	29 mm2: 6 x 4.9(SOIC), 8 mm2: 2.8 x 2.9(SOT-23), 15 mm2: 4.9 x 3(VSSOP)	20	65	CMOS
☐	OPA192-Q1 - Automotive High-Voltage Rail-to-Rail Input/Output Precision Op Amp E-Trim™ Series	1	4.5	36	10	20	In, Out	0.025	0.15	1	5.5	120	Automotive	-40 to 125	VSSOP		15 mm2: 4.9 x 3(VSSOP)	20	65	CMOS
☐	OPA320 - Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier	1	1.8	5.5	20	10	In, Out	0.15	1.5	1.5	8.5	114	Catalog	-40 to 125	SOT-23, SOT-23	0.80 | 1ku	8 mm2: 2.8 x 2.9(SOT-23), 8 mm2: 2.8 x 2.9(SOT-23)	0.9	65	CMOS
☐	OPA320-Q1 - Automotive Qualified Precision, Zero-Crossover, 20MHz, 0.9pA Ib, RRIO, CMOS Operational Amplifier	1	1.8	5.5	120	10	In, Out	0.15	1.5	1.5	8.5	114	Automotive	-40 to 125	SOT-23	0.94 | 1ku	8 mm2: 2.8 x 2.9(SOT-23)	0.9	65	CMOS
☐	LMP7707 - Precision, CMOS Input, RRIO, Wide Supply Range Decompensated Amplifier	1	2.7	12	14	5.6	In, Out	0.2	1	0.715	9	130	Catalog	-40 to 125	SOIC, SOT-23	1.07 | 1ku	29 mm2: 6 x 4.9(SOIC), 8 mm2: 2.8 x 2.9(SOT-23)	1	66	CMOS
☐	OPA197 - 36-V, Precision, Rail-to-Rail Input Output, Low Offset Voltage Op Amp	1	4.5	36	10	20	In, Out	0.25	0.5	1	5.5	140	Catalog	-40 to 125	SOIC, SOT-23, VSSOP	0.60 | 1ku	29 mm2: 6 x 4.9(SOIC), 8 mm2: 2.8 x 2.9(SOT-23), 15 mm2: 4.9 x 3(VSSOP)	20	65	CMOS
☐	OPA322 - 20MHz Low-Noise 1.8V RRIO CMOS Operational Amplifier With Shutdown	1	1.8	5.5	20	10	In, Out	2	1.8	1.6	8.5	100	Catalog	-40 to 125	SOT-23, SOT-23	0.55 | 1ku	8 mm2: 2.8 x 2.9(SOT-23), 8 mm2: 2.8 x 2.9(SOT-23)	10	65	CMOS

Figure 8. Selection of Precision Amplifiers

To best demonstrate the performance of this reference design subsystem, the OPA2192 (a dual amplifier version of the OPA192 family) is selected mainly because it has a wide supply range and lowest noise among all in the list. The OPAx192 family of op amps also has the ability to drive a large capacitive load using a small isolation resistance.

Noise performance is a function of the amplifier design. The three common designs for low-noise amplifiers are bipolar, JFET input, and CMOS input. While each design can provide low-noise performance, their performances are not equal. Newer low-noise amplifier designs with a CMOS input stage offer voltage-noise performance that is comparable to bipolar designs. CMOS input amplifiers also meet or exceed the current-noise performance of the best JFET input designs. For example, the OPA2192 has low-input voltage-noise density (5.5 nV/√Hz), low-input current-noise density (1.5 fA/√Hz), and ultra-low distortion (0.00008% THD+N) while operating from a single supply. These features make CMOS input amplifiers an excellent choice for applications that require low noise performance. Additionally, the CMOS input stage allows for very low input-bias currents, low offset voltages, and very high input impedances, making these devices well suited for signal conditioning high-impedance sources such as an output buffer for a 16-bit DAC in this case.

Bipolar transistors inherently offer better matching, resulting in lower offset voltages for a given architecture. However, the OPAx192 family of op amps is based on CMOS architecture and manufactured using TI's e-trim technology. Each amplifier input offset voltage and input offset voltage drift is trimmed in production, thereby minimizing errors associated with input offset voltage and its drift. Op amps vary in susceptibility to EMI. If conducted EMI enters the op amp, the DC offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all pin functions in op amps can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx192 op amp family incorporates an internal input low-pass filter that reduces the amplifier response to EMI.

However, integrating the technology demonstrated in this reference design into an end-equipment system may necessitate a different precision op amp to suit the conditions of the actual system (see the Amplifiers overview page).

2.3.3 Stability Analysis

Some applications feature an external load that is heavily capacitive (for example, sample-and-hold amplifiers, reference buffers, MOSFET gate drivers, cable-shield drivers, and peak-detectors). However in this case, the circuit must be capable of driving capacitive load up to tens of µF; this mainly accounts for decoupling capacitors required by the bias or power supply pins of the detector. Driving a capacitive load is one of the troublesome and difficult problems to overcome because capacitive loads can easily cause stability problems in op amp circuits, resulting in large overshoots, ringing, and in some severe cases, sustained oscillations.

2.3.3.1 Stability Criterion

Figure 9 represents a traditional control model representing an op amp with feedback. Aol is the open loop gain of the op amp. Feedback factor (β) is the amount of output voltage from V_{OUT}, which gets fed back as feedback to the op amp input. The β network in this example is a resistor feedback network. Equation 1 shows that the closed loop gain (Acl) is directly defined by Aol and β.

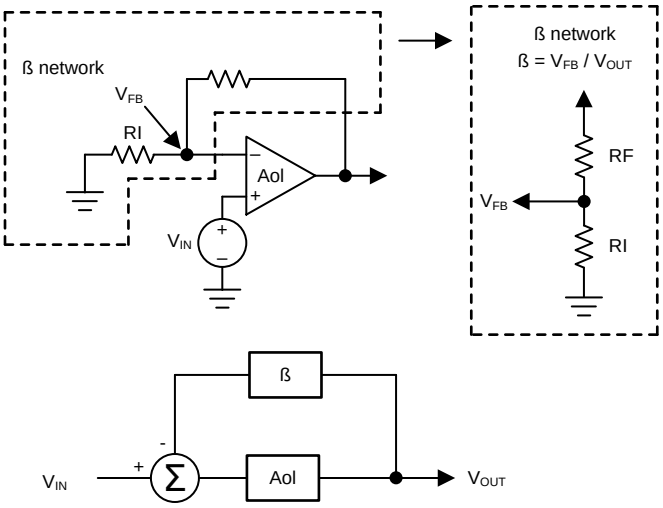


Figure 9. Model of Loop Gain for Op Amp

$$Acl = \frac{V_{OUT}}{V_{IN}} = \frac{Aol}{1 + (Aol \times \beta)} \quad (1)$$

If Loop Gain = Aol × β = –1, then

$$Acl = \frac{V_{OUT}}{V_{IN}} = \frac{Aol}{0} \rightarrow \infty \text{ (Unbounded gain)} \quad (2)$$

Any small changes in V_{IN} result in large changes in V_{OUT}, which feeds back to V_{IN} and result in even larger changes in V_{OUT}.

- The loop gain is unity in absolute magnitude (that is, |Aol × β| = 1)
- Phase shift around the loop is zero or integer multiple of 2π, that is, ∠(Aol × β) = 2πn, n = 0, 1, 2…..

The main cause of op amp's instability is too much delay in the feedback path as shown in Figure 10. This delay occur because the inherent output impedance (Ro) of the op amp interacts with a capacitive load (CL), forming an additional pole in the open-loop gain (Aol) response that reduces the loop-gain (Aol × β) phase margin below acceptable levels. In simple words, phase margin is nothing but a measure of "delay" in the loop. The perfectly damped response in Figure 10 occurs with no delay in the feedback signal reaching the inverting input. The op amp responds by ramping toward the final value, gently slowing down as the feedback signal detects closure on the proper output voltage.

Problems develop when the feedback signal is delayed. With delay in the loop, the amplifier does not immediately detect its progress toward the final value. The amplifier overreacts by racing too quickly toward the proper output voltage. Note the faster initial ramp rate with delayed feedback. The inverting input fails to receive timely feedback that it reached and passed the proper output voltage. It overshoots its mark and requires several successively smaller polarity corrections before finally settling. A little delay merely results in some overshoot and ringing. Too much delay and these polarity corrections continue indefinitely—an oscillator.

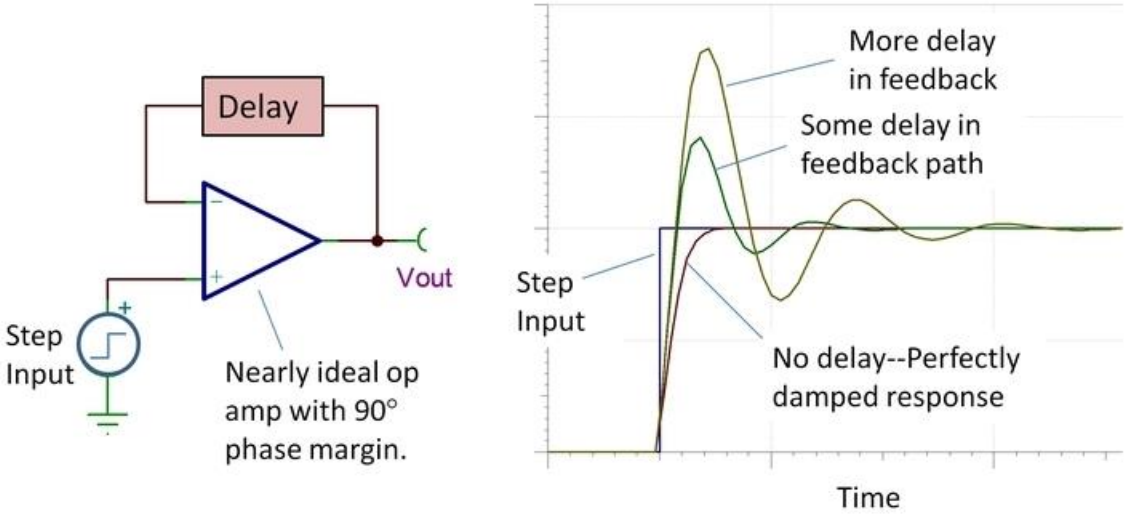


Figure 10. Effect of Delay in Feedback Loop on Stability of Op Amp

The source of delay is often a simple low-pass R-C network. Although the network is not a constant delay for all frequencies, the gradual phase shift of this network from 0° to 90° produces a first-order approximation of time delay, td = R-C. There are two commonly encountered situations where this R-C network unintentionally sneaks into these circuits. The first R-C network is formed between the open-loop output resistance and capacitive load (Figure 11a). The resistor is the open-loop output resistance of the op amp. The capacitor is the load capacitance. In the second case (Figure 11b), the feedback resistance and the input capacitance of the op amp form the R-C network. Circuit board connections also contribute to the capacitance at this sensitive circuit node. Note that the two circuits have identical feedback loops. The only difference is the node at which the output is taken. From a loop stability standpoint, these loops can create the same issues, and these two causes of delayed feedback often occur in combination.

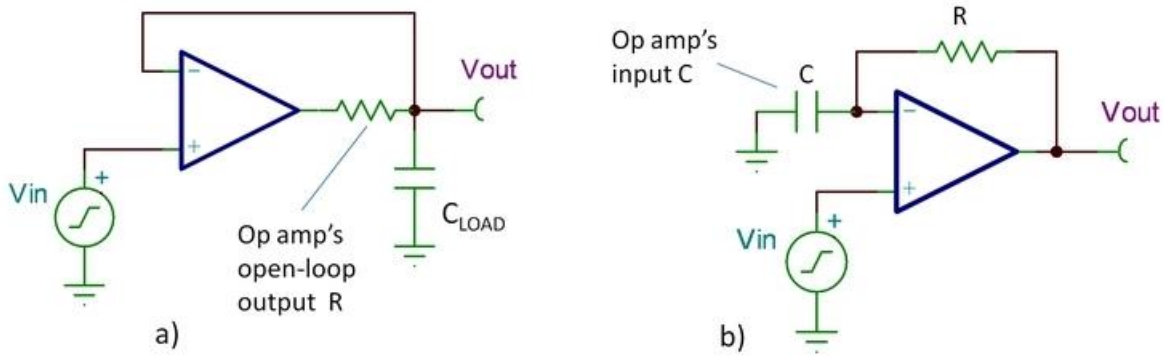


Figure 11. Sources of Delay in Feedback Path

Regarding the second case, a feedback resistor is not needed for the simple G = 1 buffer so the more common situation is in a gain configuration using a feedback resistor and resistor to ground (Figure 12). The parallel combination of these resistors (R1 and R2) forms the effective R = R1||R2 in the R-C circuit.

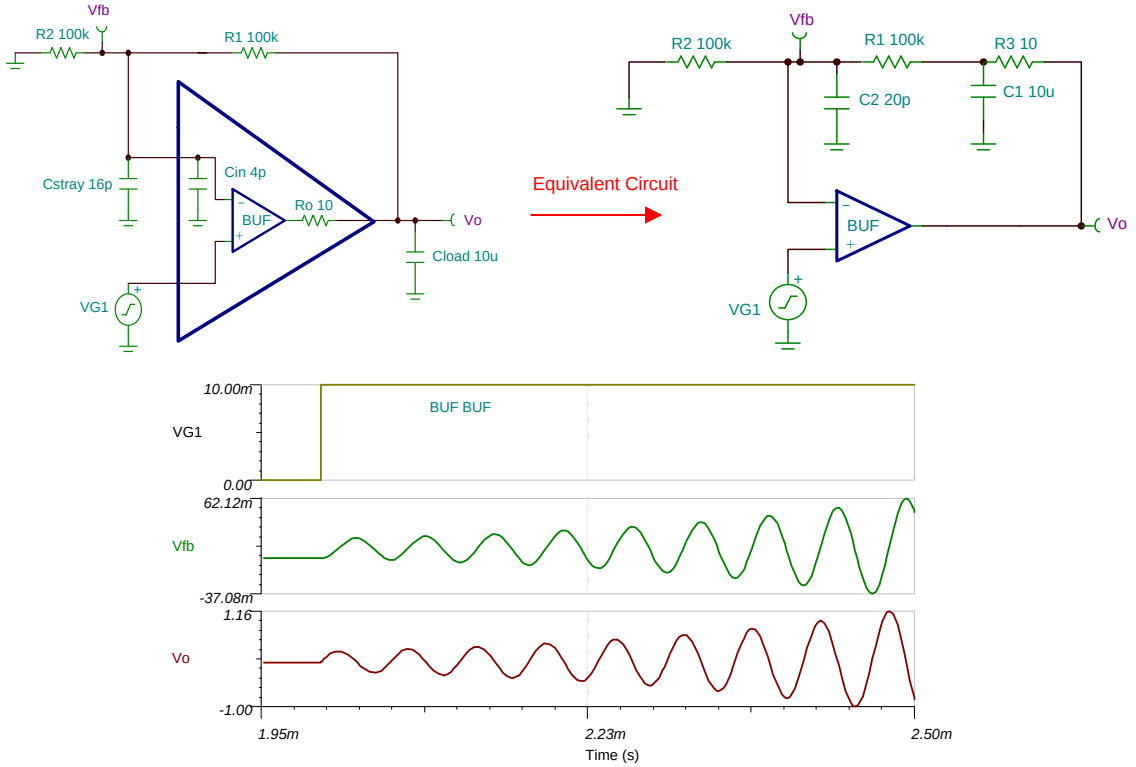


Figure 12. Stability Issue Due to Delay in Feedback Path

This simple, intuitive view of how delay or phase shift in the feedback path affects stability can help diagnose and solve the most common stability problems. Further sections discuss on how to deal with these problems using Bode analysis of feedback amplifiers.

Phase margin and rate of closure (ROC) are the tools to study stability of an op amp circuit. ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of the open-loop gain and open-loop output impedance of the amplifier. Therefore, it is a good practice to check the SPICE macro-model of the op amp for proper open loop gain (Aol) and open loop output impedance (Zo) before proceeding with any stability analysis simulations.

Figure 13 and Figure 14 confirm that both Aol and Zo graphs generated using OPA192 SPICE macro-model in TINA-TI simulation software match with the graphs given in *OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™*.

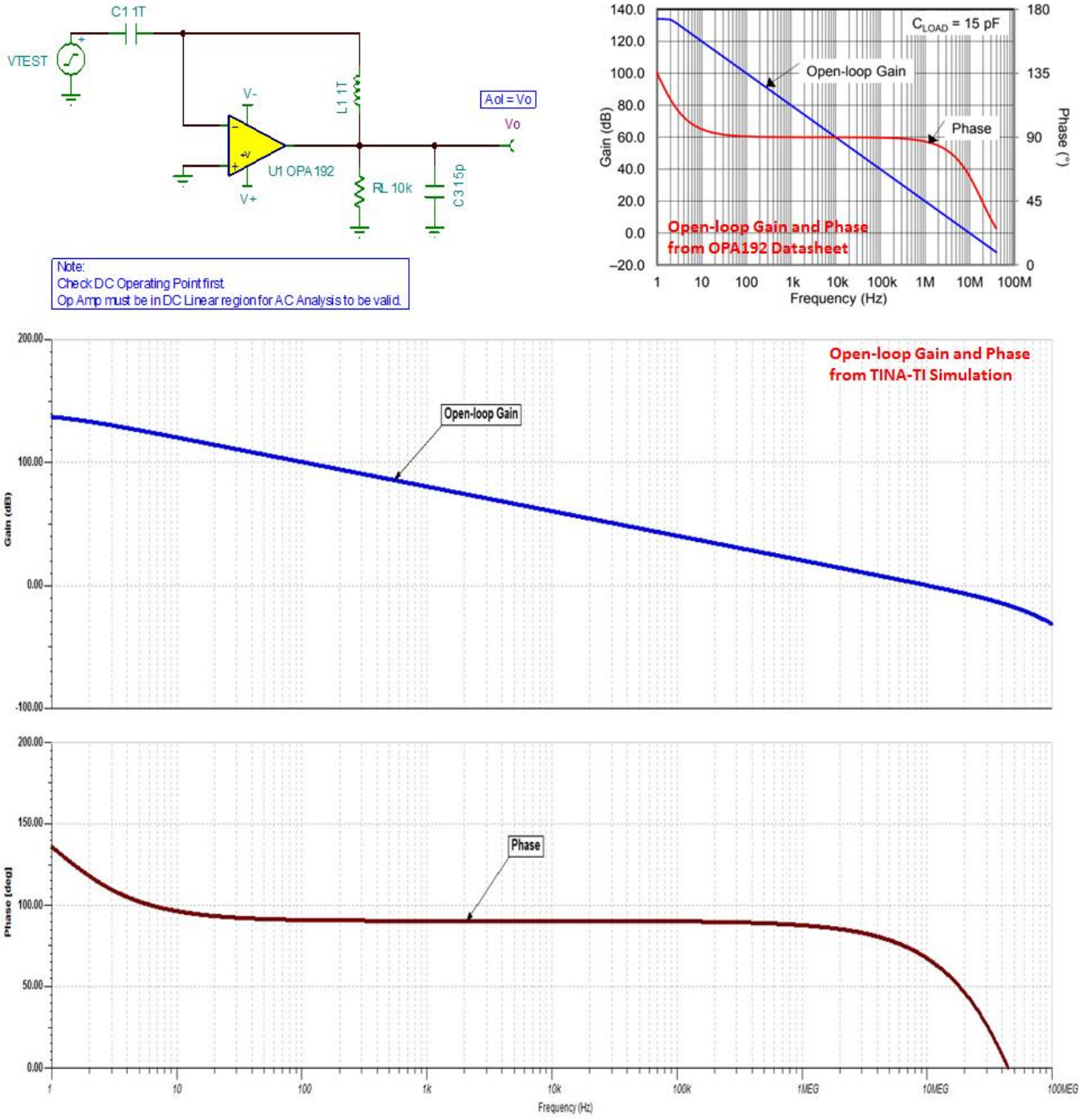


Figure 13. Aol Test of OPA192 SPICE Macro Model

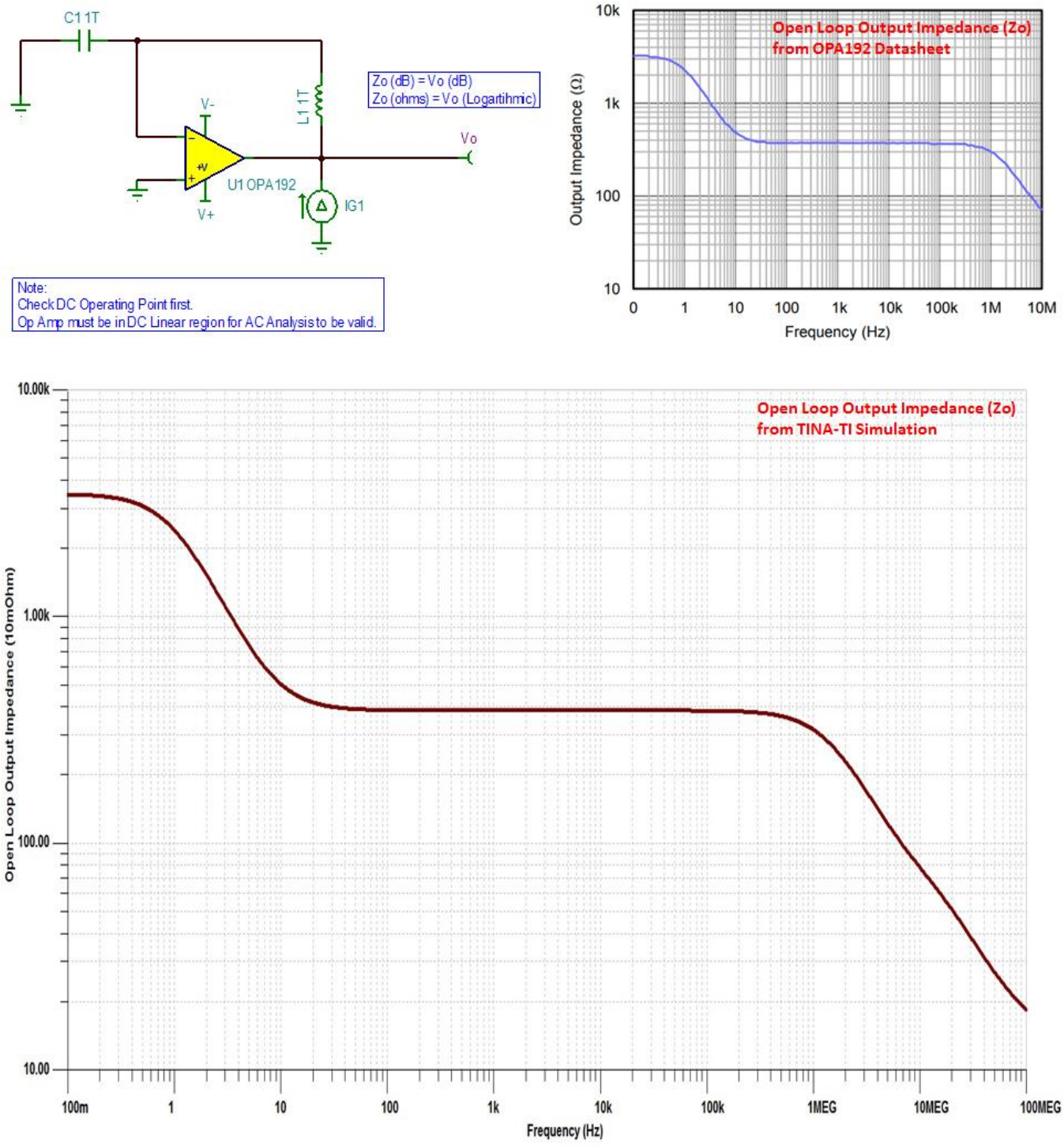


Figure 14. Open Loop Output Impedance (Zo) Test of OPA192 SPICE Macro Model

Phase margin is the difference (expressed as a positive number) between 180° and the phase shift where |Aol × β| crosses 0 dB. As phase margin approaches zero, the loop phase shift approaches –180° and the op amp circuit approaches towards instability. The more commonly used metric is phase margin because an amplifier circuit must be designed to have a phase margin of at least 45°. Typically, a phase margin of much less than 45° can cause problems such as "peaking" in frequency response and overshoot or "ringing" in step response. To maintain conservative phase margin, the pole generated by capacitive loading must be at least a decade above the closed loop bandwidth of the amplifier circuit.

ROC is the rate at which 1/β and AoI curves intersect each other at frequency (fcl) where loop gain goes 0 dB. Once one plots 1/β on the AoI curves, there is an easy first-order check for stability. A 40 db/decade ROC implies an *unstable* circuit and a 20 dB/decade ROC implies a *stable* circuit. The 40 dB/decade ROC implies instability because it implies two poles in the AoI × β plot before fcl, which can mean a 180° phase shift.

$$\text{Rate of Closure (ROC)} = \text{Slope}\left(\frac{1}{\beta}\right) - \text{Slope (AoI)} \tag{3}$$

Figure 15 shows four examples with their respective ROC.

- fcl1: 1/β1 – AoI = (20dB/decade) – (-20dB/decade) = 40dB/decade rate-of-closure & UNSTABLE
- fcl2: 1/β2 – AoI = (0dB/decade) – (-20dB/decade) = 20dB/decade rate-of-closure & STABLE
- fcl3: 1/β3 – AoI = (-20dB/decade) – (-40dB/decade) = 20dB/decade rate-of-closure & STABLE
- fcl4: 1/β4 – AoI = (0dB/decade) – (-40dB/decade) = 40dB/decade rate-of-closure & UNSTABLE

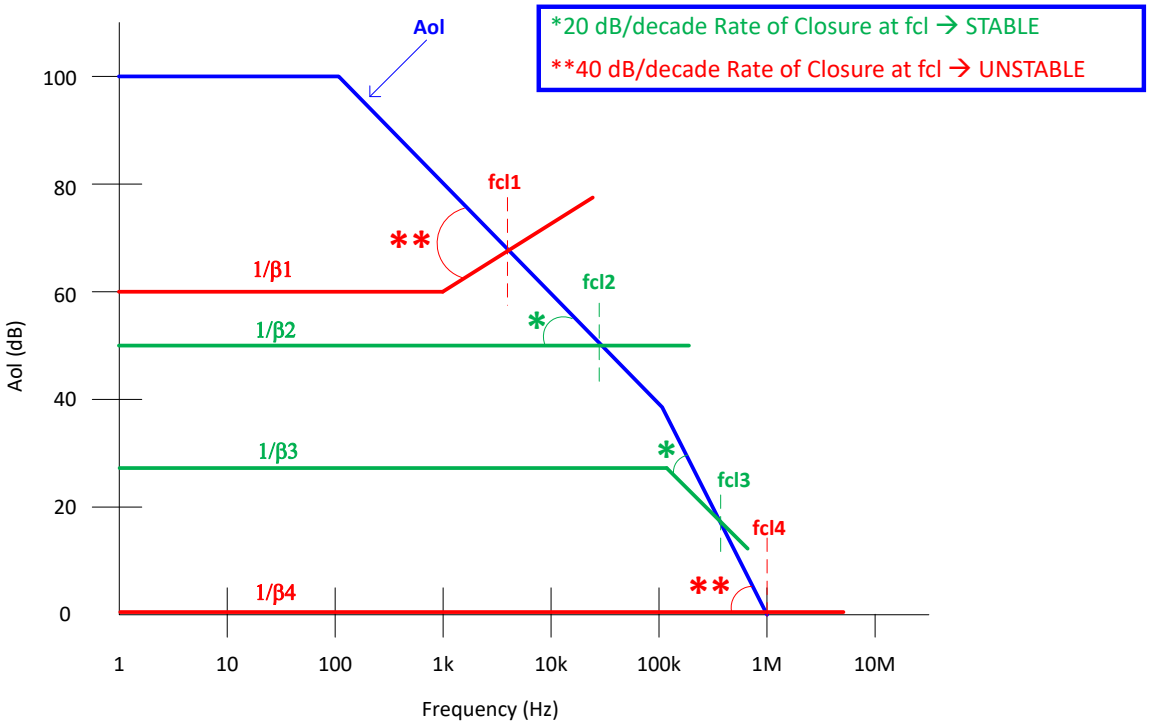


Figure 15. ROC Stability Test

The unity-gain buffer is the most sensitive configuration to capacitive loading. Figure 16 shows the bode plot of the OPA192 unity-gain buffer circuit with and without capacitive loading. The load capacitance (Cload) forms a pole with the open-loop output resistance (Ro). The loaded gain can be expressed as follows:

$$\text{Loaded Aol} = \text{Aol} \times \left(\frac{1}{1 + j\frac{f}{fp2}} \right), \text{where } fp2 = \frac{1}{2\pi \times R_0 \times \text{Cload}} \quad (4)$$

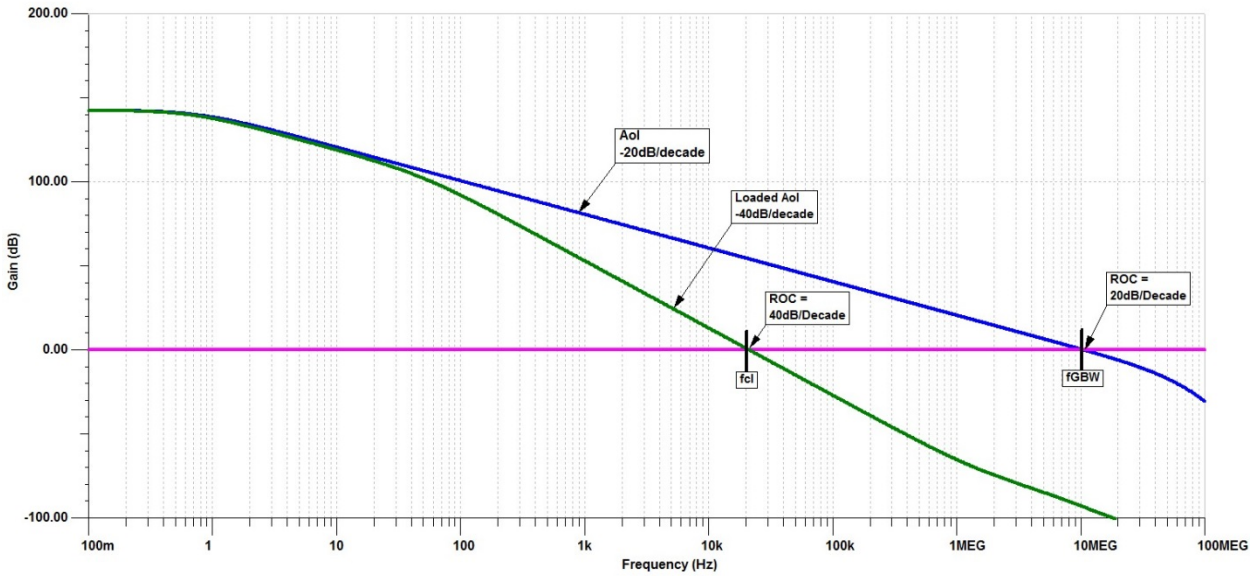


Figure 16. Bode Plot for OPA192 Unity-Gain Buffer With and Without Capacitive Load

The transient response (time-domain analysis) of the OPA192 unity-gain buffer driving capacitive load shows ringing for a step input (see Figure 17).

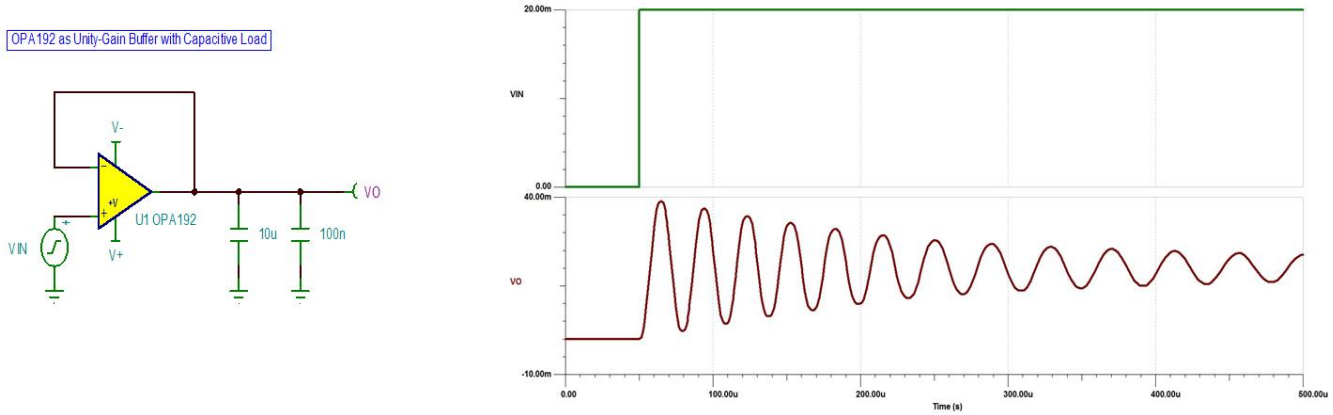


Figure 17. Transient Response of OPA192 as Unity-Gain Buffer With Capacitive Load

Looking at the simplified representation of the open loop circuit, the input signal passes through the Aol block and then the output impedance (Ro) before reaching the output voltage of the op amp (Vo). When a capacitor (Cload) is connected from the output to ground, the op amp Aol curve is loaded by the RC voltage divider formed by Ro and Cload.

Figure 18 shows the bode plot (frequency-domain analysis) of the OPA192 unity-gain buffer that drives the capacitive load. From Figure 18, the ROC at fcl is 40 dB/decade and the phase margin (PM) is 0.86°. The –20-dB/decade slope and 90° lag contributed by the pole, added to the –20-dB slope and 90° contributed by the amplifier, results in an increase in the ROC to a value of at least 40 dB/decade, which, in turn, causes instability.

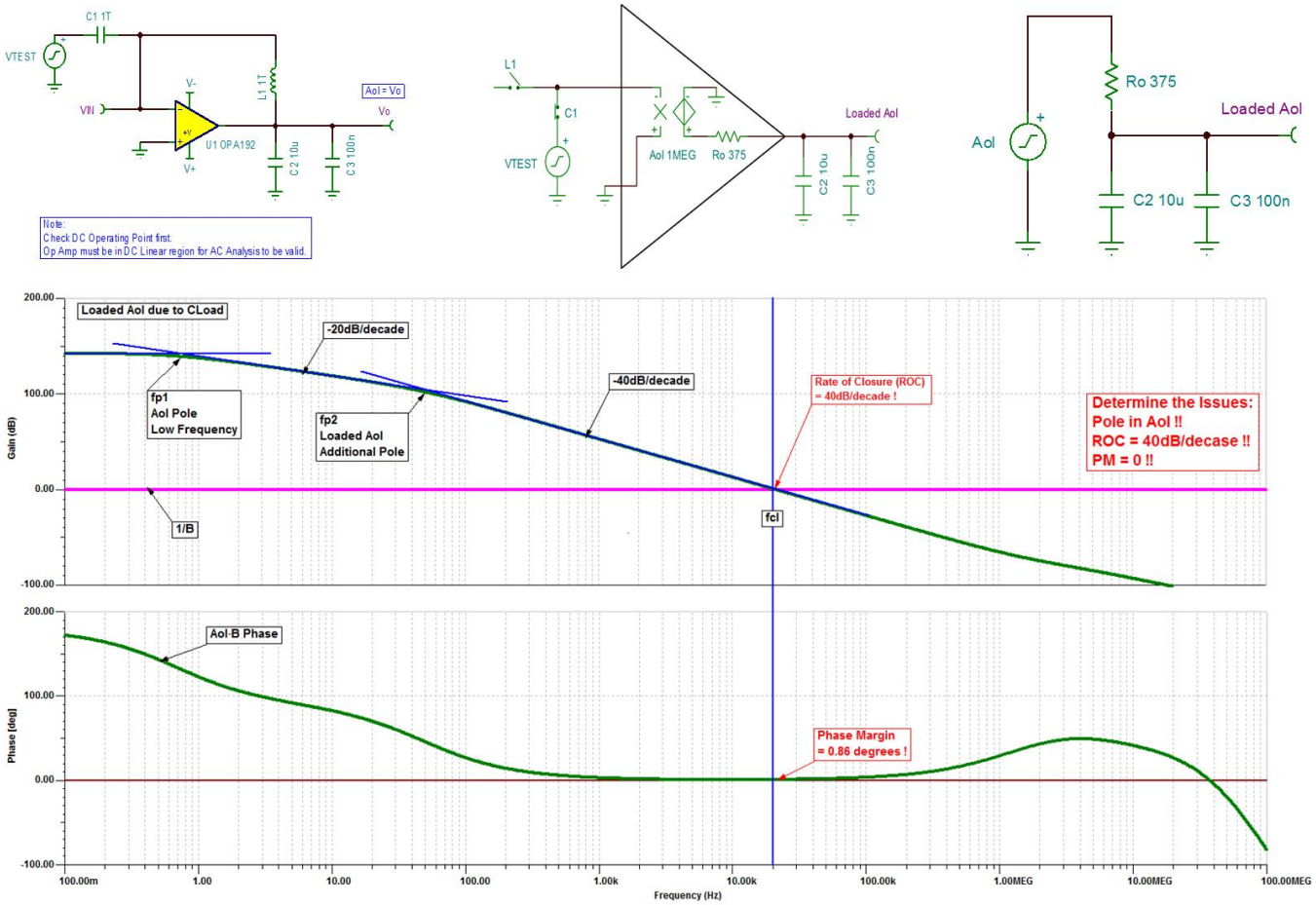


Figure 18. Bode Plot for OPA192 Unity-Gain Buffer With Capacitive Load

There are different compensation circuits that allow the op amp to remain stable while driving the capacitive load. With the help of two design examples, this reference design explores two popular compensation techniques for circuits using high-speed amplifiers to drive large capacitive loads. These techniques are out-of-loop compensation and in-loop compensation.

2.3.3.2 Out-of-Loop Compensation

The most common and easiest-to-design method to stabilize the output of an op amp for a capacitive load drive is to place an isolation resistor (Riso) in series with the capacitive load. Though apparently outside the feedback loop, the isolation resistor (Riso) adds a zero to the loop gain (Aol × β) transfer function, which cancels the phase shift from the pole and returns the ROC to 20 dB/decade.

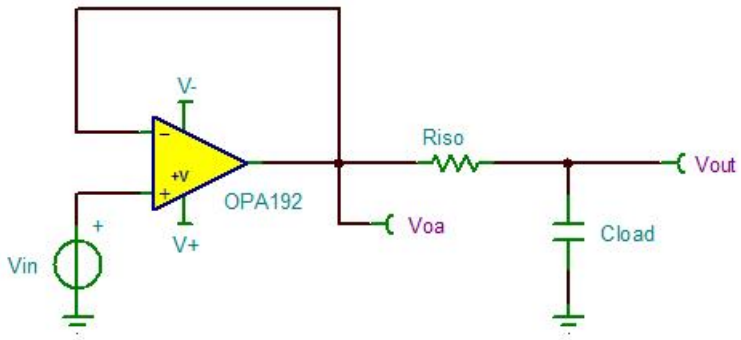


Figure 19. OPA192 Unity-Gain Buffer With Riso Stability Compensation

Examine the open loop Riso circuit in the same way as the capacitive load circuit. Once again, the Aol is loaded by an impedance divider. But this time, both Riso and Cload are on the bottom side of the divider, and Ro is on the top of the divider (see Figure 20).

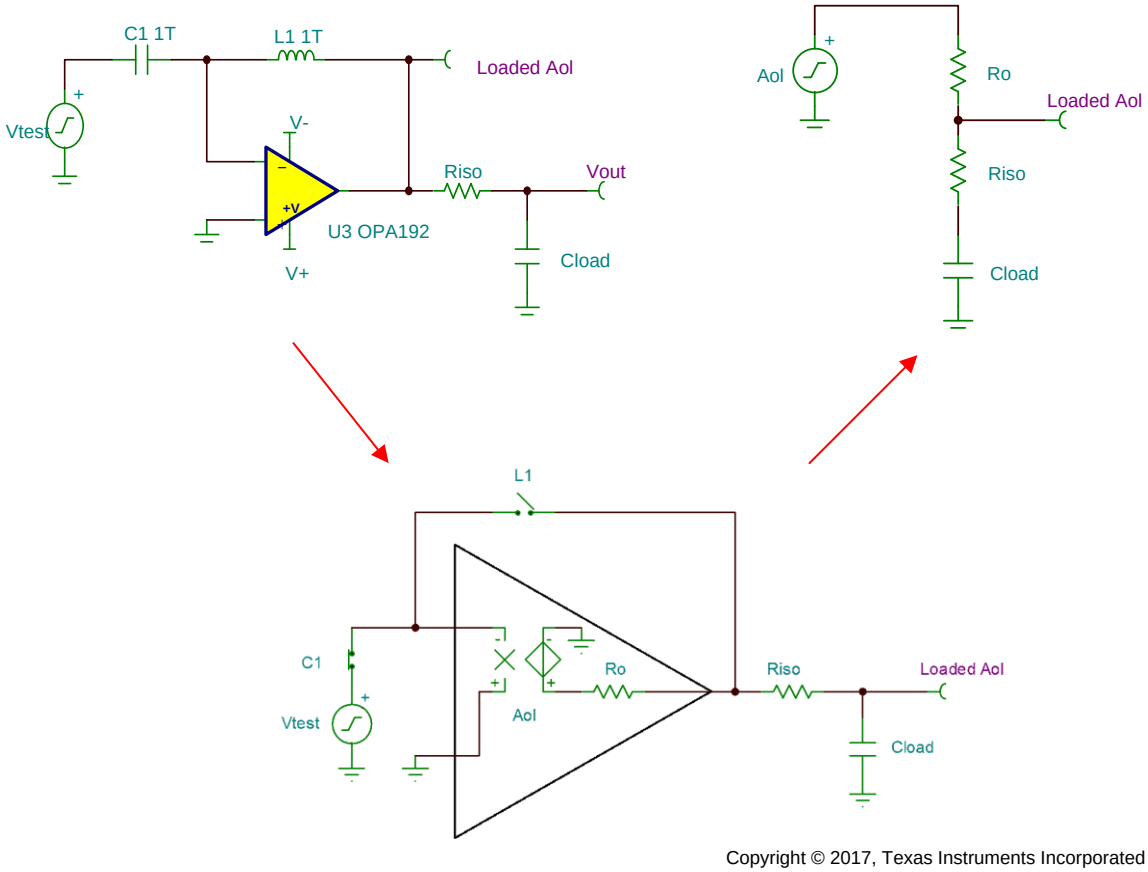


Figure 20. OPA192 Equivalent Loop Gain Model

Using Figure 20, the transfer function for Loaded Aol can be easily derived in the form of poles and zeros.

$$\text{Loaded Aol}(s) = \frac{1 + (\text{Cload} \times \text{Riso} \times s)}{1 + (\text{Ro} \times \text{Riso}) \times \text{Cload} \times s} \quad (5)$$

$$\text{fp2} = \frac{1}{2\pi \times (\text{Ro} + \text{Riso}) \times \text{Cload}} \quad (6)$$

$$\text{fz1} = \frac{1}{2\pi \times \text{Riso} \times \text{Cload}} \quad (7)$$

Loaded Aol in Equation 5 has a pole and a zero. The frequency of the pole (fp2) is determined by (Ro + Riso) and Cload. Riso and Cload determine the frequency of the zero (fz1). A stable system is obtained by selecting Riso such that the ROC between the open loop gain (Aol) and 1/β is 20 dB/decade. Figure 21 shows this concept.

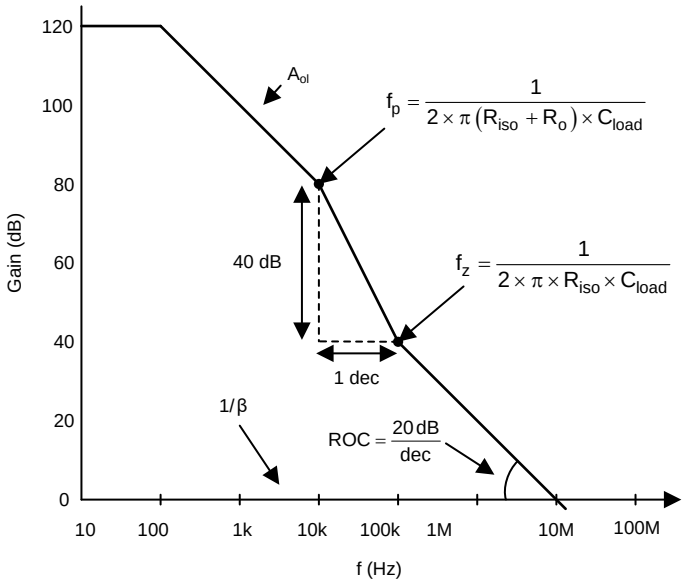


Figure 21. Gain Plot for OPA192

2.3.3.2.1 Design Procedure

1. Set Riso = 0 Ω to use the Loaded Aol phase plot to determine the pole locations (fp2). The measured value of fp2 in TINA-TI simulation is 51.078668 Hz.

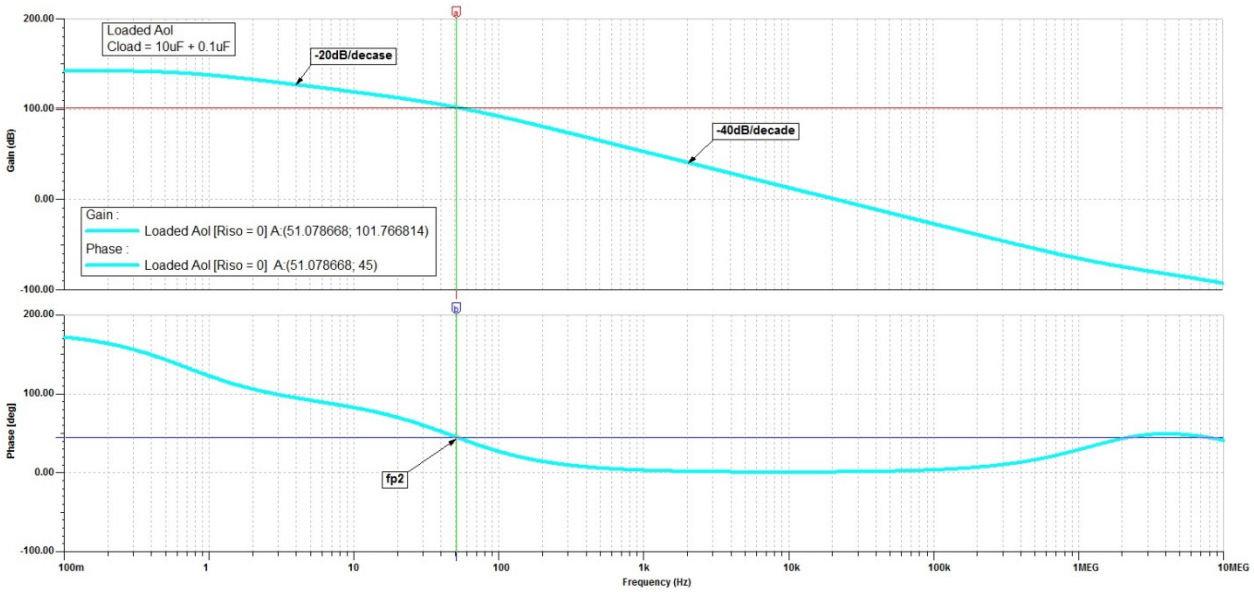


Figure 22. Gain and Phase Plot for Riso = 0

2. For the Riso compensation design, add zero such that fz1 ≤ 10 × fp2, meaning fz1 ≤ 510.78668 Hz. Therefore, calculate Riso using Equation 8:

$$\text{Riso} = \frac{1}{2\pi \times \text{fz1} \times \text{Cload}} = \frac{1}{2\pi \times 510.78668\,\text{Hz} \times 10\,\mu\text{F}} = 31.17\ \Omega \quad (8)$$

3. Set Riso to 31 Ω (nearest 1% standard value to 31.17 Ω) to yield the ROC analysis shown in Figure 23. The added zero at fz1 into the Loaded Aol with Riso compensation provides a –20-dB/decade slope crossing 0 db at fcl. This slope results in a stable circuit by ROC criteria of 20 dB/decade, indicating stability. If required, Riso can also be adjusted to achieve the desired phase margin.

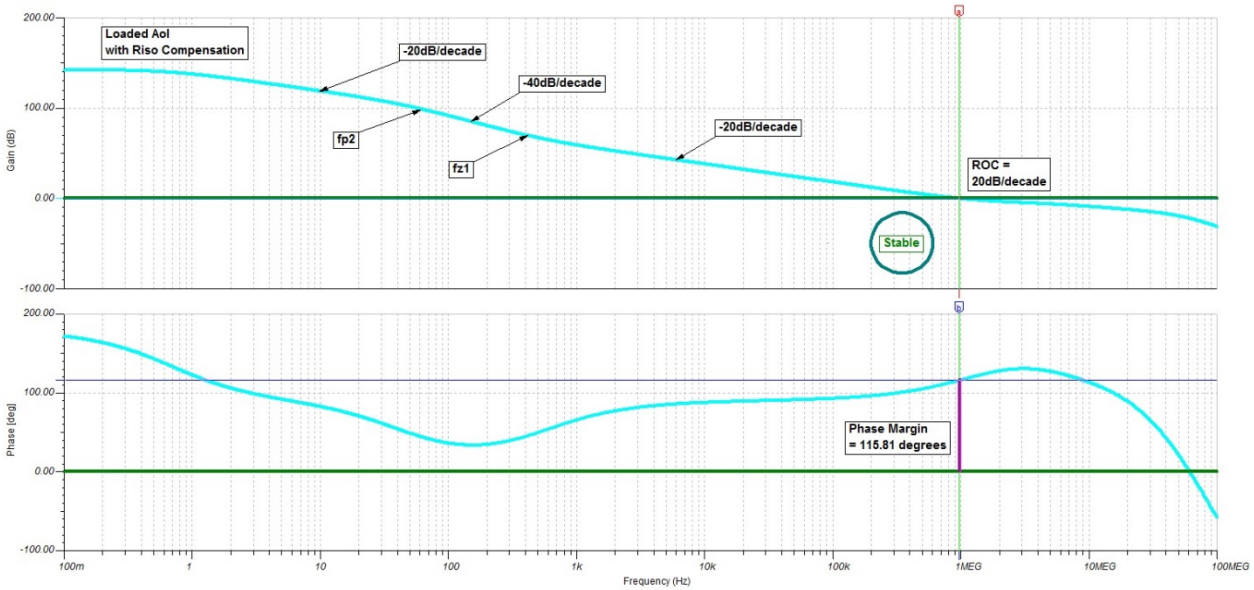


Figure 23. Gain and Phase Plot for Riso = 31 Ω

Figure 24 shows the unstable (SW1 = Closed) and stable (SW1 = Open) transient responses.

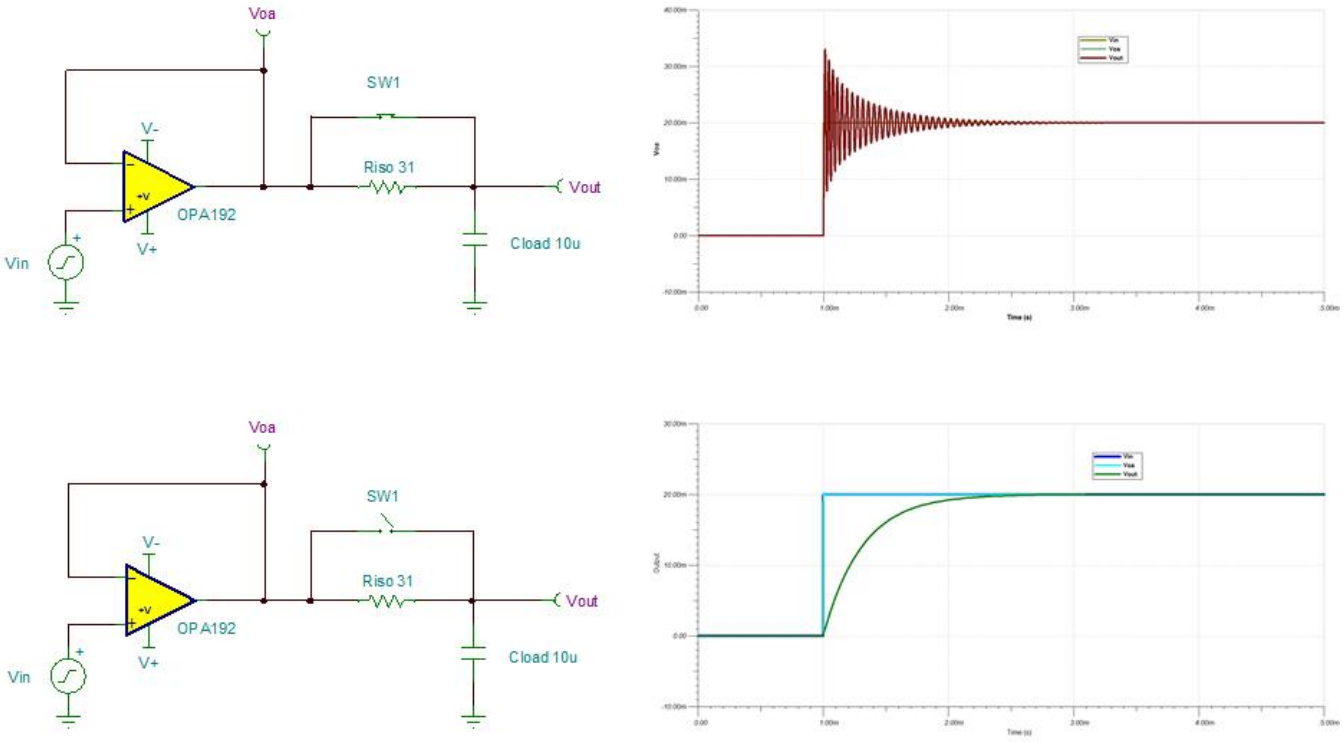


Figure 24. Unstable and Stable Transient Responses

The main disadvantage of stabilizing the unity-gain buffer circuit for capacitive load by using the out-of-loop compensation method is that there will be a voltage drop across Riso, which reduces the DC accuracy of the circuit when driving a load. However, reducing Riso also reduces the phase margin.

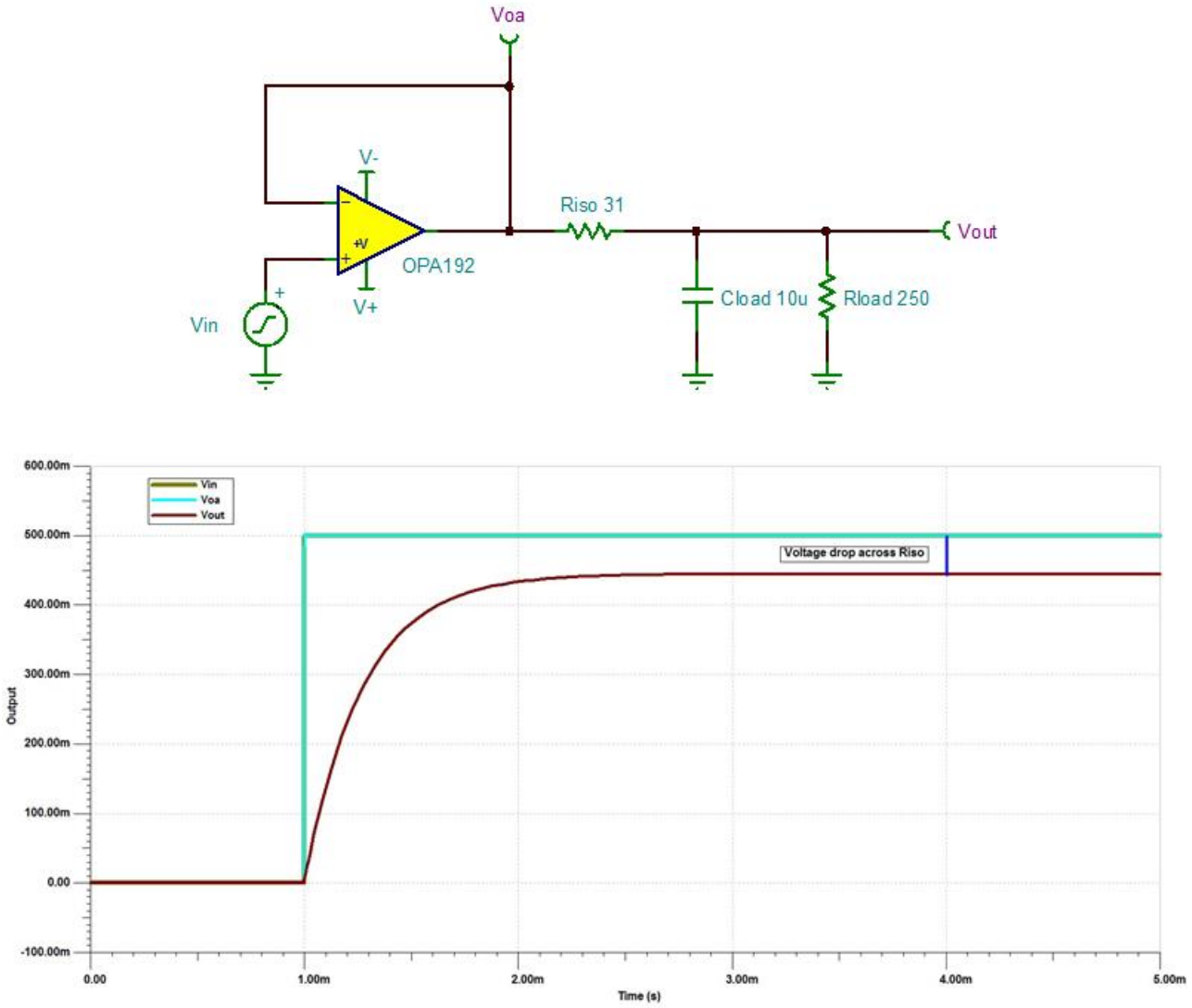


Figure 25. Riso Compensation Disadvantage

2.3.3.3 In-Loop Compensation

2.3.3.3.1 Bias Voltage Generation Circuit

A common solution to maintain DC accuracy while stabilizing the load is to use the Riso plus dual-feedback (Riso + DFB) circuit. As the name suggests, this compensation circuit has two feedback paths. The first feedback path (FB#1) is a DC feedback path through Rf and R1 to the input of operational amplifier that regulates the voltage at the load to be equal to input voltage. The second feedback path (FB#2) is an AC feedback through Cf back to the input of the op amp, which makes the circuit act like the Riso compensation circuit at high frequencies to stabilize against capacitive load. The Riso creates isolation between FB#1 and FB#2.

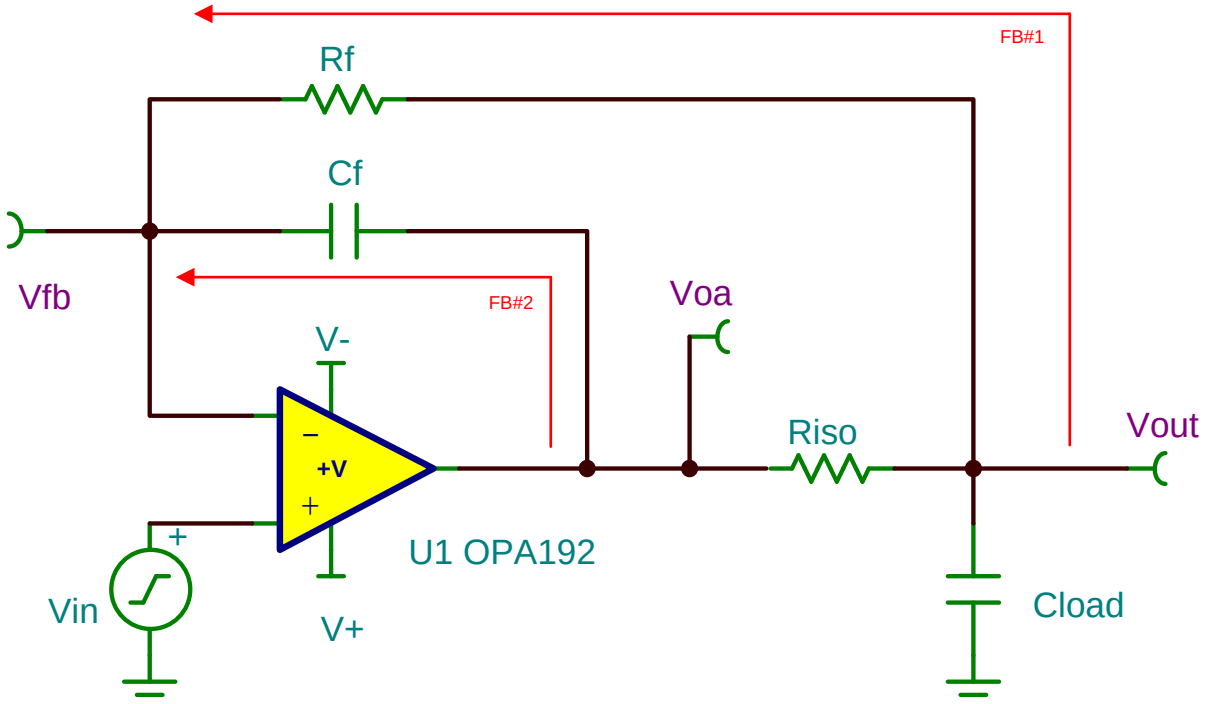


Figure 26. Riso Plus Dual Feedback Circuit (In-Loop Compensation)

The operation of the Riso plus dual feedback circuit can be analyzed using the DC and AC equivalent representations of the circuit. At DC, the feedback capacitor (Cf) acts as an open circuit, and Rf closes the feedback loop around Riso. Because Riso is now in the op amp feedback loop, the op amp output increases to overcome the Riso voltage drop such that the output voltage (Vout) is equal to Vin. At AC frequencies, Cf acts as a short. When this happens, Rf can be thought of as an open circuit because the impedance of Cf is much smaller than the impedance of Rf. Therefore at AC, this circuit looks effectively the same as the standard Riso circuit. The first design step in this circuit is to select Riso.

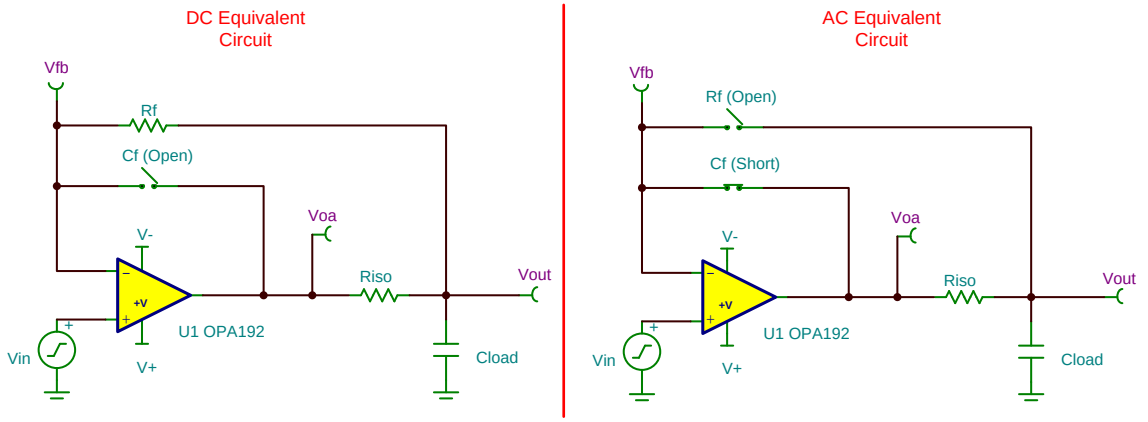


Figure 27. DC and AC Equivalent Circuit of OPA192 With Isolation Resistor

2.3.3.3.1.1 Design Procedure

1. Find out the value of Riso using out-of-loop compensation method. The Riso is selected to produce a zero in the loaded Aol curve such that fz ≤ 10 × fp. Found using the same method in Section 2.3.3.2.1, the value of Riso is 31 Ω.
2. Select Rf to any value greater than 100 × Riso to prevent any interaction with Riso. Therefore, Rf ≥ 100 × 31 Ω = 3.1 kΩ. The selected value for Rf is 6.2 kΩ. Another reason to choose 6.2 kΩ for Rf is to match with the filter resistance on the non-inverting input terminal of the op amp.
3. Analyze the Riso with dual feedback topology by plotting 1/β curves for both feedback paths FB#1 and FB#2 independently on the Aol curve of the op amp. When more than one feedback path is used around an op amp, the feedback path that feeds back the largest voltage to the op amp's input becomes the dominant feedback path. This implies that if 1/β is plotted for each feedback that the feedback with the lowest 1/β at a given frequency will dominate at that point. Remember that the smallest 1/β implies the largest β and the largest β implies the most voltage fed back to the input of the op amp. From Figure 28, the ROC between 1/β of FB#1 and Aol is 40 dB/decade. That means with FB#1 alone, the circuit is unstable. Therefore, FB#2 must be added such that it dominates at higher frequencies and help to bring the ROC with Aol back to 20 dB/decade as shown in Figure 28.

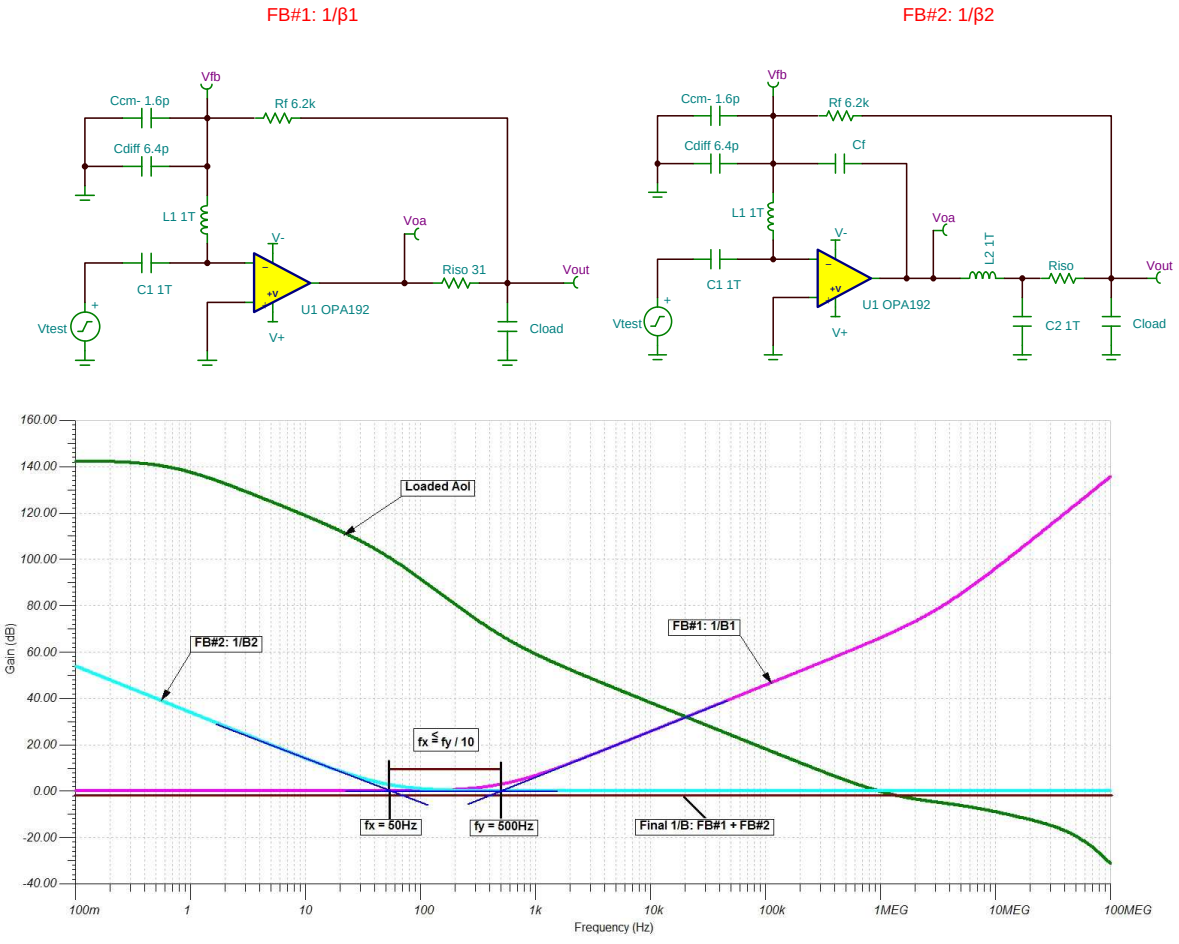


Figure 28. ROC Between 1/β of FB#1 and Aol

4. Position FB#2 such that fx ≤ fy/10. From Figure 28, fy = 500 Hz means fx must be less than or equal to 50 Hz.

$$fx = \frac{1}{2\pi \times Rf \times Cf} \leq 50\ Hz \tag{9}$$

$$\frac{1}{2\pi \times 6.2\ k\Omega \times 50\ Hz} \leq Cf \tag{10}$$

$$Cf \geq 0.514\ \mu F$$

The next standard closest value is 0.56 µF. Riso plus the dual feedback circuit is not as tolerant to changes in the output capacitance and can quickly become unstable. Therefore, Riso plus the dual feedback circuit is best for situations where the output capacitance is known and does not vary significantly. With Cf = 0.56 µF, the circuit is stable with a loop gain phase margin of 115.7°.

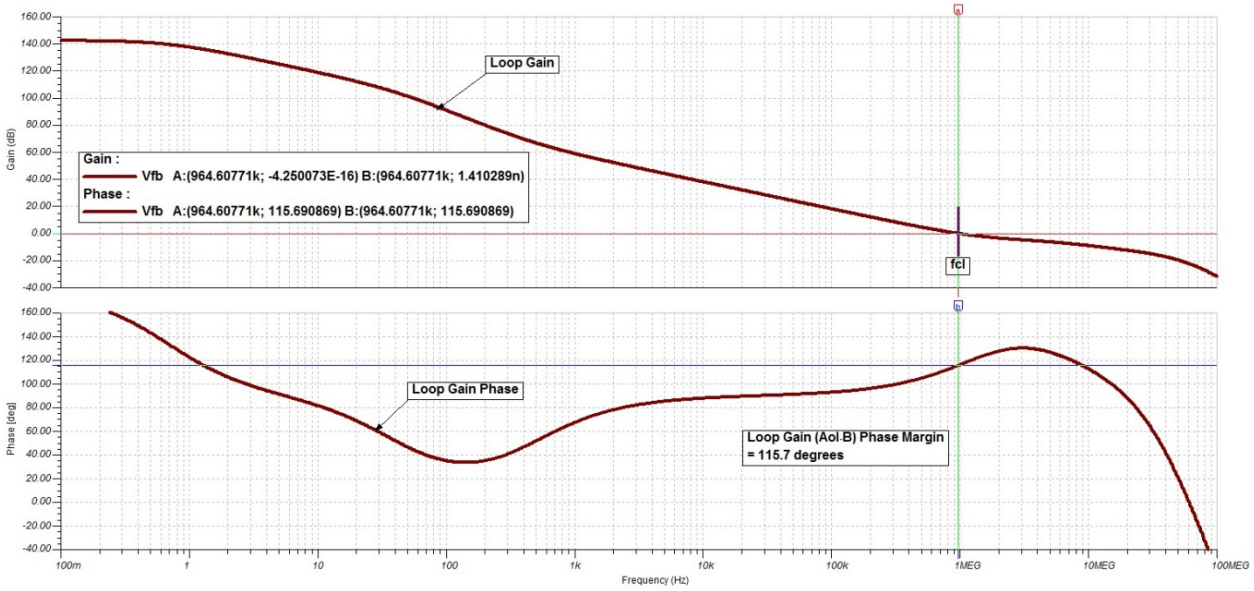


Figure 29. Stability Analysis With Cf = 0.56 µF

The final circuit that is proposed for ultra-low noise, precision bias voltage is shown in Figure 30.

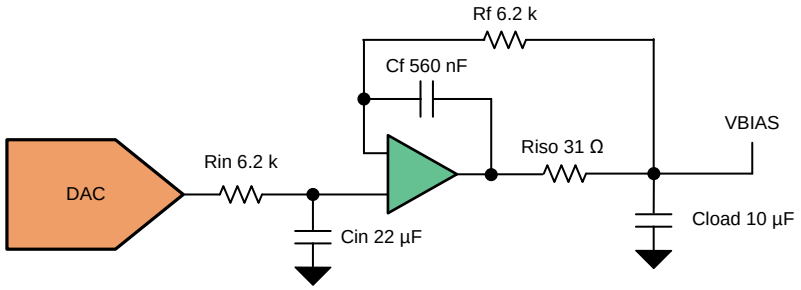


Figure 30. Proposed Ultra-Low Noise, Precision Bias Voltage Circuit

2.3.3.3.2 Power Supply Circuit

A power supply circuit for the sensor is required to deliver higher load currents. Usually, op amps are not capable of supplying that much output current. However, to have an op amp control the power supply voltage that can deliver hundreds of mA, add an external bipolar transistor on the output of the op amp. The op amp still controls the power supply voltage, and the load current is supplied by the transistor. Because the external transistor is part of a negative feedback loop, the external transistor characteristics are not critical. Virtually any transistor with sufficient voltage, current, and power rating can be used. Basic requirements are as follows:

- $V_{CEO} > V_{CE}$ (Operation, Max)
- $\beta = 40$ minimum
- Must be able to handle power dissipation, $P_D = V_{CE(MAX)} \times I_{LOAD(MAX)}$

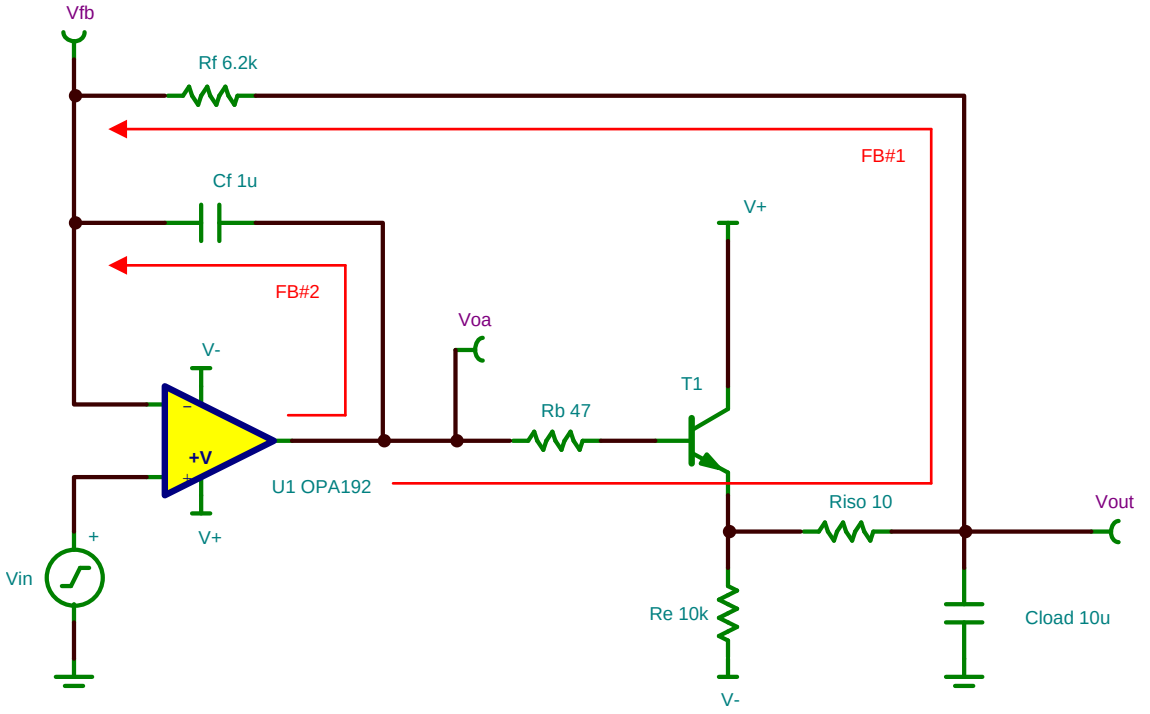


Figure 31. Stability Analysis With FB#1 Only

2.3.3.3.2.1 Design Procedure

1. Find out the value of Riso using the out-of-loop compensation method. Riso is selected to produce a zero in the loaded AoI curve such that fz ≤ 10 × fp. Found using the same method as Section 2.3.3.3.1.1, the value of Riso is 31 Ω.
2. Select the Rf to any value greater than 100 × Riso. Therefore, Rf ≥ 100 × 10 Ω = 1 kΩ. The selected value for Rf is 6.2 kΩ. Another reason to choose 6.2 kΩ for Rf is to match with the filter resistance on the non-inverting input terminal of the op amp.
3. First plot the 1/β of FB#1 on the AoI curve. From Figure 32 without FB#2, the circuit is unstable because the ROC between 1/β of FB#1 and open-loop gain (AoI) is 40 dB/decade.

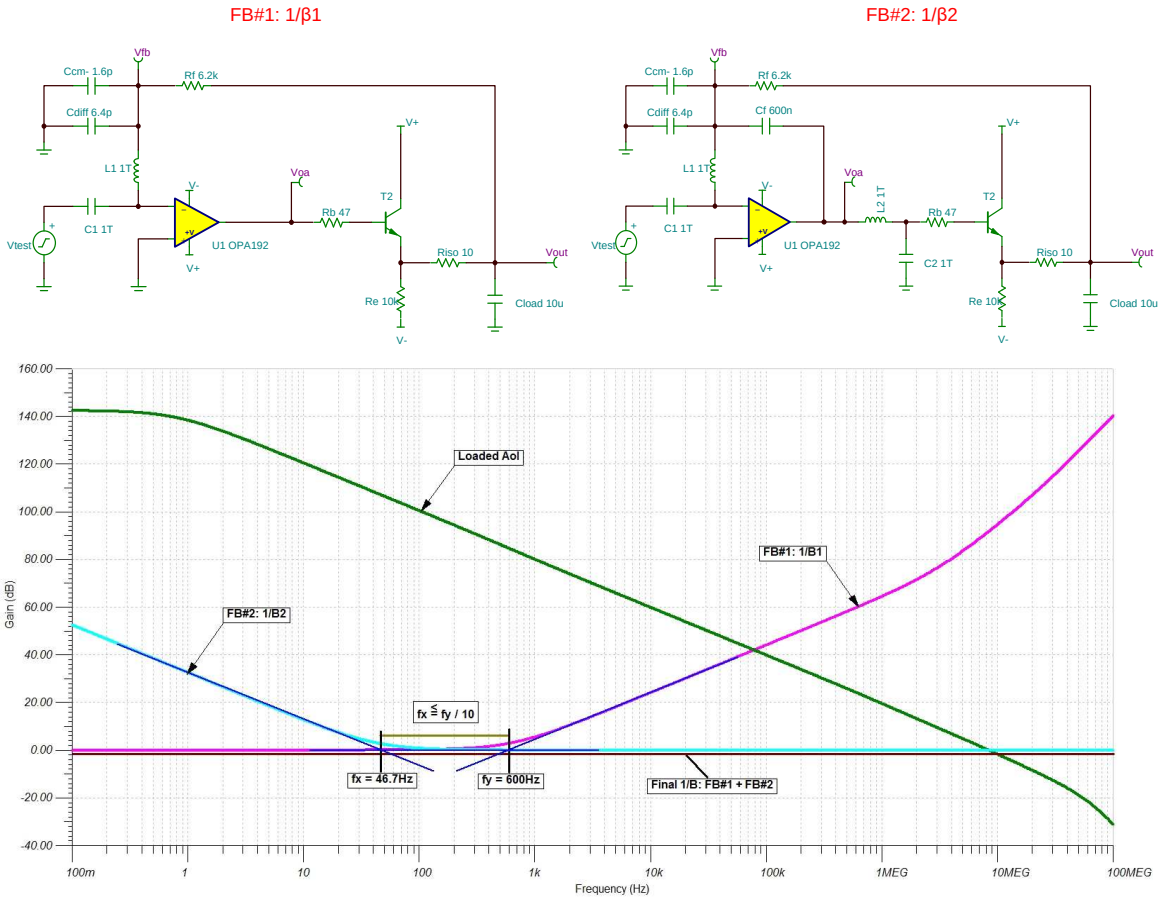


Figure 32. Stability Analysis With FB#1 and FB#2

4. Position the FB#2 by changing value of Cf such that fx is either less than or equals to fy/10. From Figure 32, fy = 600 Hz means that fx must be less than or equal to 60 Hz. From the TINA simulation, fx is 46.7 Hz with a Cf value of 0.6 µF. The circuit is stable with a loop gain phase margin of 69.7°.

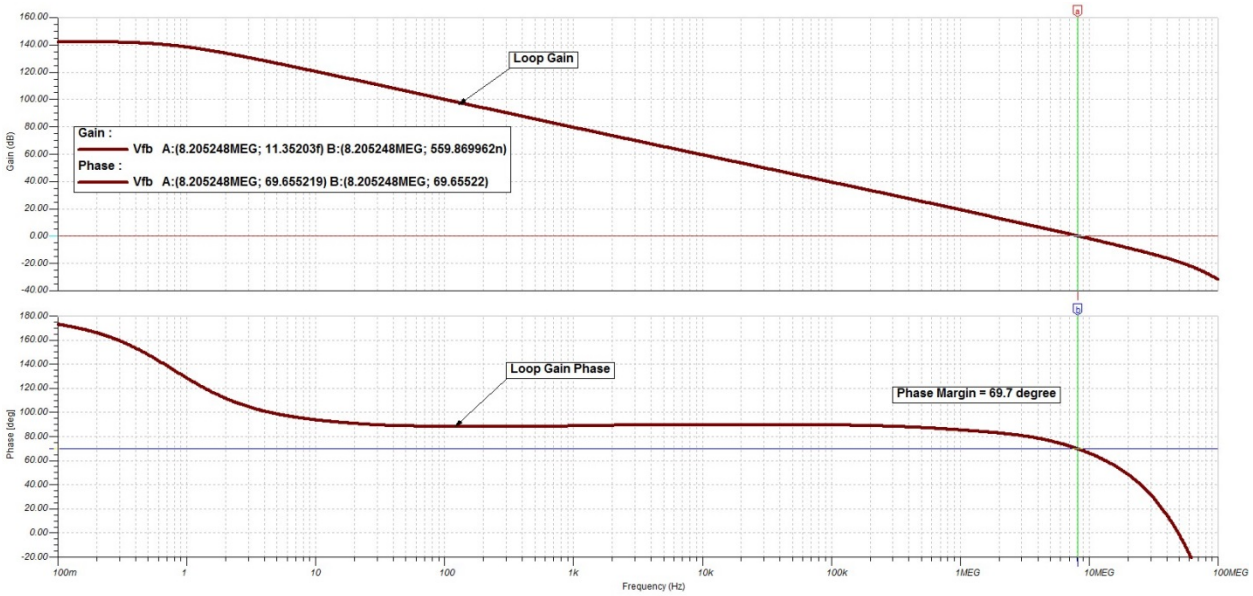


Figure 33. Stability Analysis With Cf = 0.6 µF

The final circuit that is proposed for ultra-low noise, precision power supply is shown in Figure 34.

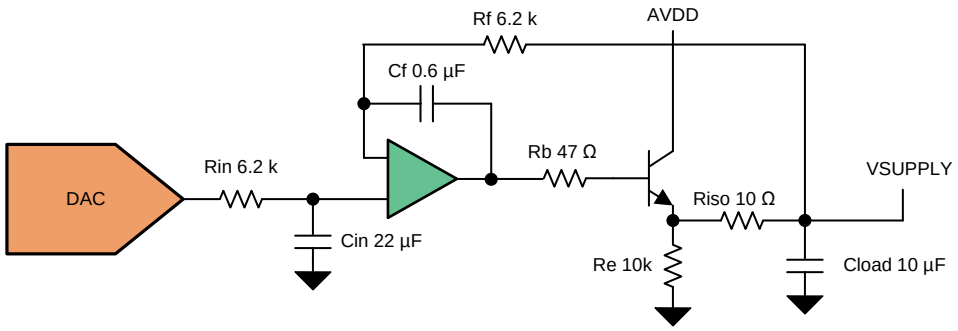


Figure 34. Final Proposed Circuit for Ultra-Low Noise, Precision Power Supply

2.3.4 Noise Analysis

For noise analysis in TINA-TI, the DAC must be represented by a voltage source in series with a noise source. Edit the macro-model of the noise source manually, as shown in Figure 35, to match with the noise specification of the DAC. Finally, compile the macro and close the netlist.

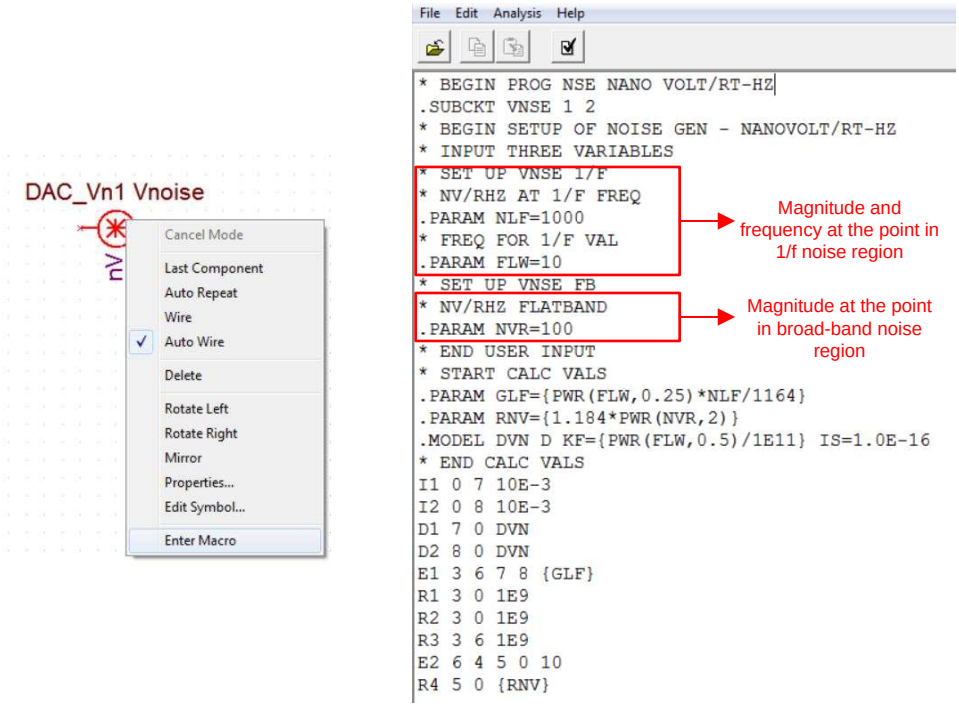


Figure 35. Editing Marco Model for Noise Source in TINA-TI

2.3.4.1 Bias Voltage Circuit

This circuit implements a heavy low-pass filter suppressing most of the noise from DAC. If the noise frequency of interest is well above the cutoff frequency of the filter, the DAC noise is negligible, and the output noise is the op amp noise multiplied by the closed-loop gain. From simulation, the total output noise over a bandwidth from 0.1 Hz to 1 MHz is around 3.711 μV_{RMS}.

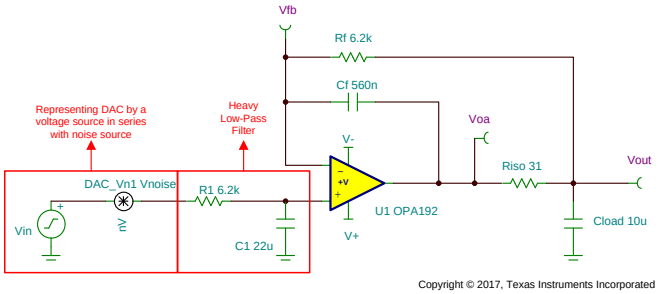


Figure 36. TINA-TI Schematic for Bias Voltage Circuit

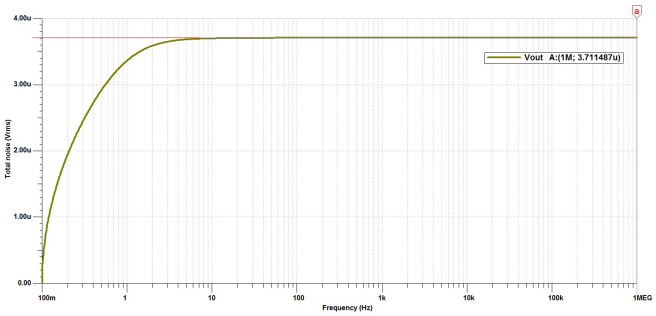


Figure 37. TINA-TI Simulation for Total Output Noise for Bias Voltage Circuit

2.3.4.2 Power Supply Circuit

This circuit implements a heavy low-pass filter suppressing most of the noise from DAC. If the noise frequency of interest is well above the cutoff frequency of the filter, the DAC noise is negligible, and the output noise is just the op amp noise multiplied by the closed-loop gain. From simulation, the total output noise over a bandwidth from 0.1 Hz to 1 MHz is around 3.712 μV_{RMS}. In this case, the BJT noise is suppressed by the loop and has no effect on the output noise.

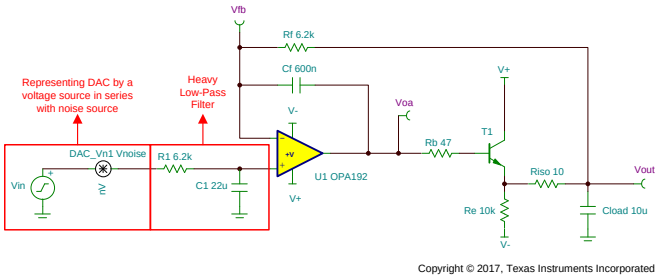


Figure 38. TINA-TI Schematic for Power Supply Circuit

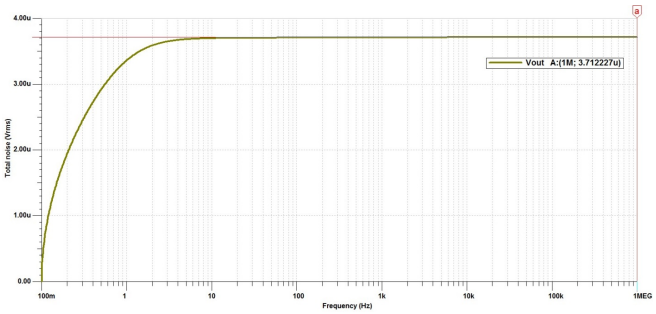


Figure 39. TINA-TI Simulation for Total Output Noise for Power Supply Circuit

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

Figure 40 shows the hardware for this reference design. The printed circuit board (PCB) is 50.80-mm × 60.96-mm rectangular form factor. This design comes as BoosterPack™ to TI MSP430™ LaunchPad™ family. The design can be programmed using the TI MSP430G2 LaunchPad. Hardware comes with four independent SMA connectors for outputs to provide ease of use while performing lab measurements. All the integrated circuits (DAC80508, OPA2192, TPS71750, and TPS71733), several test points, and jumpers are located on the top side of the PCB. The DAC80508 device is an octal channel DAC. Only the first four channels (CH0 to CH3) are used. All op amp buffers are in unity gain configuration. Their gain resistors have not been populated. Jumpers JP4, JP6, JP8, and JP10 provide facility to connect or disconnect the on-board load resistors.

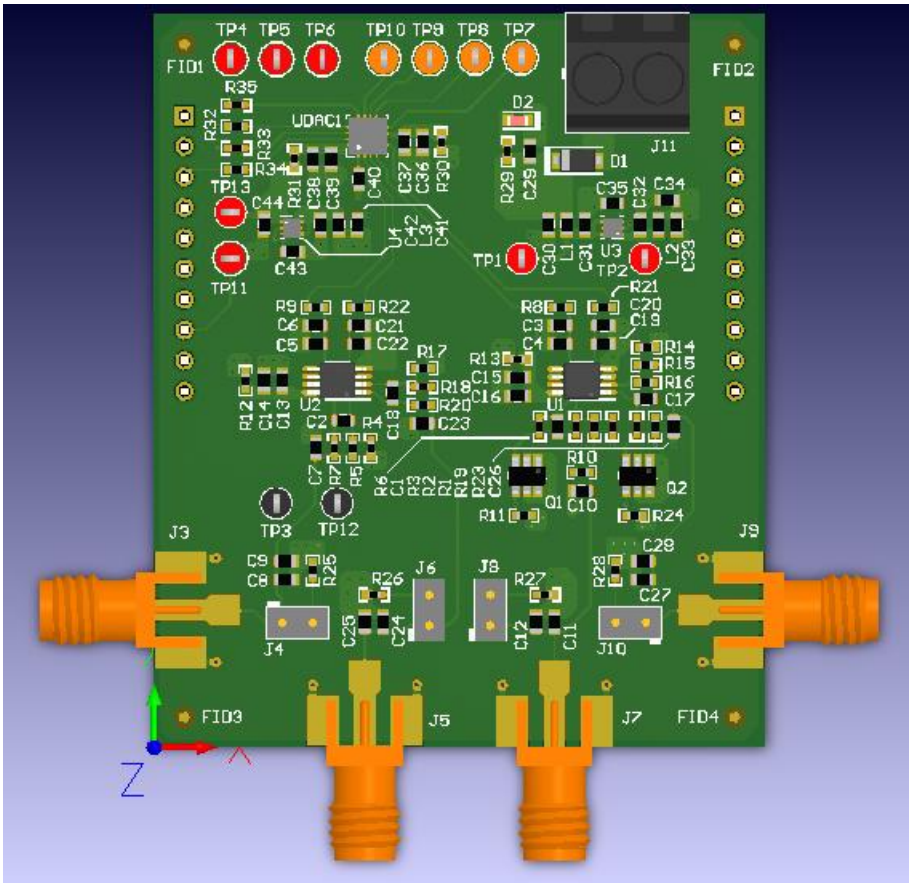


Figure 40. Hardware Image of TIDA-01583

3.2 Testing and Results

3.2.1 Test Setup

The noise of the device under test (DUT) is generally specified by two separate categories:

1. 1/f or low-frequency (0.1 Hz to 10 Hz) specified as μV_{P-P}
2. Wideband noise as μV_{RMS} for a given band (for example, 10 Hz to 1 MHz), or spectral-voltage noise density at a frequency where the noise spectral density has reached its flatness, specified as nV/√Hz.

Figure 41 shows the test setup for 1/f noise measurement. The 1/f noise is captured in time-domain using oscilloscope. This circuit is designed to amplify low-frequency noise (0.1 Hz to 10 Hz) to a level that is easily measured by an oscilloscope. The oscilloscope achieves this function with a 0.1-Hz, second-order, high-pass filter and a 10-Hz, fourth-order, low-pass filter. The offset of the DUT is not important, as the input to the filter is AC-coupled. The output of the filter is connected to an oscilloscope and the peak-to-peak voltage is measured for 10 seconds to capture the full 0.1-Hz to 10-Hz bandwidth (1/10 seconds = 0.1 Hz). The results shown on the scope are then divided by the gain of 105 to calculate the 0.1-Hz to 10-Hz noise.

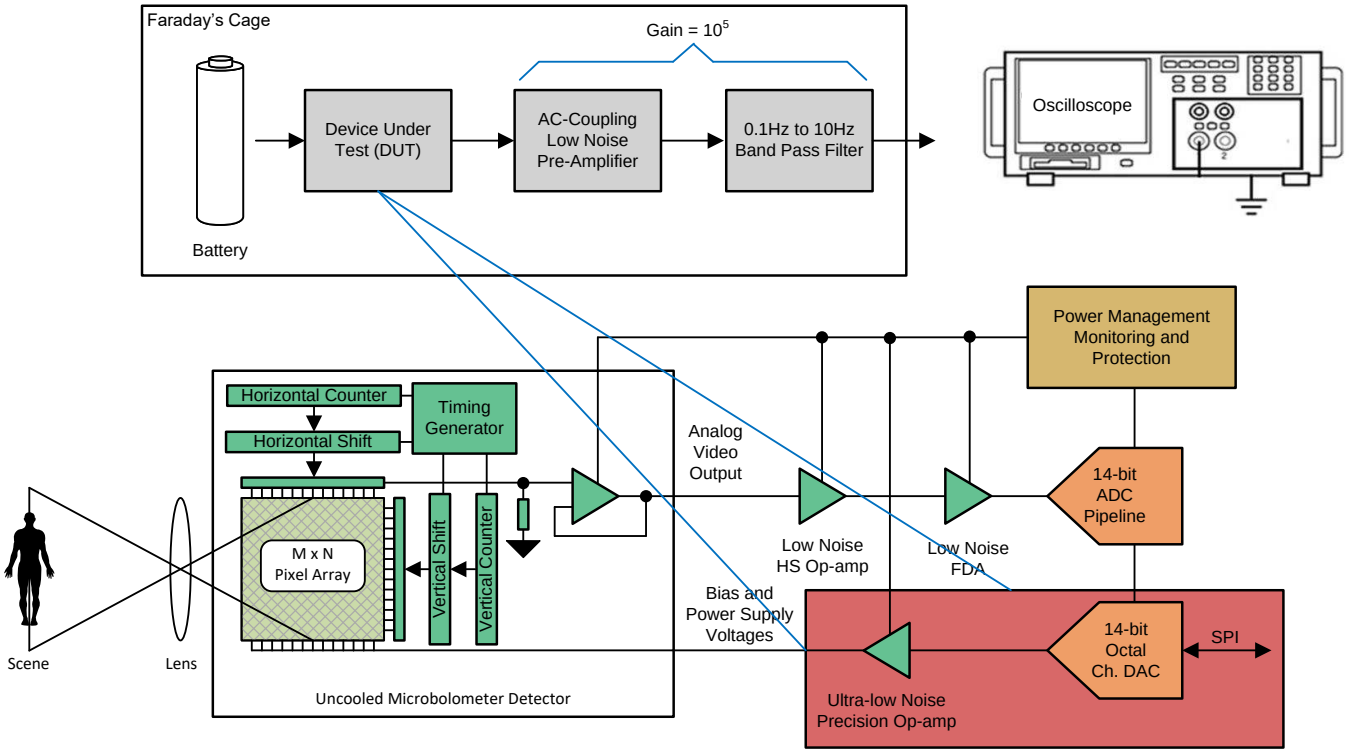


Figure 41. 1/f Noise Measurement Setup

Figure 42 shows the test setup for broadband noise measurement. The AC coupling capacitor only allows the AC signal to be transmitted to the subsequent circuitry. The amplifier is also optional and allows the spectrum analyzer to measure the signal more easily. The amplifier is only needed if the noise floor (noise measured without DUT connected) is too high.

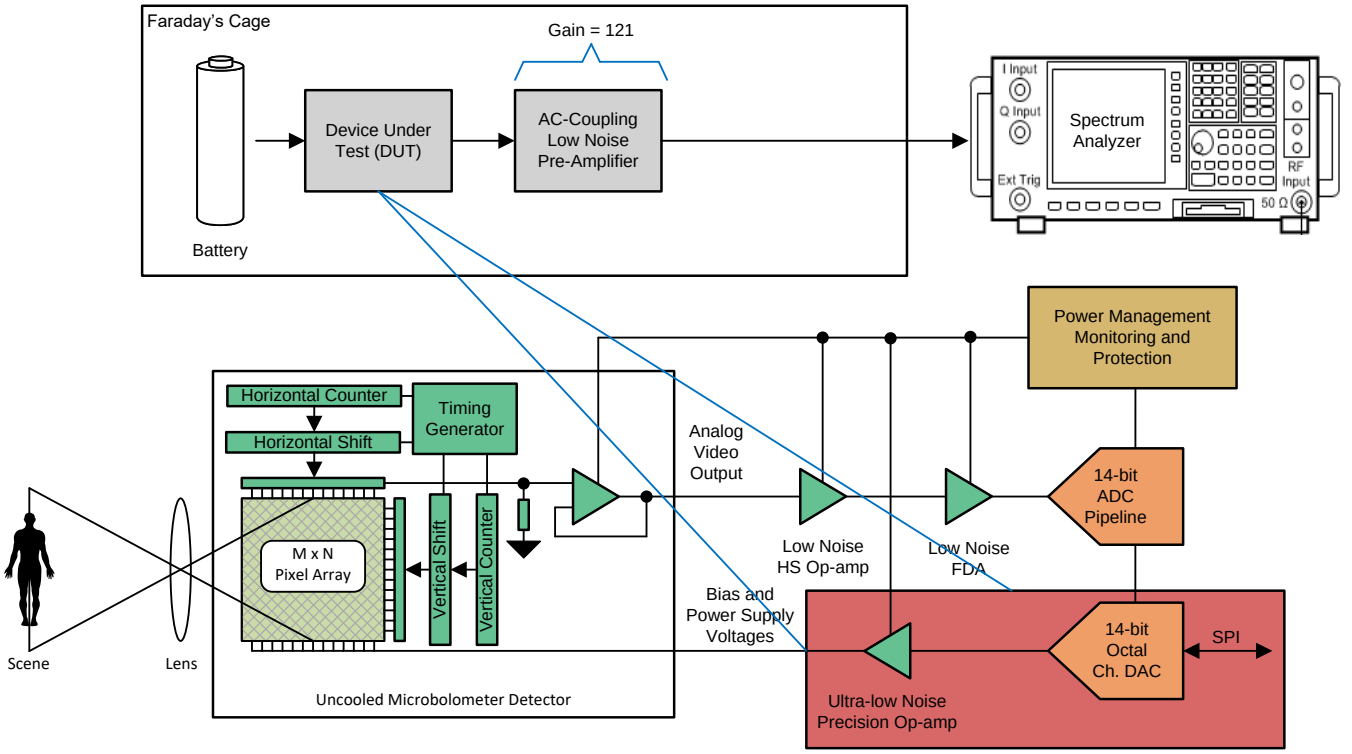


Figure 42. Broadband Noise Measurement Setup

When measuring the intrinsic noise of the DUT, it is important to minimize the effect of noise from other sources, including the environment. Therefore, it is important to use a shielded environment (Faraday's Cage) to get the best results from this test. This shield is effective at shielding the noise filter from 60 Hz and other noise pickup. The shield also minimizes temperature shifts by protecting the board from air turbulence. It is important that the entire shield is grounded with minimal air gaps (slot antennas). If a paint can is used, make sure that the lid and can are sealed completely. If necessary, sand the rim in the lid of the paint can to ensure that the lid and can make good electrical contact.

The DACx0508 family of DACs incorporates a power-on-reset (POR) circuit that ensures the DAC outputs power up and remain at either zero-scale (Z) or mid-scale (M) until a valid code is written to the device. For the noise measurement, the DAC80508M is chosen to output a midscale voltage (that is, 2.5 V) after POR.

3.2.2 Test Results

3.2.2.1 Noise Measurement for Bias Voltage Circuit

RMS 1/f noise (V_{n1}) from 0.1 Hz to 10 Hz = Peak-to-peak noise / 6 = 15.4 µV / 6 = 2.57 μV_{RMS}.

Wideband noise (V_{n2}) integrated from 10 Hz to 1 MHz = 2.80 μV_{RMS}.

The total integrated noise (V_n) from 0.1 Hz to 1 MHz is calculated by Equation 11:

$$\sqrt[2]{(V_{n1})^2 + (V_{n2})^2} = \sqrt[2]{(2.57)^2 + (2.80)^2} = 3.801\ \mu V_{RMS} \quad (11)$$

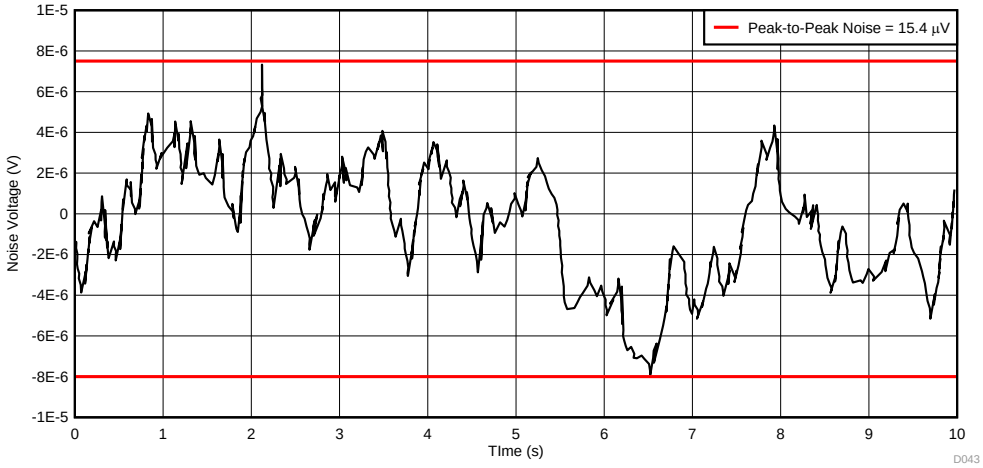


Figure 43. 0.1-Hz to 10-Hz Noise for Bias Voltage Circuit

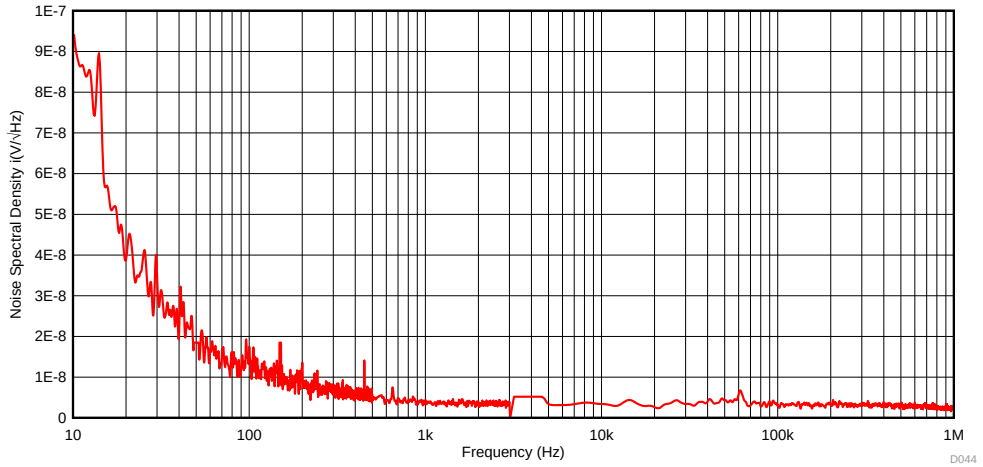


Figure 44. Spectral Voltage Noise Density for Bias Voltage Circuit

3.2.2.2 Noise Measurement for Power Supply Circuit

The RMS 1/f noise (V_{n1}) from 0.1 Hz to 10 Hz = Peak-to-Peak Noise / 6 = 16 µV / 6 = 2.67 μV_{RMS}.

Wideband noise (V_{n2}) integrated from 10 Hz to 1 MHz = 2.92 µV.

The total integrated noise (V_n) from 0.1 Hz to 1 MHz is calculated by Equation 12:

$$\sqrt[2]{(V_{n1})^2 + (V_{n2})^2} = \sqrt[2]{(2.67)^2 + (2.92)^2} = 3.957\ \mu V_{RMS} \quad (12)$$

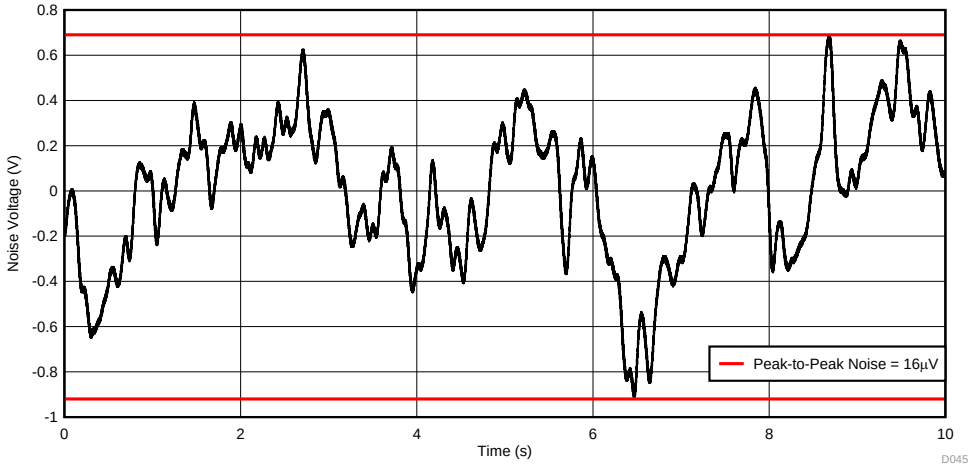


Figure 45. 0.1-Hz to 10-Hz Noise for Power Supply Circuit

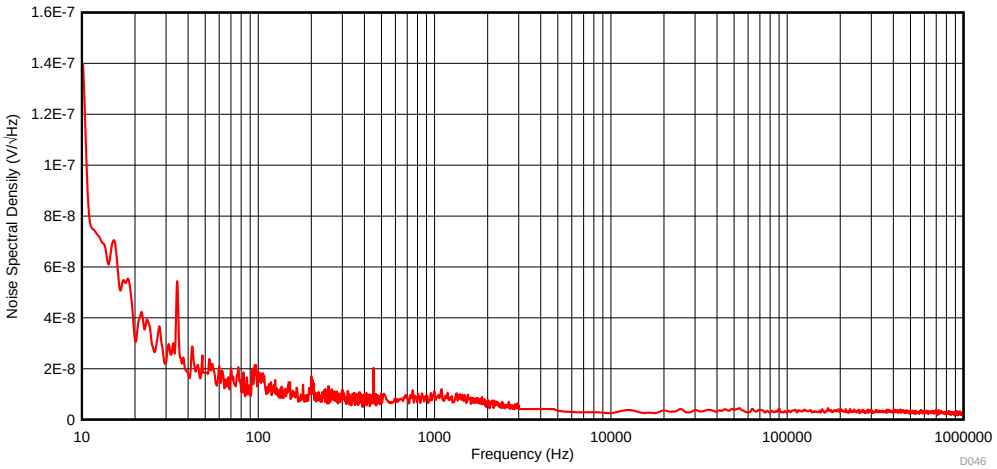


Figure 46. Noise Density of Spectral Voltage for Power Supply Circuit

3.2.2.3 Accuracy and Precision Test

For accuracy and precision measurement, all the outputs are programmed to generate a fixed mid-scale output, which is 2.5 V. More than 4096 samples are recorded over time using a 6½ digit multimeter. The minimum and maximum voltages recorded for bias voltage circuit are 2.505095 V and 2.505132 V, respectively. The peak-to-peak variation due to noise is 37 µV.

Similarly, the minimum and maximum voltages recorded for power supply circuit are 2.504132 V and 2.504162 V, respectively. The peak-to-peak variation due to noise is 30 µV.

At room temperature under lab conditions, the accuracies of both bias and power supply voltages are better than ± 10 mV without any offset and gain calibration.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01583.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01583.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01583.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01583.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01583.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01583.

5 Related Documentation

1. Texas Instruments, *DAC80508 Octal, 16-, 14-, 12-Bit, SPI, Voltage Output DAC with Internal Reference Data Sheet*
2. Texas Instruments, *OPA2192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™ Data Sheet*
3. Texas Instruments, *TPS717xx Low-Noise, High-Bandwidth PSRR, Low-Dropout, 150-mA Linear Regulator*
4. Texas Instruments, *TIPD128 Capacitive Load Drive Solution using an Isolation Resistor Design Guide*
5. Sergio Franco, *Design With Operational Amplifiers And Analog Integrated Circuits*, McGraw-Hill
6. Texas Instruments, *Operational amplifier gain stability, Part 1: General system analysis*
7. Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis*
8. Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis*
9. TI E2E Community, *Solving Op Amp Stability Issues*

5.1 Trademarks

6 About the Authors

MIKE WANG is a field application engineer (FAE) at TI, where he has supported the video surveillance market for over 3 years, including sectors such as thermal imaging cameras, IP network cameras, video recorders, and so on. He received his master of science in mechatronic engineering at Zhejiang University in Hangzhou, Zhejiang.

SHARAD YADAV is a systems architect at Texas Instruments India, where he is responsible for developing reference design solutions for the industrial segment. Sharad has twelve years of experience in high-speed digital, mixed-signal boards, low-noise analog, and EMI/EMC protection circuit design.

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