

# 400-W GaN-Based MPPT Charge Controller and Power Optimizer Reference Design



## Description

This reference design is a Maximum Power Point Tracking (MPPT) solar charge controller for 12-V and 24-V batteries, that can be used as a power optimizer in the future. This compact reference design targets small- and medium-power solar charger designs and is capable of operating with 15- to 60-V solar panel modules, 12-V or 24-V batteries, and providing upwards of 16-A output current. The design uses a buck converter to step down the panel voltage to the battery voltage. The half-bridge power stage with internal integrated drivers is controlled by a microcontroller unit (MCU), which calculates the maximum power point using the perturb and observe method. The solar MPPT charge controller is created with real-world considerations, including reverse battery protection, software programmable alarms and indications, and surge and ESD protection.

## Resources

<a href="#">TIDA-010042</a>	Design Folder
<a href="#">LMG2100R044</a> , <a href="#">CSD18540Q5B</a>	Product Folder
<a href="#">MSPM0G1506</a> , <a href="#">TPSM365R6V5</a>	Product Folder
<a href="#">INA241</a> , <a href="#">TPS7A2033</a> , <a href="#">OPT3004</a> , <a href="#">TMP303</a>	Product Folder

## Features

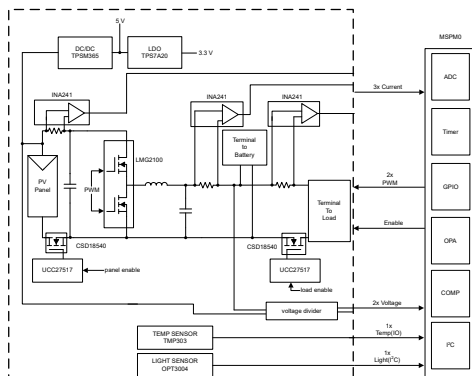
- 98.3% efficiency in 12-V systems and 98.5% efficiency in 24-V systems
- Wide input voltage range: 15 V to 60 V
- Flexible design supports 12-V and 24-V battery voltages
- High-rated output current: 16 A
- Battery reverse polarity, over-charge and over-discharge protections
- System overtemperature and ambient light detection capabilities
- Small board form factor: 95 mm × 68.2 mm × 25 mm

## Applications

- [Solar charge controller](#)
- [Solar power optimizer](#)



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## 1 System Description

This reference design is developed around TI gallium nitride (GaN) FETs with integrated gate drivers and MSPM0G1506 MCU. The design is targeted for small and medium power solar charger controller designs, capable of operating with 15- to 60-V solar panel modules and 12-V or 24-V batteries with up to 16-A output current.

The design uses the perturb-and-observe algorithm for MPPT and has an operating efficiency of greater than 98%. The high efficiency can be reached due to the half-bridge GaN FETs module with low  $R_{DS(on)}$ , low  $P_{switch}$ , and zero reverse recovery charge in the design. Usage of small sized components is made possible by the high switching frequency (up to 250 kHz) of the buck converter.

### 1.1 Key System Specifications

**Table 1-1. Key System Specifications**

PARAMETER	SPECIFICATIONS	UNIT
Input panel voltage range	15 – 60	V
Battery nominal voltage	12, 24	V
Rated maximum current	16	A
MPPT efficiency	> 98	%
Interleaved buck operating frequency	250	kHz

## 2 System Overview

### 2.1 Block Diagram

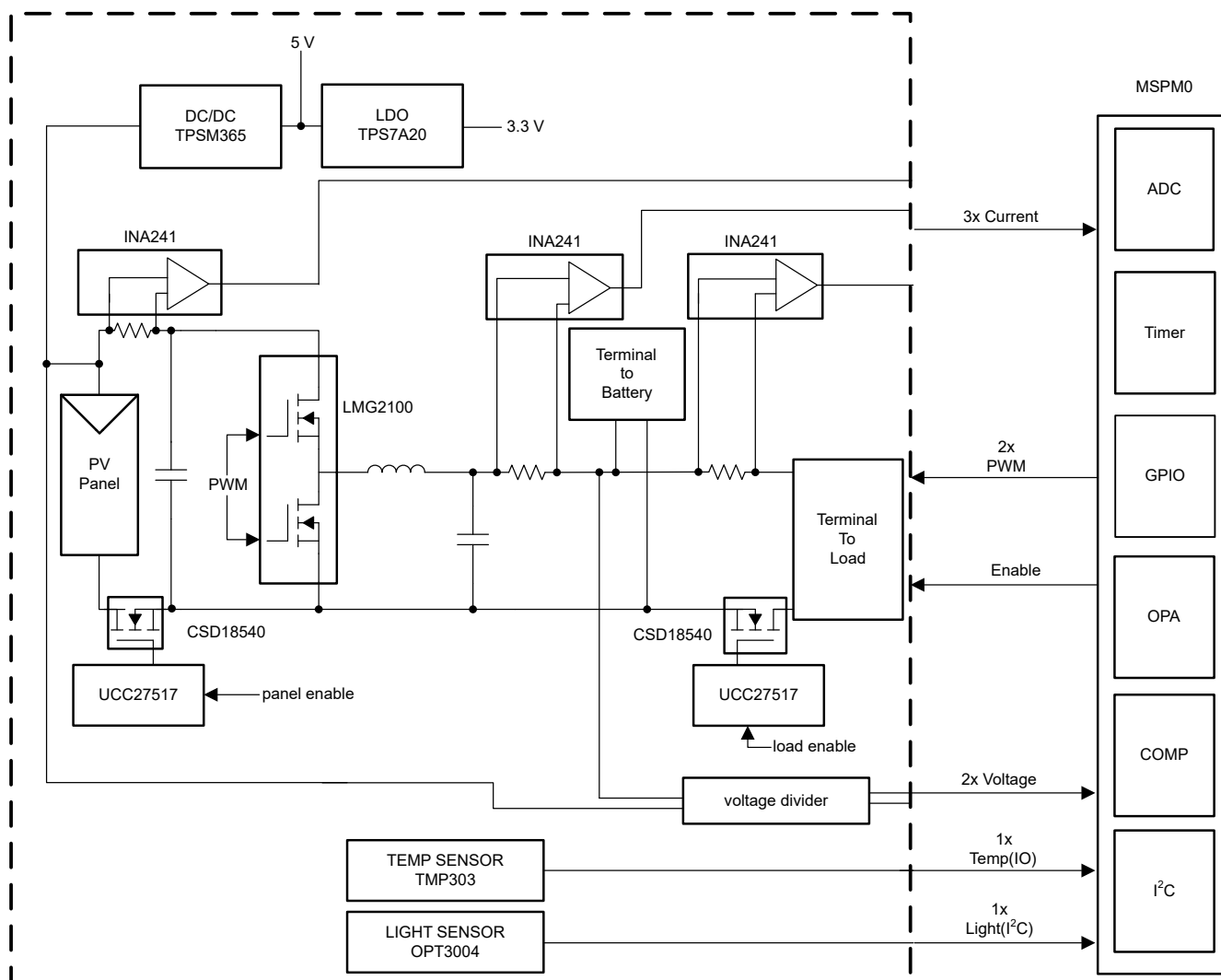


Figure 2-1. TIDA-010042 Block Diagram

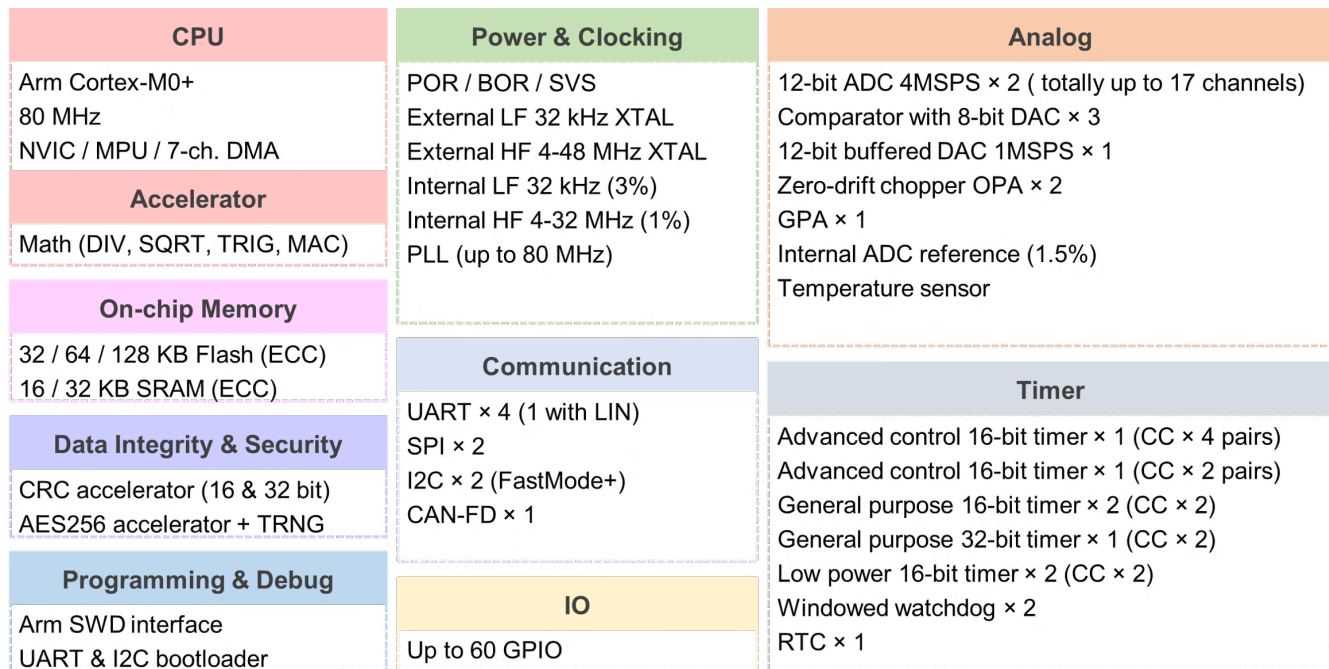
### 2.2 Design Considerations

The TIDA-010042 board consists of an MCU (MSPM0G1506) that gathers data about panel and battery voltage, as well as panel, battery, and load current and uses this information to track the maximum power point. The MCU then generates PWM signals that directly drive the half-bridge GaN module (LMG2100R044). The buck converter modulates the output voltage of the panel to maximize the transmission power or modulates the output current to prevent battery over-charge to increase the lifetime of the battery. A load enable gate (CSD18540Q5B) is also in place to protect from battery over-discharge, another means of extending the lifetime of the battery.

To power the system, a switching regulator (TPSM365R6V5) is used to step down the panel voltage to 5 V for the GaN module and gate drivers. From the 5 V, a low-dropout (LDO) regulator (TPS7A2033) is used to regulate a 3.3-V line for the rest of the components.

## 2.3 Highlighted Products

### 2.3.1 MSPM0G1506



**Figure 2-2. MSPM0G1506 Block Diagram**

The MSPM0G1506 is an 80-MHz MCU with seven timers support up to 22 PWM channels, 64KB flash, 32KB RAM, two 12-bit 4-MSPS ADC, two zero-drift zero-crossover chopper op-amps, three high-speed comparators with 8-bit reference DACs and a 12-bit 1-MSPS DAC with integrated output buffer.

- Wide supply voltage range: 1.62 V to 3.6 V
- Optimized low-power modes
  - RUN: 96  $\mu$ A/MHz (CoreMark)
  - SLEEP: 458  $\mu$ A at 4 MHz
  - STOP: 47  $\mu$ A at 32 kHz
  - STANDBY: 1.5  $\mu$ A with RTC and SRAM retention
  - SHUTDOWN: 78 nA with IO wake-up capability
- 32-Bit Cortex-M0+ platform with a holistic ultra-low-power system architecture
- Flexible Power-Management System
  - Internally regulated core supplies
  - Supply Voltage Supervision, Monitoring, and Brownout
- Clock System
  - Internal 4- to 32-MHz oscillator with up to  $\pm 1.2\%$  accuracy (SYSOSC)
  - Phase-locked loop (PLL) up to 80 MHz
  - Internal 32-kHz low-frequency oscillator (LFOSC) with  $\pm 3\%$  accuracy
  - External 4- to 48-MHz crystal oscillator (HFXT)
  - External 32-kHz crystal oscillator (LFXT)
  - External clock input
- Math accelerator supports DIV, SQRT, MAC and TRIG computations
- 7-Channel DMA controller
- Up to 60 GPIOs, Two high-drive IOs with 20-mA drive, Two 5-V tolerant IOs
- Timers
  - Two 16-bit advanced timers with deadband support up to 12 PWM channels
  - One 32-bit high-resolution general-purpose timer
  - Two 16-bit general-purpose timers support low-power operation in STANDBY mode
  - One 16-bit general-purpose timer supports QEI

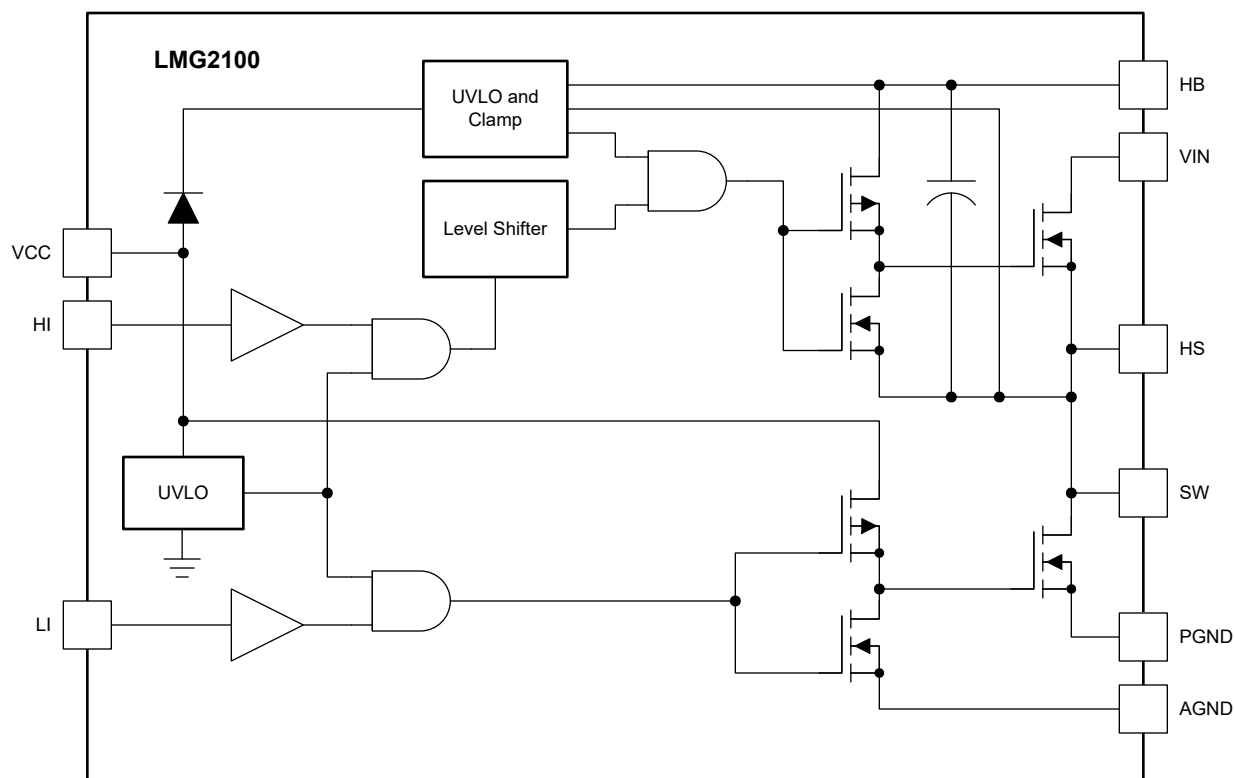
- One 16-bit general-purpose timer
- Four UART interfaces; one supports LIN, IrDA, DALI, Smart Card, Manchester, and three support low-power operation in STANDBY mode
- Two I2C interfaces support up to FM+ (1 Mbit/s), SMBus/PMBus, and wakeup from STOP mode
- Two SPIs, one SPI supports up to 32 Mbits/s
- Two simultaneous sampling 12-bit 4-Msps ADCs
  - 14-bit effective resolution at 250-ksps with hardware averaging
  - 12-bit output resolution at 4Msps with greater than 11 ENOB
  - Up to 17 total external input channels with individual result storage registers
  - Internal channels for temperature sensing, supply monitoring, and analog signal chain (interconnection with OPA, DAC, etc.)
  - Software selectable reference
  - Operates in RUN, SLEEP, and STOP modes
- Three high-speed comparators (COMP) with 8-bit reference DACs
  - Programmable hysteresis
  - Programmable reference voltage
  - Configurable operation modes
  - Programmable output glitch filter delay
  - Supports 6 blanking sources
  - Output connected to advanced timer fault handling mechanism
- Supports TI System Configuration Tool

The voltage and current of the panel and battery lines are used to calculate and track the MPP and the MSPM0G1506 enables quick data acquisition from the various analog signals using the internal analog-to-digital converter (ADC). Operating at 40 MHz allows for fast conversion and calculation to efficiently perform MPPT and adjust the duty cycle of buck converter accordingly.

During battery charging mode, the MSPM0G1506 generates pulse-width modulated (PWM) signals to the buck converter, where the duty cycle is proportional to the current output, or battery charging current, of the buck stage. The MCU is also responsible for managing the battery voltage by preventing over-charging of the battery. The MCU does this by turning the converter into constant voltage mode once a threshold voltage is reached. Additionally, the MCU protects the battery from over-discharging by disconnecting the load once a threshold load current is reached or once the battery voltage falls below another threshold. By effectively managing the battery, this reference design maximizes the lifespan and optimizes the performance capabilities.

Status indicators and alarms, controlled by the MCU, are also included in the design to provide feedback to the user; however, some are left uninitialized.

### 2.3.2 LMG2100R044



**Figure 2-3. LMG2100 Functional Block Diagram**

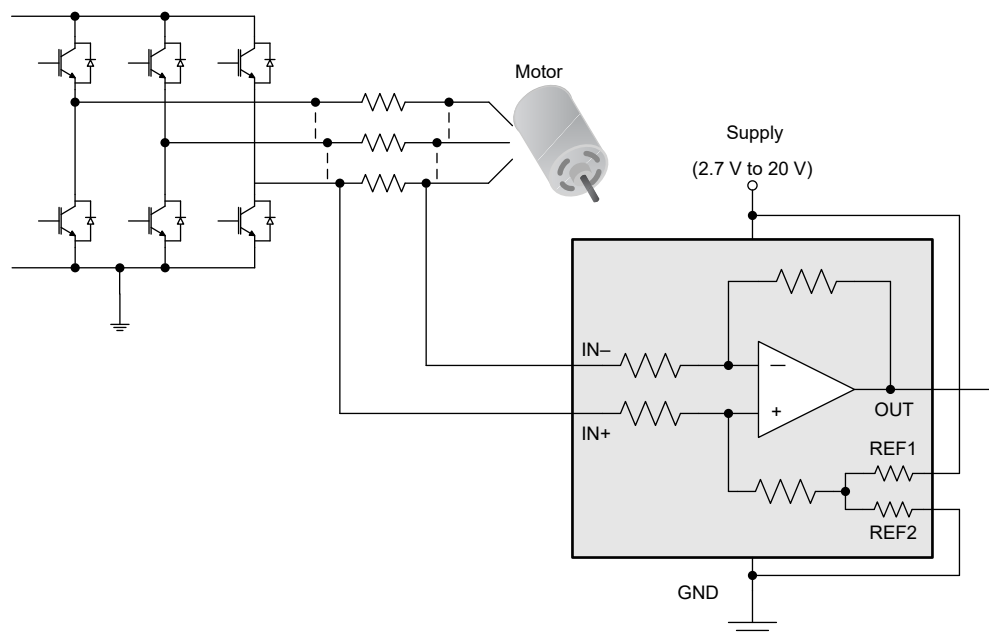
The LMG2100R044 device is an 80-V continuous, 100-V pulsed, 35-A half-bridge power stage, with integrated gate-driver and enhancement-mode Gallium Nitride (GaN) FETs, 4.4-m $\Omega$   $R_{DS(on)}$ .

- 5-V external bias power supply
- Near zero reverse recovery
- Very small input capacitance  $C_{ISS}$  and output capacitance  $C_{OSS}$
- High slew rate switching with low ringing
- Internal bootstrap supply voltage clamping to prevent GaN FET Overdrive
- Excellent propagation delay (29.5-ns typical) and matching (2-ns typical)
- Low power consumption
- Exposed top QFN package for top-side cooling
- Package optimized for easy PCB layout
- 5.5 mm  $\times$  4.5mm  $\times$  0.89 mm lead-free package

The device extends advantages of discrete GaN FETs by offering a more user-friendly interface. This device is an excellent choice for applications requiring high-frequency, high-efficiency operation in a small form factor.

The LMG2100R044, half-bridge, GaN power stage with highly integrated high-side and low-side gate drivers, which includes built-in UVLO protection circuitry and an overvoltage clamp circuitry. The clamp circuitry limits the bootstrap refresh operation to make sure that the high-side gate driver overdrive does not exceed 5.4 V. The device integrates two, 4.4-m $\Omega$  GaN FETs in a half-bridge configuration. The device can be used in many isolated and non-isolated topologies allowing very simple integration. HI and LI can be independently controlled to minimize the third quadrant conduction of the low-side FET for hard switched buck converters. The package is designed to minimize the loop inductance while keeping the PCB design simple. TI recommends a size of 0402 to minimize trace length to the pin. Place the bypass and bootstrap capacitors as close as possible to the device to minimize parasitic inductance. The drive strengths for turn on and turn off are optimized to provide high-voltage slew rates without causing any excessive ringing on the gate or power loop.

### 2.3.3 INA241



**Figure 2-4. INA241 Example Application**

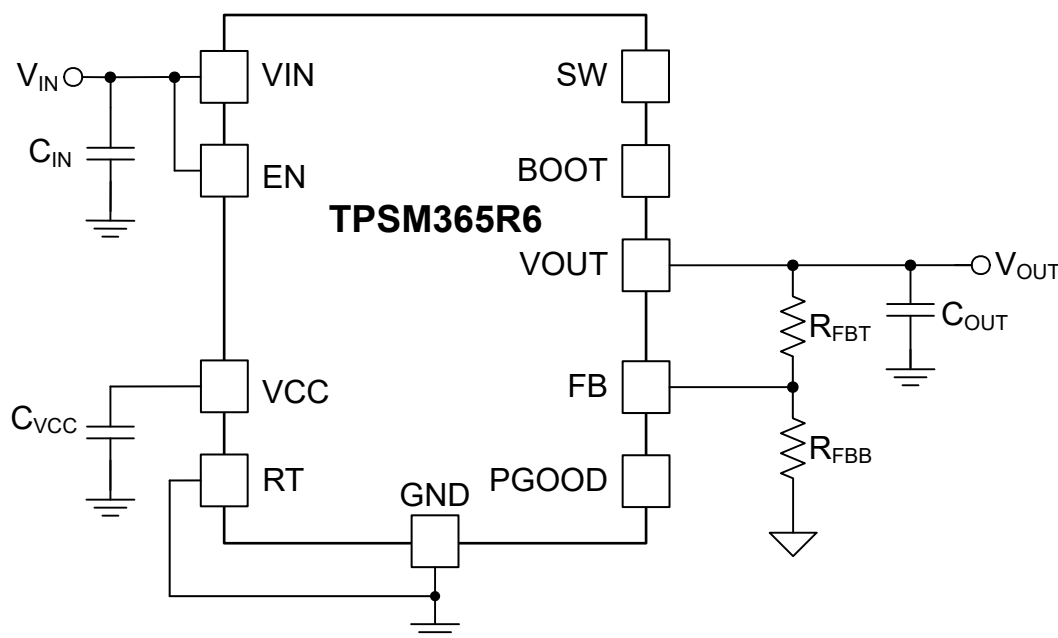
The INA241 is an 110 V, zero-drift current sense amplifier with enhanced PWM rejection.

- Enhanced PWM Rejection
- Excellent CMRR:
  - 166-dB DC CMRR
  - 104-dB AC CMRR at 100 kHz
- Wide Common-Mode Range: –5 V to 110 V
- Accuracy:
  - Gain:
    - Version A:  $\pm 0.01\%$ ,  $\pm 1$  ppm/ $^{\circ}\text{C}$  drift (Maximum)
    - Version B:  $\pm 0.1\%$ ,  $\pm 5$  ppm/ $^{\circ}\text{C}$  drift (Maximum)
  - Offset:
    - Version A:  $\pm 10$   $\mu\text{V}$ ,  $\pm 0.1$   $\mu\text{V}/^{\circ}\text{C}$  drift (Maximum)
    - Version B:  $\pm 150$   $\mu\text{V}$ ,  $\pm 0.5$   $\mu\text{V}/^{\circ}\text{C}$  drift (Maximum)
- Available Gains:
  - INA241A1, INA241B1 : 10 V/V
  - INA241A2, INA241B2 : 20 V/V
  - INA241A3, INA241B3 : 50 V/V
  - INA241A4, INA241B4 : 100 V/V
  - INA241A5, INA241B5 : 200 V/V
- Quiescent Current: 3.2 mA (Maximum)

The high common mode voltage (110 V) allows for support of various battery systems without sacrificing accuracy and the negative common mode voltage (–5 V) allows the device to operate below ground to accommodate flyback.

The INA241 device is offered with 5 preset gain values of 10-, 20-, 50-, 100-, and 200 V/V with a maximum gain error of 0.1%. With support for a maximum system current of 16 A, the A3 (50-V/V gain) variation is used in this design to maximize current reading resolution and minimize power dissipation through the shunt resistor.

### 2.3.4 TPSM365



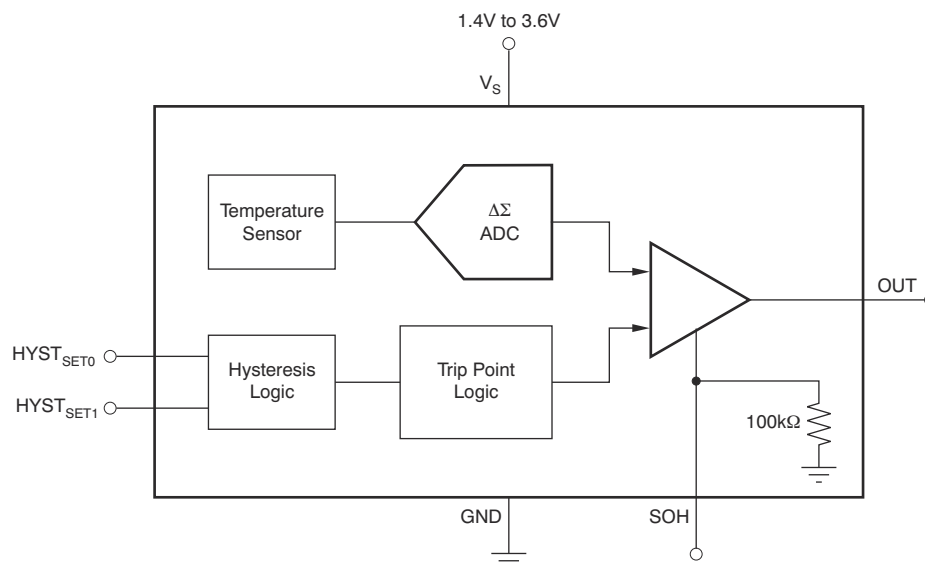
**Figure 2-5. TPSM365 Example Circuit**

The TPSM365 device is a 65-V, 600-mA or 300-mA peak synchronous buck converter power module.

- Integrated MOSFETs, inductor, and controller
- Wide input voltage range: 3 V to 65 V, input transient up to 70 V
- 4.5-mm × 3.5-mm × 2-mm over-molded package
- Frequency adjustable from 200 kHz to 2.2 MHz using the RT pin or an external SYNC signal
- Greater than 85% efficiency at 24 V<sub>IN</sub>, 5-V<sub>OUT</sub>
- Ultra-low operating quiescent current at no load: 4 μA at V<sub>IN</sub> = 24 V to 3.3-V V<sub>OUT</sub>
- Optimized for ultra-low EMI requirements
  - Pseudo-random spread spectrum reduces peak emissions
  - Pin selectable FPWM mode for constant frequency at light loads with MODE/SYNC pin
  - FSW synchronization with MODE/SYNC pin
  - CISPR11 class B capable
- Inherent protection features for robust design
  - Precision enable input and open-drain PGOOD indicator for sequencing, control, and VIN UVLO
  - Overcurrent and thermal shutdown protections



### 2.3.5 TMP303

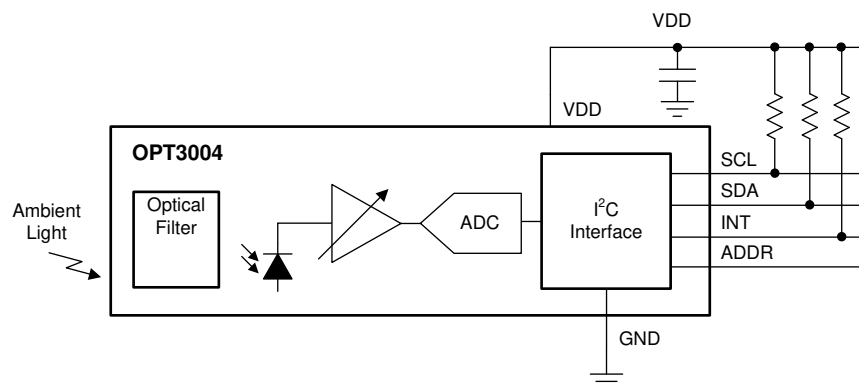


**Figure 2-6. TMP303 Block Diagram**

The TMP303 device is a factory-programmed temperature window comparator.

- Low Power: 5-μA (Maximum)
- SOT-563 Package: 1.60 mm × 1.60 mm × 0.6 mm
- Trip Point Accuracy:
  - ±0.2°C (Typical) from –40°C to 125°C
- Push-Pull Output
- Selectable Hysteresis: 1-, 2-, 5-, 10°C
- Supply Voltage Range: 1.4 V to 3.6 V

### 2.3.6 OPT3004



**Figure 2-7. OPT3004 Block Diagram**

The OPT3004 is a digital ambient light sensor (ALS) with high-precision human-eye response.

- Precision optical filtering to match human eye:
  - Rejects > 99% (typ) of IR
- Automatic full-scale setting feature simplifies software and provides proper configuration
- Measurements: 0.01-lux to 83-k lux
- 23-Bit Effective Dynamic Range With Automatic Gain Ranging
- 12 Binary-Weighted Full-Scale Range Settings: < 0.2% (typ) Matching Between Ranges
- Low operating current: 1.8 μA (typ)
- Operating temperature range: –40°C to +85°C

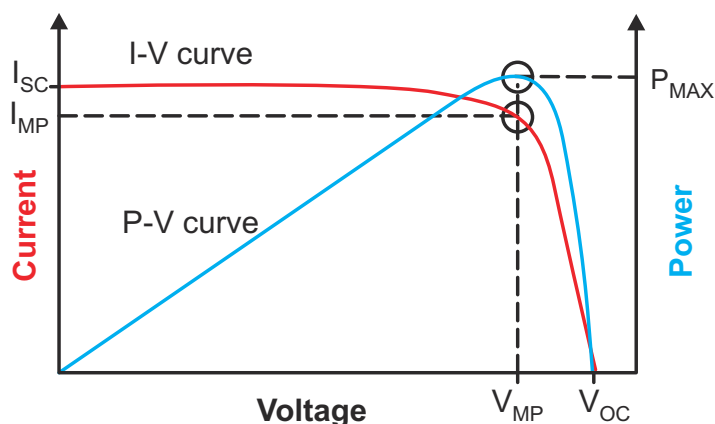
- Wide Power-Supply Range: 1.6 V to 3.6 V
- 5.5-V tolerant I/O
- Flexible Interrupt System
- Small-form factor:
  - 2 mm × 2 mm × 0.65 mm for USON package
  - 2.1 mm × 1.9 mm × 0.6 mm for SOT-5X3 package

## 2.4 System Design Theory

### 2.4.1 MPPT Operation

The power output from a PV panel depends on a few parameters, such as the irradiation received by the panel voltage, panel temperature, and so forth. The power output also varies continuously throughout the day as the conditions affecting the change.

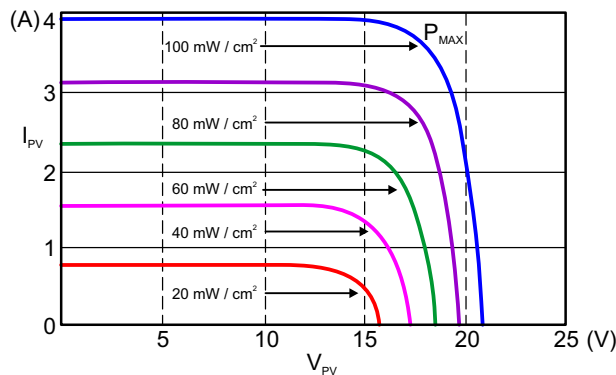
Figure 2-8 shows the I-V curve and the P-V curve of a solar panel. The I-V curve represents the relationship between the panel output current and the output voltage. As the I-V curve in the figure shows, the panel current is at the maximum when the terminals are shorted and is at the lowest when the terminals are open and unloaded.



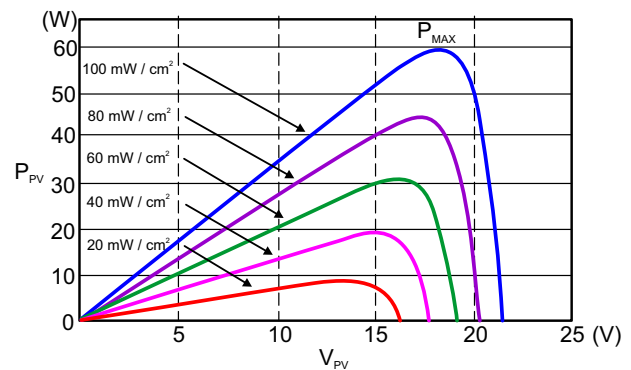
**Figure 2-8. Solar Panel Characteristics I-V and P-V Curves**

As Figure 2-8 shows, obtain the maximum power output from the panel represented as  $P_{MAX}$  at a point when the product of the panel voltage and the panel current is at the maximum. This point is designated as the maximum power point (MPP).

The graphs in Figure 2-9 and Figure 2-10 show examples of how each of the various parameters affect the output power from the solar panel. The graphs also show the variation in the power output of a solar panel as a function of irradiance. Observe in these graphs how the power output from a solar panel increases with the increase in irradiance and decreases with a decrease in irradiance. Also note that the panel voltage at which the MPP occurs also shifts with the change in irradiance.

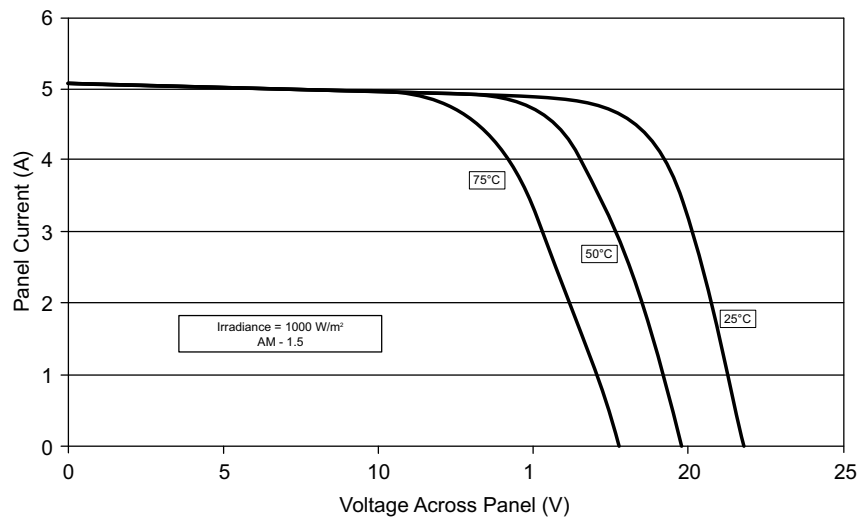


**Figure 2-9. Solar Panel Output Power Variation Under Different Irradiation Conditions—Graph A**



**Figure 2-10. Solar Panel Output Power Variation Under Different Irradiation Conditions—Graph B**

Figure 2-11 shows a typical graph representing the variation in the power output of a photovoltaic panel as a function of the temperature. Observe how the panel current (and thereby the panel power) decreases with an increase in temperature. The MPP voltage continues to shift substantially with the change in temperature.



**Figure 2-11. Solar Panel I-V Curve Variation With Temperature Under Constant Irradiation Conditions**

Draw the maximum power from a solar panel by operating the panel close to the MPP point; however, doing so poses two challenges:

1. Providing a way to connect a battery or load with a different operating voltage in comparison to the MPP of the panel
2. Identifying the MPP automatically, as the MPP varies with the environmental conditions and is not a constant

Directly connecting a solar panel with a  $V_{MPP}$  close to 17 V to a 12-V lead acid battery forces the panel to operate at 12 V, which reduces the amount of power that can be drawn from the panel. From this situation, it can be surmised that a DC/DC converter is able to draw more power from the solar panel because this converter forces the solar panel to operate close to the  $V_{MPP}$  and transfer the power to a 12-V lead acid battery (impedance matching).

The preceding paragraph explains why the user implements a synchronous buck converter to charge the lead acid battery from the solar panel and address the first challenge.

The second challenge of automatically identifying the MPP of the panel is typically performed by employing MPPT algorithms in the system. The MPPT algorithm tries to operate the photovoltaic panel at the maximum power point and uses a switching power stage to supply the load with the power extracted from the panel.

Perturb and observe is one of the most popular MPPT algorithms used. The fundamental principle behind this algorithm is simple and easy to implement in a microcontroller based system. The process involves slightly increasing or decreasing (perturbing) the operating voltage of a panel. Perturbing the panel voltage is accomplished by changing the duty cycle of the converter. Assuming that the panel voltage has been slightly increased and that this leads to an increase in the panel power, then another perturbation in the same direction is performed. If the increase in the panel voltage decreases the panel power, then a perturbation in the negative direction is done to slightly lower the panel voltage.

By performing the perturbations and observing the power output, the system begins to operate close to the MPP of the panel with slight oscillations around the MPP. The size of the perturbations determines how close the system is operating to the MPP. Occasionally this algorithm can become stuck in the local maxima instead of the global maxima, but this problem can be solved with minor tweaks to the algorithm.

The P&O algorithm is easy to implement and effective, and was chosen for this design.

## 2.4.2 Buck Converter

**Table 2-1. Buck Converter Design Criteria**

PARAMETER	SPECIFICATION
Maximum input voltage	60 V
Maximum output voltage	24 V
Max current	16 A

This reference design implements buck topology to step down panel voltage to battery voltage, so it is used in applications where panel voltage must be higher than battery voltage.

The LMG2100R044 half-bridge power stage is selected for this reference design for the high maximum  $V_{DS}$  of 80-V continuous, 100-V pulsed rating and low  $Q_g$  and  $R_{DS(on)}$  of 7.2 nC and 4.4 m $\Omega$ , respectively, at a gate voltage of 5 V, also, the 5.5 mm  $\times$  4.5mm  $\times$  0.89 mm lead-free package, with integrated gate driver, saves a lot PCB area, so it is a suitable design for a compact, high power density and high efficiency buck converter of medium power rating.

### 2.4.2.1 Output Inductance

Continuous conduction mode (CCM) is desired to maintain a high efficiency while delivering the constant current required for battery charging. When the input voltage range, output voltage and load current are defined, it leaves the inductor value as the design parameter to maintain CCM.

Therefore, the desired ripple current is defined. A typical value is 0.2 to 0.4 times the output current. Firstly, the loop speed in PV system is not that fast, so the value of inductance can be higher. Secondly, it is important to reduce the ripple voltage of the output capacitor. Finally, the size of inductor cannot be too big. So, 0.3 is selected as the coefficient of ripple current.

Considering 16-A maximum output current, and ignoring the voltage drop on the FETs and resistance of the inductor, giving:

$$L \times \frac{\Delta I}{T_{OFF}} = V_O \quad (1)$$

The worst case of CCM for a fixed output voltage converter is when  $T_{off}$  is maximum, also, the bigger the value of inductor is, the easier the converter stays in CCM, then the equation above can be transformed into:

$$L \geq \frac{V_O \times \left(1 - \frac{V_O}{V_{in\_max}}\right)}{\Delta I \times f_{sw}} \quad (2)$$

In this application,  $V_{in\_max}$  is 60 V,  $f_{sw}$  is the switching frequency 250 kHz. When the output voltage is 24 V, the inductance needs to be higher than 12  $\mu$ H. When the output voltage is 12 V, the inductance needs to be higher than 8  $\mu$ H. In the case of the same size, an inductor with a smaller inductance can have a larger saturation current. Finally, 10  $\mu$ H is chosen as the value of the inductance.

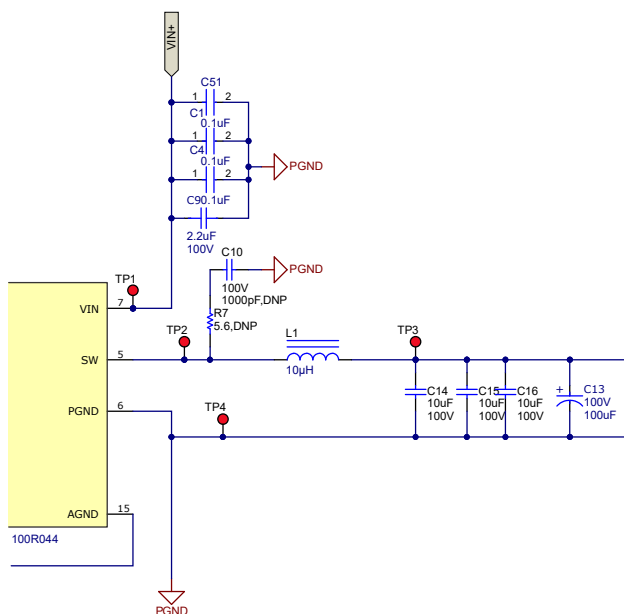


Figure 2-12. Power Stage Schematic

#### 2.4.2.2 Input Capacitance

Select input capacitors carefully to both reduce the size and satisfy the big ripple current capability (for more information, see the [How to select input capacitors for a buck converter](#) analog applications journal).

To get a satisfied MPPT effect, such as 99.5% of maximum power tracking, make sure the input ripple voltage is small. For many panels, when the  $V_{\text{panel}}$  is within 97.5% – 102.5% of the  $V_{\text{mpp}}$ , the output power of the panel is above 99.5% of maximum power. In a 12-V battery system, make sure the  $V_{\text{mpp}}$  of the panel is higher than 12 V, so the input ripple voltage can be within 0.3 V. In a 24-V battery system, make sure the  $V_{\text{mpp}}$  of the panel is higher than 24 V, so the input ripple voltage can be within 0.6 V. So, 0.3 V is taken as the maximum input ripple voltage ( $\Delta V_{\text{in}}$ ).

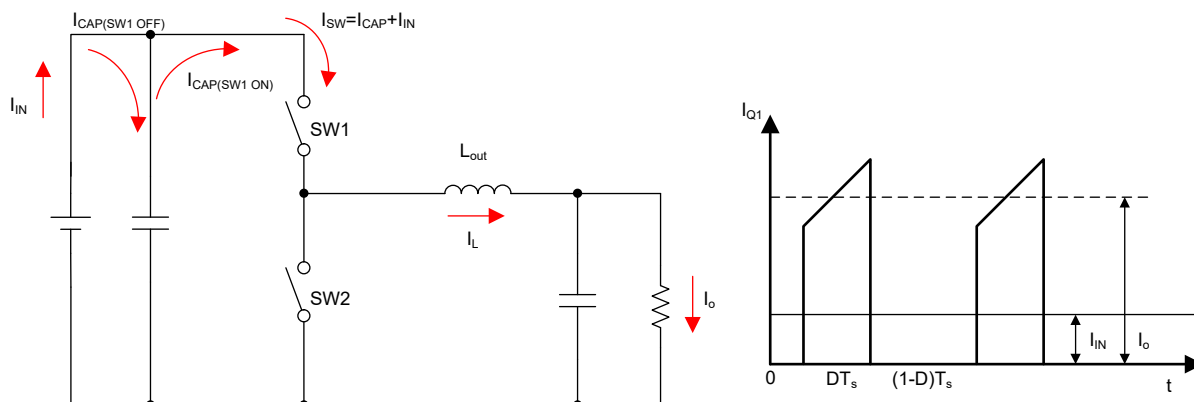


Figure 2-13. Input Current Waveform

The AC current flowing through the input capacitors results in the input voltage ripple. Even the majority of the ripple current goes through MLCC, thanks to the low equivalent series resistance (ESR), ripple voltage results from this can be ignored. The remaining ripple current flows through the electrolytic capacitor, if there is any in the system. Although electrolytic capacitor has much bigger ESR, the AC current is relatively small. As a result, the overall effect on the input voltage ripple is negligible.

Use Equation 3 to estimate the required effective capacitance that meet the ripple voltage requirement. At 50% duty cycle, the  $C_{\text{IN}}$  is biggest.

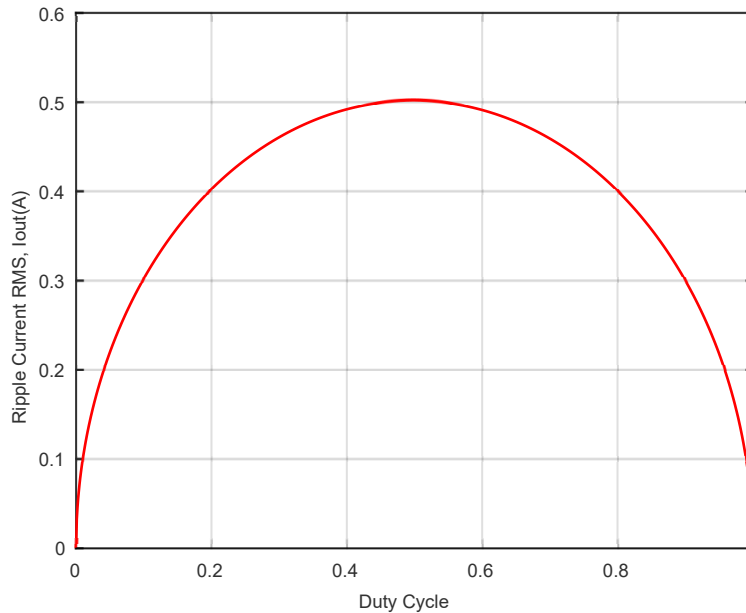
$$C_{IN} \geq \frac{D \times (1 - D) \times I_O}{\Delta V_{in} \times f_{sw}} \quad (3)$$

Where  $I_O$  is 16 A and  $f_{sw}$  is 250 kHz,  $C_{IN}$  needs to be bigger than 53  $\mu$ F. Considering the decay of the capacitance of the MLCC as the voltage increases, the actual value taken needs to be larger depending on the practical situation.

Besides, the input capacitors also need to meet the thermal stress caused by the ripple current, the bigger footprint, the lower temperature rise. Use Equation 4 to calculate the root mean square (RMS) current of the input ripple current.

$$I_{in\_rms} = I_O \times \sqrt{D \times (1 - D) + \frac{1}{12} \times \left( \frac{V_O}{L \times f_{sw} \times I_O} \right)^2 \times (1 - D)^2 \times D} \quad (4)$$

Duty cycle has a significant impact on the input RMS ripple current. Figure 2-14 is a plot of Equation 4, from which the largest ripple current RMS can be observed. The largest ripple current occurs when the duty cycle is 0.5. The maximum value of  $I_{in\_rms}$  is 8.2 A. To reduce the temperature rise of the MLCC, the 1210 footprint is chosen. Meanwhile, it is better to parallel multiple capacitors with small capacity than just use one with bigger capacity.



**Figure 2-14. Input RMS, Load Current Ratio vs Duty Cycle**

Place additional small MLCCs with low equivalent series inductance (ESL) and low ESR as close as possible to the input side of the FETs, especially using GaN devices with high  $di/dt$  and  $dv/dt$  slope. These MLCCs can greatly alleviate overshoot of the switching node waveform without sacrificing efficiency.

Bulk capacitors like aluminum electrolytic capacitors can also be added to satisfy the transient response if the response speed of the system is important. Because of the high ESR of electrolytic capacitors, the ripple current can be approximated by dividing the input ripple voltage by the ESR. Also, the waveform is triangular, so the RMS value can be estimated with Equation 5.

$$I_{bulk\_rms} = \frac{1}{2\sqrt{3}} \times \frac{\Delta V_{in}}{ESR} \quad (5)$$

Take care to select bulk capacitors for the low RMS current tolerance.

### 2.4.3 Current Sense Amplifier

**Table 2-2. Current Sense Amplifier Design Criteria**

PARAMETER	SPECIFICATION
Maximum common-mode voltage	60 V
Maximum input current	16 A
Maximum output voltage	3.3 V

This reference design requires accurate measurement of the panel and battery currents to calculate and track the maximum power point. The design supports panels of up to 60 V for 24-V battery systems, so a maximum common-mode voltage of at least 60 V is required. The design also requires a negative common-mode voltage to provide function during periods of flyback.

The INA241 is selected for this reference design. The best gain variation must be chosen, as higher gain amplifiers often have increased error and noise parameters, and paired with a shunt resistor that provides high resolution and low power dissipation. Because of the  $\pm 0.01\%$  gain error (maximum) and  $\pm 1\text{ppm}/^\circ\text{C}$  drift, the current sample error is very small. The following equations are used to calculate the resolution of the current sense amplifier and power dissipation of the shunt resistor for the parameters given in Table 2-2, examples follow.

#### 2.4.3.1 Shunt Resistor Selection

The minimum shunt resistor value for a 50-V/V gain amplifier is given by:

$$V_{\text{OUT}} = 3.3 \text{ V} > R_{\text{SHUNT}} \times (I_{\text{MAX}} \times \text{Gain}) = R_{\text{SHUNT}} \times (16 \text{ A} \times 50 \text{ V/V}) \quad (6)$$

So,  $R_{\text{SHUNT}} \leq 4.125 \text{ m}\Omega$ ; since a lower power dissipation is a higher priority, an  $R_{\text{SHUNT}} = 2 \text{ m}\Omega$  is selected for the design.

#### 2.4.3.2 Current Measurement Resolution

The current resolution of the amplifier into a 12-bit ADC is given by:

$$I_{\text{RES}} = (V_{\text{OUT}} / (\text{ADCMAX} \times R_{\text{SHUNT}} \times \text{Gain})) = (3.3 \text{ V} / (4095 \times 2 \text{ m}\Omega \times 50 \text{ V/V})) \quad (7)$$

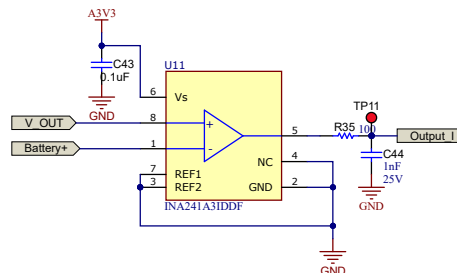
So,  $I_{\text{RES}} = 8.06 \text{ mA}$  per bit.

#### 2.4.3.3 Shunt Resistor Power Dissipation

The maximum power dissipation is given by:

$$P_{\text{DISS}} = I_{\text{MAX}}^2 \times R_{\text{SHUNT}} = (16 \text{ A})^2 \times 2 \text{ m}\Omega \quad (8)$$

So,  $P_{\text{DISS}} = 0.512 \text{ W}$ .



**Figure 2-15. Shunt Amplifier Schematic**

## 2.4.4 Switching Regulator

**Table 2-3. Switching Regulator Design Criteria**

PARAMETER	SPECIFICATION
Input voltage range	10 V to 60 V
Output voltage	5 V
Load current	600 mA

This reference design requires 5 V for the gate drivers (UCC27517 device) and GaN device (the LMG2100R044), subsequently stepped down to 3.3 V for the MSPM0G1506 device and other components, to operate. To generate the 5-V line from the power lines (panel), a wide  $V_{IN}$  buck, switching regulator is needed to support a maximum panel voltage of 60 V.

The TPSM365R6V5 device is a 5-V fixed output, wide  $V_{IN}$ , frequency adjustable buck regulator with integrated inductor and boot capacitor that provides cost effective, compact, and highly-efficient power conversion design. See the *Application and Implementation* section of the [TPSM365R6, TPSM365R3 3-V to 65-V Input, 600-mA/300-mA, 4- \$\mu\$ A No-Load IQ Synchronous Buck Converter Power Module in a HotRod™ QFN Package](#) as a starting point for this design; however, an input below 12 V was not supported during testing.



## 3 Hardware, Software, Testing Requirements, and Test Results

### 3.1 Required Hardware and Software

#### 3.1.1 Hardware

##### 3.1.1.1 TIDA-010042

Figure 3-1 and Figure 3-2 show the full design boards, with the bare PCB measuring at 95 mm × 68.2 mm.

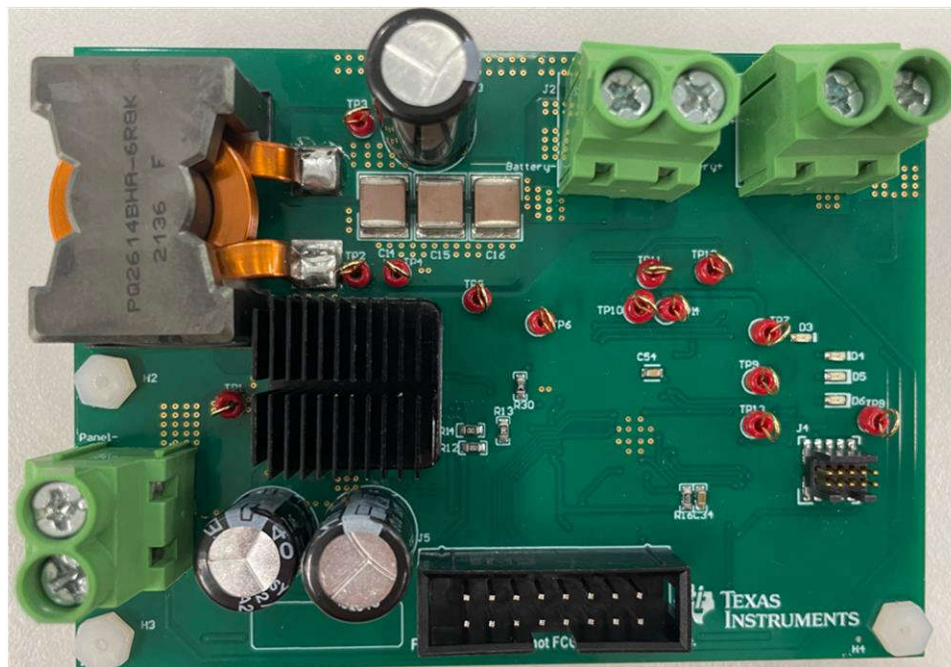


Figure 3-1. TIDA-010042 Top View

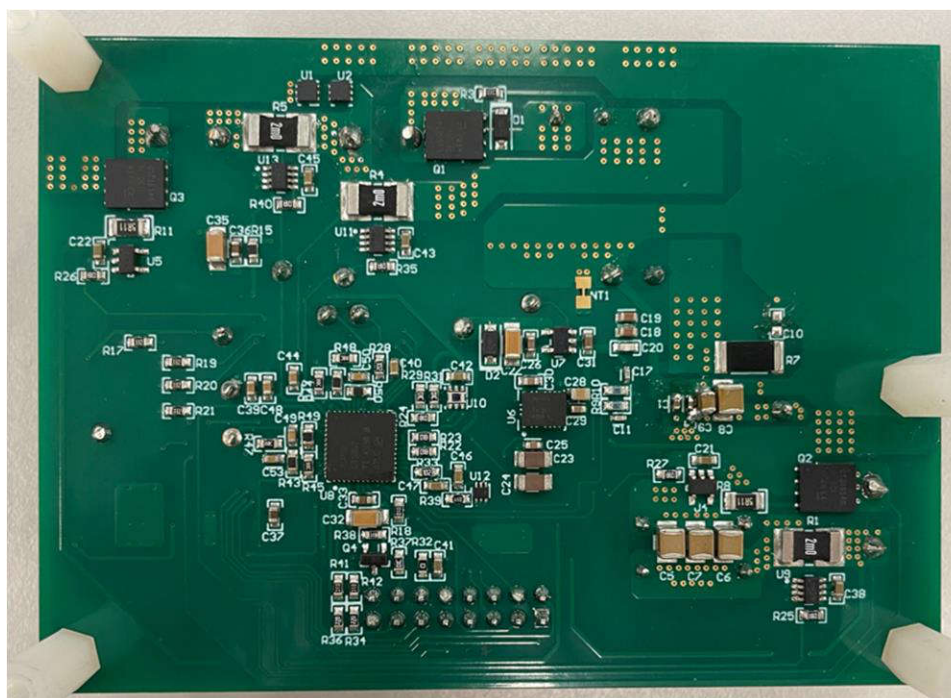


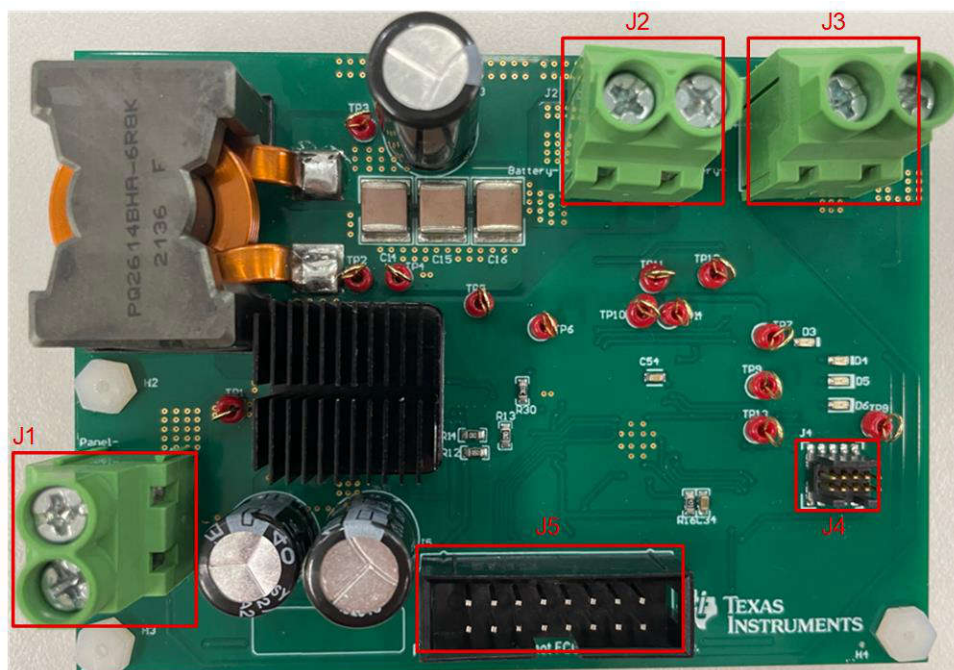
Figure 3-2. TIDA-010042 Bottom View

Table 3-1 breaks out the various headers and their associated pin connections.

J1, J2, and J3 are the PV panel, battery, and load connections, respectively.

J4 is used for XDS110 debugger.

J5 can be configured to communicate with power line communication (PLC) board in the future.



**Figure 3-3. TIDA-010042 Board Headers**

**Table 3-1. Headers Connections**

DESIGNATOR	PIN NUMBER	SIGNAL
J1 – PV panel connection	1	Negative panel (P–) terminal
	2	Positive panel (P+) terminal
J2 – battery connection	1	Positive battery (B+) terminal
	2	Negative battery (B–) terminal
J3 – load connection	1	Negative load (L–) terminal
	2	Positive load (L+) terminal
J4 – programming header	1	XDS110 Programmer voltage
	2	XDS110 SWDIO
	3	GROUND
	4	XDS110 SWCLK
	5	GROUND
	6	FLOAT
	7	GROUND
	8	FLOAT
	9	GROUND
	10	XDS110 RST

**Table 3-1. Headers Connections (continued)**

DESIGNATOR	PIN NUMBER	SIGNAL
J5 – PLC connection	1	PLC1
	2	PLC2
	3	PLC3
	4	PLC4
	5	PLC5
	6	PLC6
	7	PLC7
	8	PLC8
	9	PLC9
	10	PLC10
	11	UART_TX
	12	POWER 3.3V
	13	UART_RX
	14	Buzzer output
	15	GROUND
	16	GROUND

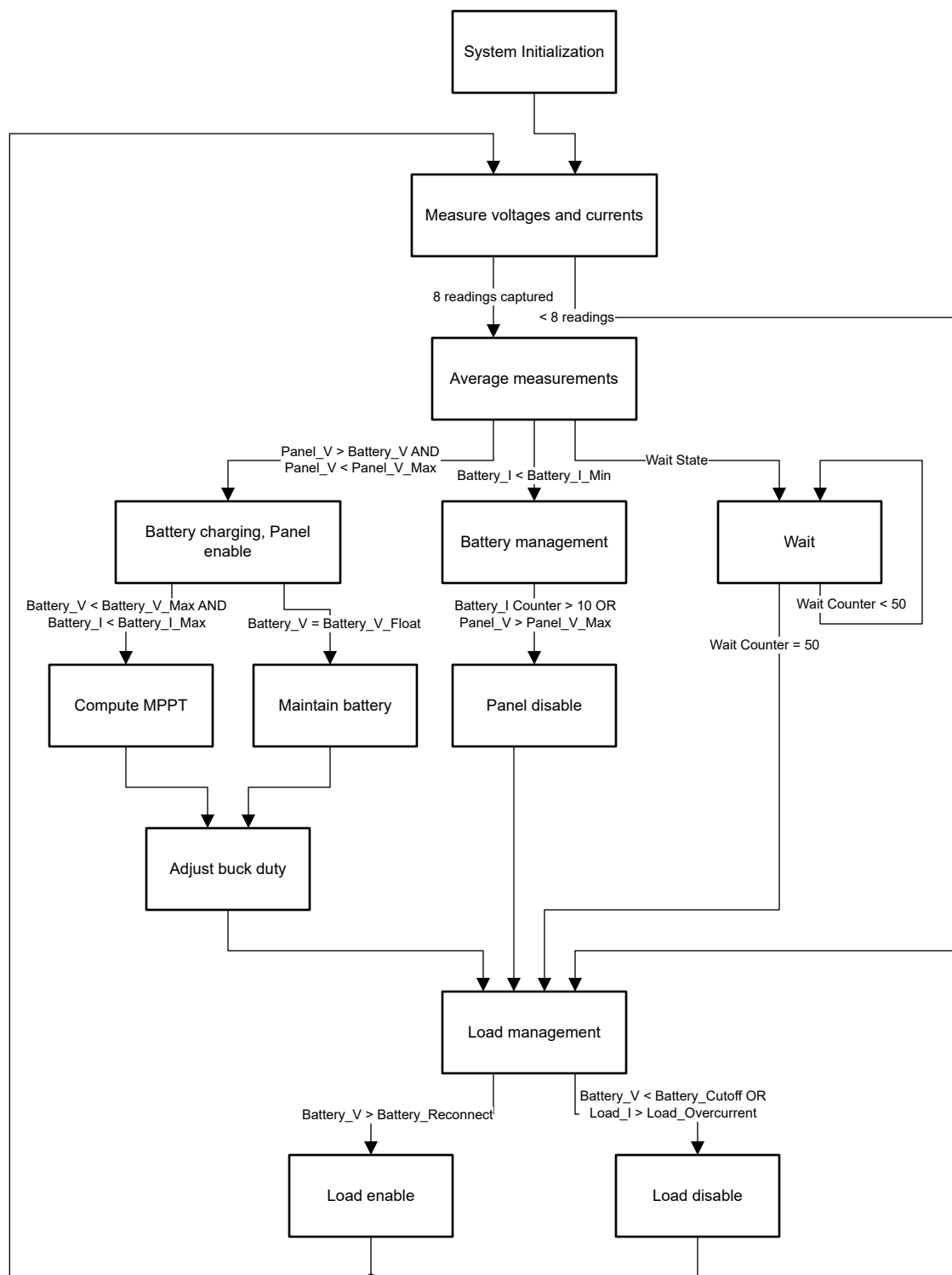
### 3.1.1.2 ITECH-IT6724H

The ITECH auto range DC power supply 1500-W DC programmable power supplies series gives the sufficient output power for testing the board, since the supply offers output voltages up to 300 V or 10 A. See [Wide Range High-Voltage Programmable DC Power Supply – Welcome to ITECH \(itechate.com\)](#) for more information.

### 3.1.1.3 Chroma, 63107A

Chroma 63107A series is used in the following measurements to draw power from the system. The single input electronic load is specified up to 250 W. See [Modular DC Electronic Load LED Simulator > Chroma \(chromausa.com\)](#) for more information.

### 3.1.2 Software



**Figure 3-4. TIDA-010042 Software Flow**

After initializing peripherals like the ADCs, GPIOs, the OPAs, the comparator and the timers, the value of the voltage and current measurements are read, as long as there are under 8 reading times. Otherwise, the software jumps to the Load management function.

Furthermore, the values get averaged and dependent on the input value the Battery Charging function, the Battery management function or a Wait State starts. The Battery Charging function enables the Panel, the Buck converter, calculates an MPP and sets the duty cycle for the Buck converter. The Battery management part disables the Panel, Buck Converter and continues with a waiting state. The Wait State lasts 4 seconds and is checking the input parameters.

To prevent from over discharging, the previous three functions are all followed by Load Management, which is able to control the load connection.

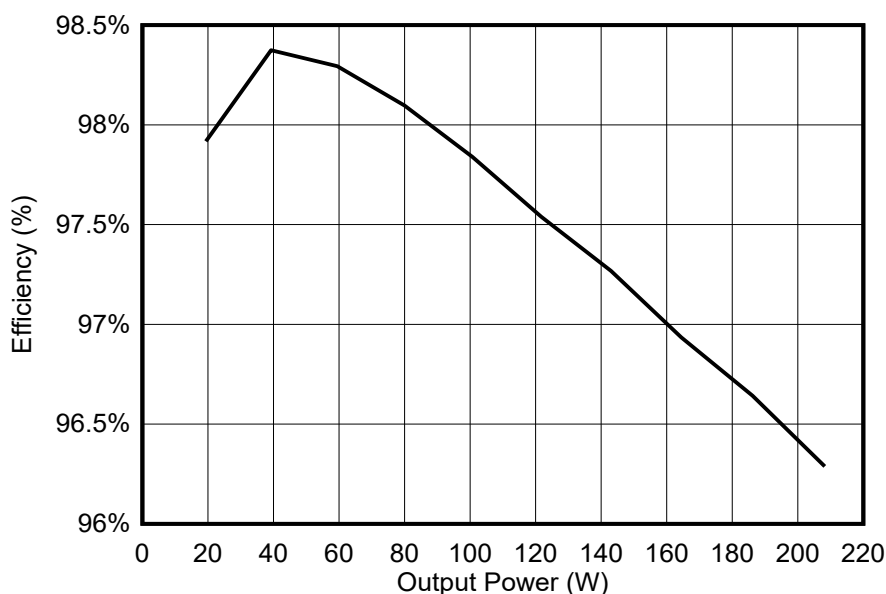
## 3.2 Testing and Results

### 3.2.1 Test Setup

Connect the DC voltage source, to the panel connection (J1). Set the input voltage ranges from 15 V to 22 V for 12-V systems and from 30 V to 44 V for 24-V systems.

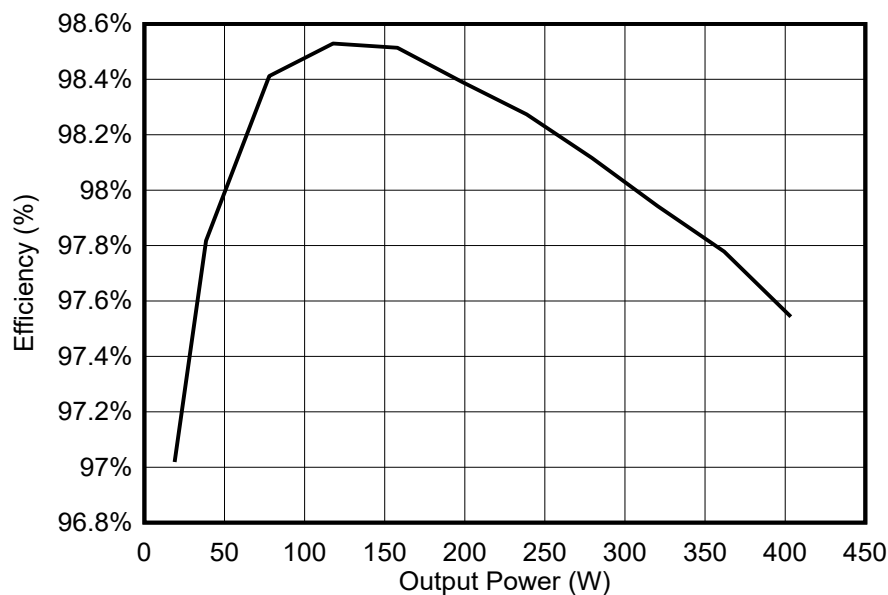
Connect the battery or electronic load to the battery connection (J2). This reference design supports 12-V, 24-V batteries. If using an electronic load to simulate a battery, set the load to constant voltage mode (CV) and to the respective voltage system regulates the voltage itself. A 1 W (5 V, 0.2 A) fan was used to cool the heat sink and PCB.

### 3.2.2 Test Results

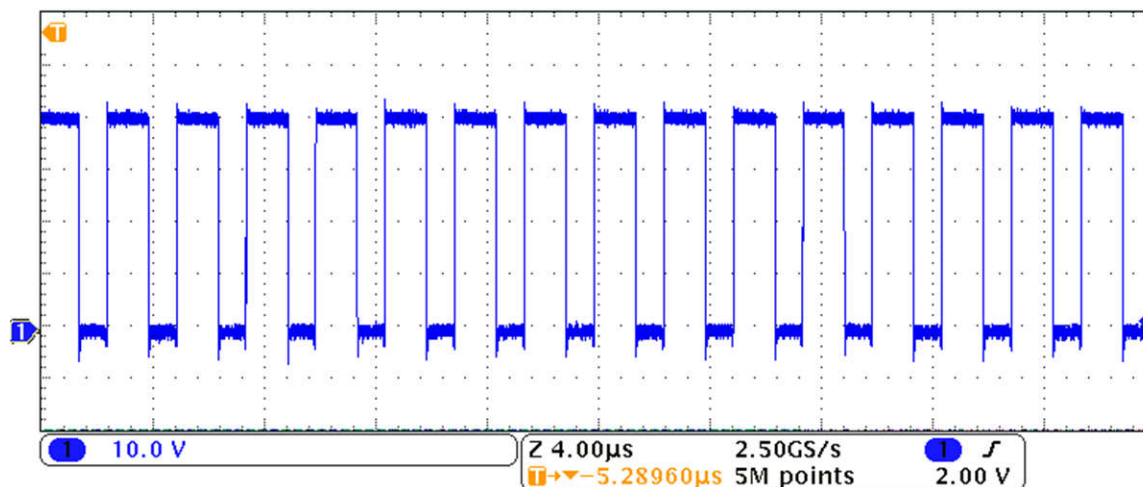


**Figure 3-5. Efficiency Curve Over Output Power for the 12-V System**

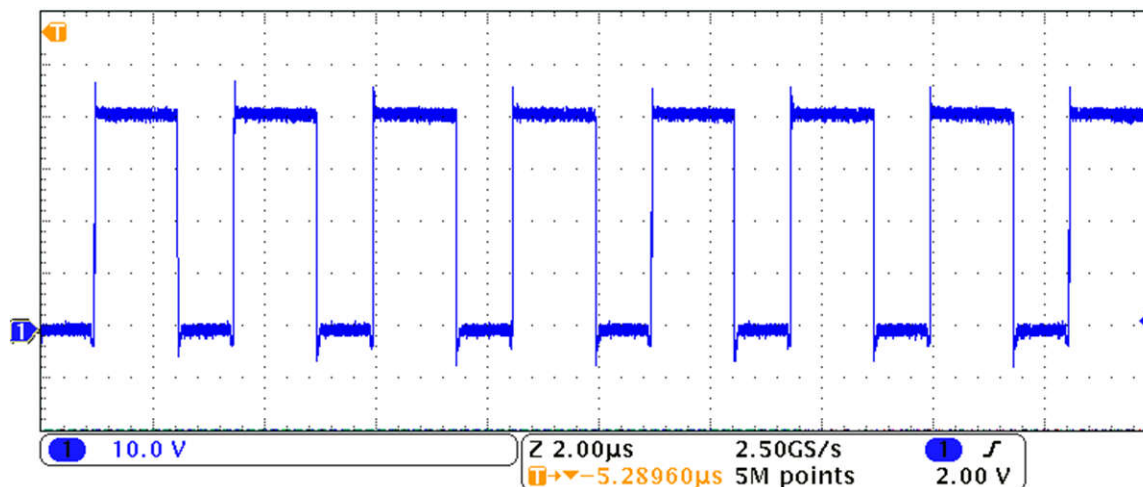




**Figure 3-6. Efficiency Curve Over Output Power for the 24-V System**



**Figure 3-7. Switch Nodes at 40-V Input; 24 V, 5-A Output**



**Figure 3-8. Switch Nodes at 40-V Input; 24 V, 10-A Output**

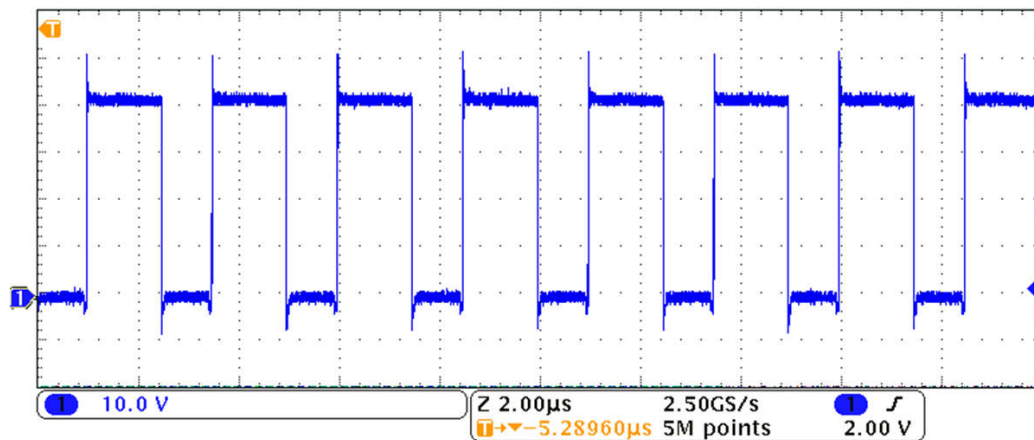


Figure 3-9. Switch Nodes at 40-V Input; 24 V, 16-A Output

Figure 3-10 shows the battery current, battery voltage, panel current, and panel voltage at 400-W output power.

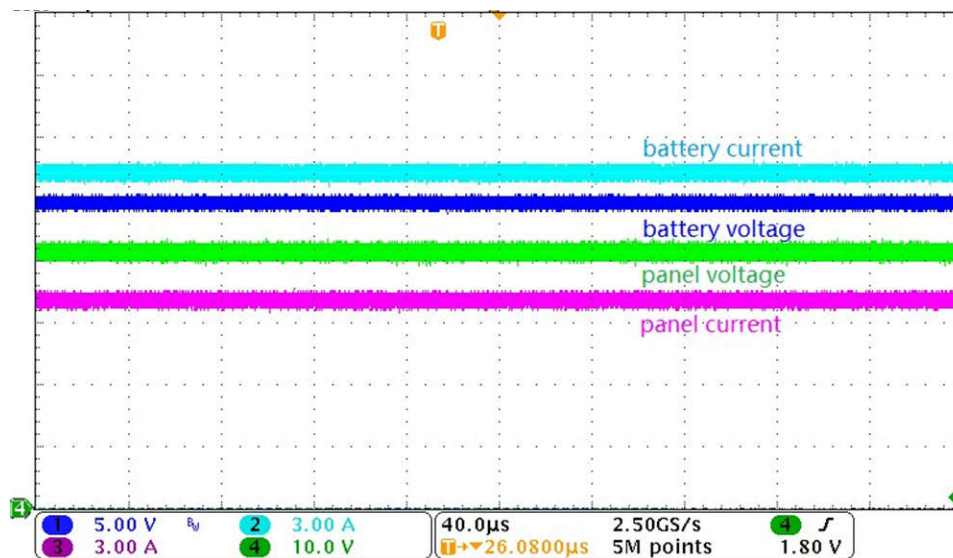


Figure 3-10. Battery Current, Battery Voltage, Panel Current and Panel Voltage

Figure 3-11 shows the system periodically goes into wait state when the battery current is lower than the limitation value (tested with the electronic load turned off).

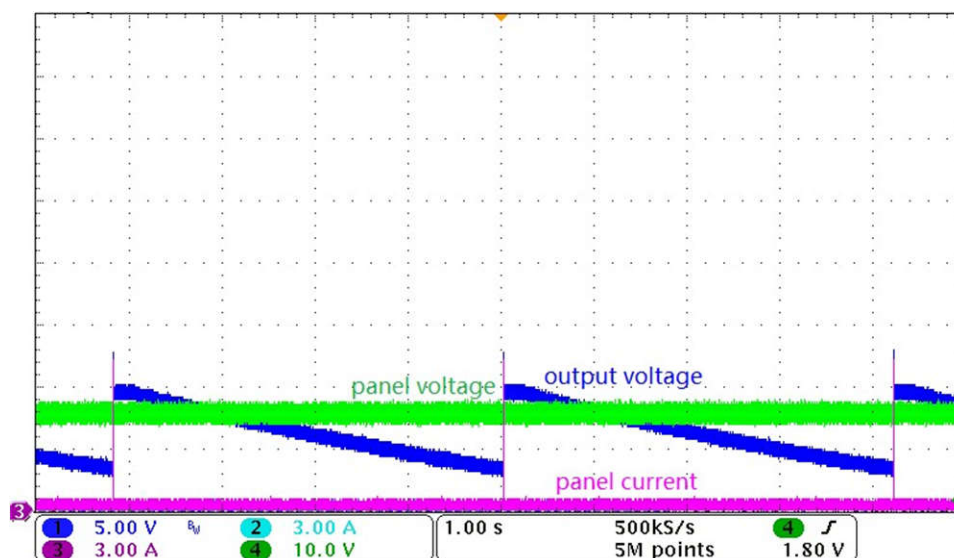


Figure 3-11. System Current and Voltage When in Wait Mode



## 4 Design Files

### 4.1 Schematics

To download the schematics, see the design files at [TIDA-010042](#).

### 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-010042](#).

### 4.3 PCB Layout Recommendations

#### 4.3.1 Loop Inductances

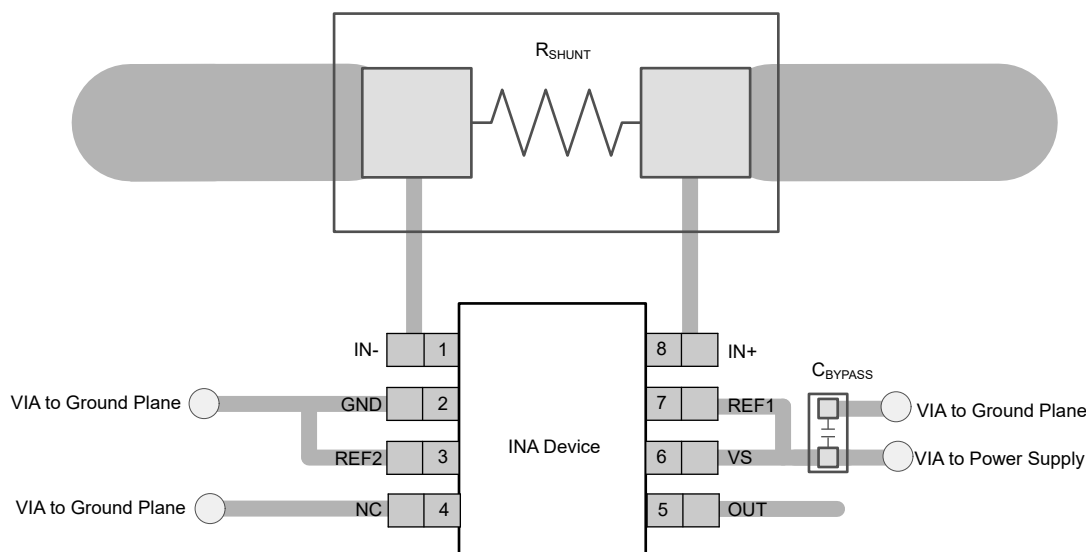
When working with high frequency switching waveforms, loop inductances need to be minimized to keep ringing at a minimum. Loop inductances can arise due to component placement and routing. Place traces along the shortest distance between components and integrate bypass capacitors into the design to maintain signal integrity.

Trace length and placement need to be taken into consideration when routing. Short, straight traces produce the lowest impedance path for the signal and minimize the current loop area, thereby reducing loop inductances present.

Bypass capacitors filter and condition signals before use and place as close to the respective component as possible. Any extraneous trace between the capacitor and component mitigates the effectiveness of the bypass capacitor.

#### 4.3.2 Current Sense Amplifiers

Poor routing of the current-sensing resistor can result in additional resistance between the input pins of the amplifier. Any additional high-current carrying impedance can cause significant measurement errors because the current resistor has a very-low-ohmic value. Use a Kelvin or 4-wire connection to connect to the device input pins. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins.



**Figure 4-1. INA241 Recommended Layout**

### 4.3.3 Trace Widths

Current capacity, or ampacity, of the trace and the allowable space between traces need to be taken into consideration when selecting traces widths for routing. For a given trace, there is a maximum current it can handle before failure. Injecting currents larger than rated leads to excess heat dissipation and can cause the trace to be destroyed.

This design can handle currents of up to 16 A. If designing for higher current systems, trace widths will need to be adjusted accordingly.

### 4.3.4 Layout Prints

To download the layer plots, see the design files at [TIDA-010042](#).

## 4.4 Altium Project

To download the Altium Designer® project files, see the design files at [TIDA-010042](#).

## 4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-010042](#).

## 4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-010042](#).

## 4.7 Software Files

To download the software files, see the design files at [TIDA-010042](#).

## 5 Related Documentation

1. Texas Instruments, [Understanding Buck Power Stages in Switchmode Power Supplies](#) Application Note
2. Texas Instruments, [High Efficiency, Versatile Bidirectional Power Converter for Energy Storage and DC Home Solutions](#) Design Guide

### 5.1 Trademarks

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## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2019) to Revision B (October 2023)	Page
• Updated the entire design guide to reflect the GaN and MSPM0 updates to the reference design.....	1
• Updated the <a href="#">Description</a> section.....	1
• Updated the <a href="#">Resources</a> section with the latest devices.....	1
• Updated the <a href="#">Features</a> section.....	1
• Updated the <a href="#">System Design Theory</a> section.....	10
• Updated the <a href="#">Hardware</a> section.....	17
• Updated the <a href="#">Testing and Results</a> section.....	21
• Updated <a href="#">Section 4.3.2</a> for the INA241 device.....	25
• Changed the current limit in <a href="#">Section 4.3.3</a> from 20 A to 16 A.....	26

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