Design Guide: TIDA-010239

AC Level 2 Charger Platform Reference Design

Description

Electric vehicle supply equipment (EVSE) facilitates power delivery to electric vehicles safely from the grid. An EVSE control system consists of an auxiliary power stage, an off-board AC/DC high-power stage (only in DC charging stations), energy metering unit, AC and DC residual current detector, an isolation monitor unit, relays and contactors with drive, two-way communication over single wire, and service and user interfaces. This reference design, an addition to the TIDA-010939 *Electric Vehicle Supply Equipment (EVSE) front-end controller,* highlights an ultra-low standby isolated AC/DC auxiliary power stage with super capacitor back-up power supply, an efficient relay and contactor drive and isolated line voltage sensing across the relay and contactor.

Features

- Ultra-low standby UCC28742-based isolated 29-W AC/DC stage to improve energy efficiency
- Supercapacitor backup supplying up to 7.5 W for 3 seconds during energy storage release (AC mains failing)
- Ultra-low standby as well as cost-optimized converters and linear regulators to power up points-of-load
- DRV8220 current controller to drive high-current relays and contactors
- Isolated line voltage sensing using a single TLV7021 comparator for welded relay and contactor detection

Applications

- AC charging (pile) station

Resources

TIDA-010239, TIDA-010939	Design Folder
UCC28742, DRV8220, TPS563211	Product Folder
TPS55330, ATL431, TL431	Product Folder
TLV7021, TL7705A	Product Folder

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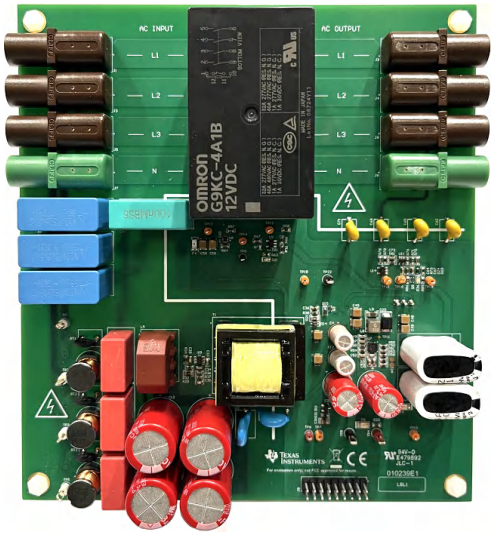
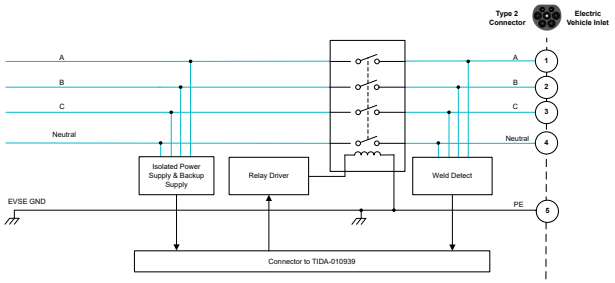




1 System Description

Electric vehicles (EVs), including plug-in hybrid electric vehicles (PHEVs), receive energy from the electrical grid through electric vehicle supply equipment (EVSE), more commonly known as EV chargers. To facilitate the power delivery to the vehicle, the EVSE sits between a stable grid connection and the vehicle.

An EVSE control system mainly consists of auxiliary power stage, off-board AC/DC high power stage (only in DC charging stations), energy metering, AC and DC residual current detection, isolation monitor unit, relays and contactors with drive, communication with the EV, the backend or a charge management system and service and user interfaces.

This reference design works as an addition to the TIDA-010939 electric vehicle charging controller. While the charging controller handles the communications, this design can be added to create an AC-charger by providing an isolated AC to DC power supply, relay and contactor drive, and a latched contact detection as shown in Figure 1-1.

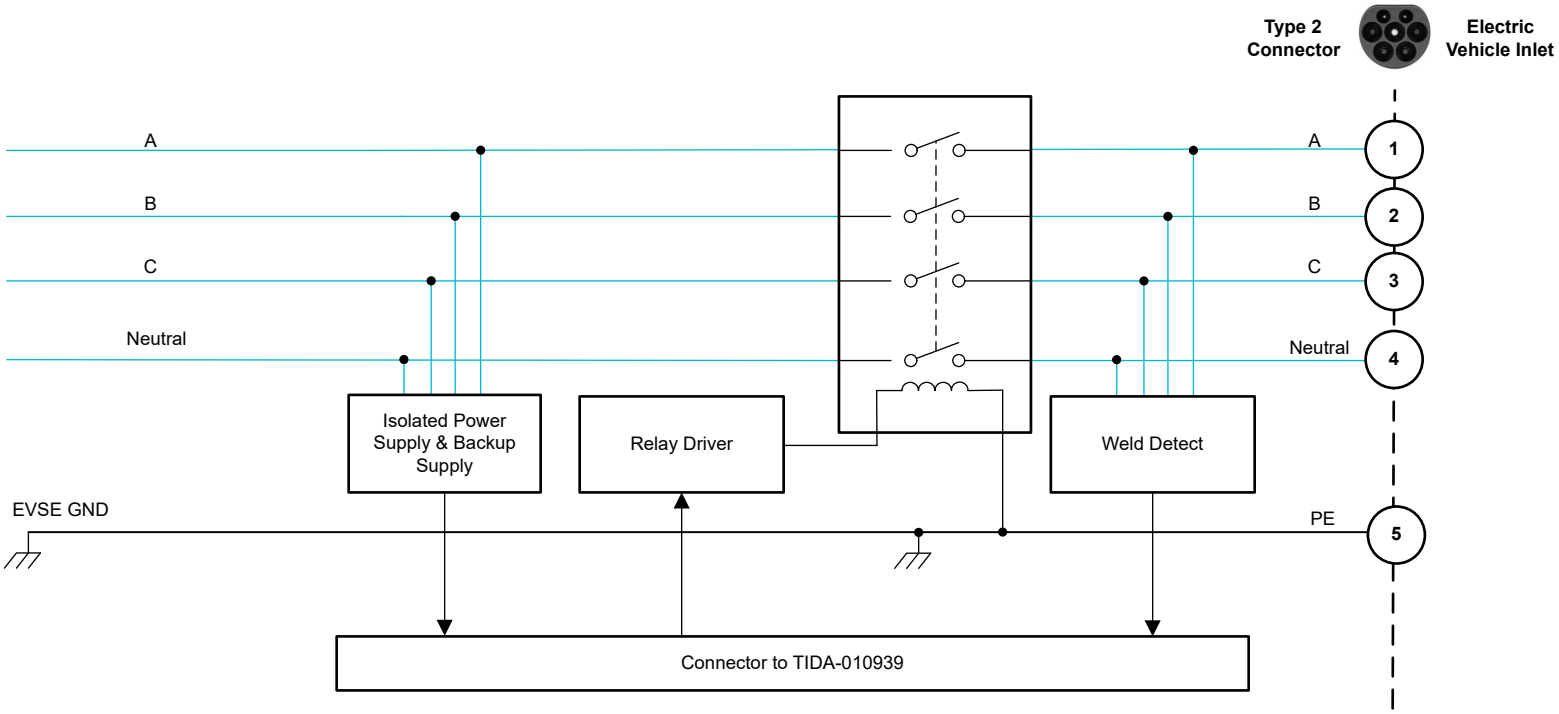


Figure 1-1. AC Level 2 Charger High-Level Block Diagram

1.1 EV Charging Station Challenges

The EVSE design for EV charging stations presents several challenges including those presented in the following sections.

1.1.1 Efficient Relay and Contactor Drive

In normal use cases, high-current relays or contactors can typically draw 10s to 100s of milliamps as an inductive load, requiring specific drive architectures. Because of the amount of time that a relay or contactor requires to remain powered, an efficient drive solution is preferred to avoid thermal problems.

1.1.2 Contact Weld Detection

For safety reasons, detecting the output voltage of the relay and contactor is critical. The contacts can experience arcing and become fused together, providing power to the plug even when not powered by the system. Checking that the operation completed correctly is important and is to be done every time the relay is opened.

This reference design showcases ultra-low standby isolated AC/DC auxiliary power stage followed by ultra-low I_Q as well as cost-optimized converters and linear regulators, efficient relay and contactor driver design, and isolated line voltage sensing to detect fusing of relay and contactor contacts due to arcing.

1.2 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT	DETAILS
INPUT CHARACTERISTICS						
Input voltage,V_{IN}		85	120, 230	460	V_{RMS}	Line voltage
Line frequency, f_{LINE}		47	60, 50	63	Hz	
OUTPUT CHARACTERISTICS						
Output voltage, V_{OUT1}	Flyback output 1		12		V	UCC28742-based AC/DC flyback power stage with 3 outputs
Output current, I_{OUT1}			2.2		A	
Output voltage, V_{OUT2}	Flyback output 2		14		V	
Output current, I_{OUT2}			0.1		A	
Output voltage, V_{OUT3}	Flyback output 3		–14		V	
Output current, I_{OUT3}			0.1		A	
Total output power, P_{OUT}	Output power of flyback power stage			28.8	W	
POINT OF LOAD AND AUXILIARY SECTION CHARACTERISTICS						
TPS7A3901(1)	Dual LDO		+12		V	Nominal current = 100 mA
TPS7A3901(1)			–12		V	Nominal current = 100 mA
TPS259470(1)	eFuse		+12		V	Overcurrent protection = 4.5 A
TPS563211(1)	Sync-Buck		+5		V	Nominal current = 1.2 A, 1.3 A maximum
TPS563211(1)	Sync-Buck		+3.3		V	Nominal current = 0.8 A, 1.5 A maximum
TPS65130(1)	Dual converter (Boost + inverting-Buck/Boost)" active during energy storage release		± 14		V	Nominal current = 0.1 A
TPS55330	Non-sync Boost: active during energy storage release		+11.5		V	Nominal current = 1.8 A
SUPERCAPACITOR BACKUP CHARACTERISTICS						
Supercap normal operating voltage	2 × 2.5-µF supercapacitors in series. Charger charges to 7.8 V. Boost UVLO sets min operating voltage to 4.3 V. Supplying 7.5 W for 3 s (after boost) during energy storage release (AC mains failing)	+4.3	+7.8		V	Peak current = 4.06 A, for 1 s from full rate voltage to half voltage.
TL7705A	Voltage supervisor for EoC of 2 × 2.5-µF supercapacitors in series		+7.49		V	Threshold for End of Charge
Linear charger	Charges supercapacitors from 0 V to 7.8 V in 81 s and from 4.3 V to 7.8 V in 36 s		+120		mA	

(1) On the TIDA-010939.

2 System Overview

2.1 Block Diagram

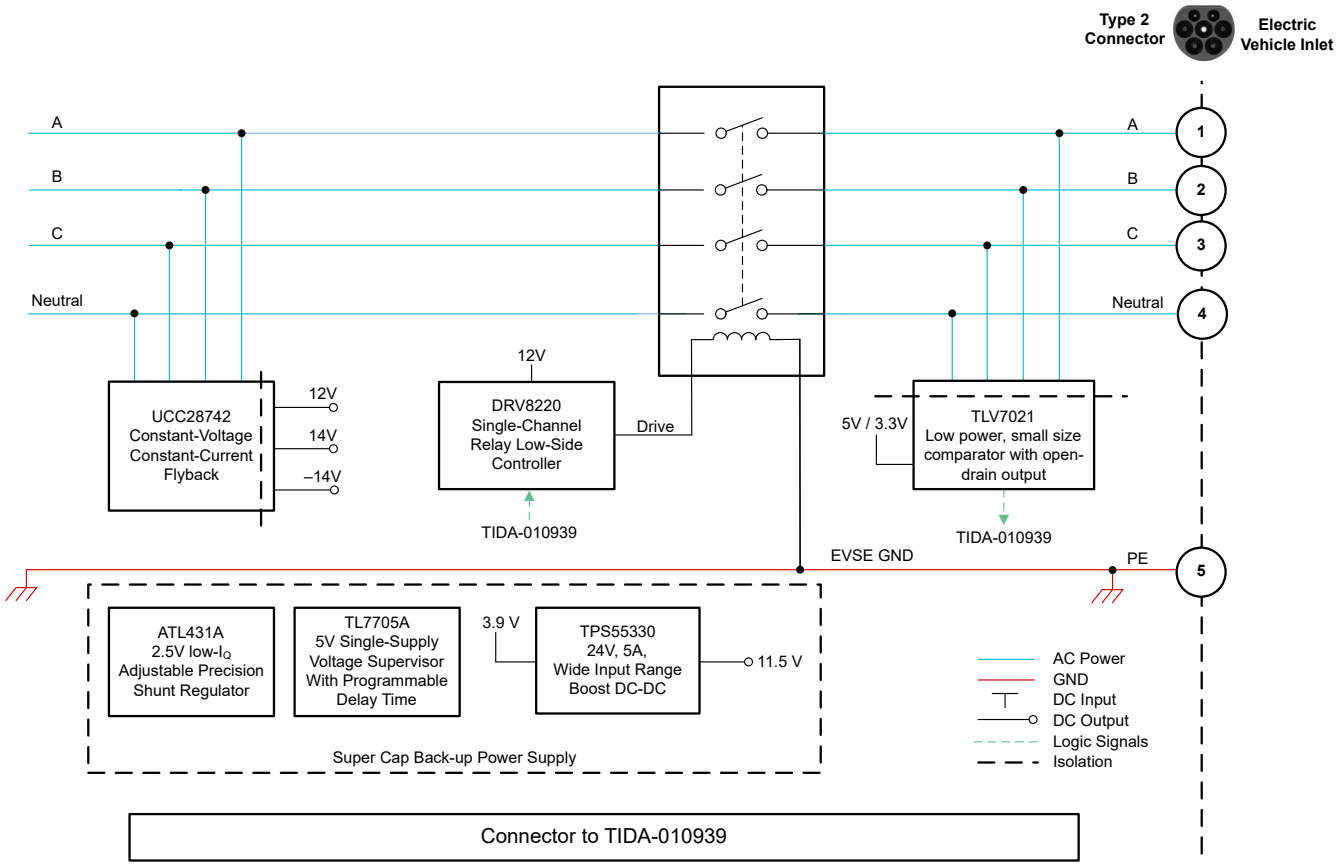


Figure 2-1. TIDA-010239 Block Diagram

2.2 Design Considerations

2.2.1 Isolated AC/DC Power Supply Design

The isolated AC/DC power stage is a multiple output winding flyback stage based on the UCC28742 device. The UCC28742 controller provides constant-voltage (CV) using an optical coupler to improve transient response to large-load steps. Constant-current (CC) regulation is accomplished through primary-side regulation (PSR) techniques. This device processes information from the optocoupled feedback and an auxiliary flyback winding for precise high-performance control of the output voltage and current. Figure 2-2 shows the system block diagram for the power supply design of the TIDA-010239 and TIDA-010939. The power supply is separated between both boards to enable the TIDA-010939 to be used from a single 12V supply without the need of the TIDA-010239. Together with the TIDA-010239, the whole system can be supplied by a single or three-phase high-voltage input. The design parameters are shown in Table 2-1.

These are the main components of the power supply:

- A three-phase input flyback with synchronous rectification supplies three voltages: 12 V (power) and ± 14V (low power)
- Two buck converters (based on TPS563211) and one dual-LDO (TPS7A3901) take the power from the flyback and supply further 5 V, 3.3 V, and ±12 V on the TIDA-010939
- Two supercapacitors, 2.5 µF each are connected in series and are charged by means of a 120-mA constant current linear regulator, setting the charging voltage to 7.8 V
- A boost converter with TPS55330 supplies all voltages as soon as mains power is missing
- A further 12-V input port on the TIDA-010939, protected against overcurrent and reverse polarity, is managed by the eFuse TPS259470. This way the whole system can be supplied without the need of single or three-phase high-voltage input useful during debug or if the TIDA-010939 is used standalone.
- An inverting buck-boost converter generates ±14V for the dual-LDO during energy storage discharge, taking power from the regulated 5-V rail located on the TIDA-010939

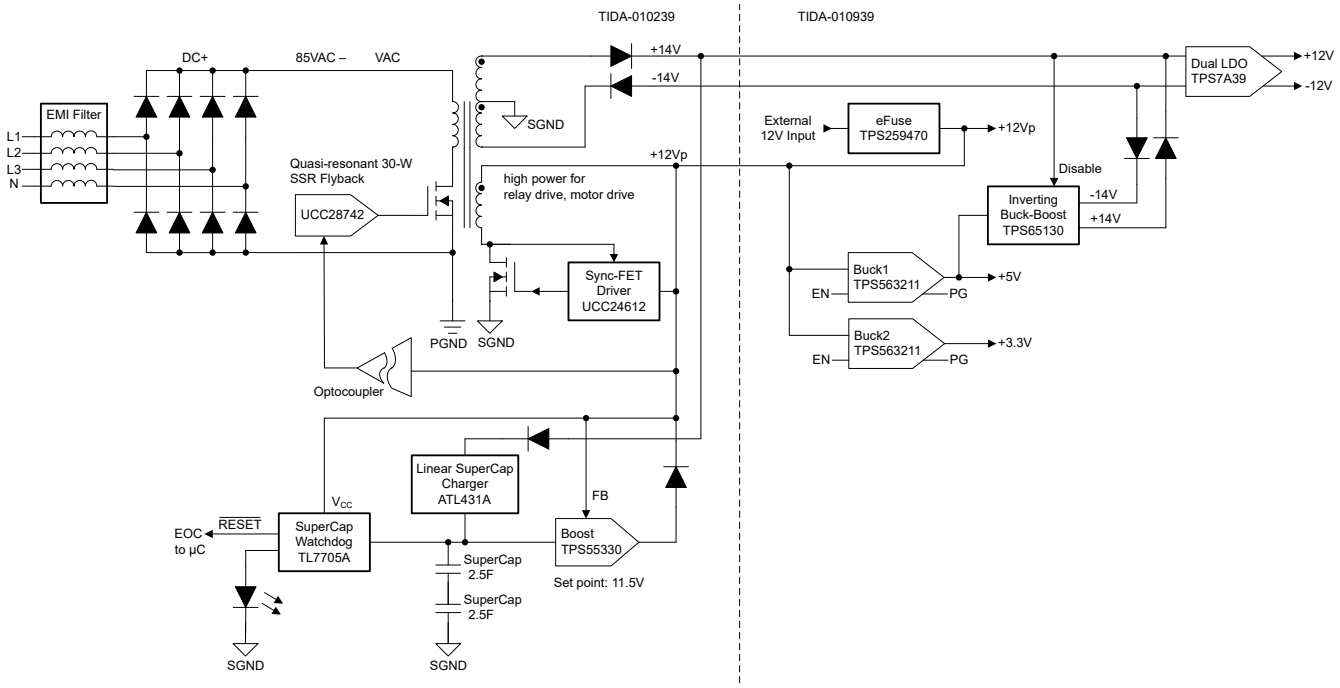


Figure 2-2. Isolated AC/DC Power Supply Block Diagram

Table 2-1. Design Parameters

PARAMETER	NOTES AND CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS					
Input voltage,V_{IN}		85	115, 230	460	V_{RMS}
Maximum input current	$V_{IN} = V_{IN(min)}$, $I_{OUT} = I_{OUT(max)}$		0.8		A_{RMS}
Line frequency		47	60, 50	63	Hz
Desired capacitor bulk voltage, $V_{BULK(desired)}$		85			V
No load input power consumption	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, I_{OUT} = 0 A			500	mW
OUTPUT CHARACTERISTICS					
Output voltage, V_{OUT1}	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$	11.4	12	12.6	V
Output current, I_{OUT1}				2.2	A
Output voltage, V_{OUT2}	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$	10.5	12	12.1	V
Output current, I_{OUT2}				0.1	A
Output voltage, V_{OUT3}	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$	–10.5	–12	–12.1	V
Output current, I_{OUT3}				0.1	A
Total output power, P_{OUT}				28.8	W
Output voltage regulation	Line regulation: $V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT1} \le I_{OUT1(max)}$		0.1%		
	Load regulation: 0 A $\le I_{OUT1} \le I_{OUT1(max)}$		0.2%		
Output voltage ripple	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, 0 A $\le I_{OUT1} \le I_{OUT1(max)}$			100	mVpp
Total output overcurrent, I_{OCC}	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$			2.4	A
Minimum output voltage, CC mode	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT} = I_{OCC}$		5		V
Brown-out protection	$I_{OUT} = I_{OUT(max)}$	49.9	55.9	61.8	V_{RMS}
Transient response overshoot	$I_{OUT} = I_{OUT(max)}$ to 0-A load transient			0.2	V
Transient response time	$I_{OUT} = I_{OUT(max)}$ to 0-A load transient			5	ms
SYSTEMS CHARACTERISTICS					
Switching frequency, f_{SW}		1.2		40	kHz
Average efficiency	25%, 50%, 75%, 100% load average at nominal input voltages	84.8	85.5	86.2	%
Operating temperature			25		°C

2.2.1.1 Input Bulk Capacitance and Minimum Bulk Voltage

The minimum voltage on the input bulk capacitance is needed to determine the maximum primary-to-secondary turns-ratio of the transformer. The input power of the converter based on target full-load efficiency, the minimum input RMS voltage, and the minimum AC input frequency determine the input capacitance requirement. Maximum input power is determined based on Equation 1:

$$P_{IN} = \frac{V_{OCV} \times I_{OCC}}{\eta} = \frac{12\ V \times 2.2\ A + |-14\ V| \times 0.1\ A + |+14\ V| \times 0.1\ A}{0.8} \approx 36.5\ W \quad (1)$$

where

- V_{OCV} is the regulated output voltage of the converter
- I_{OCC} is the converter total output CC target
- η is the converter overall efficiency at full-power output

Equation 2 provides an accurate solution for the total input capacitance based on a target minimum bulk capacitor voltage. Alternatively, to target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance value.

$$C_{BULK} = \frac{2P_{IN} \times \left\{0.25 + \frac{1}{2\pi} \times arcsin\left(\frac{V_{BULK(\text{desired})}}{\sqrt{2} \times V_{IN(\text{min})}}\right)\right\}}{\left(2V_{IN(\text{min})}{}^2 - V_{BULK(\text{desired})}{}^2\right) \times f_{LINE(\text{min})}} \approx 58.9\ \mu F \quad (2)$$

$$C_{BULK(selected)} = 68\ \mu F \quad (3)$$

Four 68-µF electrolytic capacitors were used at the input to create an equivalent 68-µF bulk capacitor to support a maximum input voltage of 460 V_{RMS}. This selection changes the minimum V_{BULK} voltage to 90.7 V (also called V_{BULK_VALLEY}) per the UCC28742 design calculator.

2.2.1.2 Transformer Turns-Ratio, Primary Inductance, and Primary Peak Current

The target maximum switching frequency at full load, the minimum input-capacitor bulk voltage, and the estimated DCM resonant time determine the maximum primary-to-secondary turns-ratio of the transformer. Initially, determine the maximum-available total duty-cycle of the on-time and secondary conduction time based on the target switching frequency (f_{MAX}) and DCM resonant time (t_R).

At the transition-mode operation limit of DCM, the interval required from the end of the secondary current conduction to the first valley of the V_{DS} voltage is ½ of the DCM resonant period (t_R), or 1 µs assuming 500-kHz DCM resonant frequency. The maximum allowable MOSFET on-time D_{MAX} is determined using Equation 4:

$$D_{MAX} = 1 - D_{MAGCC} - \left(\frac{t_R}{2} \times f_{MAX}\right) = 1 - 0.475 - 38\ kHz \times \frac{2\ \mu s}{2} = 0.485 \quad (4)$$

where

- t_R is the estimated period of the LC resonant frequency at the switch node
- D_{MAGCC} is defined as the duty cycle of the secondary-diode conduction during CC operation and is fixed internally by the UCC28742 device at 0.475

When D_{MAX} is known, the maximum primary-to-secondary turns ratio is determined with Equation 5. The total voltage on the secondary winding must be determined, which is the sum of V_{OCV} and V_F.

$$N_{PS(\text{max})} = \frac{D_{MAX} \times V_{BULK\_\text{VALLEY}}}{D_{MAGCC} \times (V_{OCV} + V_F)} \quad (5)$$

Assuming V_F = 0.8 V:

$$N_{PS(max)} = \frac{0.485 \times 90.7\ V}{0.475 \times (12\ V + 0.8\ V)} = 7.24 \quad (6)$$

$$N_{PS(selected)} = 7 \quad (7)$$

A higher turns-ratio generally improves efficiency, but can limit operation at a low input voltage. Transformer design iterations are generally necessary to evaluate system-level performance trade-offs.

The primary transformer inductance is calculated using the standard energy storage equation for flyback transformers. The primary current, maximum switching frequency, output voltage and current targets, and transformer power losses are included in Equation 8:

$$L_P = \frac{2 \times (V_{OCV} + V_F) \times I_{OCC}}{\eta_{XFMR} \times I^2_{PP(max)} \times f_{MAX}} = 627.7\ \mu H \quad (8)$$

$$L_{P(selected)} = 700\ \mu H \quad (9)$$

The UCC28742 CC regulation is achieved by maintaining D_{MAGCC} at the maximum primary peak current setting. The product of D_{MAGCC} and $V_{CST(max)}$ defines a CC-regulating voltage factor V_{CCR} which is used with N_{PS} to determine the current-sense resistor value necessary to achieve the regulated CC target, I_{OCC} (see Equation 10).

$$R_{CS} = \frac{V_{CCR} \times N_{PS}}{2 \times I_{OCC}} \times \sqrt{\eta_{XFMR}} \quad (10)$$

$$R_{CS} = \frac{0.363\ V \times 7}{2 \times 2.2\ A} \times \sqrt{0.9} = 0.547\ \Omega \quad (11)$$

$$R_{CS(selected)} = 0.5\ \Omega \quad (12)$$

where

- V_{CCR} is the CC regulation factor (from the *UCC28742 High-Efficiency Flyback Controller with Optocoupler Feedback* data sheet)
- V_{CST} is the CS-pin current-sense threshold (from the *data sheet*)

$$I_{PP(max)} = \frac{V_{CST(max)}}{R_{CS}} = \frac{0.83\ V}{0.5\ \Omega} = 1.66\ A \quad (13)$$

$$I_{PP(nom)} = \frac{V_{CST(nom)}}{R_{CS}} = \frac{0.77\ V}{0.5\ \Omega} = 1.54A \quad (14)$$

N_{AS} is determined by the lowest target operating output voltage while in CC regulation and by the V_{DD} UVLO turnoff threshold of the UCC28742 device. Additional energy is supplied to V_{DD} from the transformer leakage-inductance which allows a lower turns ratio to be used in many designs.

$$N_{AS} = \frac{V_{DD(off)} + V_{FA}}{V_{OCC} + V_F} = \frac{8.15\ V + 0.8\ V}{5\ V + 0.8\ V} = 1.54 \quad (15)$$

where

- $V_{DD(off)}$ is UCC28742 turnoff threshold (from the *data sheet*)
- V_{OCC} is the lowest output voltage target of the converter while in constant-current regulation
- V_{FA} is voltage drop across rectifier diode on auxiliary side of flyback stage

$$N_{AS(selected)} = 1.455 \quad (16)$$

This implies:

$$N_{PA(selected)} = 4.81 \quad (17)$$

Since the ±14-V rails are unregulated, the turn ratio determines their output voltage:

$$N_{PT} = \frac{N_{PS}}{(V_{OV14} + V_F)/(V_{OCV} + V_F)} = \frac{7}{(14\ V + 0.8\ V)/(12\ V + 0.8\ V)} = 6.05 \quad (18)$$

$$N_{PT(selected)} = 5.92 \quad (19)$$

2.2.1.3 Transformer Parameter Calculations: Primary and Secondary RMS Currents

With the primary inductance of 700 µH, the absolute maximum switching frequency is calculated from:

$$f_{MAX} = \frac{2 \times (12\ V + 0.8\ V) \times 2.2\ A}{0.9 \times (1.54\ A)^2 \times 700\ \mu H} = 37.7\ kHz \quad (20)$$

The maximum switching period is:

$$t_{SW} = \frac{1}{f_{MAX}} = \frac{1}{37.7\ kHz} = 26.5\ \mu s \quad (21)$$

The actual maximum on-time is given by:

$$t_{ON(\max)} = \frac{I_{PP(nom)} \times L_P}{V_{BULK\_VALLEY}} = \frac{1.54\ A \times 700\ \mu H}{90.7\ V} = 11.88\ \mu s \quad (22)$$

The maximum duty cycle of operation (D_{MAX}) is:

$$D_{MAX} = \frac{t_{ON(max)}}{t_{SW}} = \frac{11.88\ \mu s}{26.5\ \mu s} = 0.448 \quad (23)$$

The transformer primary RMS current (I_{PRMS}) is:

$$I_{PRMS} = I_{PP(max)} \sqrt{\frac{D_{MAX}}{3}} = 1.66\ A \times \sqrt{\frac{0.448}{3}} = 0.641\ A \quad (24)$$

The transformer secondary peak current RMS current ($I_{SEC(max)}$) is:

$$I_{SEC(max)} = I_{PP(max)} \times N_{PS} = 1.66\ A \times 7 = 11.62\ A \quad (25)$$

The transformer secondary RMS current (I_{SEC_RMS}) is:

$$I_{SEC\_RMS} = I_{SEC(max)} \sqrt{\frac{D_{MAX}}{3}} = 11.62\ A \times \sqrt{\frac{0.448}{3}} = 4.49\ A \quad (26)$$

Based on these calculations, a Würth Elektronik™ transformer was designed for this application (part number 750320029), which has the following specifications:

- N_{PS} = 7 ±2% (primary to secondary turns-ratio)
- N_{PT} = 5.92 ±2% (primary to tertiary turns-ratio)
- N_{PA} = 4.81 ±2% (primary to auxiliary turns-ratio)
- L_P = 700 ±10% µH (primary inductance)
- L_{LK} = 10 µH (primary leakage inductance)

2.2.1.4 Main Switching Power MOSFET Selection

The drain-to-source RMS current, I_{DS_RMS}, through switching FET is calculated using:

$$I_{DS\_RMS} = I_{PRMS} = 0.641\ A \quad (27)$$

Select a MOSFET with five times the I_{DS_RMS} calculated. The maximum voltage across the FET can be estimated using:

$$V_{DSPK} = \left(V_{IN(max)} \times \sqrt{2}\right) + \left(V_{OCV} + V_F\right) \times N_{PS} + V_{LK} = \left(460\ V \times \sqrt{2}\right) + \left(12\ V + 0.8\ V\right) \times 7 + 63\ V = 803.1\ V \quad (28)$$

Considering a de-rating of 15% and leakage spike of around 150 V, the voltage rating of the MOSFET must be around 925-V DC. A 950-V MOSFET is selected.

2.2.1.5 Rectifying Diode Selection

Calculate the secondary output diode or synchronous rectifier FET reverse voltage or blocking voltage needed ($V_{DIODE\_BLOCKING}$):

$$V_{DIODE\_BLOCKING} = \frac{V_{IN\_DC(max)}}{N_{PS}} + V_{OCV} = \frac{460\ V \times \sqrt{2}}{7} + 12\ V = 104.9\ V \quad (29)$$

For this reference design, a 200-V, 24-A rated synchronous rectifier FET is selected for the +12-Vp rail to reduce losses. For the ±14 rails, Schottky diodes with 200-V voltage and 1-A forward current ratings are selected.

$$V_{DIODE\_BLOCKING\_AUX} = \frac{V_{IN\_DC(max)}}{N_{PA}} + \left(V_{OCV} + V_F\right) \times N_{AS} - V_{FA} = \frac{460\ V \times \sqrt{2}}{4.81} + \left(12\ V + 0.8\ V\right) \times 1.455 - 0.6\ V = 153\ V \quad (30)$$

For the auxiliary rail, a Schottky diode with 400-V voltage and 1-A forward current ratings is selected. Here normally a 200-V diode is sufficient, but spikes over 153 V must be considered. If a 300-V diode, is selected, the diode does not bring any advantage because 300-V and 400-V small diodes have no difference in terms of reverse recovery time, nor V_F.

2.2.1.6 Output Capacitor Selection

For this reference design, the output capacitor (C_{OUT}) for output is selected to prevent V_{OUT} (12 V) from dropping below the minimum output voltage (V_{OTRM}) during transients up to 0.1 V and ripple voltage less than 100 mV.

$$C_{OUT} \geq \frac{\frac{I_{OCC}}{2} \times \left(t\right)}{V_{OCV} - V_{OTRM}} \quad (31)$$

Assuming V_{OTRM} = 11.9 V,

$$C_{OUT} \geq \frac{\frac{2.2\ A}{2} \times (50\ \mu s)}{12\ V - 11.9\ V} \geq 550\ \mu F \quad (32)$$

$$C_{OUT(selected)} = 2\ \times\ 680\ \mu F \quad (33)$$

Considering the allowable output ripple voltage of 100 mV (5%), the ESR and RMS current of the capacitor must be:

$$ESR = \frac{V_{OUT\_RIPPLE}}{I_{SEC(max)}} = \frac{200\ mV}{11.62\ A} = 17.2\ m\Omega \quad (34)$$

$$I_{COUT\_RMS} = \sqrt{\left(I_{SEC\_RMS}\right)^2 - \left(I_{OCC}\right)^2} = \sqrt{(4.49\ A)^2 - (2.2\ A)^2} = 5.0\ A \quad (35)$$

2.2.1.7 Capacitance on VDD Pin

The capacitance on VDD needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in CC regulation. The capacitance on VDD must supply the primary-side operating current used during start-up and between low-frequency switching pulses. The largest result of two independent calculations denoted in Equation 36 determines the value of C_{VDD}.

At start-up, when $V_{VDD(on)}$ is reached, C_{VDD} alone supplies the device operating current and MOSFET gate current until the output of the converter reaches the target minimum operating voltage in CC regulation, V_{OCC}. Now the auxiliary winding sustains VDD for the UCC28742 device above UVLO. The total output current available to the load and to charge the output capacitors is the CC-regulation target, I_{OCC}. Equation 36 assumes that all of the output current of the converter is available to charge the output capacitance until V_{OCC} is achieved.

For typical applications, Equation 37 includes an estimated $q_G \times f_{SW(max)}$ of average gate drive current and a 1-V margin added to V_{VDD}.

$$C_{VDD} \geq \frac{\left(I_{RUN} + q_G f_{SW(max)}\right) \times \frac{C_{OUT} \times V_{OCC}}{I_{OCC}}}{V_{DD(on)} - \left(V_{DD(off)} + 1\ V\right)} \tag{36}$$

$$C_{VDD} \geq \frac{(2\ mA + 10\ nC \times 37.7\ kHz) \times \frac{1360\ \mu F \times 12\ V}{2.2\ V}}{21\ V - (8.5\ V + 1\ V)} \geq 0.128\ \mu F \tag{37}$$

The current design uses 10-µF and 0.1-µF capacitors.

2.2.1.8 Open-loop Voltage Regulation Versus Pin Resistor Divider, Line Compensation Resistor

The resistor divider at the VS pin determines the output voltage regulation point of the flyback converter. Also, the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on transformer auxiliary-to-primary turns ratio and desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)} \times \sqrt{2}}{N_{PA} \times I_{VSL(min)}} \tag{38}$$

where

- N_{PA} is the transformer primary-to-auxiliary turns ratio
- $V_{IN(run)}$ is the AC_{RMS} voltage to enable turn-on of the controller (run); in case of DC input, leave out the $\sqrt{2}$ term in the equation
- $V_{SL(run)}$ is the run threshold for the current pulled out of the VS pin during the switch on-time (see the *Electrical Characteristics* section of the UCC28742 data sheet)

$$R_{S1} = \frac{80\ V \times \sqrt{2}}{4.81 \times 210\ \mu A} = 112\ k\Omega \tag{39}$$

$$R_{S1(selected)} = 121\ k\Omega \tag{40}$$

The low-side VS pin resistor is selected based on the desired V_{OUT} regulation voltage in open-loop conditions and sets the maximum allowable voltage during open-loop conditions.

$$R_{S2} = \frac{R_{S1} \times V_{OVPTH}}{N_{AS} \times (V_{OV} + V_F) - V_{OVPTH}} \tag{41}$$

where

- V_{OV} is the maximum allowable peak voltage at the converter output
- V_F is the output-rectifier forward drop at near-zero current
- N_{AS} is the transformer auxiliary-to-secondary turns ratio
- V_{OVPTH} is the overvoltage detection threshold at the VS input (see the Electrical Characteristics section of the UCC28742 data sheet)

$$R_{S2} = \frac{121\ k\Omega \times 4.65\ V}{1.455 \times (15\ V + 0.8\ V) - 4.65\ V} = 30.7\ k\Omega \tag{42}$$

$$R_{S2(selected)} = 33.2\ k\Omega \tag{43}$$

The UCC28742 device maintains tight CC regulation over varying input lines by using the line-compensation feature. The line-compensation resistor (R_{LC}) value is determined by the current flowing in R_{S1} and the total internal gate drive and external MOSFET turn-off delay. Assuming an internal delay of 50 ns in the UCC28742 device:

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_D \times N_{PA}}{L_P} \quad (44)$$

where

- t_D is the current-sense delay including MOSFET turn-off delay
- K_{LC} is a current-scaling constant (see the Electrical Characteristics section of the UCC28742 data sheet)

$$R_{LC} = \frac{25 \times 121\ k\Omega \times 0.5\ \Omega \times (46\ ns + 50\ ns) \times 4.81}{700\ \mu H} = 998\ \Omega \quad (45)$$

$$R_{LC(selected)} = 1\ k\Omega \quad (46)$$

2.2.1.9 Feedback Elements

The output voltage is set through the sense network resistors R_{FB1} and R_{FB2}. Select the value of the feedback resistor based on the desired output voltage with:

$$V_{th} = \frac{V_{OCV} \times R_{FB2}}{R_{FB1} + R_{FB2}} \quad (47)$$

where

- V_{th} = 2.5 V

The op amp compensation network, Z_{FB}, is determined using well-established design techniques for control-loop stability. Typically, a type-II compensation network is used. See the *UCC28742 data sheet* and the design calculator for details.

2.2.1.10 Backup Power Supply

There are three possible power scenarios:

1. Single or three-phase power available:
   a. The converter supplies all voltages and charges the supercapacitors in a variable time between 1 minute and 21 seconds as first charge, and 36 seconds as successive recharges.
   b. The switching waveform present on the secondary side winding is peak-rectified and is used to disable the inverting buck-boost converter.
   c. At the same time, as the voltage on the supercapacitors is in the range of 4.3 V to 7.8 V, the boost converter is active and delivers 11.5 V. This voltage level, slightly lower than 12 V, is on purpose to avoid delivering current when mains is present. Keeping the boost converter active eliminates the delay due to the device soft start.
   d. When the supercapacitors are charged, a voltage supervisor TL7705A is enabling the flag *EOC* (end of charge, useful for a digital output to uC) and turning an LED on.
2. Power unavailable:
   a. Since the boost converter with TPS55330 is always active, the 12-Vp bus droops from 12 V to 11.5 V, keeping all rails alive.
   b. At the same time, both ± 14-V outputs from the flyback converter go to zero and the peak rectified voltage used for the signal *Disable* goes to zero.
   c. Next, the inverting buck-boost converter, located on the TIDA-010939, starts and supplies ±14 V, which are connected by ORing diodes to the input of the dual LDO, supplying ± 12 V.
   d. The power is delivered until the supercapacitors are discharged below boost UVLO (4.3 V). At this point all rails are off.
3. Powered from TIDA-010939 with an external 12V supply:
   a. In this scenario, the supercapacitors are not recharged because there is no voltage on auxiliary winding of the flyback.
   b. The 12 V from external power supply on the TIDA-010939 is powering all the rails normally. The inverting buck-boost converter is also supplying ±14 V for dual LDO.

2.2.1.11 Supercapacitor Selection

The supercapacitors supply the 12-V and the 5-V rails (TIDA-010939) in case of unexpected AC input shut down to turn off the main relay and unlock the plug. Assume 1 s duration time as the initial specification.

- 12-V rail: Peak current 1.8 A for 200 ms (unlock plug and relay off)
- 12-V rail: Average current 1.8 A × 0.2 s + 0.1 A × 0.8 s = 0.44 A
- 5-V rail: Average current 0.275 A for 1 s

The total peak power required from supercap, P_{PK_SC}:

$$P_{PK\_SC} = (V_{12Vp} \times I_{PK\_1} + V_{5V} \times I_{PK\_2} / \eta_{BUCK}) / \eta_{BOOST} \quad (48)$$

$$P_{PK\_SC} = (12\ V \times 1.8\ A + 5\ V \times 0.275\ A / 0.9) / 0.85 = 27.2\ W \quad (49)$$

Total 27.2 W peak for 200 ms or a peak current of approximately 3.5 A (that is, 27.2 W / 7.8 V). Total average power required from supercapacitor, P_{AVE_SC}:

$$P_{AVE\_SC} = (V_{12Vp} \times I_{AVE\_1} + V_{5V} \times I_{AVE\_2} / \eta_{BUCK}) / \eta_{BOOST} \quad (50)$$

$$P_{AVE\_SC} = (12\ V \times 0.44\ A + 5\ V \times 0.275\ A / 0.9) / 0.85 = 8\ W \text{ (that is, 8 J in 1 s)} \quad (51)$$

Consider that the supercapacitor is charged up to 7.8 V and then discharged down to 4.3 V (that is, UVLO of the TPS55330 boost converter):

$$C_{MIN\_SERIES} = 2 \times (E) / ((V_2)^2 - (V_1)^2) = 2 \times (8\ J) / ((7.8\ V)^2 - (4.3\ V)^2) = 0.3778\ F \quad (52)$$

$$C_{MIN} = 2 \times C_{MIN\_SERIES} = 0.76\ F \text{ (for 1 s)} \quad (53)$$

where

- C_{MIN_SERIES} is the minimum equivalent series capacitor
- C_{MIN} is the minimum individual capacitance

Now, for 3 s $C_{MIN} = 3 \times 0.76 = 2.28$ F is needed.

For this design, two 2.5-F in series that support up to 47.5 W and 4 A peak are selected.

The TL7705 voltage supervisor monitors for charge completion at an slightly lower voltage of 7.49 V. The supercapacitor energy available from 7.49 V to 4.3 V, E_{SC_7p5}:

$$E_{SC\_7p5} = 0.5 \times C \times (V_1{}^2 - V_2{}^2) = 0.5 \times 1.25\ F \times (7.49^2 - 4.3^2) = 23.5\ J \quad (54)$$

The energy available after accounting for boost efficiency, $E_{SC\_7p5\_BOOST}$:

$$E_{SC\_7p5\_BOOST} = E_{SC\_7p5} \times \eta_{BOOST} = 23.5\ J \times 0.85 = 20\ J \quad (55)$$

The power available during 3 s, P_{SC_7p5}:

$$P_{SC\_7p5} = E_{SC\_7p5\_BOOST} / \text{time} = 20\ J / 3\ s = 6.65\ W \quad (56)$$

The supercapacitor energy available from 7.8 V to 4.3 V, E_{SC_7p8}:

$$E_{SC\_7p8} = 0.5 \times C \times (V_1{}^2 - V_2{}^2) = 0.5 \times 1.25\ F \times (7.8^2 - 4.3^2) = 26.5\ J \quad (57)$$

The energy available after accounting for boost efficiency, $E_{SC\_7p8\_BOOST}$:

$$E_{SC\_7p8\_BOOST} = E_{SC\_7p8} \times \eta_{BOOST} = 26.5\ J \times 0.85 = 22.5\ J \quad (58)$$

The power available during 3 s, P_{SC_7p8}:

$$P_{SC\_7p8} = E_{SC\_7p8\_BOOST} / \text{time} = 22.5 \text{ J} / 3 \text{ s} = 7.5 \text{ W} \quad (59)$$

2.2.1.12 Supercapacitor Charger Design

The shunt voltage reference (U6) sets the final charge voltage to 7.8 V. The NPN transistor (Q5) and 4.99-Ω resistor (R42) limit the charge current to approximately 120 mA (0.6 V / 4.99 Ω). The NMOS FET (Q4) operates in saturation region to maintain the required charge voltage drop. U6 pulls down the gate of Q4 as soon as Vbackup reaches 7.8 V. This way, Vbackup stays constant at the nominal 7.8 V. There are two charging scenarios:

1. Charging time as first power supply turn-on: here Vbackup is zero. The ΔV that must be covered is from zero to 7.8 V; therefore, the charging time is ΔT = C × ΔV / I = 1.25 F × 7.8 V / 120 mA = 81.25 seconds (1 minute and 21 seconds).
2. Charging time after energy storage release: here Vbackup is the UVLO of the boost converter (4.3 V). The ΔV that must be covered is from 4.3 V to 7.8 V; the charging time is ΔT = C × ΔV / I = 1.25 F × (7.8 V – 4.3 V) / 120 mA = 36.46 seconds.

In summary, the worst-case charging time is 1 minute and 21 seconds, while recharging between energy storage releases is 36.46 seconds.

2.2.2 Relay Drive and Weld Detect

The primary functionality of the EVSE is the reliable control of large currents directed toward an electric vehicle at the mains voltage. In a normal use case, the relay or contactor must be held closed for several hours to fully charge a vehicle; however, the relays cannot be welded because of safety concerns. If something fails in the control system, the relays must fail open. These high-current relays or contactors can typically draw tens to hundreds of milliamps as an inductive load, requiring specific drive architectures.

Because of the amount of time that a relay or contactor requires to remain powered, an efficient drive device is preferred to the typical Darlington array, or even discrete transistor configuration. For this reason, the DRV8220 current controller is selected to drive the relays or contactors in the design. The DRV8220 device is designed to regulate the current with a well-controlled waveform to reduce power dissipation.

Relays and contactors use electromechanical solenoids for operation. Activation starts when EN pin voltage is pulled high either by an external driver or internal pullup. Once the EN pin is driven to GND, the DRV8220 device allows the solenoid current to decay to zero. The solenoid current is ramped up fast to enable opening of the relay or contactor. After initial ramping, the solenoid current is kept at a peak value to maintain correct operation, after which the current is reduced to a lower hold level to avoid thermal problems and reduce power dissipation.

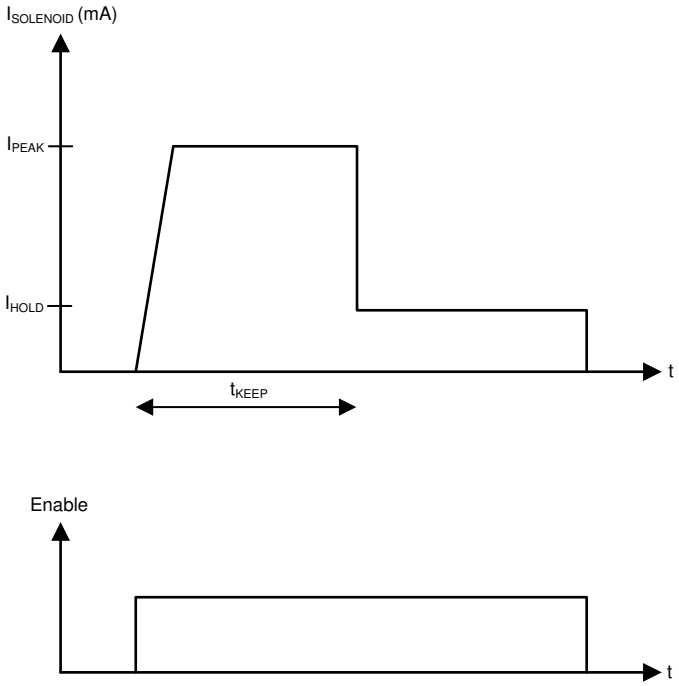


Figure 2-3. Typical Current Waveform Through the Solenoid

For safety reasons, detecting the output voltage of relays and contactors is critical. Due to aging and wear, contacts can suffer from arcing and can become permanently welded, resulting in a closed state that continues to supply power to the plug even when the system is off. To prevent this hazard, proper operation must be checked every time the relay is opened.

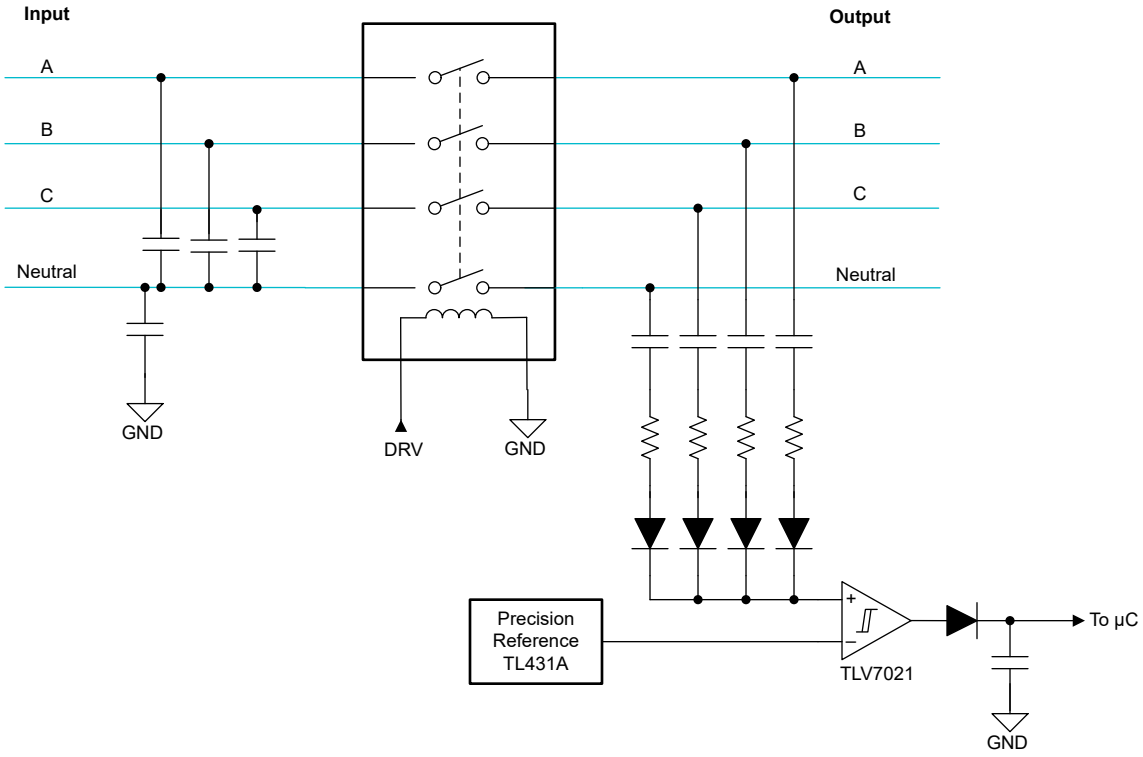


Figure 2-4. AC Weld Detect Block Diagram

The weld detection circuit of the TIDA-010239 monitors each phase and the neutral line at the output of the contactor. Each phase is monitored through a safety capacitor. The safety capacitors provide an isolated design that also passes high-potential testing. The AC-coupled signals are first voltage- and current-limited, then combined using an ORing circuit and monitored by a single comparator. At the mains input, before the contactor, Class-X and Class-Y safety capacitors provide a current return path from the isolated ground of the charger back to the grid.

If the relay is welded, or if voltage is present at the output of the relay, the comparator drives a logic-high signal through a peak-detect circuit into the fault detection input of the MCU.

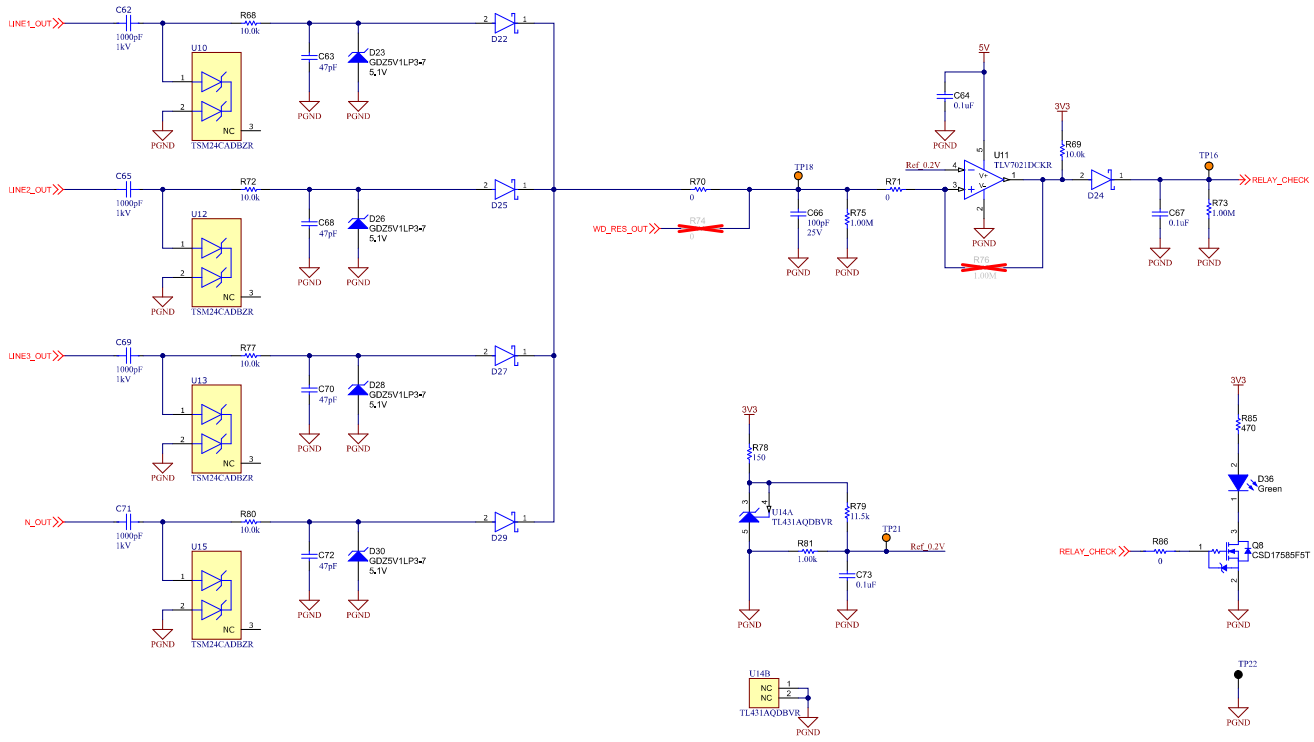


Figure 2-5. AC Weld Detect Circuit

The weld detection in this design uses the TLV7021 comparator. The TLV701x and TLV702x devices provide micropower operation with rail-to-rail input capability, combining a propagation delay of 260 ns with a quiescent supply current of only 5 µA. This balance of speed and low power enables the system to quickly detect fault conditions while minimizing energy consumption.

Internal hysteresis and immunity to output phase inversion provides robust and noise-resistant operation, which is critical when monitoring slow or distorted signals in harsh environments. The TLV7021 features an open-drain output stage, making the device an excellent choice for level shifting and flexible system integration. If a push-pull output is required, the TLV701x variant can be used instead.

The comparator reference voltage is generated by a TL431 precision programmable reference, configured to 200 mV in this design. Depending on environmental conditions and system noise levels, the reference can be set to a higher value (for example, 5 V) to increase noise immunity and prevent false triggering.

2.3 Highlighted Products

2.3.1 UCC28742

The UCC28742 is a flyback power-supply controller which provides high-performance voltage regulation using an optically coupled feedback signal from a secondary-side voltage regulator. The device provides accurate constant-current regulation using primary-side feedback. The controller operates in discontinuous-conduction mode (DCM) with valley-switching to minimize switching losses and allow for the use of low cost output rectifiers. The control law scheme combines frequency with primary peak-current amplitude modulation to provide high conversion efficiency across the load range. The control law provides a wide dynamic operating range of output power which allows the power-supply designer to achieve low standby power dissipation. During low-power operating conditions, the power-management features of the controller reduce the device operating current at switching frequencies below 25 kHz. At and above this frequency, the UCC28742 includes features in the modulator to reduce the EMI peak energy of the fundamental switching frequency and harmonics. A complete low-cost and low component-count system is realized using a straight-forward design process.

2.3.2 DRV8220

DRV8220 is an integrated H-bridge driver with multiple control interface options: PWM (IN1, IN2) interface (DRL and DSG packages), PH/EN (DSG only), or half-bridge interface (DSG only). To reduce area and external components on a printed circuit board, the device integrates a charge pump regulator and its capacitors. Both DSG and DRL packages support a timed auto-sleep mode which reduces microcontroller GPIO connections by eliminating a disable/sleep pin and automatically putting the device into a low-power sleep mode when the inputs remain inactive for 1-2 ms. When using autosleep for PWM or PH/EN mode, the nSLEEP pin can be tied high. The nSLEEP pin allows the device to be put to sleep in half-bridge mode where autosleep is not available.

2.3.3 ATL431

The ATL431 and ATL432 are three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and industrial temperature ranges. The output voltage can be set to any value between Vref (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.05 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies.

2.3.4 TL431

The TL431 and TL432 devices are three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between Vref (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies. The TL432 device has exactly the same functionality and electrical specifications as the TL431 device, but has different pinouts for the DBV, DBZ, and PK packages.

2.3.5 TPS55330

The TPS55330 is a monolithic nonsynchronous switching regulator with integrated 5-A, 24-V power switch. The device can be configured in several standard switching-regulator topologies, including boost, SEPIC, and isolated flyback. The device has a wide input voltage range to support applications with input voltage from multicell batteries or regulated 3.3- V, 5-V, and 12-V power rails. The TPS55330 regulates the output voltage with current mode pulse width modulation (PWM) control, and has an internal oscillator. The switching frequency of PWM is set by either an external resistor or by synchronizing to an external clock signal. The user can program the switching frequency from 100 kHz to 1.2 MHz.

2.3.6 TPS259470

The TPS25947xx family of eFuses is a highly integrated circuit protection and power management design in a small package. The devices provide multiple protection modes using very few external components and are a robust defense against overloads, short-circuits, voltage surges, reverse polarity and excessive inrush current. With integrated back-to-back FETs, reverse current flow from output to input is blocked at all times, making the devices a good choice for power MUX and ORing applications as well as systems which need load side energy hold up storage in case input power supply fails. The devices use linear ORing based scheme to make sure almost zero DC reverse current and emulate the best diode behavior with minimum forward voltage drop and power dissipation.

2.3.7 TL7705A

The TL77xxA family of integrated-circuit supply voltage supervisors is designed specifically for use as reset controllers in microcomputer and microprocessor systems. The supply-voltage supervisor monitors the supply for undervoltage conditions at the SENSE input.

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware Requirements

Figure 3-1 shows the top view of the board and different sections of the TIDA-010239 PCB.

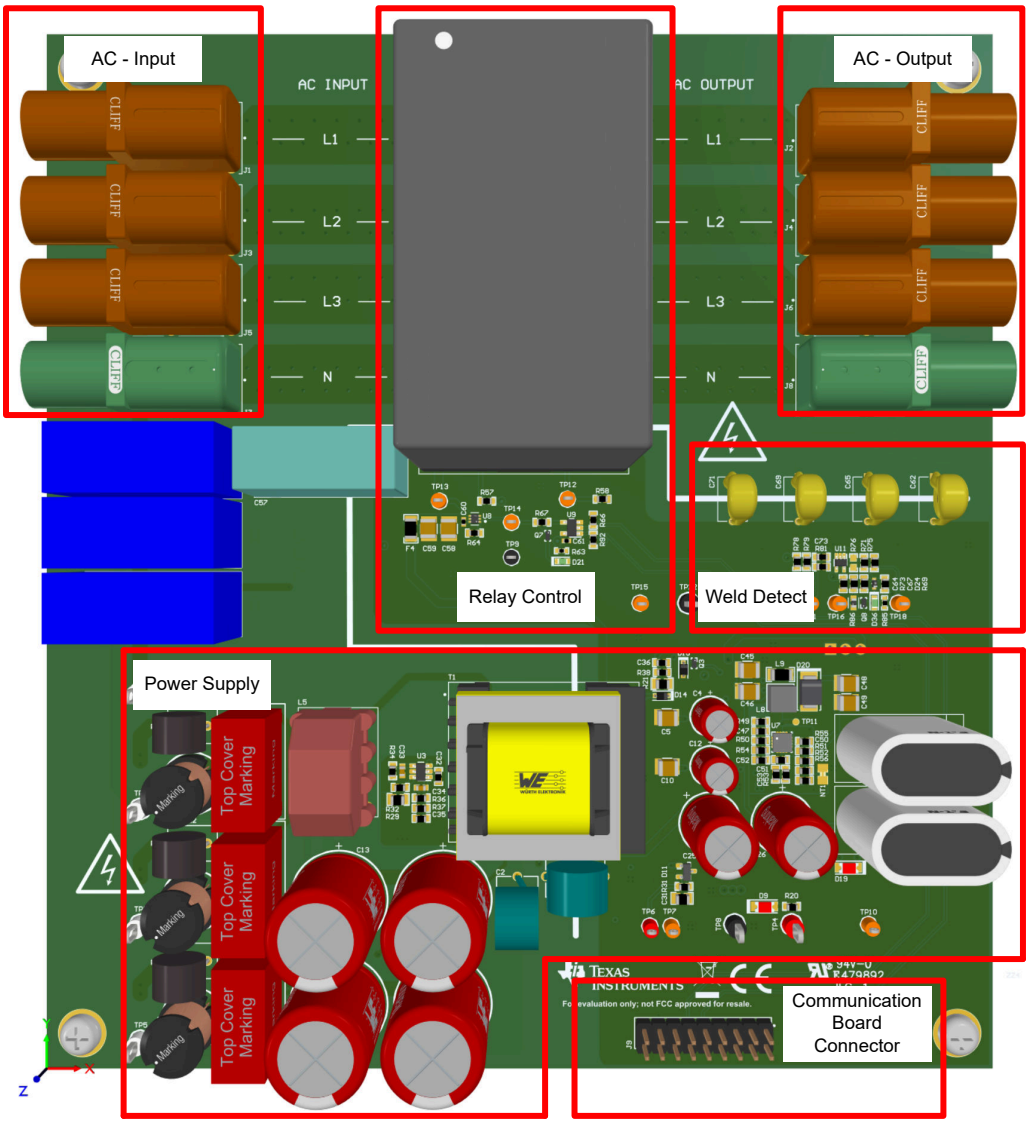


Figure 3-1. TIDA-010239 PCB Top View

3.2 Test Requirements

3.2.1 Power Supply Test Setup

Figure 3-2 shows a block diagram of the external component arrangement and final connections in the test setup.

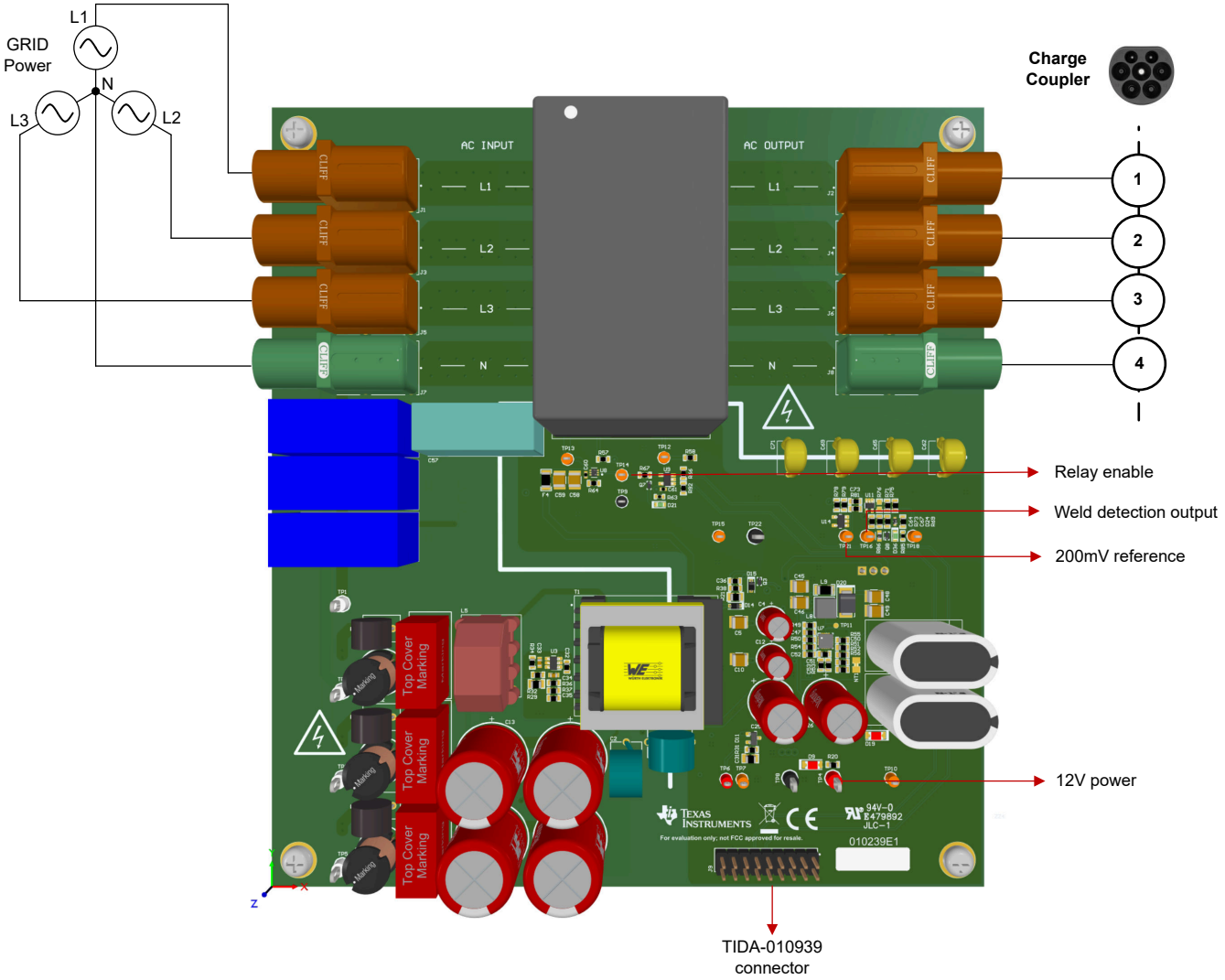


Figure 3-2. External Component Connections With TIDA-010239 Hardware

Figure 3-3 shows the test setup. The test setup for the linear regulator and converters consists of the TIDA-010239 board, DC supply, digital multimeter, electronic load, voltage and current probe.

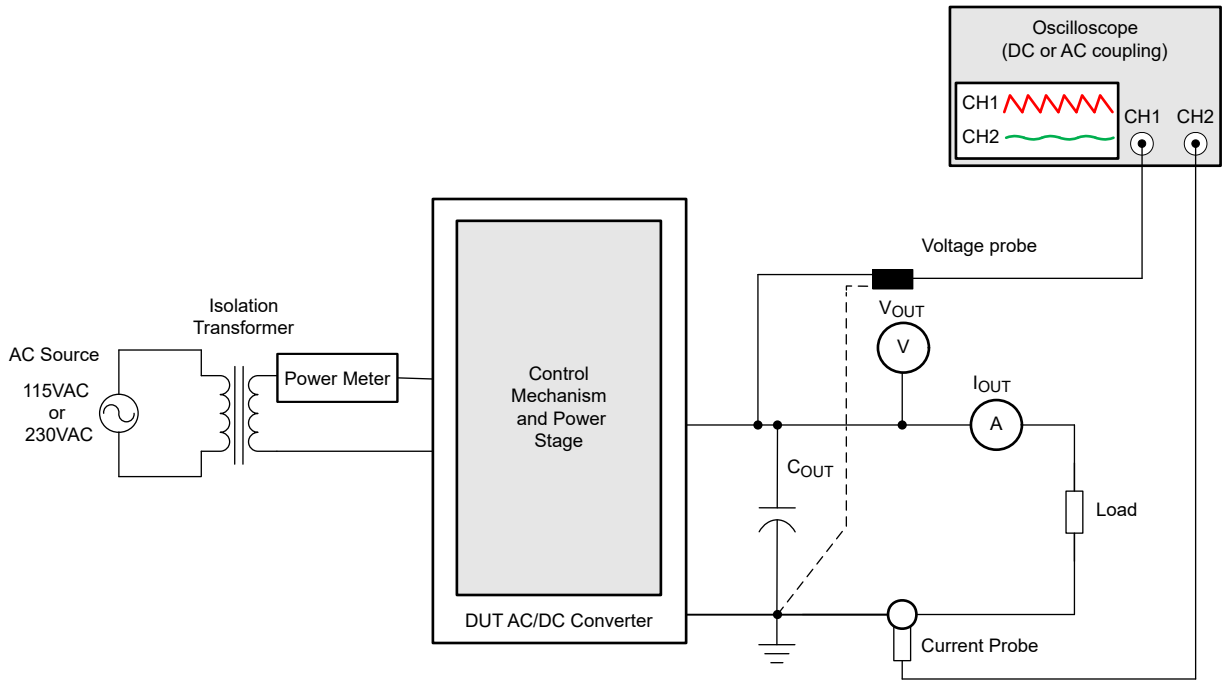


Figure 3-3. Test Setup for Linear Regulator and Converters in TIDA-010239

Note

- DUT is Device Under Test.
- The oscilloscope analog signal bandwidth requires greater than 400 times the switching frequency.
- The oscilloscope requires higher memory depth and sampling rate to capture ripple waveform accurately (at least 4 GSPS, memory depth > 1Mpts).
- Oscilloscope probe terminated to 50 Ω.

The tests conducted for this design are as follows:

- Device efficiency and system efficiency at various loads
- Ripple voltage, ripple frequency at full and light load conditions, output voltage accuracy
- Load transient response

3.2.2 Weld Detect Test Setup

An overview of the weld detect test setup follows:

- The system checks for the AC signal through the comparator U11 when the relay is open. A normal (unwelded) condition means there are no output pulses.
- The system checks for the AC signal through the comparator U11 when the relay is closed. A normal (AC present) condition means there are output pulses.

Complete the following work before powering the TIDA-010239 board.

- Connect the R_ENABLE (J9, pin 9) to external 3.3 V to enable the K1 relay at power up.
- Connect an isolated HV oscilloscope probe 1 to LINE1_IN (TP1). Connect the probe 1 reference clip to neutral (TP5).
- Connect oscilloscope probe 2 to RELAY_CHECK (TP16). Connect the probe 2 reference clip to PGND (TP22).
- Connect oscilloscope probe 3 to the comparator input (TP18). There is no need to connect the probe 3 reference clip.
- Connect oscilloscope probe 4 to Ref_0.2V (TP21). There is no need to connect the probe 4 reference clip.

Supplying power to the board for testing:

- Apply external 3.3 V to the connector J9 pin 6 and external 5 V to pin 5 of the J9 connector.
- Connect GND of the external power supply to one of the ground pins of the J9 connector (pin 7, 8, 13, 14, 17) or to one of the GND test points (TP8, TP9, TP22).
- The measurement can be repeated with the relay open by disconnecting the R_ENABLE from 3.3 V.

3.3 Test Results

3.3.1 Isolated AC/DC Power Supply Based on UCC28742

This section shows test data for efficiency over full-scale load variation, output voltage regulation, output ripple, cross regulation, and transient load response waveforms, and thermal performance. For all measurements shown in the screenshots, VAC is set to 115V_{RMS}, 60Hz with the oscilloscope set to 20MHz bandwidth and in AC coupling (for the voltage ripple measurements).

Note

- +12 V is the 12-V power output (TP4) here called also as *12-Vp*, where *p* stands for *power*.
- +12 Va is the low noise +12-V out of the TPS7A3901.
- –12 Va is the low noise –12-V out of the TPS7A3901.
- 5 V and 3.3 V are the outputs of the TPS563211 buck converters.

3.3.1.1 Efficiency and Output Voltage Cross Regulation

Total zero-load current power consumption (all outputs active, ultra-capacitor charged):

- 115 VAC, 60 Hz: 485 mW
- 230 VAC, 50 Hz: 548 mW

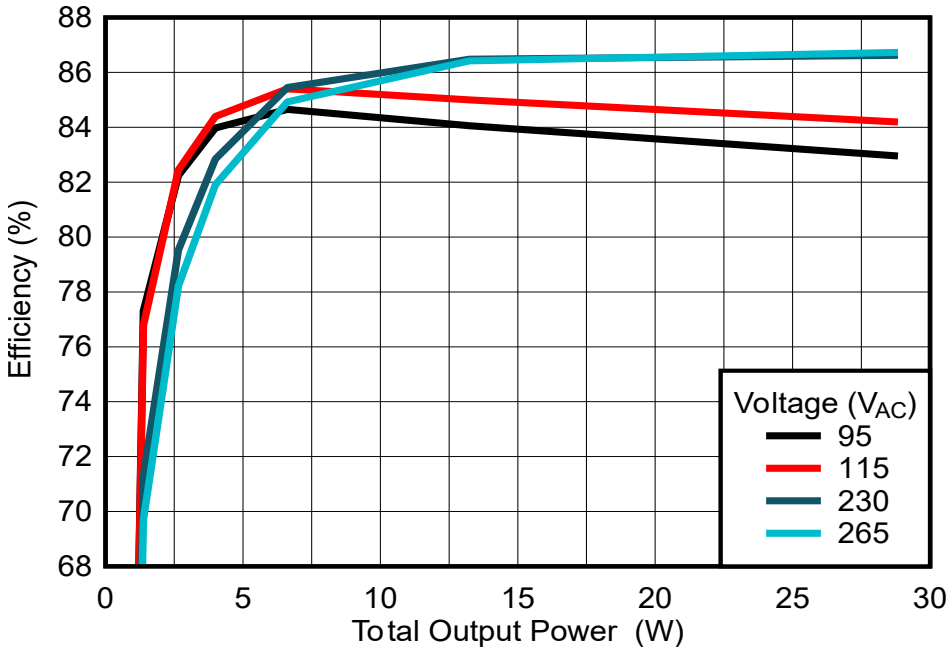


Figure 3-4. Output Power vs Efficiency at 95 V and 115 V AC, 60 Hz; 230 V and 265 V AC, 50 Hz

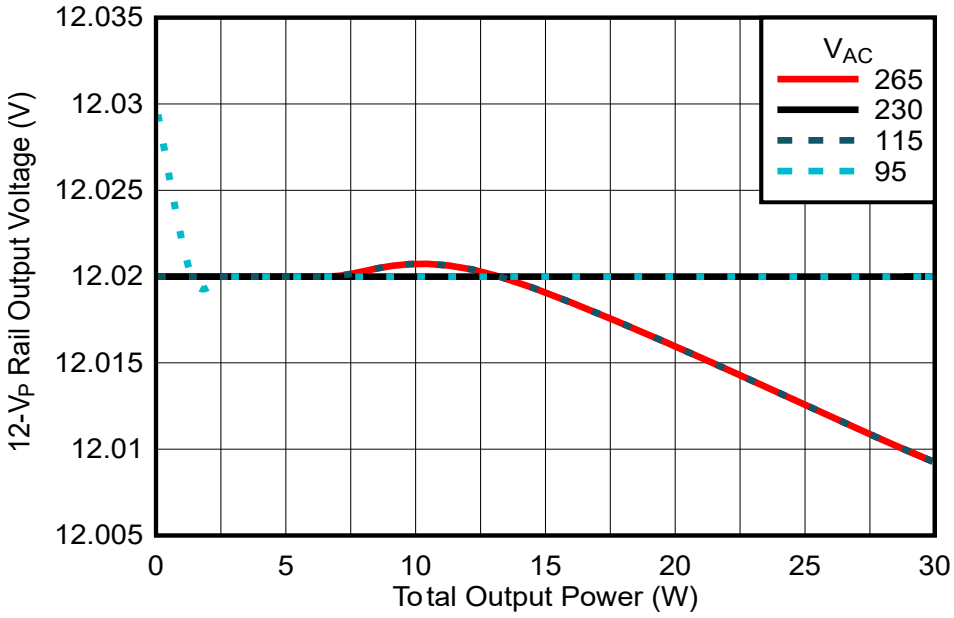


Figure 3-5. Output Power vs Voltage Regulation

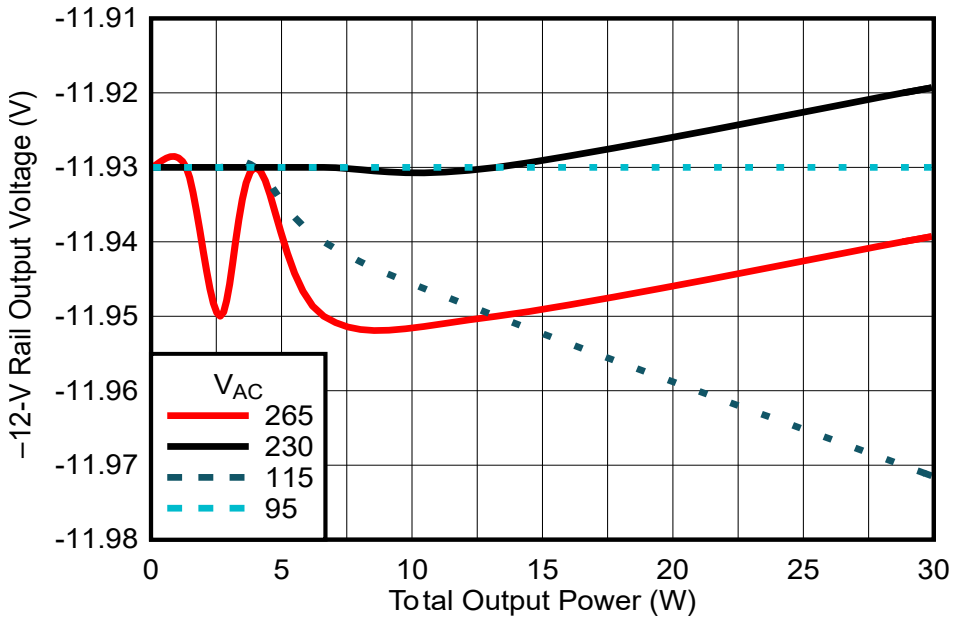


Figure 3-6. Output Power vs Voltage Regulation

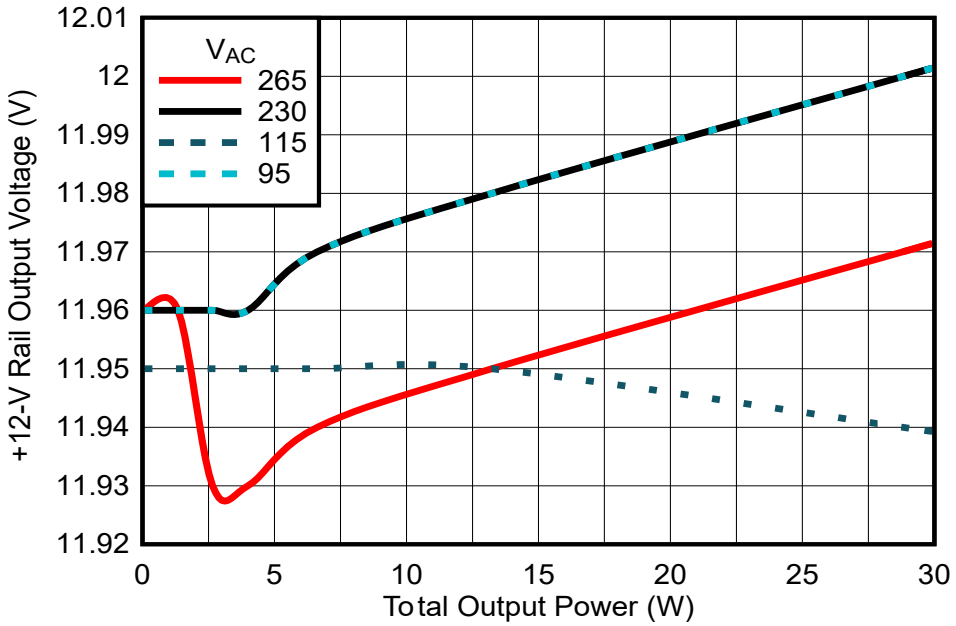


Figure 3-7. Output Power vs Voltage Regulation

Table 3-1. Test Data at 95 VAC, 60 Hz AC Input

P_{IN} (W)	12 Vp (V)	+12 V (V)	–12 V (V)	I(12 Vp) (mA)	I(+12 V) (mA)	I(–12 V) (mA)	P_{OUT} (W)	Efficiency (%)
0.209	12.03	11.96	–11.93	0.00	0.00	0.00	0.00	0.00%
1.782	12.02	11.96	–11.93	104.7	4.98	–4.97	1.38	77.30%
3.225	12.02	11.96	–11.93	200.9	9.97	–9.94	2.65	82.24%
4.759	12.02	11.96	–11.93	302.8	14.95	–14.91	4.00	83.97%
7.821	12.02	11.97	–11.93	501.3	24.94	–24.85	6.62	84.65%
15.745	12.02	11.98	–11.93	1002.0	49.92	–49.71	13.24	84.06%
34.754	12.02	12.00	–11.93	2200.0	100.00	–99.42	28.83	82.95%

Table 3-2. Test Data at 115 VAC, 60 Hz AC Input

P_{IN} (W)	12 Vp (V)	+12 V (V)	–12 V (V)	I(12 Vp) (mA)	I(+12 V) (mA)	I(–12 V) (mA)	P_{OUT} (W)	Efficiency (%)
0.216	12.02	11.95	–11.93	0.00	0.00	0.00	0.00	0.00%
1.753	12.02	11.95	–11.93	102.1	4.98	–4.97	1.35	76.78%
3.219	12.02	11.95	–11.93	201.0	9.96	–9.94	2.65	82.45%
4.735	12.02	11.95	–11.93	302.8	14.94	–14.91	4.00	84.39%
7.752	12.02	11.95	–11.94	501.3	24.90	–24.88	6.62	85.40%
15.570	12.02	11.95	–11.95	1002.0	49.79	–49.79	13.23	85.00%
34.213	12.01	11.94	–11.97	2200.0	99.50	–99.75	28.80	84.19%

Table 3-3. Test Data at 230VAC, 50 Hz AC Input

P_{IN} (W)	12 Vp (V)	+12 V (V)	–12 V (V)	I(12 Vp) (mA)	I(+12 V) (mA)	I(–12 V) (mA)	P_{OUT} (W)	Efficiency (%)
0.308	12.02	11.96	–11.93	0.00	0.00	0.00	0.00	0.00%
1.888	12.02	11.96	–11.93	102.1	4.98	–4.97	1.35	71.30%
3.337	12.02	11.96	–11.93	201.0	9.97	–9.94	2.65	79.53%
4.824	12.02	11.96	–11.93	302.8	14.95	–14.91	4.00	82.84%
7.748	12.02	11.97	–11.93	501.3	24.94	–24.85	6.62	85.45%
15.304	12.02	11.98	–11.93	1002.0	49.92	–49.71	13.24	86.48%
33.280	12.02	12.00	–11.92	2200.0	100.00	–99.33	28.83	86.62%

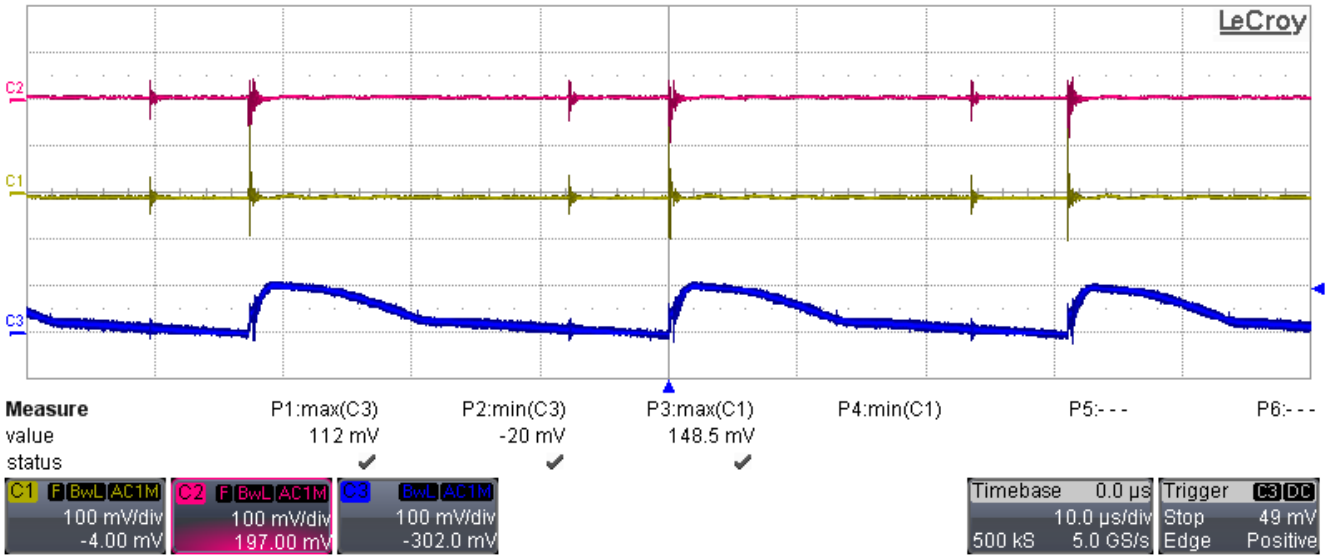
Table 3-4. Test Data at 260VAC, 50 Hz AC Input

P_{IN} (W)	12 Vp (V)	+12 V (V)	–12 V (V)	I(12 Vp) (mA)	I(+12 V) (mA)	I(–12 V) (mA)	P_{OUT} (W)	Efficiency (%)
0.334	12.02	11.96	–11.93	0.00	0.00	0.00	0.00	0.00%
1.932	12.02	11.96	–11.93	102.1	4.98	–4.97	1.35	69.69%
3.391	12.02	11.93	–11.95	200.9	9.94	–9.96	2.65	78.22%
4.878	12.02	11.93	–11.93	302.8	14.91	–14.91	4.00	81.91%
7.795	12.02	11.94	–11.95	501.3	24.88	–24.90	6.62	84.93%
15.312	12.02	11.95	–11.95	1001.9	49.79	–49.79	13.23	86.42%
33.212	12.01	11.97	–11.94	2200.0	99.75	–99.50	28.80	86.73%

Table 3-5. Output Voltage Cross Regulation at 115-V AC, 60-Hz AC Input

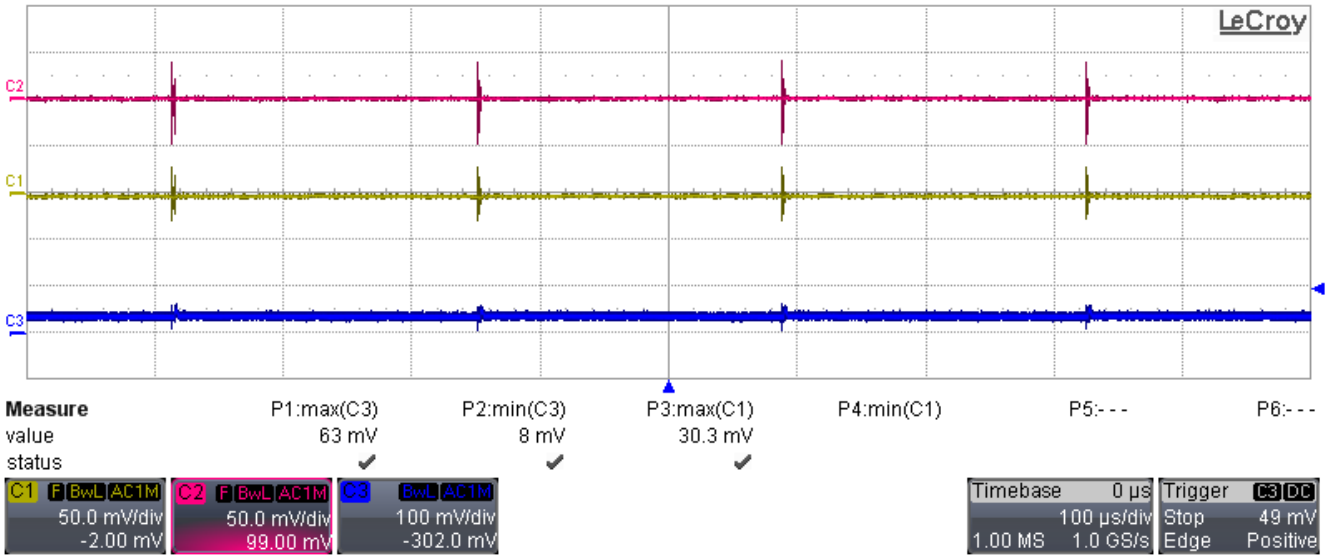
I(12 Vp) (mA)	I(+12 V) (mA)	I(–12 V) (mA)	12 Vp (V)	+12 V (V)	–12 V (V)
2000	100	100.00	12.09	11.95	–11.94
5	100	100.0	12.01	10.88	–10.88
2000	100	0.0	12.09	11.92	–11.93
2000	0	100.0	12.09	11.94	–11.95
50	100	100.0	12.10	11.95	–11.95
0	0	100.0	12.10	11.94	–10.76
0	0	0.0	12.10	11.94	–11.91
0	100	0.0	12.10	10.48	–11.88
2000	0	0.0	12.09	11.94	–11.91

3.3.1.2 Output Voltage Ripple Waveforms



In detail: C1 is –12V output at 100mA, C2 is +12V output at 100mA, C3 is +12Vp at 2.2A

Figure 3-8. Voltage Ripple on –12V, +12V and +12Vp at Full Load



In detail: C1 is –12V output at 0mA, C2 is +12V output at 0mA, C3 is +12Vp at 0A

Figure 3-9. Voltage Ripple on –12V, +12V and +12Vp at No Load

3.3.1.3 Start, Shutdown, Backup Power, and Transient Response Waveforms

Figure 3-10 shows the behavior of the converter during start-up (AC source turned on) with –12 V, +12 V and +12 Vp at full load. C1 is –12-V output at 100 mA, C2 is +12-V output at 100 mA, C3 is +12 Vp at 2.2 A.

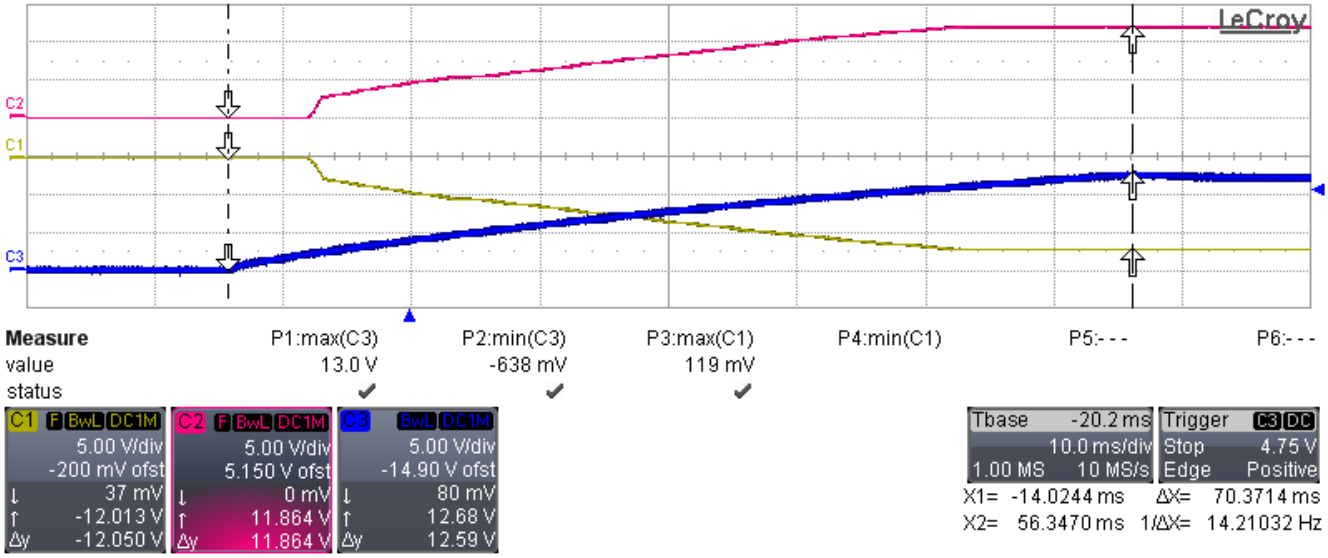


Figure 3-10. Behavior of the Converter During Start-Up

Figure 3-11 shows the behavior of the converter during shutdown (AC source disconnected) with –12 V, +12 V and +12 Vp at full load. C1 is –12-V output at 100 mA, C2 is +12-V output at 100 mA, C3 is +12 Vp at 2.2 A.

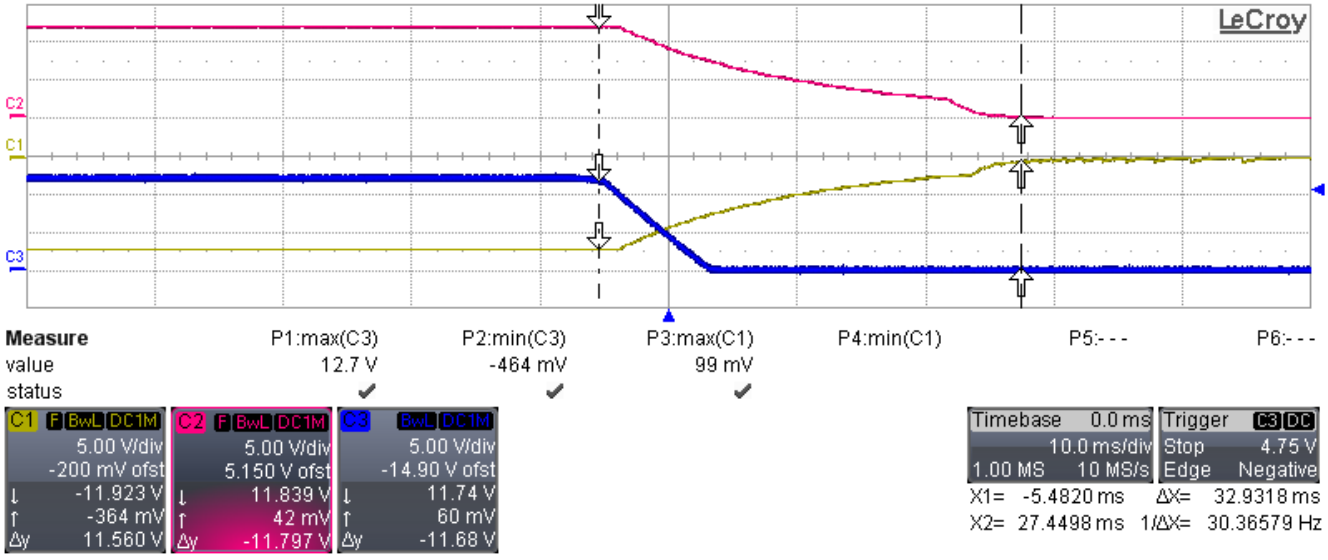


Figure 3-11. Behavior of the Converter During Shutdown

Figure 3-12 shows the behavior of the converter, loaded according to the specifications with 12 Vp at 0.44 A, and 5-V rail at 275 mA. Here the trace C2 is 12-Vp output (TP4_P), C1 is 5-V output and C4 is input VAC.

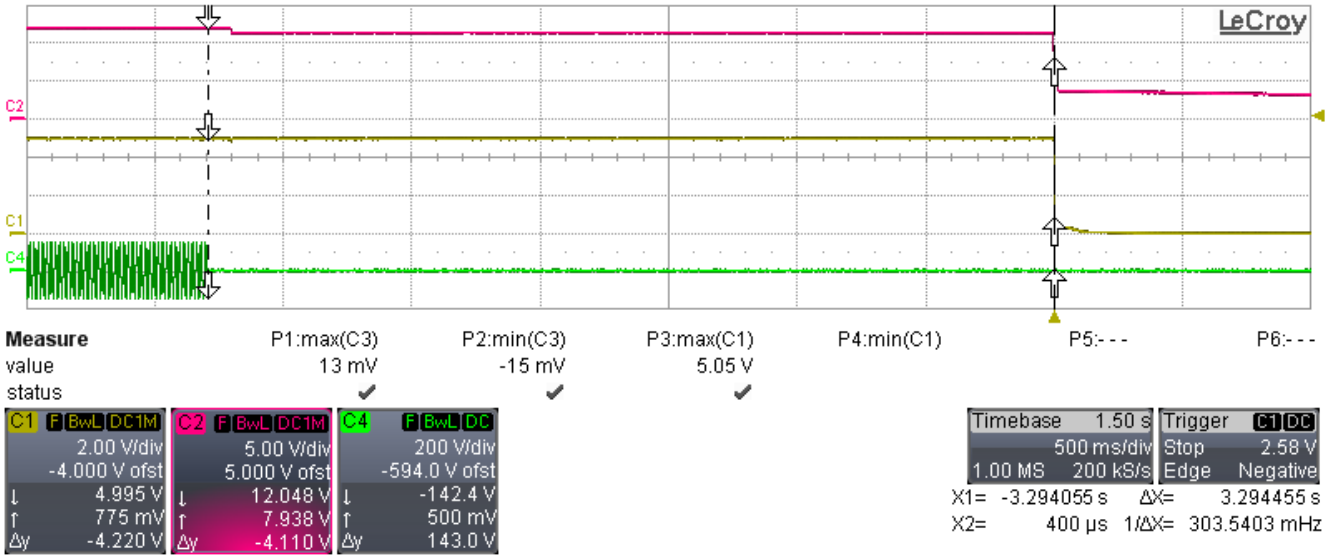


Figure 3-12. Backup Supply Behavior After AC Source is Disconnected

Figure 3-13 shows the transient response of the 5 V_{OUT} when switched between zero and 1 A load current.

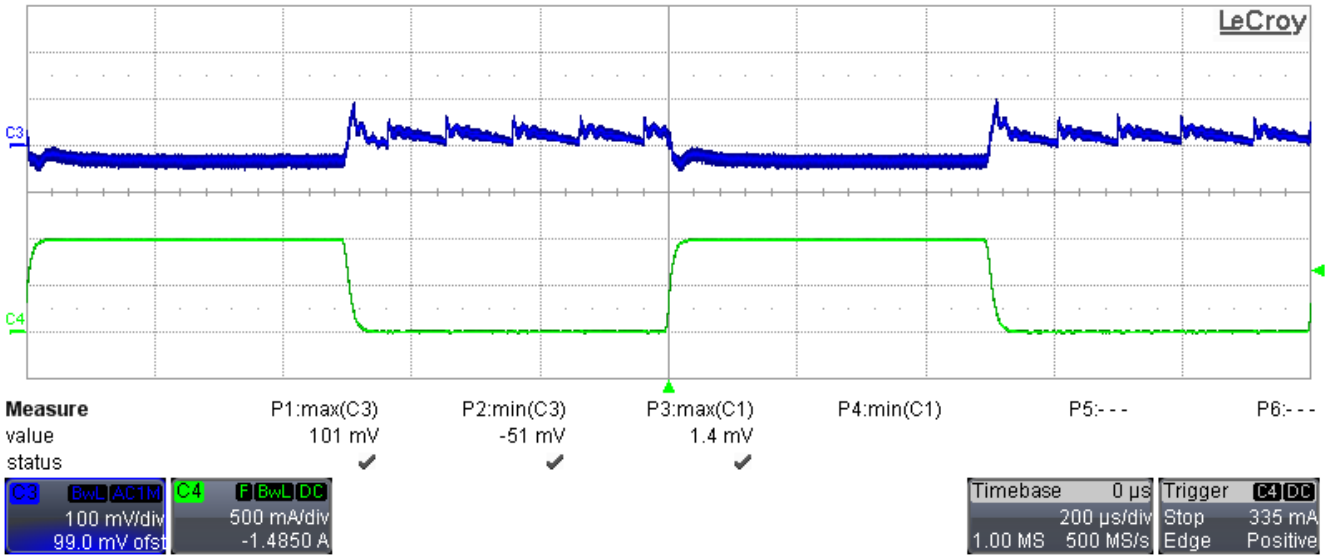


Figure 3-13. Transient on 5 V_{OUT} 0–1 A Load

Figure 3-14 shows the transient response of the 3.3 V_{OUT} when switched between zero and 1-A load current.

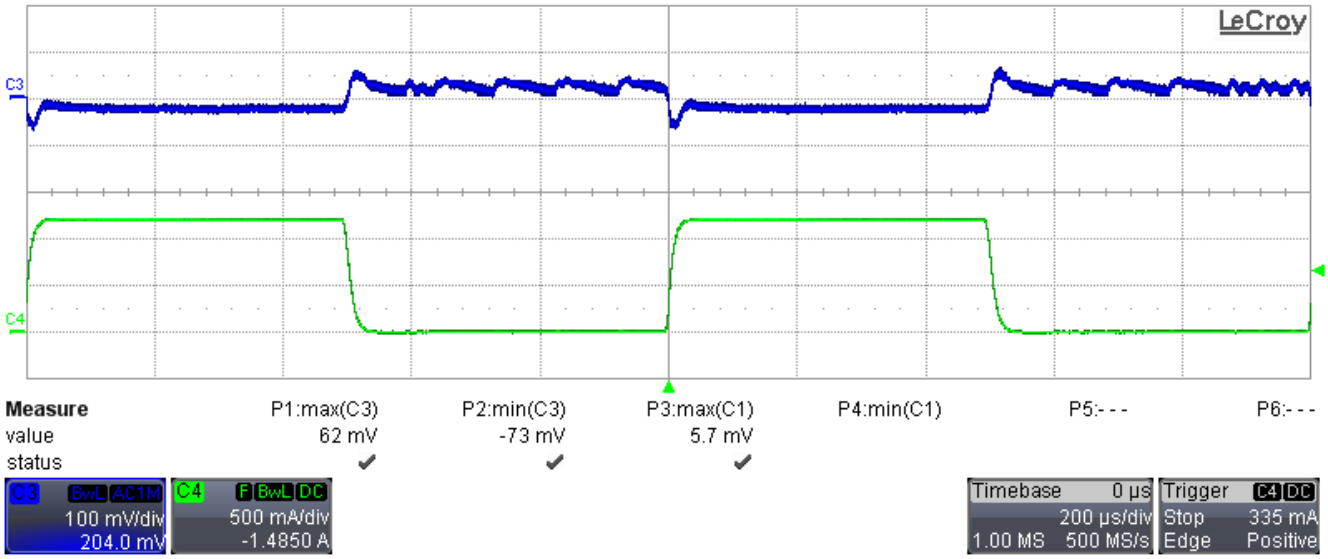


Figure 3-14. Transients on 3.3 V_{OUT} 0 A to 1 A

Figure 3-15 shows the transient response of the converter with zero to 2-A transients on 12 V_{OUT}, while 12 V and –12 V are loaded both at 100 mA. C1 is –12-V output at 100 mA, C2 is +12-V output at 100 mA, C3 is +12 Vp with switched load and C4 is the 12 Vp output current.

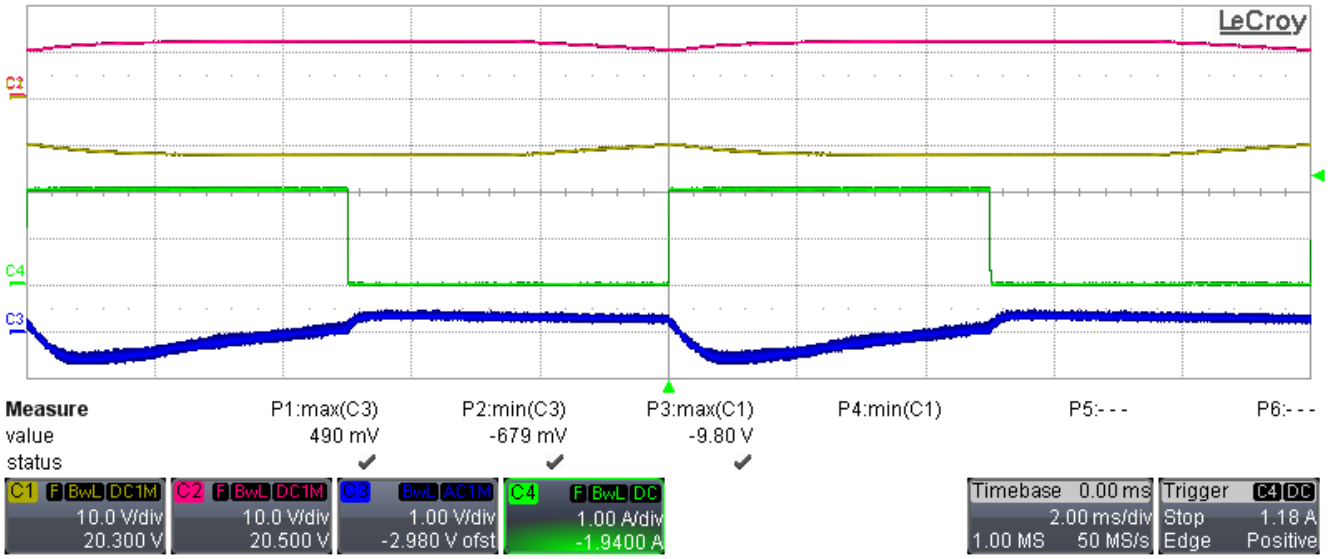


Figure 3-15. Transient Response of the Converter With Zero to 2-A Transients on 12 V_{OUT}

Figure 3-16 shows the transient response of the converter with zero to 2-A transients on 12 V_{OUT}, while 12 V and –12 V are both loaded at zero current. C1 is –12-V output at 0 mA, C2 is +12-V output at 0 mA, C3 is +12 Vp with switched load and C4 is the 12-Vp output current.

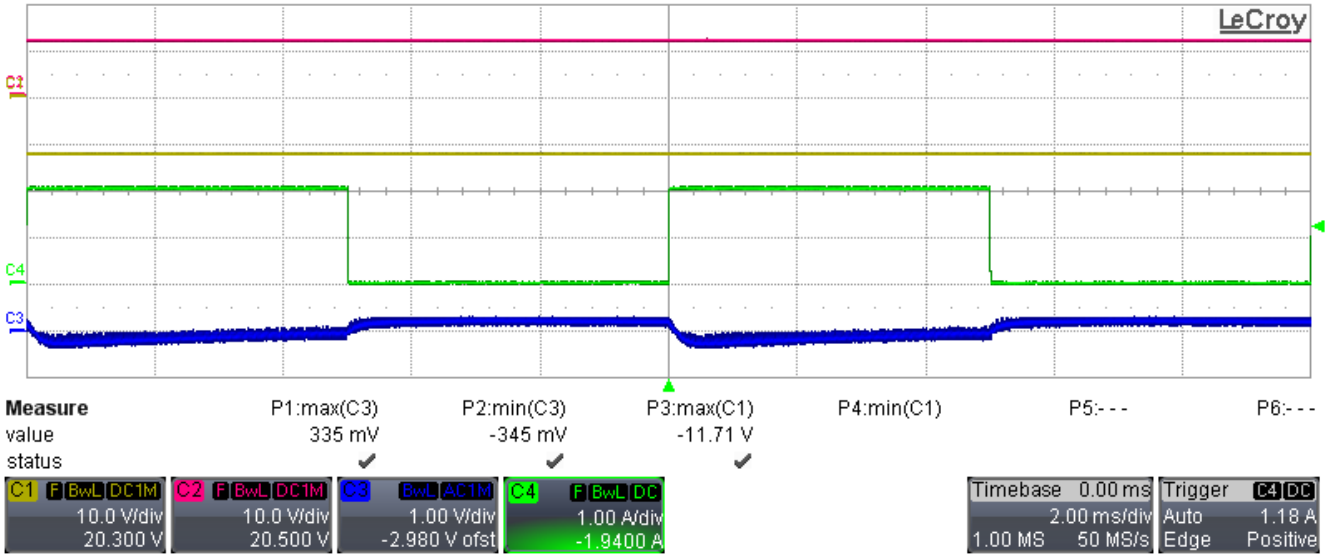


Figure 3-16. Transient Response of the Converter With Zero to 2-A Transients on 12 V_{OUT}

Figure 3-17 shows the transient response of –12-V output with 12 Vp fully loaded. C1 is –12-V output switched from 100 mA to zero and C4 is the –12-V output current.

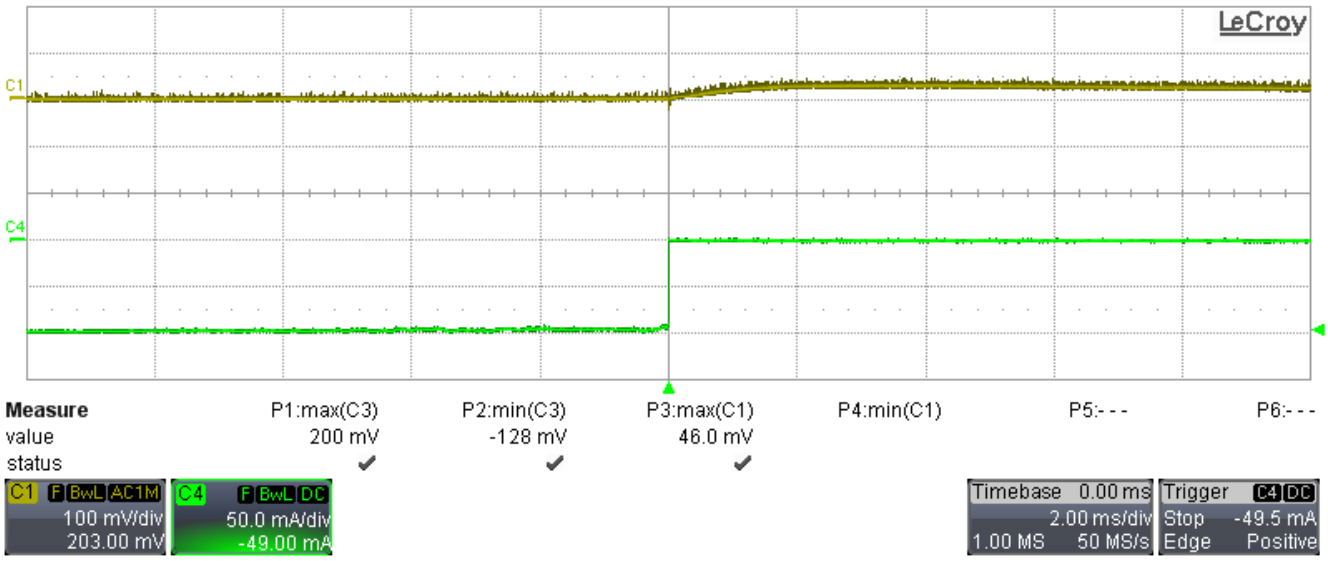


Figure 3-17. Transient Response of –12-V Output With 12 Vp Fully Loaded

Figure 3-18 shows the transient response of –12-V output with 12 Vp fully loaded. C1 is –12-V output switched from zero to 100 mA and C4 is the –12-V output current.

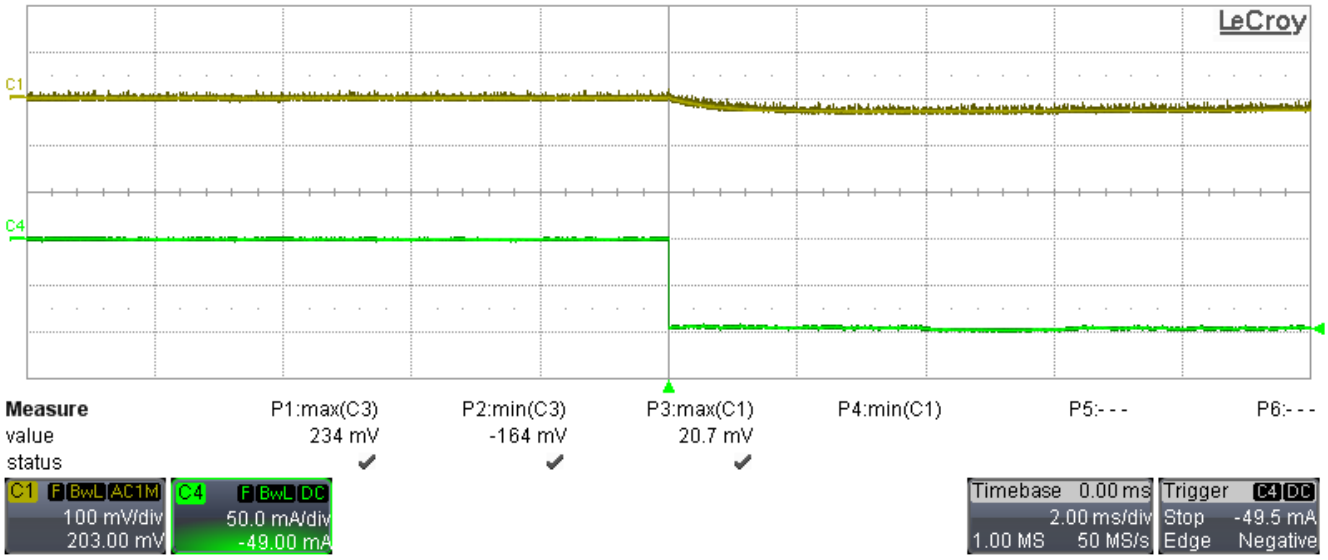


Figure 3-18. Transient Response of –12-V Output With 12 Vp Fully Loaded

Figure 3-19 shows the transient response of +12-V output with 12 Vp fully loaded. C2 is +12-V output switched from zero to 100 mA and C4 is the +12-V output current.

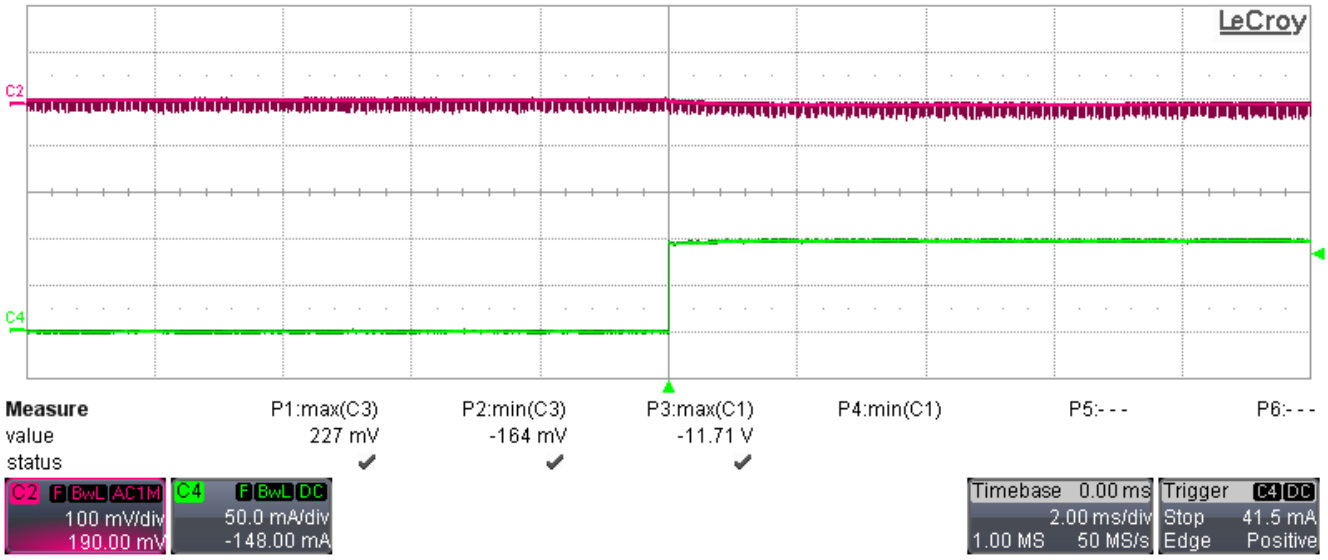


Figure 3-19. Transient Response of +12-V Output With 12 Vp Fully Loaded

Figure 3-20 shows the transient response of +12-V output with 12 Vp fully loaded. C2 is +12-V output switched from 100 mA to zero and C4 is the +12-V output current.

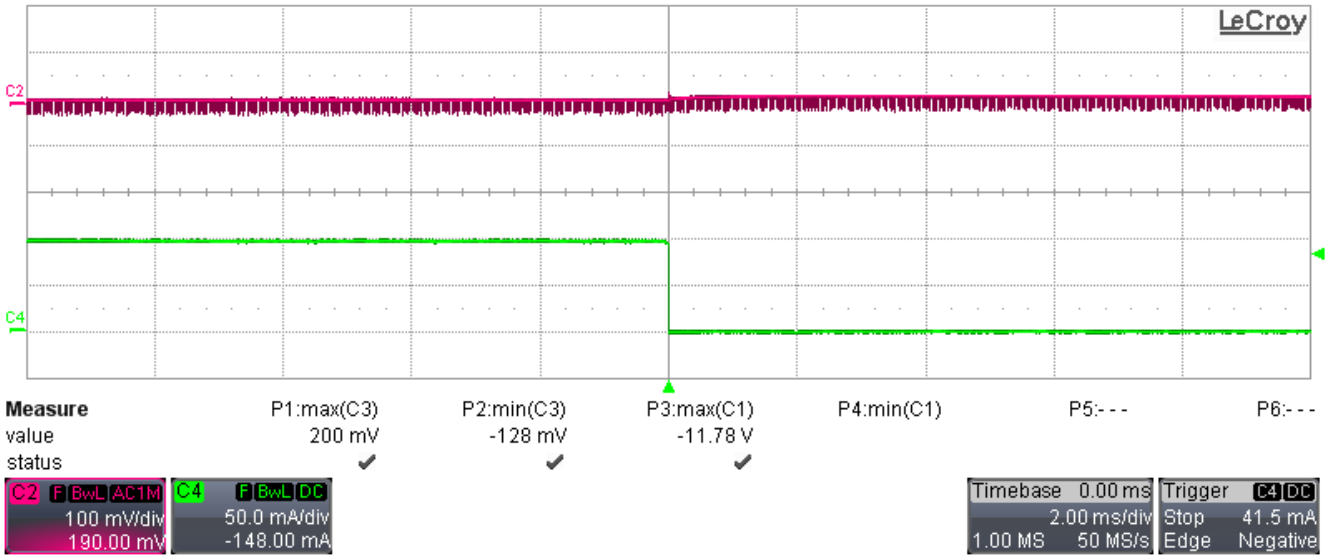


Figure 3-20. Transient Response of +12-V Output With 12 Vp Fully Loaded

3.3.1.4 Thermal Performance

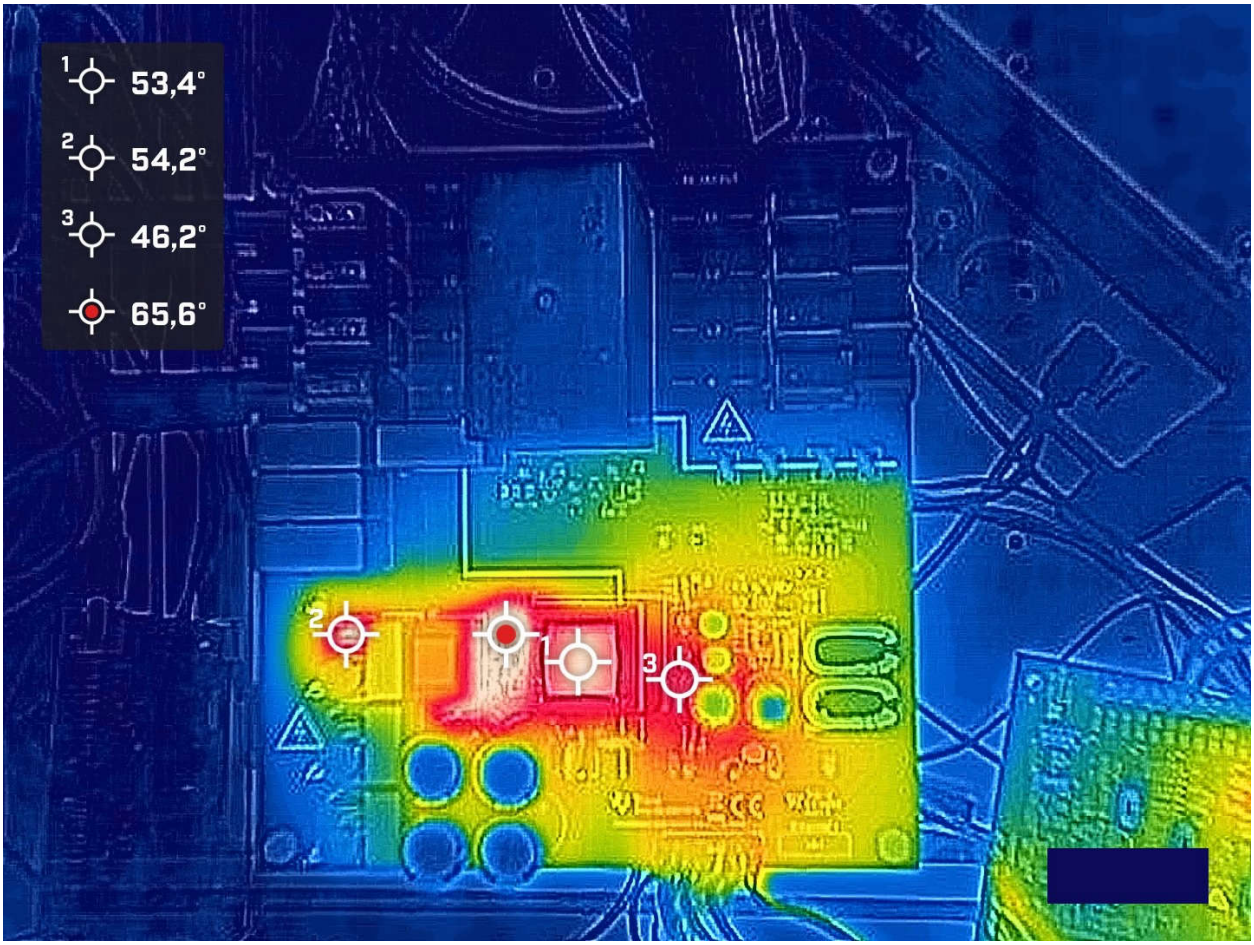


Figure 3-21. Top View of AC/DC Stage at 120-V AC, 60-Hz AC Input, Fully Loaded

Table 3-6. Main Image Markers (Top Side)

NAME	DEVICE	TEMPERATURE	BACKGROUND
Hot Spot	U3	65.5°C	25.5°C
1	T1	53.4°C	25.5°C
2	RT1	54.2°C	25.5°C

3.3.2 DRV8220-Based Relay Drive

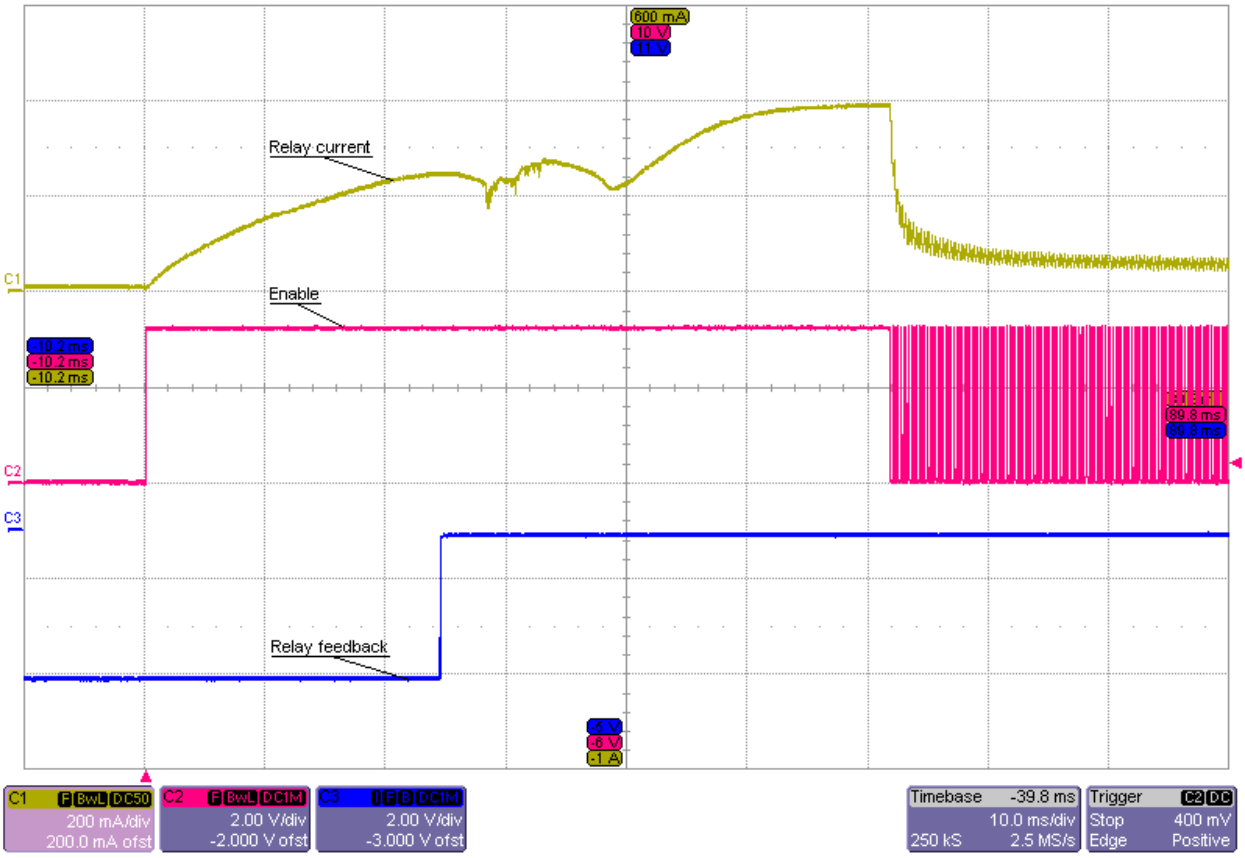


Figure 3-22. Relay Drive Waveforms

3.3.3 Isolated Line Voltage Sensing

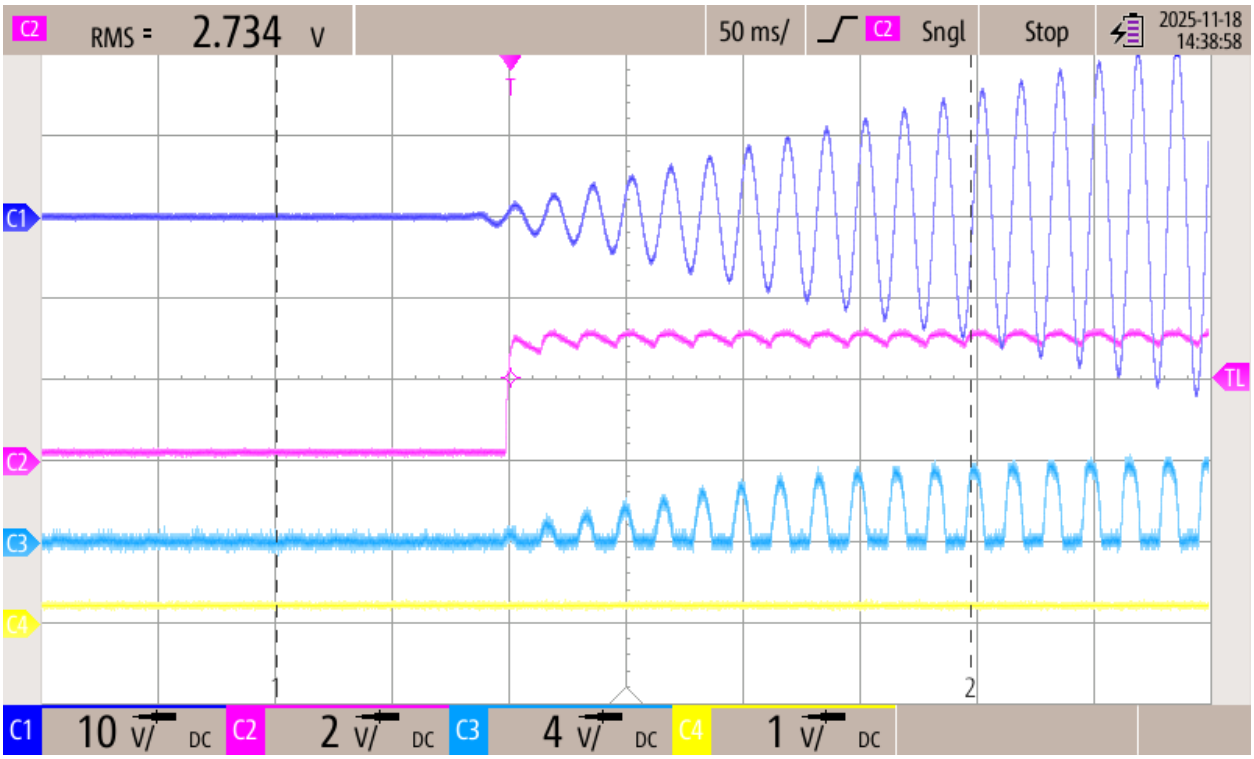


Figure 3-23. Digital Output and Input Line Voltage When Relay is Closed

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010239.

4.1.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010239.

4.2 Documentation Support

1. Texas Instruments, *TIDA-010239: AC level 2 charger platform reference design*
2. Texas Instruments, *TIDA-010939: Electric Vehicle Supply Equipment Front-End Controller Reference Design*

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5 About the Author

KELVIN LE is a systems engineer at Texas Instruments, where he is responsible for developing system solutions for the grid sector with a focus on EV charging. Kelvin has been with TI since 2015. Kelvin earned his Bachelor of Science in Biomedical Engineering from the University of Central Oklahoma and his Master of Science in Electrical and Computer Engineering from the University of Texas at Austin.

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2022) to Revision A (December 2025)	Page
• Changed list of *Resources*	1
• Changed the *Features* section	1
• Updated board image and functional block diagram	1
• Updated *System Description* section including the functional block diagram	2
• Deleted *Control Pilot Signal Interface* section	15
• Deleted *Residual Current Detection* section	16
• Updated *TIDA-010239 PCB* image	21
• Updated *External Component Connections With TIDA-010239 Hardware* image	22

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