Design Guide: TIDA-010275

Industrial Wideband Radio Frequency Sampling Transceiver Reference Design

Description

This reference design is a discrete radio frequency (RF) sampling transceiver supporting instantaneous signal bandwidths up to 5GHz. This RF sampling transceiver offers support to applications such as Radar and Electronic Warfare systems that need wide bandwidth up to X-band.

Resources

TIDA-010275	Design Folder
ADC12DJ5200RF, DAC39RF10	Product Folder
LMK04832, LMX2820, TRF1208	Product Folder
TRF1108, TPSM82913, TPS62916	Product Folder
TPS543620, TPS7A94, TPS63710	Product Folder

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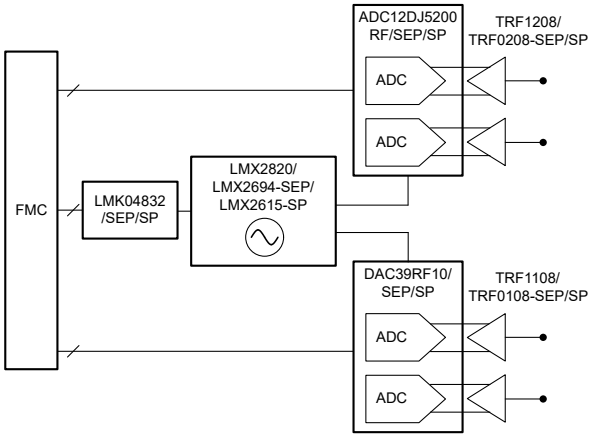
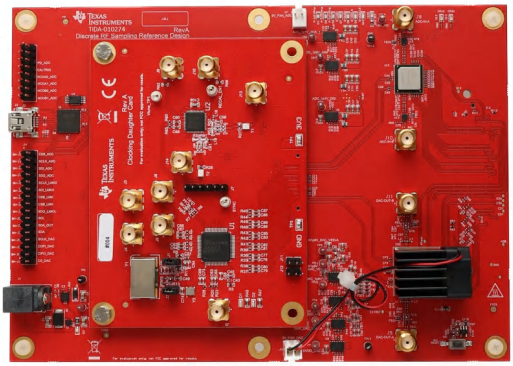
Features

- Up to 5GHz instantaneous bandwidth
- Operation up to X-band
- 10GHz and 5GHz clocking design
- Broadband active data converter interface
- Swappable clocking design
- Swappable power design

Applications

- Radar
- Electronic warfare
- Software defined radio





1 System Description

Communications and radar applications use wide instantaneous bandwidth signals to support large amounts of data. The applications require flexible, configurable designs that can quickly reconfigure in different bands. The RF sampling architecture directly supports applications up to around 8GHz. For applications through Ka-band (27GHz to 40GHz), the RF sampling architecture is used as an IF stage to up- or down-convert to or from the higher frequency.

1.1 Terminology

ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
NCO	Numerically Controlled Oscillator
IF	Intermediate Frequency
LO	Local Oscillator
BW	Bandwidth
OFDM	Orthogonal Frequency Division Multiplexed

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the block diagram of the reference design. Figure 2-2 shows the block diagram of the power design.

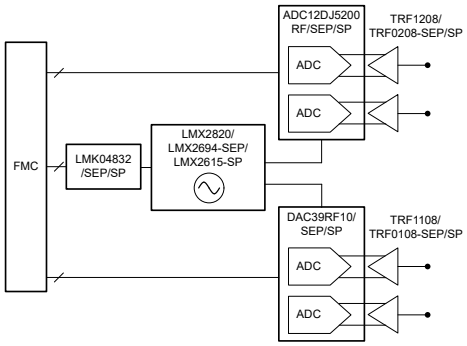


Figure 2-1. TIDA-010275 Block Diagram

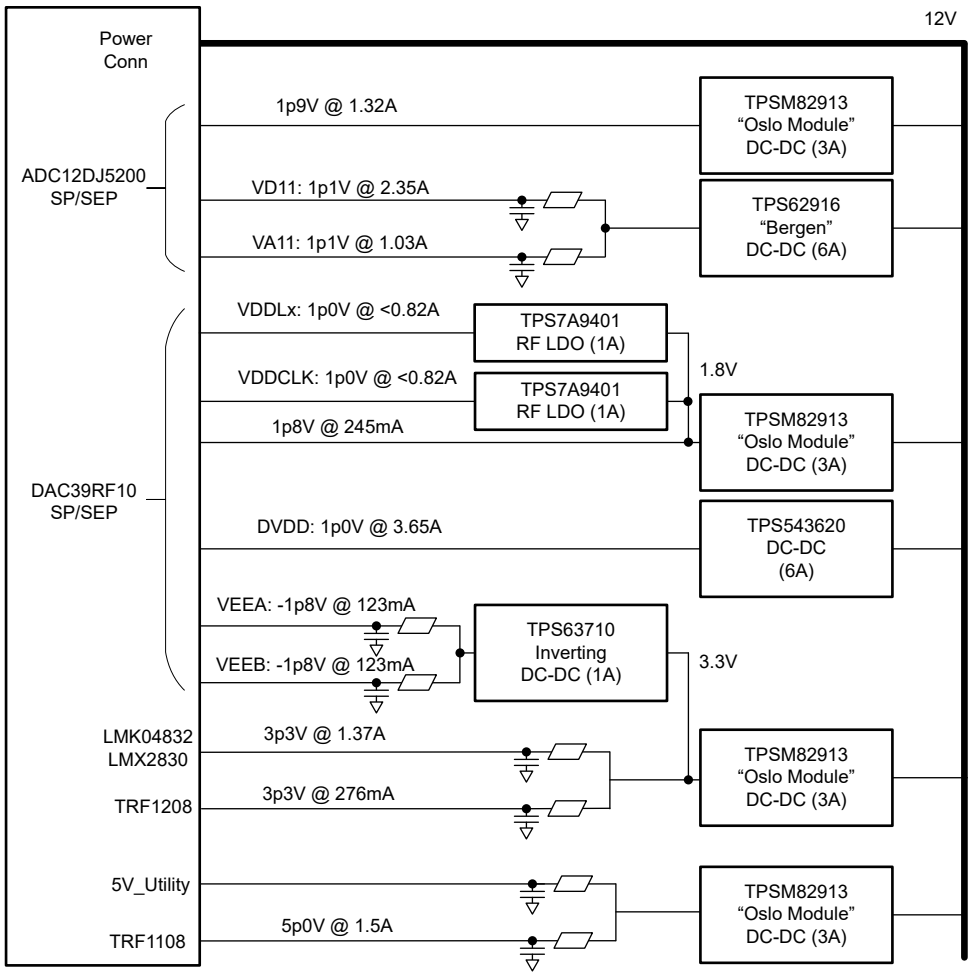


Figure 2-2. TIDA-010275 Power Block Diagram

2.2 Design Considerations

The design is centered on the discrete DAC and ADC devices that support wide, instantaneous bandwidth signals. The receive channels use active baluns to convert single-ended inputs to differential outputs to interface with the ADC input. The transmit channels use a different active balun to convert the differential interface to single-ended. Because industrial, -SEP, and -SP grade parts related to the data converters and active baluns are all in plastic with the same pin-out, a single PCB design supports all grade flavors.

The clocking design is on a daughtercard that snaps onto the top of the data converter board. The clocking daughtercard houses the LMK04832 and the LMX2820 devices. The LMK provides a low-frequency reference to the LMX synthesizer. The LMK also provides the low-frequency clock signals for the FPGA and the SysRef signals to the data converters and FPGA to support the JESD204B digital interface protocol. The LMX2820 provides the low-phase noise, high-frequency sampling clock to the data converters. Because both DAC and ADC clocks come from the same device, the ADC clock must be an integer divider of the DAC clock.

A power design is on a daughtercard that snaps into the bottom of the board. The power board provides all the power rails for the DAC, ADC, clock chips, RF active baluns, and current sensors. The approach generally uses low-noise switchers on the sensitive analog rails to maintain the best performance and efficiency. Standard DC-DC converters provide direct power to less sensitive digital rails.

2.3 Highlighted Products

2.3.1 DAC39RF10

The DAC39RF10 is a RF sampling DAC. The DAC39RF10 supports a sampling rate up to 10.24GSPS. The DAC39RF10 operates in a variety of JESD204B and JESD204C modes supporting wide instantaneous bandwidth up to 10GHz and wide frequency of operation up to 10GHz. The device boasts very low-phase noise performance. On-chip DDS function facilitates generating a CW tone without the need for an FPGA pattern generator.

2.3.2 ADC12DJ5200

The ADC12DJ5200 is a RF sampling ADC. The ADC12DJ5200 supports a sampling clock up to 5.2GHz. In the nominal operating mode the ADC samples up to 5.2GSPS and has two outputs. With dual-edge sampling (DES), the effective sample clock doubles (by using both falling and rising edge of the clock). In this mode, the device has only one channel output but supports 5GHz of instantaneous bandwidth. The device operates in a variety of JESD204B JESD204C modes with a wide frequency of operation up to 8GHz.

2.3.3 LMK04832

The LMK04832 is a high-performance clock conditioner with JESD204B and JESD204C support. The LNK04832 has 14 clock outputs configurable as clock or SysRef outputs and has two phased locked loops (PLLs). The first PLL operates as a jitter cleaner to lock a localized low jitter reference source, like a VCXO, to a low-frequency system reference. The second PLL locks the internal Voltage Controlled Oscillator (VCO) to the low-jitter reference. The device supports dual PLL, single PLL, or clock distribution modes.

2.3.4 LMX2820

The LMX2820 device is a low-phase noise, wideband phase-locked loop (PLL) with an integrated voltage-controlled oscillator (VCO) supporting a frequency between 45MHz to 22.6GHz. The device has two outputs with independent output divider control.

2.3.5 TPS543620

The TPS543620 is a synchronous step-down DC/DC converter capable of driving up to 6A of load current from a supply voltage ranging from 4V to 18V. The device provides exceptional efficiency and output accuracy in a very small design size.

2.3.6 TPSM82913

The TPSM82913 is a low-noise and low-ripple buck power module with integrated ferrite bead filter compensation. The device can output up to 3A of current. The module integrates the power inductor inside the package. This device has the efficiency of a switcher with the noise performance of an LDO. TPSM82913 is an excellent choice for powering sensitive analog and RF devices.

2.3.7 TPS62916

The TPS62916 is a low-noise and low-ripple buck power converter with integrated ferrite bead filter compensation. The device can output up to 6A of current. This device has the efficiency of a switcher with the noise performance of an LDO and is an excellent choice for powering higher power sensitive analog and RF devices.

2.3.8 TPS7A9401

The TPS7A9401 is a low noise, low drop-out (LDO) voltage regulator. The device can output up to 1.0A of current. The low-noise output makes the device an excellent choice for sensitive analog and RF power rails.

2.3.9 TPS63710

The TPS63710 is a low-noise synchronous inverting buck converter that is capable of converting a positive input voltage to a negative voltage. The device supports up to 1A of current. The TPS63710 provides an easy and efficient way to generate a negative supply for sensitive analog rails.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The evaluation of the reference design requires the following hardware:

- TIDA-010275 reference design board
- TSW14J59EVM Rev B (or later)
- Agilent PSA E4445A spectrum analyzer or equivalent
- Rohde and Schwarz SMA100B signal generator or equivalent for input
- Signal generator for 10MHz reference (optional)
- Fixed or variable attenuator
- TSW14J59 power supply (12V, 2A)
- TIDA-010275 reference design power supply (12V, 2A)

3.2 Software Requirements

The evaluation of the reference design requires the following software:

- TIDA-01027x_GUI_v2p0 (or later)
- HSDC Pro GUI (5.0.3 or later)
- AMD Vivado™: Xilinx_HW_Server_Win_2019.1_0524_1430
- TI JESD FW: j59_ui.exe

3.3 Test Setup

Figure 3-1 shows a block diagram of the test setup.

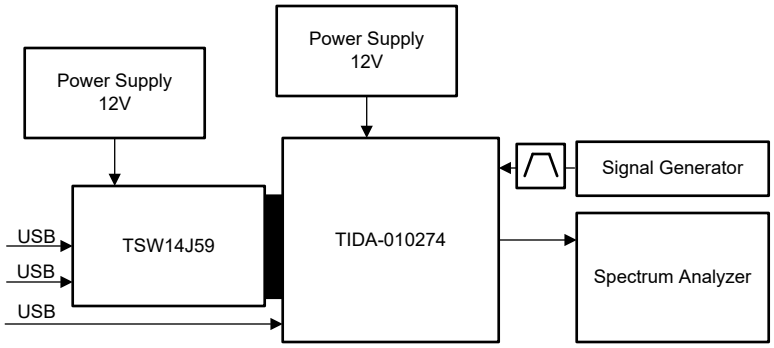


Figure 3-1. TIDA-010275 Test Setup Block Diagram

3.3.1 Test Procedure

Follow Section 3.3.1.1 through Section 3.3.1.5 for the TIDA-010275 test procedure.

3.3.1.1 Initial Hardware Setup

- Connect TIDA-010275 reference design to TSW14J59 pattern or capture card.
- Connect RF cable from DAC output J9 to ADC input J8 through 20dB attenuator.
- Connect 10MHz reference to connector J5 on the clocking board (optional).
- Connect both USB cables to TSW14J59. Connect USB cable to TIDA-010275.
- Connect 12V supply to TSW14J59. Confirm current limit is set to 2A or higher.
- Connect 12V supply to TIDA-010275. Confirm current limit is 2A or higher.
- Connect spectrum analyzer to J11 to monitor DAC output (optional).

3.3.1.2 Initial Power Up

- Engage 12V supply for TSW14J59.
- Engage 12V supply for TIDA-010275. Expect the initial current to be 0.85A.

3.3.1.3 Initial Software Setup

- Launch HSDC Pro GUI version 5.3.03 or later.
  - Select device ADC.
  - Set ADC output data rate to 10G.
- Launch TSW14J59 GUI.
  - Verify software connects to TSW14J59 board.

3.3.1.4 Software Execution

- Launch TIDA-01027x GUI.
- Select and verify Case0 is selected for wide-band mode.
- On the TIDA-01027x GUI, press the *Run* button.
  - Verify the comm error indicator is not on.
  - If the comm error indicator is not on, rerun and check the USB connections and power to the device.
  - Verify current increases to 1.5A.
  - Verify current monitor indicates DAC power at 3.3W and ADC power at 3.8W.

3.3.1.5 Transceiver Capture Procedure

- On `j59_ui.exe`, run script file *Master Transceiver*.
- Wait for the code script to load the pattern, capture data, and transfer to HSDC Pro.
- Verify FFT capture display on the HSDC Pro GUI.

3.4 Test Results

The test signal is a wide-band Orthogonal Frequency Division Multiplexed (OFDM) modulated signal operating at a 5GSPS data rate. The patterns are configured with a 2GHz and 4GHz signal bandwidth. Figure 3-2 and Figure 3-3 show the spectrum performance out of the transmitter.

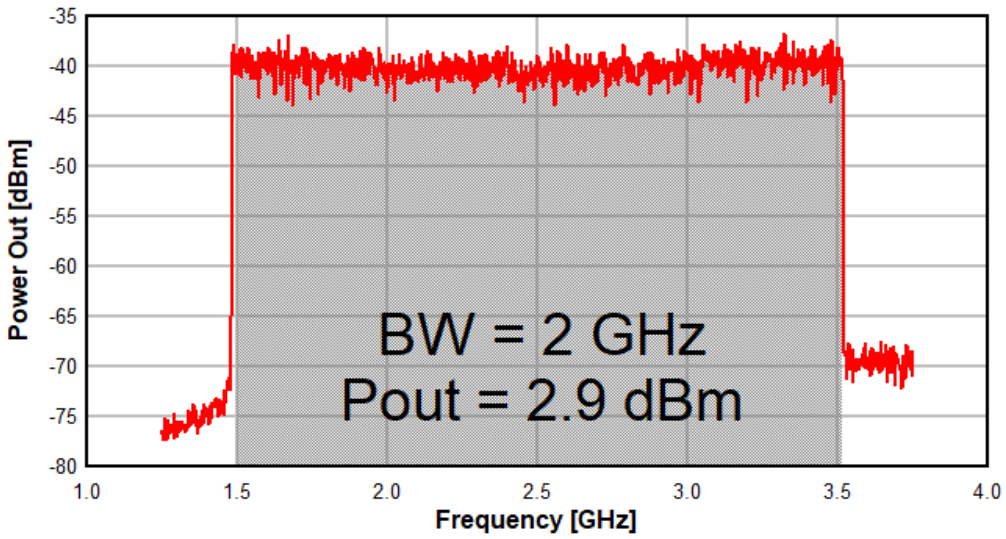


Figure 3-2. DAC Output With 2GHz Wide OFDM Signal

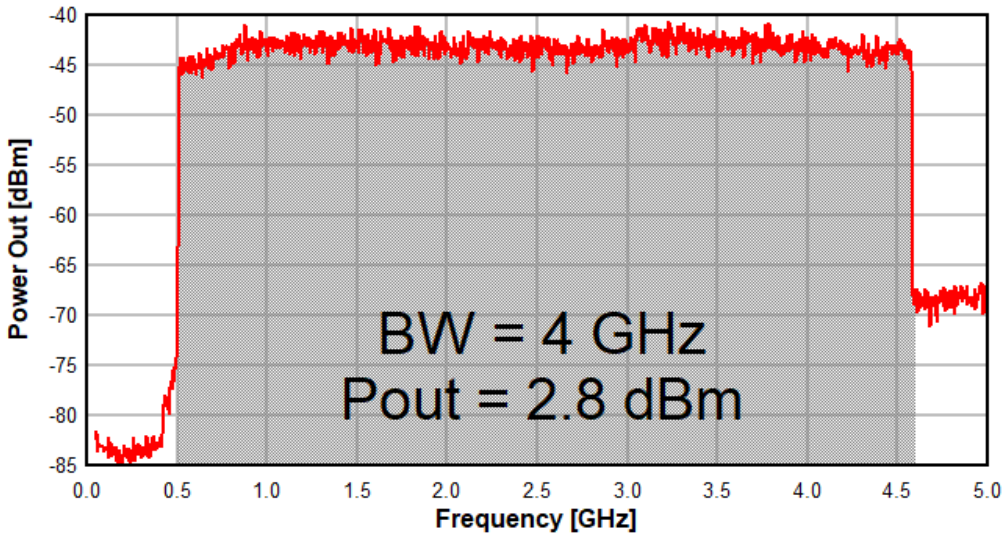


Figure 3-3. DAC Output With 4GHz Wide OFDM Signal

The modulated output signal is looped back to the transmitter through a 20dB attenuator to provide a signal low enough as to not overdrive the receiver. Figure 3-4 and Figure 3-5 show the FFT spectrum of the captured waveform from the receiver.

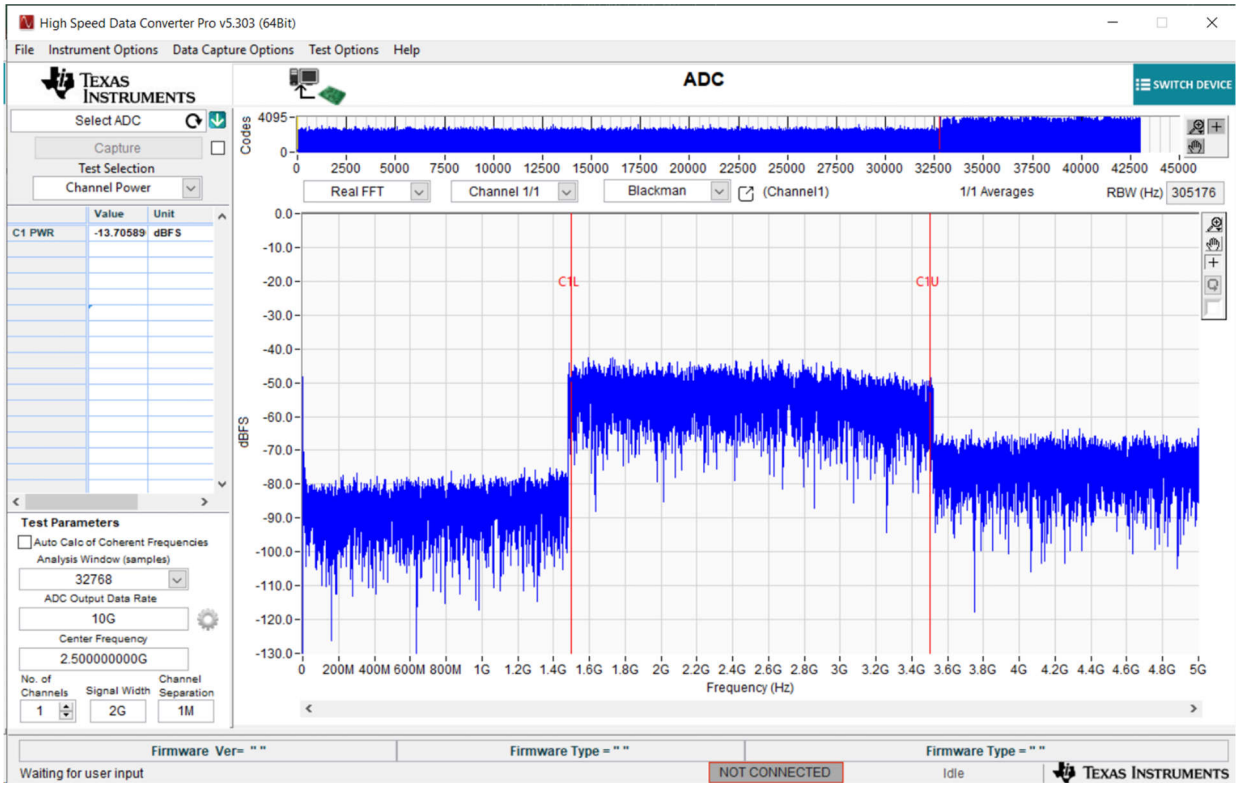


Figure 3-4. ADC Capture of 2GHz Wide OFDM Signal (Loopback)

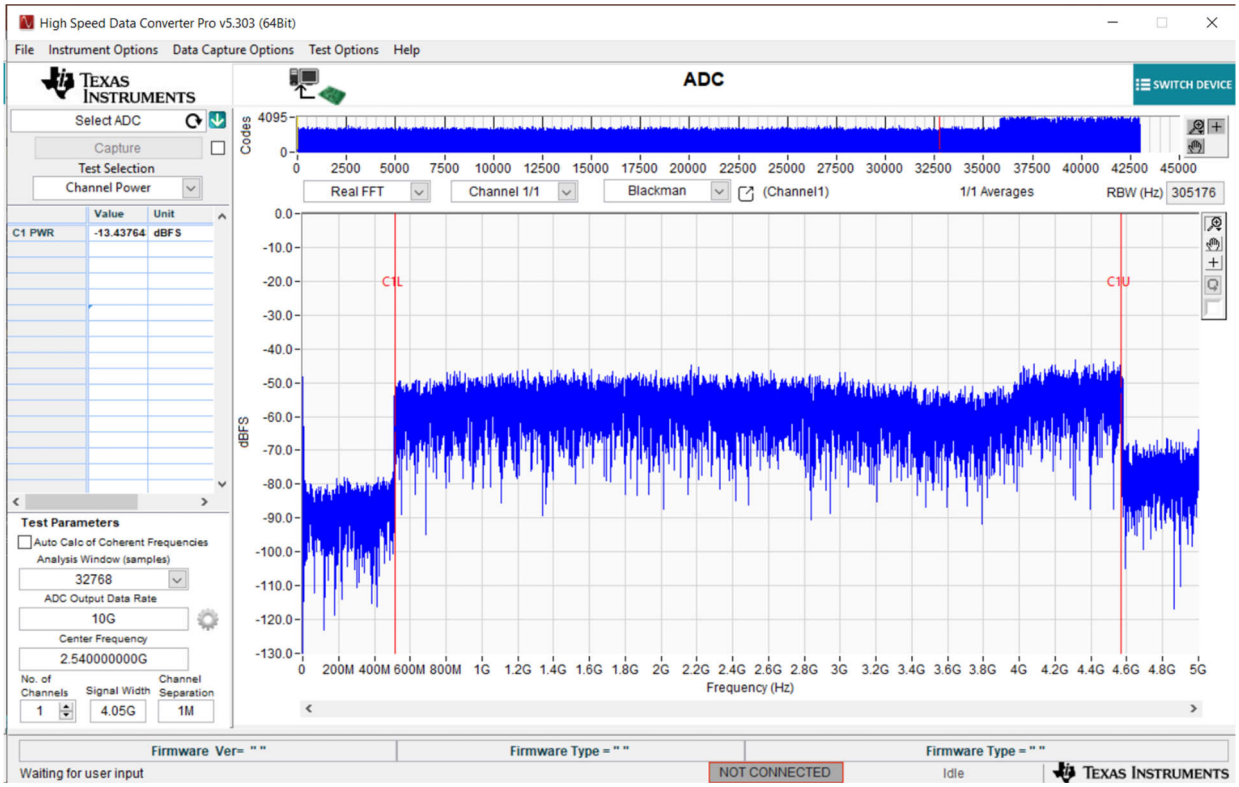


Figure 3-5. ADC Capture of 4GHz Wide OFDM Signal (Loopback)

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010275.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010275.

4.2 Tools and Software

Tools

TSW14J59	JESD204B and JESD204BC Pattern and Capture Card

Software

HSDC Pro	TSW14J59 GUI
TIDA-01027x_GUI_v2p0	TIDA-01027x Programming GUI (version 2.0 or later)

4.3 Documentation Support

1. Texas Instruments, *DAC39RF10, DAC39RFS10 10.24, 20.48-GSPS, 16-bit, Dual and Single Channel, Multi-Nyquist Digital-to-Analog Converter (DAC) with JESD204B, C Interface,* data sheet.
2. Texas Instruments, *ADC12DJ5200-SEP 10.4-GSPS Single-Channel or 5.2-GSPS Dual-Channel, 12-bit,RF-Sampling Analog-to-Digital Converter (ADC),* data sheet.

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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