Design Guide: TIDA-010289

High-Power Amplifier Bias Controller Reference Design

Description

High-power amplifiers (HPA) typically require proper biasing from a power controller in RF front-end transmitters to meet front-end power efficiency requirements. This reference design combines a TI HPA biasing controller with a TI GaN half-bridge power stage to demonstrate variable GaN HPA gate-biasing control along with GaN HPA gate or drain pulsing.

Resources

TIDA-010289	Design Folder
LMG2100R026	Product Folder
AFE20408	Product Folder
TLV709A01	Product Folder
TPS7A3001	Product Folder
LP5907	Product Folder

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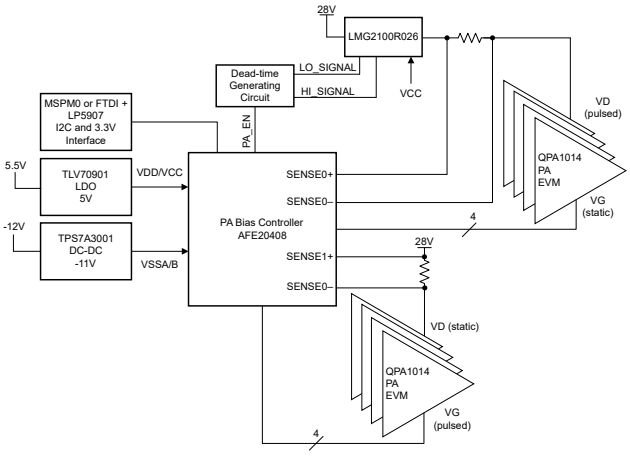
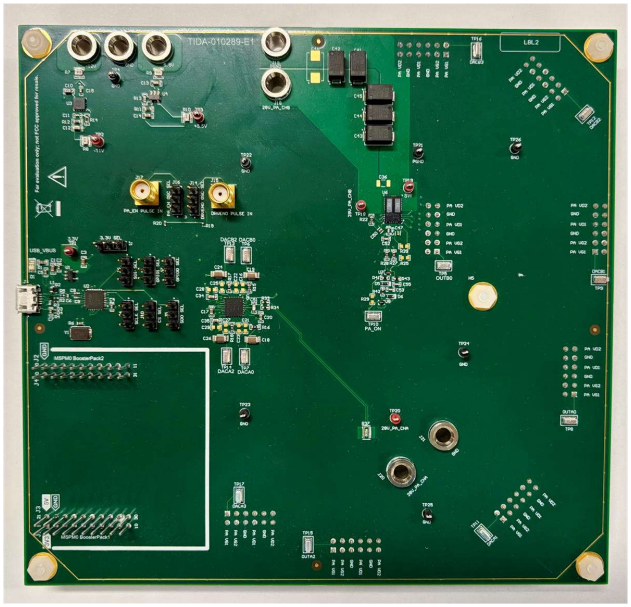
Features

- Pulsed drain or gate of HPA configuration
  - 70ns drain rise time and 88ns gate rise time
- Up to 28V supply on HPA drain
- Optional SPI or I^2C interface with the MSPM0 BoosterPack™ Plug-in Module
- Integrated current and HPA drain monitoring
- Power sequencing features to provide proper bias to power amplifiers (PA)

Applications

- Radar
- Electronic warfare
- Seeker front end
- Software defined radio



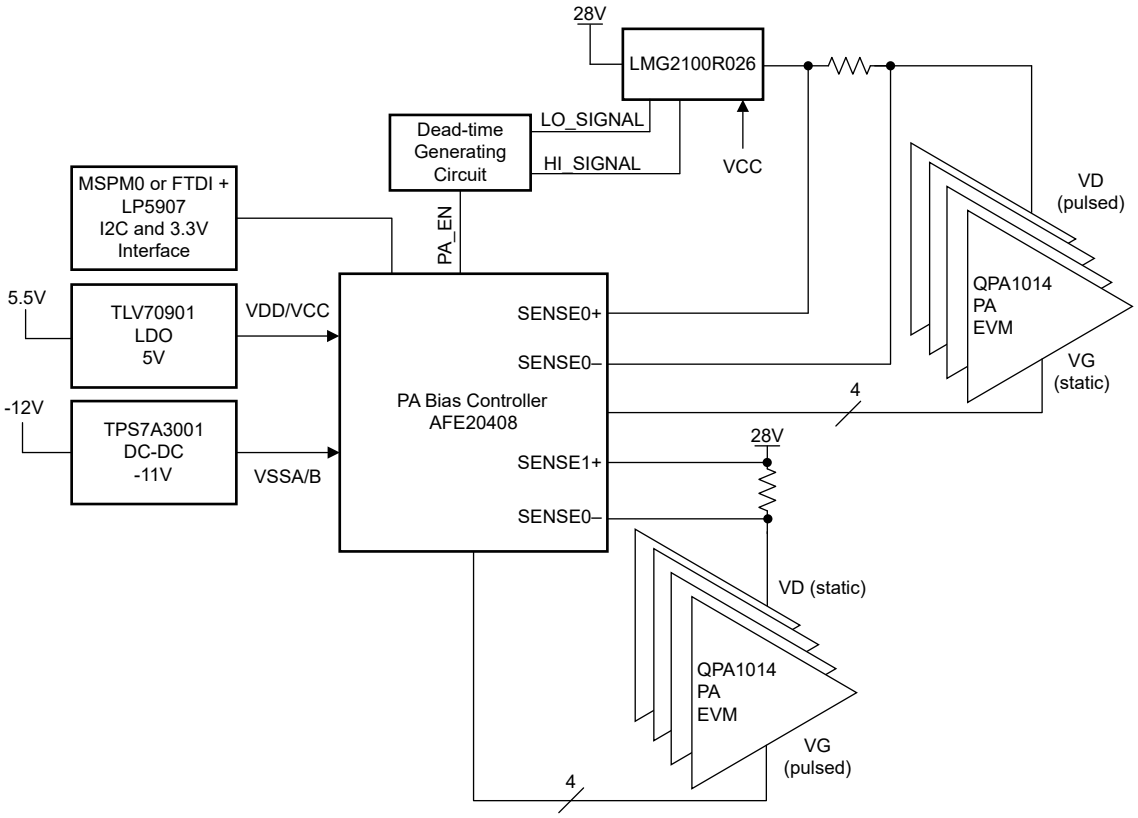


1 System Description

Defense applications, such as radar, electronic warfare, and seeker front ends, transmit RF signals utilizing high-power amplifiers to amplify the signal with enough power to overcome channel losses in often-contested RF environments. Of particular interest is the GaN HPA which provides higher power density, better linearity at given power levels and better efficiency than traditional laterally diffused metal-oxide-semiconductor (LDMOS) HPAs. HPAs dominate performance of the transmitter front end in linearity and efficiency. HPAs also are costly in terms of power consumption. Appropriately biasing and monitoring the HPA bias point improves efficiency and reduces operating costs. The drain current changes based on factors such as temperature, drain voltage, and gate voltage. The drain or gate bias voltage needs to be varied as the HPA changes in temperature over operational time to maximize output efficiency. Operators monitor HPA drain current and temperature to improve reliability. This monitoring enables adjustments to be made to drain or gate voltage levels. Adjustments compensate for changes in HPA drain current levels. The PA biasing circuit traditionally is designed discretely with some GaN bias modules that can be > 125mm^2 for just a single output. In the center of this reference design is Texas Instrument's AFE20408 single chip that can monitor and bias up to eight HPAs with an 80% size reduction in biasing circuitry. The AFE20408 offers a standalone gate biasing design that can be toggled on and off. This can be paired with a half-bridge power stage to provide a two-chip drain pulsing and monitoring system for multiple HPAs.

2 System Overview

2.1 Block Diagram



2.2 Design Considerations

In the HPA control and monitoring system, either the gate or the drain biasing point is modified to achieve the desired efficiency of the HPA and maintenance of a consistent HPA drain current. In applications, such as pulsed RADAR, not only is the gate or drain bias point of the HPA modified but the gate or drain is pulsed between a pinch-off voltage and the bias-on voltage. Additionally, to set the correct bias point the temperature and the drain current of the HPA can be monitored and fed back into a controller to determine the correct HPA bias point to keep the drain current constant under operation of the HPA to maintain efficient operation of the HPA and avoid HPA damage. Designers assess critical design factors when building an HPA bias control and monitoring system. In this section, the key considerations discussed include:

- Driver and slew rate control to facilitate safe drain pulsing
- Power dissipation in FETs when drain pulsing
- Storage capacitor bank design on HPA drain

2.2.1 Half-Bridge Topology

The half-bridge power stage on the drain of the HPA controls the pulse rise time and fall time, the duty cycle, and pulse width. The half-bridge power-stage topology on the HPA drain allows the pulse rise and fall time to be driven to either the 28V rail or the 0V rail correlating to if the high-side FET or low-side gate of the FET is being driven. The rise- and fall-time speeds can be determined by the resistor values on the high-side GaN FET source pin and the VCC pin of the half bridge, respectively. By increasing the resistor values, the overshoot and ringing can be reduced at the expense of decreasing slew rate speeds.

The PWM input into the driver of the half-bridge power stage determines the pulse width and duty cycle of the pulsing sequence. In this reference design, the PA_ON signal from the PA bias controller is being passed through a dead-time generating circuit to provide a complementary PWM signal with a dead-time band to prevent both FETs from being driven high at the same time and thereby preventing damage to the half bridge. At a high level, the dead-time generating circuit consists of two inverter paths each with an RC circuit that produces a complementary PWM signal with a dead-time band on the input of the driver of the half-bridge power stage. Increasing the resistors on each inverter path increases the dead-time band which minimizes the risk of turning on both FETs at the same time. The reference design has the ability to attach an MSPM0 BoosterPack onto the board and wires can be connected from two PWM pins on the MSPM0 to the high and low inputs to the half-bridge power stage driver (make sure to unpopulate the resistors connected to the high and low inputs of the half-bridge power stage). Using the MSPM0 BoosterPack in this manner allows for drain pulse control while bypassing the dead-time generating circuit.

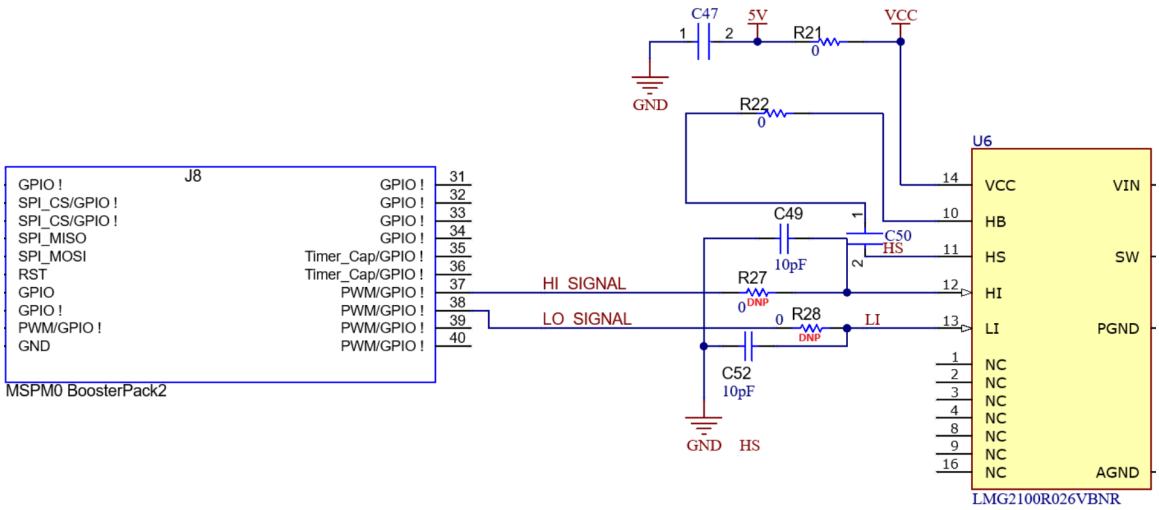


Figure 2-1. MSPM0 Wiring Diagram

2.2.2 Power Dissipation Design Consideration

The power dissipation through the FETs need to be considered to show that the thermals are tolerable for the system when implementing a half-bridge implementation for hard switching to generate the drain pulse. The following formulas and system parameters are useful to consider when calculating power loss going through the half-bridge FETs and comparing between different half-bridge architectures for the system.

Conduction loss formula: $I^2 \times R_{DS(on)} \times D$ (1)

Gate charge loss formula: $V_{IN} \times Q_{OSS} \times f_{SW}$ (2)

Output capacitance losses formula: $V_{IN}{}^2 \times C_{LOAD} \times f_{SW}$ (3)

where

- D is duty cycle as a percentage
- f_{SW} is switching frequency
- C_{LOAD} is load capacitance
- I is the output current
- V_{IN} is the input voltage
- $R_{DS(on)}$ and Q_{OSS} are defined in the half-bridge power stages or MOSFET data sheet

The losses above can be multiplied by the junction-to-board thermal resistance found in the thermal information of the half-bridge power stages or MOSFET data sheet to calculate the temperature rise of the end user's board.

2.2.3 HPA Drain Capacitor Bank Design

Designers must select a capacitor bank capable of handling fast slew rate loads during on and off switching operations in HPA applications. The design requires the correct value of capacitance based on the maximum current expected, the maximum pulse width expected, and the acceptable amount of voltage droop during the pulse. The impedance and equivalent series resistance (ESR) must also be assessed to show that the switching frequencies are not limited by the bandwidth of the design when selecting capacitors. The equations used to solve for the amount of capacitance and maximum impedance needed to handle the load transient are as follows:

$I = C\ (dV/dt)$ (4)

$Z_{TARGET} = \Delta V_{OUT} / I_{Step}$ (5)

where

- I is the maximum allowable current
- C is total capacitance
- dV is the voltage droop
- dt is the maximum pulse width
- Z_{TARGET} is the target impedance
- ΔV_{OUT} is the allowable ± swing on VOUT during a transient
- I_{Step} is the load transient step size

For this reference design, the maximum allowable current is 3.7A driven by the recommended operating condition for drain current (under drive) in the HPA data sheet. The maximum pulse width assumed is 100µs and a voltage droop of 7.5% on the 28V HPA drain rail. These yield the capacitance on the input of the half-bridge power stage device driving the HPA drain. The current and voltage droop can be plugged into the second equation as I_{Step} and ΔV_{OUT} to yield the target impedance. Using the target impedance and capacitance, a capacitor selection tool from a capacitor vendor can be leveraged to determine which capacitor selections meet impedance and ESR over the desired bandwidth.

2.2.4 Gate and Drain Pulsing Considerations

The AFE20408 has up to eight outputs that can be utilized to set the gate bias of eight HPAs and each one can be pulsed between the desired bias point and the pinch-off voltage. The OUT pins can quickly pulse with fast rise and fall times determined by the difference in capacitance between the DAC setting the high-voltage level and the corresponding OUT (for example, DACA0 corresponds to OUTA0, DACA2 corresponds to OUTA2, and so forth). However, the DACA1, DACB1, DACA3, and DACB3 pins have a slower rise time but maintain a fast fall time when pulsing due to higher impedance switches on these outputs. To quickly pulse eight HPAs, an alternative design consideration is to pulse the half bridge leading into the drain of the HPA and then use the eight outputs of the AFE20408 to bias voltage incrementally throughout the operation of the system.

2.2.5 Additional Considerations

This reference design pairs with the Qorvo GaN HPA QPA1014 EVM through the J22 to J29 headers at a recommended operating drain voltage of 28V.

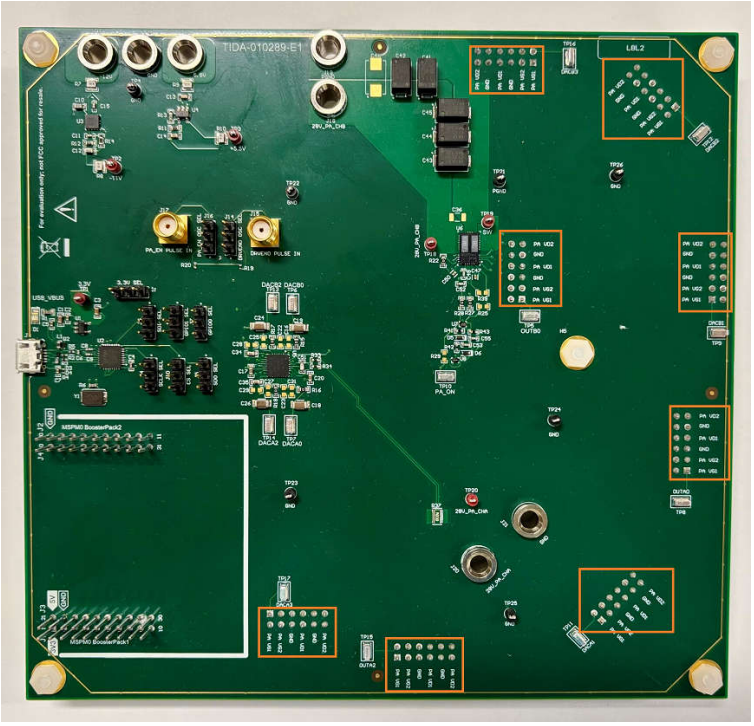


Figure 2-2. TIDA-010289 Board: J22 Through J29 Highlighted

In general, GaN HPA can exceed this voltage up to around 50V and the power rail pin mapping into the HPA EVMs vary between EVMs. To make this reference design compatible with other HPAs, the pin mappings on J22 to J29 need to be assessed with the intended EVM to evaluate to check for differences and make any needed adjustments. The designer also needs to replace the capacitor bank with capacitors that have the appropriate power deratings. See the *HPA Drain Capacitor Bank Design* section of this design guide to verify the capacitance, impedance, and ESR of the capacitor bank can support the higher power transients. The LMG2100R026 selected is a 93V continuous, 100V pulsed, 53A half-bridge power stage supplying the drain voltage can support GaN HPAs even for higher power levels.

The QPA1014 EVM gate voltage range has an upper limit of 0V. The gate voltage range of the AFE20408 is selected based off the VSS and the VCC pins for the lower and upper voltage limits, respectively. A higher voltage limit of up to 10V can be selected by tying the VCC pins to a 10V rail but this requires rework of the reference design.

2.3 Highlighted Products

2.3.1 AFE20408

The AFE20408 PA bias controller drives the gate voltage of the HPA interface using eight output pins (that is, all four OUT pins, DACA1, DACB1, DACA3, and DACB3 pins) with two independent A and B channel groups. The output voltage of the AFE20408 can be toggled to any voltage within the voltage range set by the VCC and VSS inputs for either of the two channel groups. The eight outputs can be pulsed between a high and low voltage within the voltage range of the AFE20408 by the DRIVEN0 pin or internal registers. The AFE20408 has two pairs of current sense and voltage sense pins to monitor drain current and voltage of the HPA.

2.3.2 LMG2100R026

The LMG2100R026 is a half-bridge GaN power stage used to pulse the HPA drain supply on and off. The LMG2100R026 is fed a high signal and a low signal from a dead-time generating circuit on the board sourced from the PA_EN GPIO signal to drive the HPA between the 28V to 0V. As an alternative option, the MSPM0 can be mounted to the board and configured with the two complementary PWM signals with programmable dead-time generation. The LMG2100R026 is also capable of driving the drain of the HPA to higher voltage such as 50V which is common among GaN HPAs. Alternative TI half-bridge GaN power stages include the LMG2100R044 and LMG5200 that can be considered when deciding upon switching the HPA drain. Additionally, using external FETs with TI's half-bridge drivers LMG1210 and LMG1205 can also be considered as shown in the *Design Considerations for LMG1205 Advanced GaN FET Driver During High-Frequency Operation* application note.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

Evaluation of the reference design requires the following hardware:

- TIDA-010289 reference design board
- Signal generator for gate pulsing (optional)
- QPA1014 HPA or equivalent -10V to 0V gate input and 28V drain input HPA
- Power supplies (12V and 5.5V, 10mA and 28V, 4.5A)
- USB A to USB micro-B cable
- MSPM0L1306 BoosterPack or equivalent device with SPI (optional)
- Tektronix 3 Series oscilloscope or equivalent

3.2 Software Requirements

Evaluation of the reference design requires the following software:

- TIDA-010289_GUI_v1p0 (or later)

3.3 Test Setup

This section shows how to set up and test the reference design. Figure 3-1 shows the test setup of the reference design.

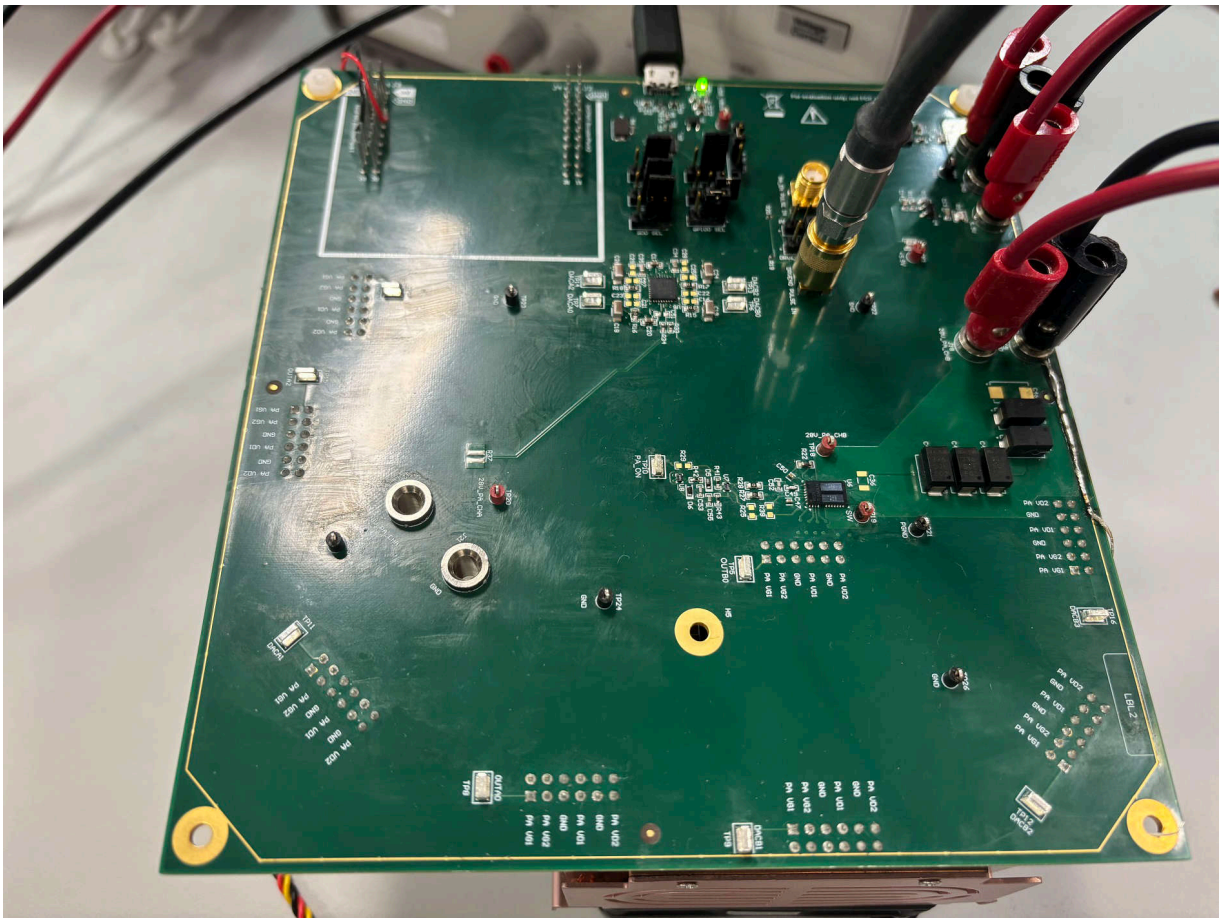


Figure 3-1. TIDA-010289 Test Setup

3.3.1 Initial Hardware Setup

- **Power Supply Input** - Connect the –12V input to J11 and the +5.5V input to J12 using J13 as the ground reference for both. Set the current limit for the power supply at 10mA. Engage the –12V and 5.5V supply.
- **Enable Jumpers** - Place a shunt across pin 1 and 2 of the following six headers: J1, J4, J5, J6, J7, and J10. If using the MSPM0 Booster Pack with the reference design to drive the 3.3V, SPI, and GPIO0 signals, then place a shunt between 2 and 3 instead of the aforementioned headers.
- **Plug in USB cable** – Plug in a cable with a USB micro-B plug into the onboard receptacle (J3) and then connect the other end of the cable into a computer.

3.3.2 Install HPA

To evaluate the LMG2100R026 drain pulsing paired with the AFE20408 PA bias controller:

- Plug the HPA EVM into any of the following headers: J23, J25, J27, or J29.
- Connect the 28V input to J18 and J19 (GND) and set current limit based on HPA drain current limit.
- Engage the 28V supply.

To evaluate the AFE20408 PA bias controller without a drain pulse enable:

- Plug the HPA EVM into any of the following headers: J22, J24, J26, and J28.
- Connect the 28V input to J20 and J21 (GND) and set current limit based on HPA drain current limit.
- Do not engage the 28V supply until the associated pinch off gate voltage (see Bias up and down the HPA section).

3.4 Test Results

The test results shown in this section use the following test conditions:

- HPA EVM plugged into J29 (unless otherwise indicated)
- 28V HPA drain voltage
- Qorvo QPA1014 HPA EVM setup
  - Gate voltage source: OUTB0 from J29
  - Drain voltage source: LMG2100R026 output (that is, PAVDD1)
  - To avoid slow gate voltage rise time, the 10µF bulk capacitor (C1) is removed from QPA1014 EVM (see page 12 of data sheet)

3.4.1 Bias Up and Down the HPA

To bias up the QPA1014 HPA on header J22, perform the following:

- Launch the TIDA-010289 GUI
- Go to the *Manual Operation* tab in the GUI
- Change the values set by the DACA2 field from to –10V to –6V
- Click on DRVEN0 Low button in the GUI to trigger the voltage change. Now the button reads DRVEN0 High.
- 28V can be applied manually by turning on the 28V power supply.
- Change the DACB0 field from –6V to around –2.7V until current reads 450mA on the power supply or measured using SENSE0 field. Be careful to ramp up slowly to avoid damaging the HPA.

To bias down the HPA, perform the bias down procedure in reverse. The same procedure can be followed for J24, J26 and J28 by modifying the DACA3, DACA1 and DACA0, respectively.

Figure 3-2 shows the results of the HPA bias up and bias down procedure by manually setting a drain voltage through a power supply.

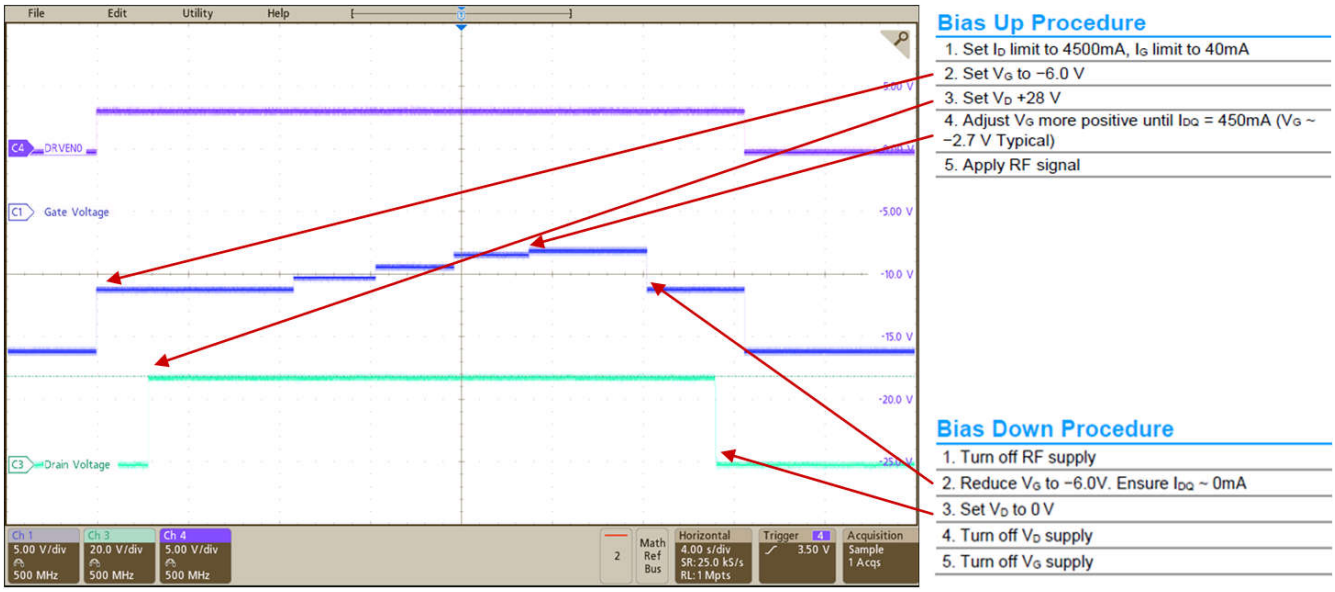


Figure 3-2. Bias Up and Down the HPA

To perform the biasing sequence using header J29, connect position 2 of J4–J6 and J10 to a MSPM0 or FT4232 SPI instead of the onboard FT4222 SPI and perform the following:

- Launch the TIDA-010289 GUI
- Set power supply voltage on J11 to the pinch-off voltage of the device (for example, –6V for the QPA1014)
- In the GUI, go to the *HPA Bias Operation* tab
- Select the end voltage to be around –2.7V
- Set DRIVEN length field (where units are in µs) up to 1200
- Click on the Start Sequence button

The same procedure can be followed for J23, J25 and J27 by modifying the DACB2, DACB3 and DACB1, respectively.

Figure 3-3 shows the results of the HPA bias up and bias down procedure leveraging a LMG2100R026 to bias up and down the HPA using a DRIVEN pulse of 1.2ms.

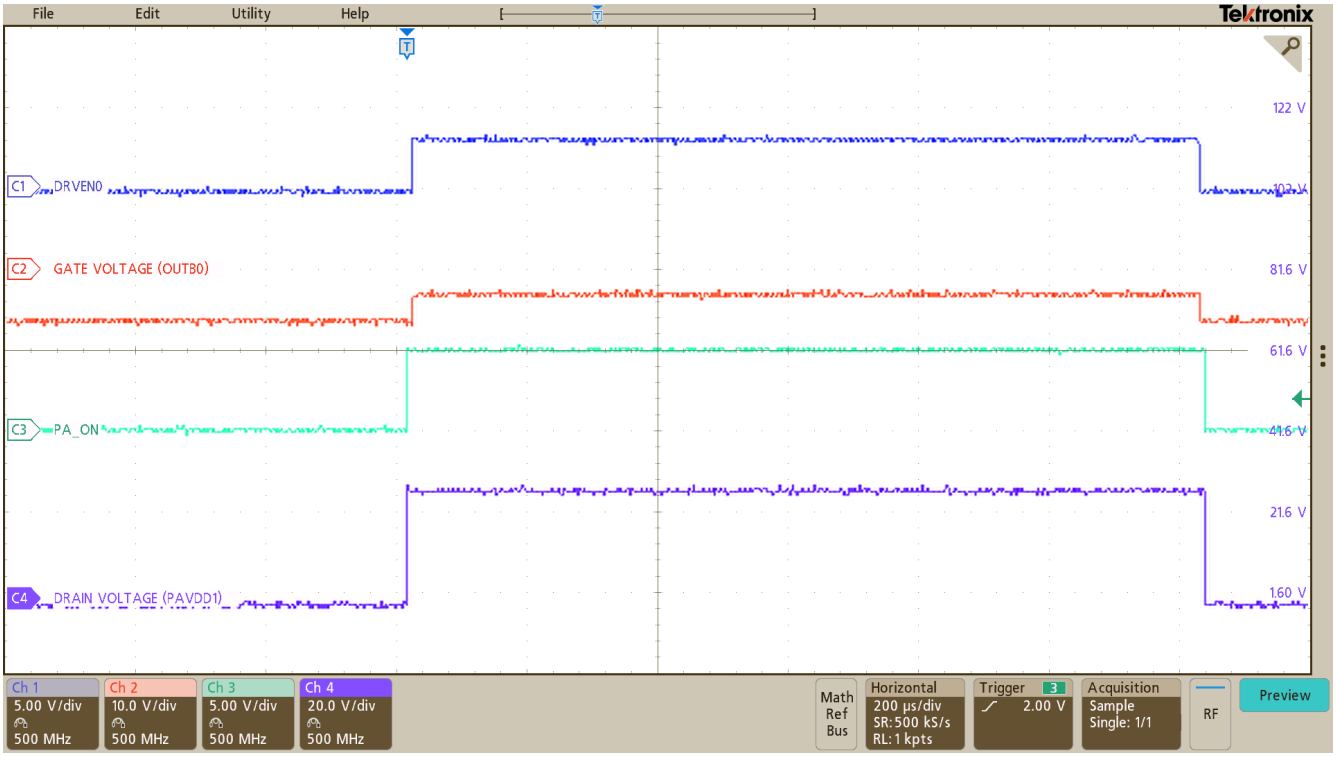


Figure 3-3. Bias Up and Bias Down HPA Sequence

3.4.2 HPA Drain Modulation

To perform PA drain modulation, enter the desired values into the milliseconds on and milliseconds off fields in the TIDA-010289 GUI and click the button to the left labeled *PAON Pulse*. Figure 3-4 through Figure 3-7 show the results of pulsing the HPA with the LMG2100R026 from a PWM signal derived from pulsing the PA_ON signal from the AFE20408. The rise time is about 6ns and time to rise and settle, with about 1.5V of overshoot, from base to top line is < 70ns.

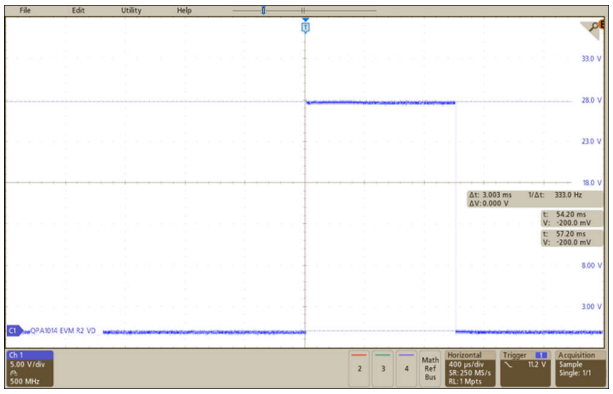


Figure 3-4. HPA Drain Modulation - Drain Pulse

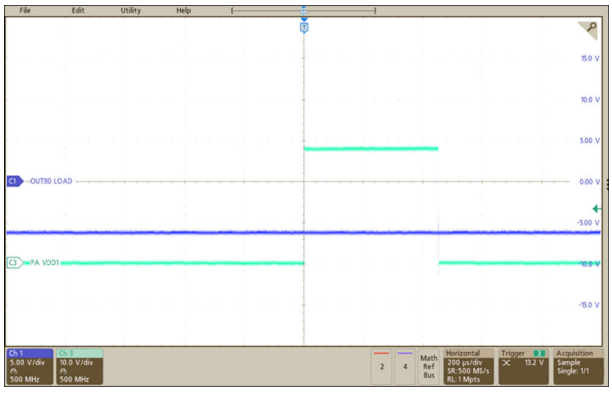


Figure 3-5. HPA Drain Modulation - Drain Pulse with Gate Bias

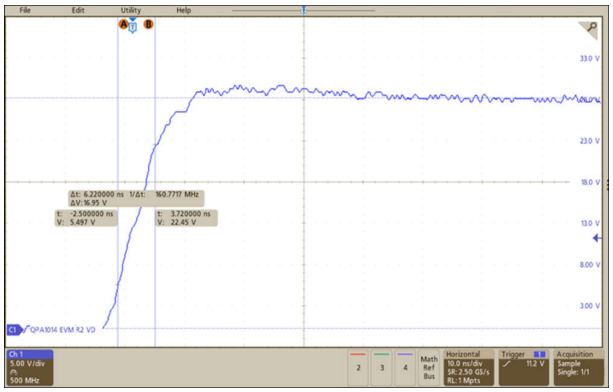


Figure 3-6. HPA Drain Modulation - Rise Time (20% to 80%)

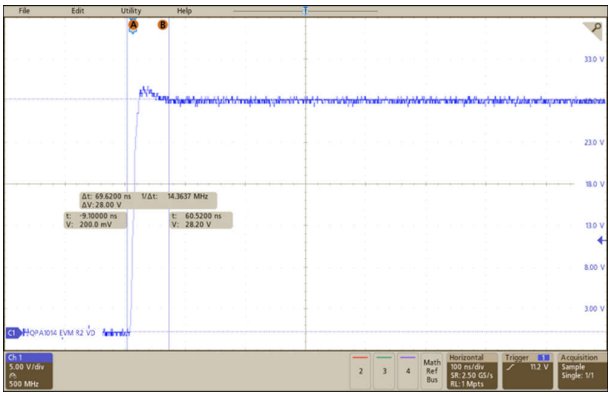


Figure 3-7. HPA Drain Modulation - Top to Base Line Rise Time

3.4.3 HPA Gate Modulation

To perform HPA gate modulation, connect a function generator to the J15 SMA female connector on the board. Install a shunt on pins 2 to 3 on header J14. Set the desired pulse width and pulse interval. Figure 3-8 and Figure 3-9 show the results of pulsing the HPA gate with a frequency of 100kHz, pulse width of 1µs at a 10% duty cycle and a frequency of 300kHz, pulse width of 2µs at a 60% duty cycle. Figure 3-10 and Figure 3-11 show the gate base to top line rise time of about 88ns and the DRVEN0 to HPA gate voltage input 94ns delay time.

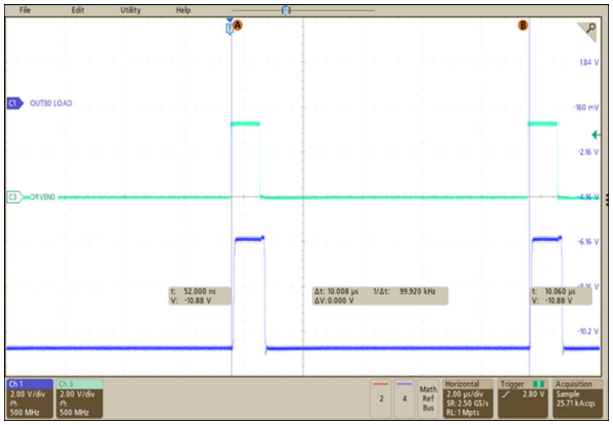


Figure 3-8. HPA Gate Modulation - Pulse Width: 1µs at 10% Duty Cycle

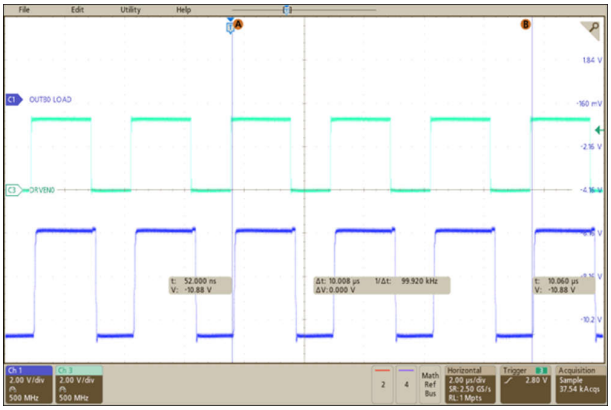


Figure 3-9. HPA Gate Modulation - Pulse Width: 2µs at 60% Duty Cycle

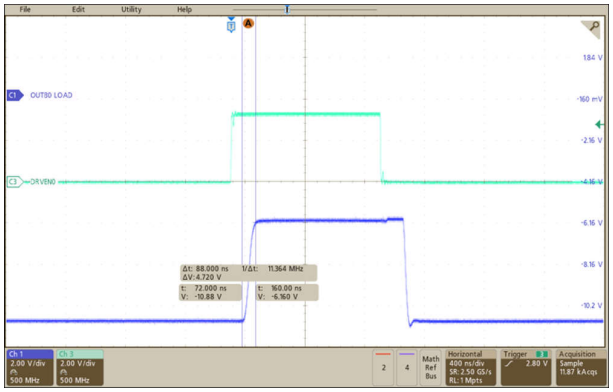


Figure 3-10. HPA Gate Modulation - Base to Top Line Rise Time

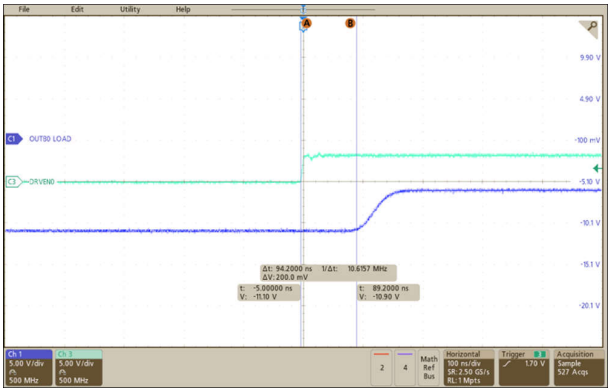


Figure 3-11. HPA Gate Modulation - DRVEN0 to HPA Gate Voltage Delay Time

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-010289.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010289.

4.2 Tools and Software

Software

Software	TIDA-010289 GUI

4.3 Documentation Support

1. Texas Instruments, *LMG2100R026 100V, 53A GaN Half-Bridge Power Stage Data Sheet*
2. Texas Instruments, *AFE20408 8-Channel Power-Amplifier Monitor and Controller Data Sheet*
3. Texas Instruments, *TLV709 150mA, 30V, 3.2µA Quiescent Current, Low-Dropout Linear Regulator Data Sheet*
4. Texas Instruments, *TPS7A30 –35V, –200mA, Ultra-Low-Noise, Negative Linear Regulator Data Sheet*
5. Texas Instruments, *LP5907 250mA, Low-Noise, Low-I_Q LDO Data Sheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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