Design Guide: TIDA-050082

High-Voltage, Positive Rail Active Precharge Reference Design

Description

This reference design utilizes a buck-converter topology to precharge large high-voltage (HV) DC-link capacitances in hybrid electric vehicles (HEV), electric vehicles (EV), and energy storage systems (ESS). This design expands upon and updates *High-Voltage Solid-State Relay Active Precharge Reference Design*.

Resources

TIDA-050082	Design Folder
TPSI31P1-Q1	Product Folder

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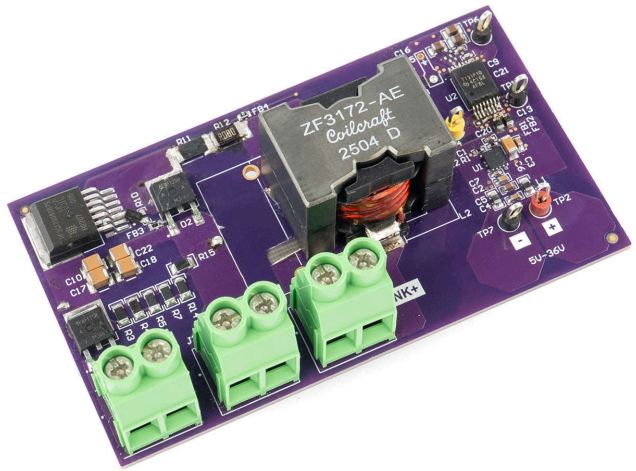
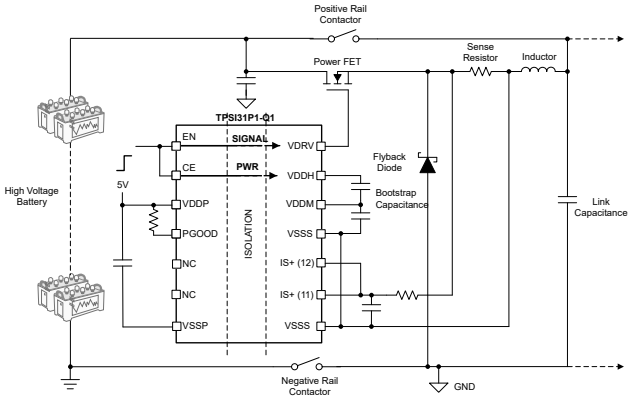
Features

- Charges 2mF capacitance from 0V to 800V within 400ms
- 4.5A_{AVG}, 10A_{PK-PK} charging current
- 5kV_{RMS} reinforced isolation
- Integrated isolated bias supply for high-side rail and positive-rail MOSFET or IGBT gate drive
- Integrated comparators for hysteretic current control

Applications

- High-voltage battery systems
- Battery junction box
- ESS – Battery management system (BMS)





1 System Description

Many HV applications (EV, HEV, and ESS) utilize large capacitances to manage transient current demands for downstream loads. At system start-up, these capacitances are in a discharged state. Connecting them directly to an HV source causes high inrush current due to a large voltage potential difference. This can damage cables, connectors, and fuses.

The simplest method to limit inrush current is adding a series resistor, called passive precharge. The time required to charge the capacitor to 99.3% of the input voltage follows $5\tau = 5RC$. While passive precharge is an excellent choice for minimal complexity, typical resistors for precharge applications are bulky, heavy, and expensive due to high-voltage ratings and the need to handle significant transient power.

This reference design implements an active precharge circuit using a buck converter topology shown in Figure 2-1. Although an active approach increases design complexity, this method significantly reduces component footprint and power dissipation, preserving energy for system operation.

2 System Overview

2.1 Block Diagram

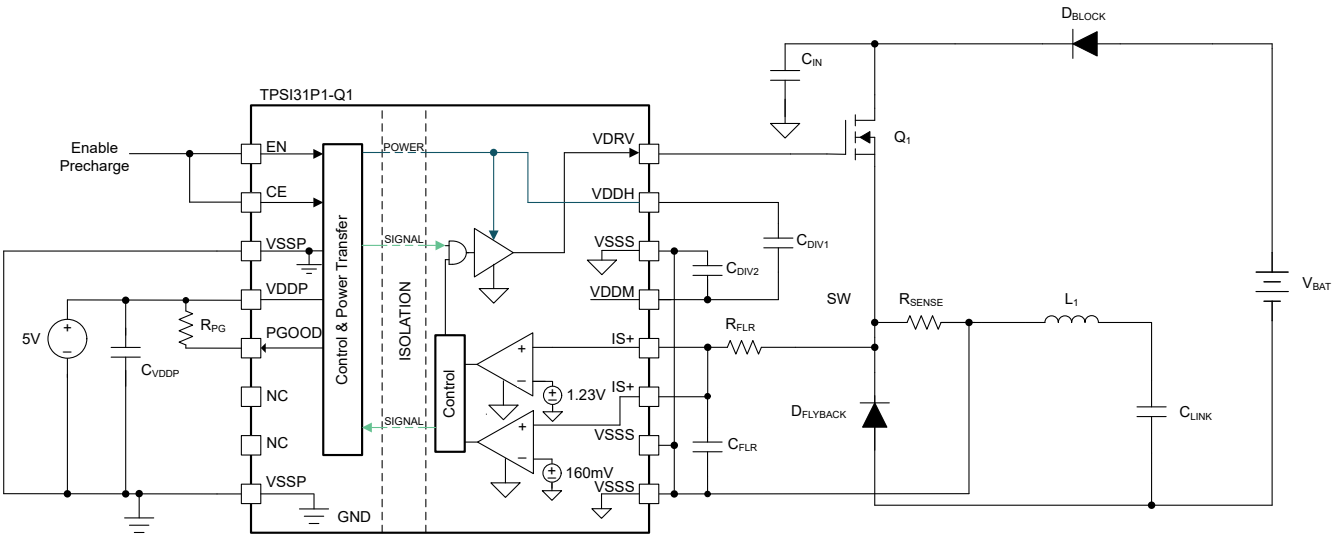


Figure 2-1. Active Precharge Schematic With Detailed TPSI31P1-Q1

2.2 Design Considerations

2.2.1 Control Logic

The TPSI31P1-Q1 uses hysteretic control to manage current by monitoring the voltage across a sense resistor (R_{SENSE}).

1. **Start-up**: At power-on, zero current results in zero voltage across R_{SENSE}, signaling the driver to turn the MOSFET on.
2. **Charging Current Rise**: Current increases, charging the capacitor at increasing rate ($+di_L/dt$) and storing energy in the magnetic field of the inductor.
3. **Peak Threshold**: Once current exceeds I_{PEAK_TARGET} ($V_{SENSE} > V_{REF+}$), the driver turns the MOSFET off.
4. **Charging Current Decay**: Once the MOSFET is off, the magnetic field of the inductor collapses and current flows through the flyback diode path, charging the link capacitor at a decaying rate ($-di_L/dt$).
5. **Minimum Threshold**: When current falls below I_{MIN_TARGET} ($V_{SENSE} < V_{REF+}$), the driver turns the MOSFET on again.

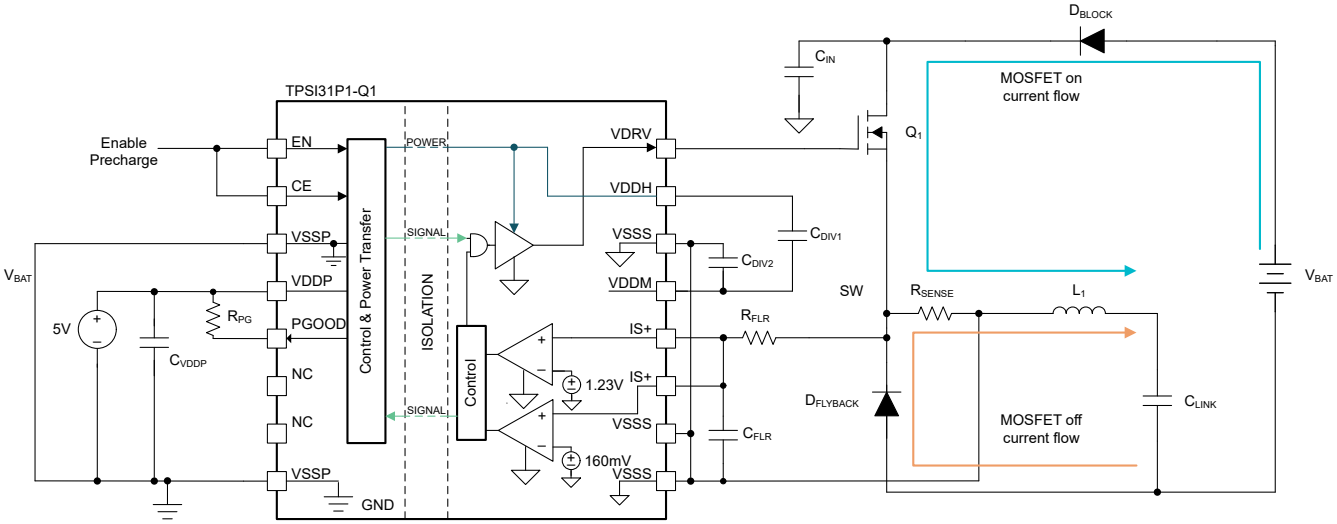


Figure 2-2. Current Flow in Active Precharge

This cycle repeats until V_{LINK} equals V_{BAT}. The hysteretic feedback makes sure the inductor current is bounded, resulting in an average current that linearly charges the link capacitance as shown in Figure 2-3.

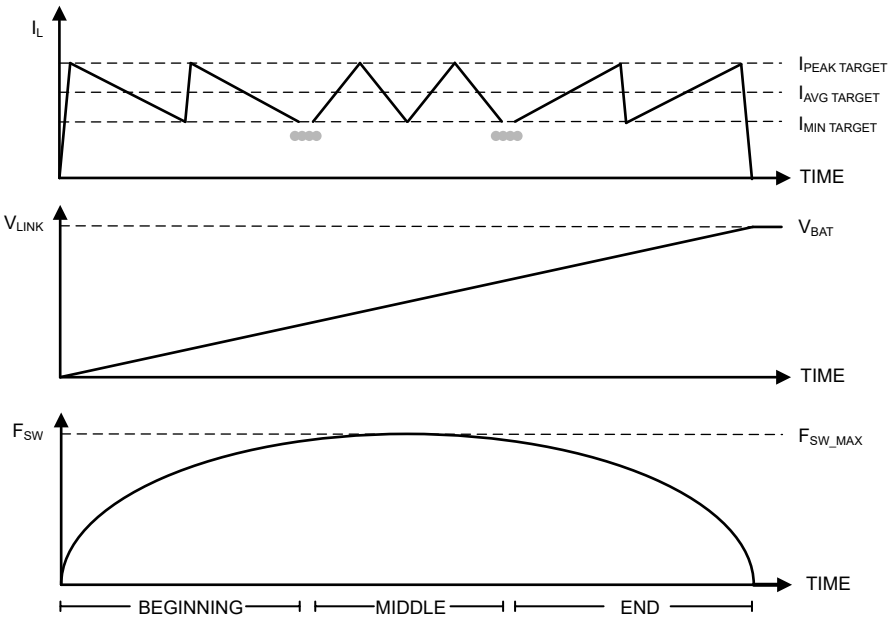


Figure 2-3. Active Precharge Expected Charging Behavior

2.2.2 Switching Power

The TPSI31P1-Q1 transfers a minimum of 55mW for MOSFET switching. Selection of the MOSFET, inductor, and sense resistor is critical, as these components dictate switching power consumption. Power consumption peaks in the middle of precharge where the driver duty cycle (D) is also 0.5.

2.2.2.1 Calculation: D

$$V_{LINK} = D \times V_{BAT}$$

$$V_L = V_{BAT} - V_{LINK}$$

$$\frac{di_L}{dt} = \frac{V_{BAT} - V_{LINK}}{L}$$

$$t_{ON} = \frac{di_L \times L}{V_{BAT} - V_{LINK}}$$

$$t_{ON} = \frac{di_L \times L}{V_{BAT}} \times \frac{1}{1 - D} \quad (1)$$

2.2.2.2 Calculation: 1 – D

$$V_{LINK} = D \times V_{BAT}$$

$$V_L = -V_{LINK}$$

$$\frac{di_L}{dt} = -\frac{V_{LINK}}{L}$$

$$t_{OFF} = \frac{di_L \times L}{V_{LINK}}$$

$$t_{OFF} = \frac{di_L \times L}{V_{BAT}} \times \frac{1}{D} \quad (2)$$

2.2.2.3 Calculation: D + (1 – D)

$$t = t_{ON} + t_{OFF}$$

$$t = \frac{di_L \times L}{V_{BAT}} \times \left(\frac{1}{1-D} + \frac{1}{D}\right)$$

$$t = \frac{di_L \times L}{V_{BAT}} \times \left(\frac{1}{D \times (1-D)}\right)$$

$$di_L = I_{PEAK} - I_{MIN}$$

$$f = \frac{1}{t}$$

$$f = \frac{V_{BAT}}{(I_{PEAK} - I_{MIN}) \times L} \times (D \times (1-D)) \quad (3)$$

Since V_{BAT}, $I_{PEAK} – I_{MIN}$, and L are constants, the maximum switching frequency occurs at D = 0.5, resulting in Equation 4.

1. Maximum Switching Frequency:

$$f_{SW\_MAX} = f(D = 0.5)$$

$$f_{SW\_MAX} = \frac{V_{BAT}}{4 \times L \times (I_{PEAK} - I_{MIN})} \quad (4)$$

2. Maximum Switching Power Consumption:

$$I = Q \times f$$

$$I_{SW\_MAX} = Q_G \times f_{SW\_MAX}$$

$$I_{SW\_MAX} = Q_G \times \frac{V_{BAT}}{4 \times L \times (I_{PEAK} - I_{MIN})}$$

$$P = V \times I$$

$$P_{SW\_MAX} = V_{GS} \times Q_G \times \frac{V_{BAT}}{4 \times L \times (I_{PEAK} - I_{MIN})} \quad (5)$$

To provide reliability, make sure P_{SW_MAX} is less than the output capability of the driver (P_{OUT_VDDH}). Power consumption can be reduced by selecting MOSFETs with lower gate charge (Q_G), using higher inductance (L), or increasing ripple current ($I_{PEAK} – I_{MIN}$).

2.2.3 Propagation Delay

Real-world propagation delays (comparator-to-driver and system RC delays) cause current to overshoot or undershoot target thresholds. This is critical during the first switching cycle when di_L/dt is at the maximum. If di_L/dt is excessive, the inductor can saturate, resulting in low impedance and high currents that can damage the system.

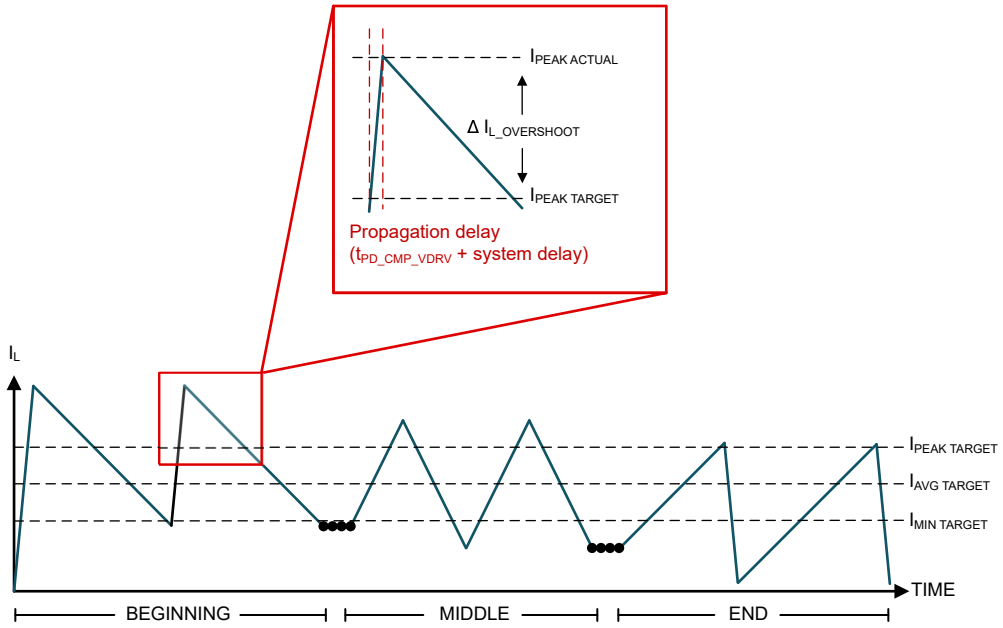


Figure 2-4. Precharge Delays Causing Current Overshoot and Undershoot

Designers must select a shunt resistance that makes sure the actual peak current remains below the saturation limit of the inductor.

$$I_{PEAKACTUAL} = I_{PEAKTARGET} + \Delta i_{L\_OVERSHOOT}$$

$$\Delta i_{L\_OVERSHOOT} = \frac{di_L}{dt} \times t_{DELAY}$$

$$\Delta i_{L\_OVERSHOOT} = \frac{V_{BAT} - V_{LINK}}{L} \times (t_{DELAY}) \quad (6)$$

The propagation delay also reduces switching frequency since the delay adds time to both T_{ON} and T_{OFF}, which reduces power consumption during switching.

$$f_{SW\_DELAYED} = \frac{1}{t_{ON} + t_{OFF} + 2 \times t_{DELAY}} \quad (7)$$

2.2.4 MOSFET Selection

Prioritize selecting MOSFETs with the lowest Q_G to minimize driver current demand. MOSFETs typically have on-resistance (R_{ON}) inversely proportional to the total gate charge of the MOSFET. Selecting a MOSFET with lower gate charge typically results in higher heat dissipation because $P_{DIS} = I^2 \times R_{ON}$. Since precharge is a transient event (< 1 second), the MOSFET can handle higher power dissipation than in steady state. According to the *transient thermal resistance, 1 layer Copper foil surface area 73.8mm^2 (footprint)* image in *Thermal Resistance Data: TO263-5* application note, the TO263 package with a single layer footprint-size copper foil surface area has steady-state thermal resistance (R_{TH}) of 74.7°C/W. However, at a 1s pulse, the thermal resistance drops to 7.2°C/W. Given the thermal resistance and power dissipation, Equation 8 shows the thermal rise of the MOSFET package.

$$T_{FINAL} = P_{DIS} \times R_{TH} + T_{AMBIENT} \quad (8)$$

Figure 2-5 shows typical MOSFET turn-on behavior.

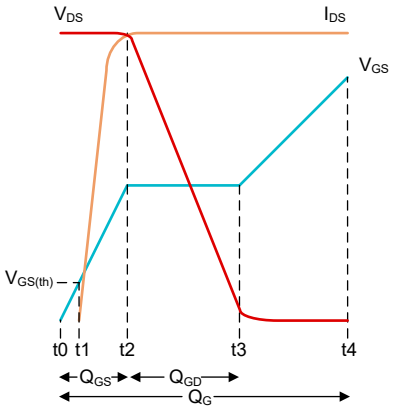


Figure 2-5. Typical MOSFET Turn On

where

- t0 – t1: C_{GS} charges from zero to $V_{GS(th)}$. No change in V_{DS} or I_{DS}.
- t1 – t2: C_{GS} has reached threshold voltage to begin conducting so I_{DS} rises to full load current. No change in V_{DS}.
- t2 – t3: Miller plateau region with relatively flat V_{GS}, V_{DS} falls.
- t3 – t4: V_{GS} rises beyond Miller plateau, V_{DS} is down and further drops marginally with higher V_{GS}.

Make sure the driver output rail (VDDH) remains above the Miller plateau. High power dissipation occurs when the MOSFET operates in the t1 – t2 and t2 – t3 (Miller plateau) regions. For the best performance, the MOSFET operates in the t3 – t4 region to achieve the lowest on-resistance (R_{ON}).

2.2.5 Flyback or Freewheeling Diode Selection

The flyback diode must have a low forward recovery time to minimize negative voltage spikes at the switch (SW) node during MOSFET turn-off. Schottky diodes (forward recovery time < 10ns) are recommended to prevent component damage.

Figure 2-6 shows the precharge waveform of a setup using a slow flyback diode (VS-8EWF12SLHM3) and the SW node voltage (V_{SW}) becoming very negative during MOSFET turn-off. This design eventually breaks in testing with higher input voltage as the negative V_{SW} causes the MOSFET to operate outside of the safe operating area (SOA). Figure 2-7 shows the precharge waveform of a setup using a faster flyback diode (STTH1512). V_{SW} still becomes negative during MOSFET turn-off, but this setup passes higher input voltage testing because the MOSFET operates within SOA.

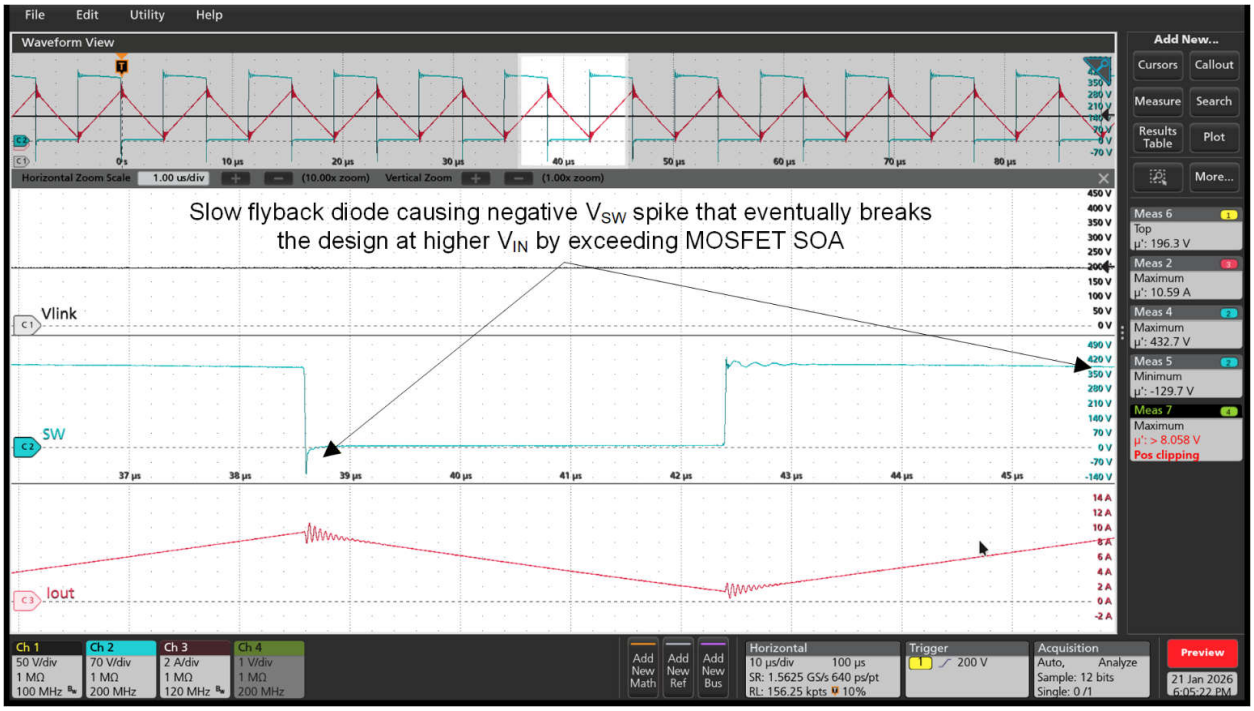


Figure 2-6. Slow Flyback Diode Setup, V_{IN} at 400V, V_{LINK} at 200V

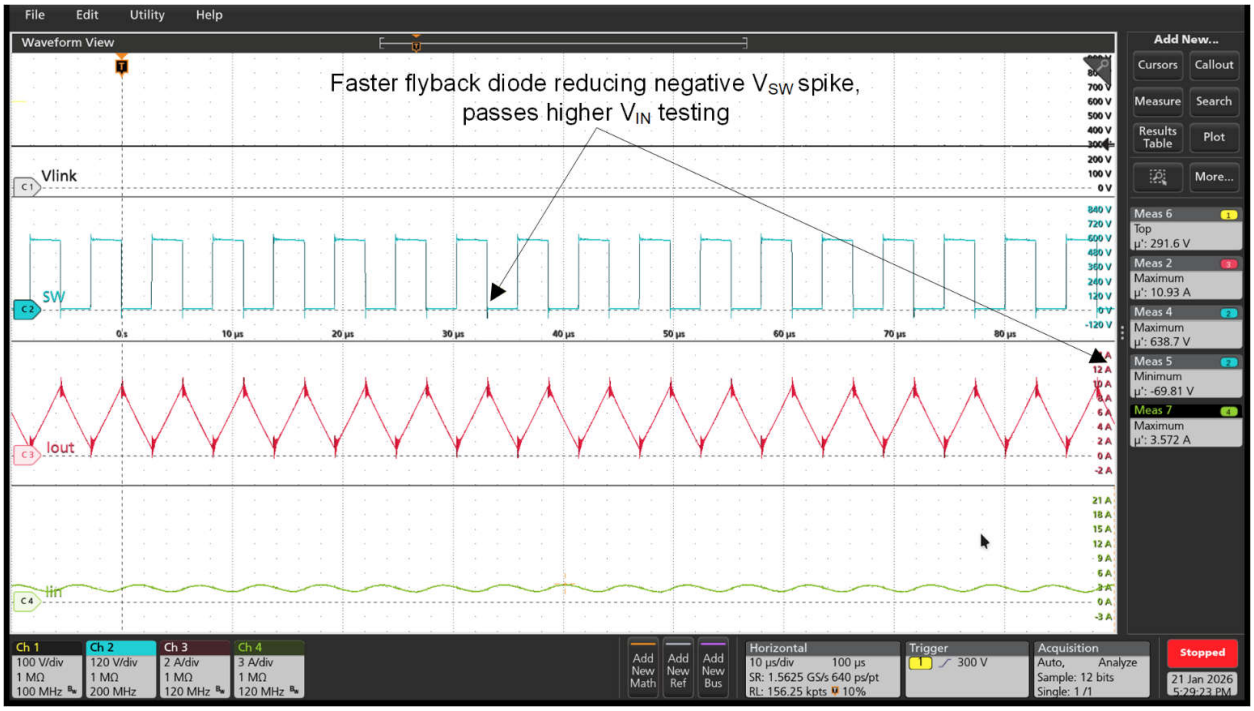


Figure 2-7. Faster Flyback Diode Setup, V_{IN} at 600V, V_{LINK} at 300V

2.2.6 Sense Resistance Selection

The sense resistor must be rated for the required power handling. While $P = I_{AVG}^{2} \times R_{SENSE}$ serves as a baseline, many resistors offer an overload rating (for example, 5 × DC power for 5s), which is adequate for transient precharge events.

2.2.7 Input Capacitance Selection

Figure 2-8 shows how the input capacitance stabilizes the voltage and provides charge during the T_{ON} period. The required capacitance can be calculated based on the allowed voltage ripple ΔV_{IN}.

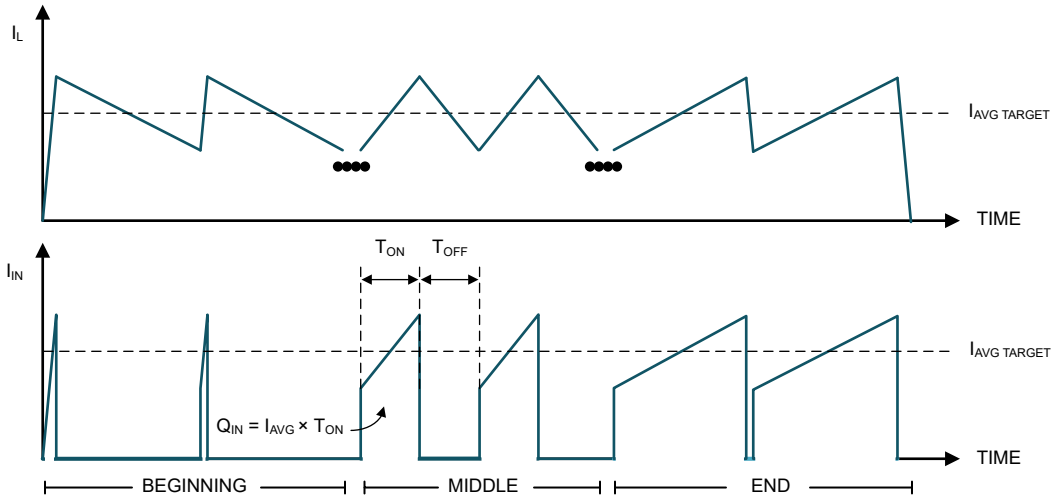


Figure 2-8. Charge Required During T_{ON}

where

$$Q_{IN} = I_{AVG} \times T_{ON};\quad Q_{IN} = C_{IN} \times \Delta V_{IN};\quad \Delta V_{IN} = \frac{I_{AVG}}{C_{IN}} \times T_{ON}$$

Depending on system parasitic elements, the input capacitance likely does not need to provide all the input charge since the battery also helps provide input charge.

2.2.8 Output Capacitance Selection

This design does not need additional output capacitance. Additional inductance between the inductor and link capacitor due to wiring acts as additional series inductance, slowing down di_L/dt, which helps in reducing current overshoot, reduce switching power consumption, while maintaining a similar average charging current.

2.2.9 Design Example #1: Single R_{SENSE} Configuration

Based on the precharge requirements in Table 2-1, component values can be determined using the equations provided in the previous sections. Alternatively, the TPSI31P1-Q1 device calculator tool simplifies this iterative process.

Table 2-1. Example Precharge Requirements

SPECIFICATION	REQUIREMENT
Link capacitance	2mF
Battery pack voltage	800V
Charging time	400ms

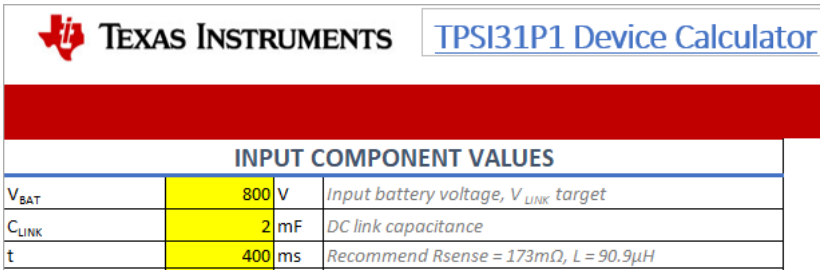


Figure 2-9. Calculator Tool Single R_{SENSE} Input

By entering the recommended sense resistance (173mΩ) and inductance (68µH) back into the tool, the calculator plots the expected voltage and current outputs (see Figure 2-10). These results confirm that the recommended values satisfy the requirements in Table 2-1. The calculator linearizes specific relationships to approximate behavior; actual performance can vary due to non-linearities and other external factors.

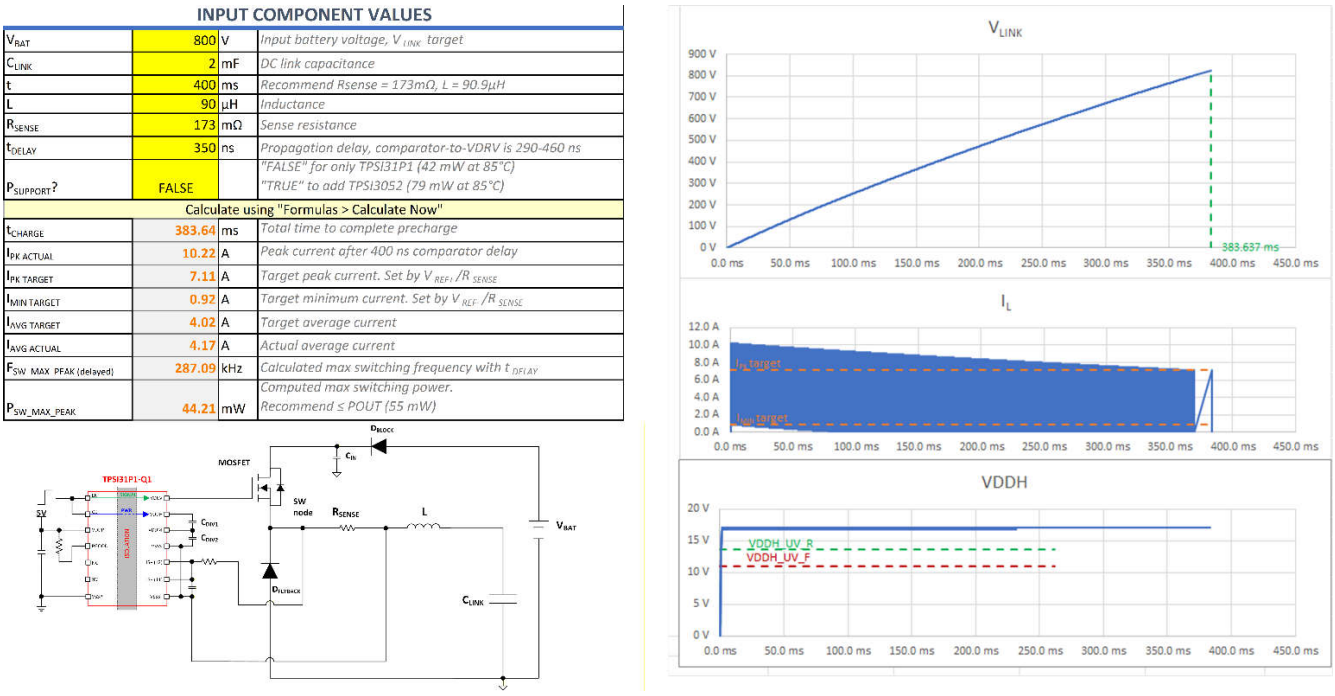


Figure 2-10. Calculator Tool Single R_{SENSE} Output

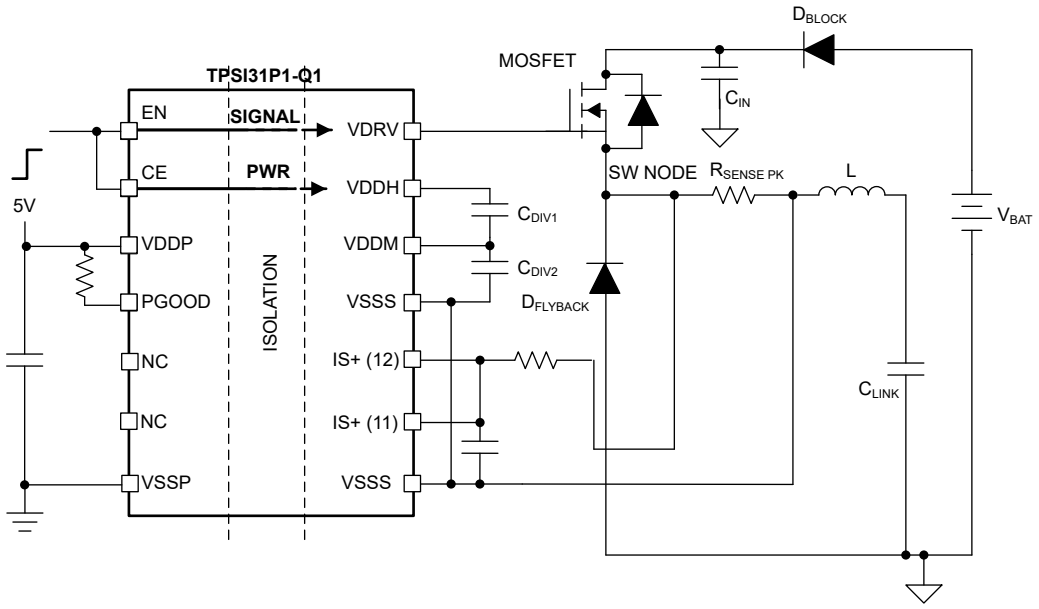


Figure 2-11. Active Precharge Single R_{SENSE} Configuration

2.2.10 Design Example #2: Double R_{SENSE} Configuration

Design Example #2 requires a faster precharge time of 360ms using the same inductor, with a peak current limit of 10.3A_{PK} to prevent saturation (see Table 2-2). Using a single sense resistor, these requirements are difficult to achieve as decreasing R_{SENSE} to increase the average charging current simultaneously pushes the peak current beyond the 10.3A_{PK} limit. However, the TPSI31P1-Q1 can monitor two different sense resistances to maintain the peak current target while independently increasing the minimum current target. This configuration increases the average charging current to meet the new timing requirement (see Figure 2-12).

Table 2-2. Example Precharge Requirements with Peak Current

SPECIFICATION	REQUIREMENT
Link capacitance	2mF
Battery pack voltage	800V
Charging time	360ms
Peak current	10.3A_{PK}
Inductor	90µH

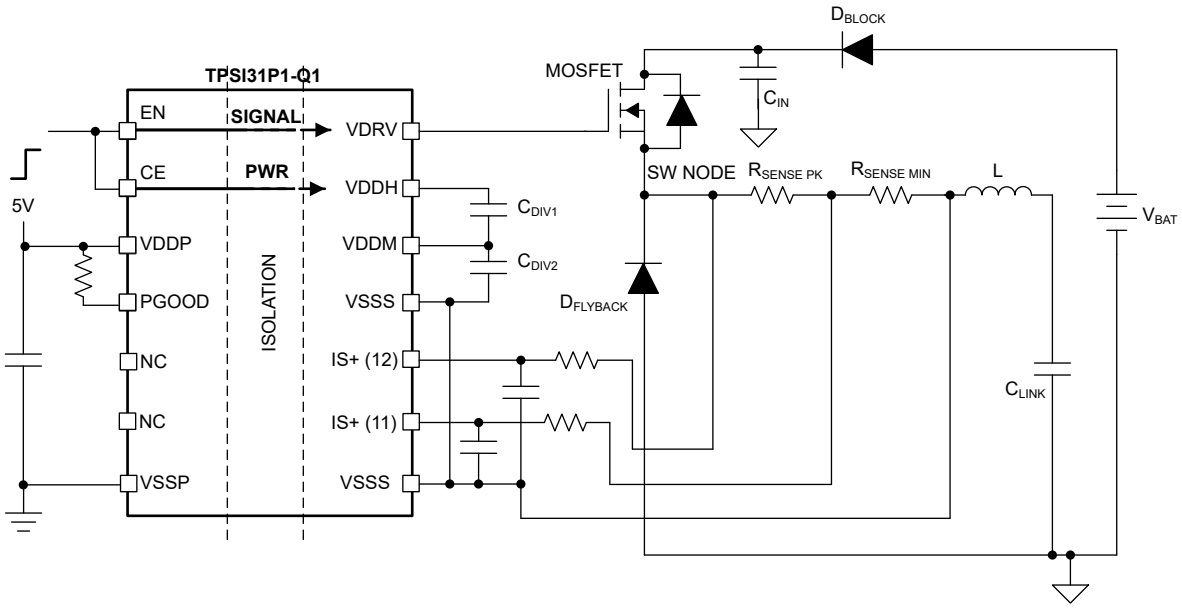
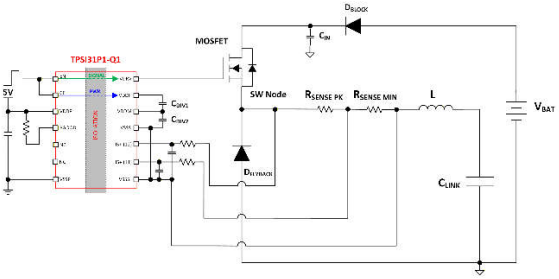


Figure 2-12. Active Precharge Double R_{SENSE} Configuration

To maintain the peak current limit, the total sense resistance must remain 173mΩ (R_{SENSE_PK} + R_{SENSE_MIN} = 173mΩ). By adjusting R_{SENSE_MIN}, the minimum current target increases which also raises the average charging current. Following iteration in the calculator tool, the values shown in Figure 2-13 satisfy these updated design requirements.

INPUT COMPONENT VALUES			
V_{BAT}	800	V	*Input battery voltage, V_{LINK} target*
C_{LINK}	2	mF	*DC link capacitance*
t	400	ms	*#DIV/0!*
$I_{PK\ TARGET}$		A	*Target maximum current, Recommends Rsense_max*
$I_{MIN\ TARGET}$		A	*Target minimum current, Recommends Rsense_min*
L	90	µH	*Inductance*
R_{SENSE_PK}	105	mΩ	*Resistance to set peak target current*
R_{SENSE_MIN}	68	mΩ	*Resistance to set minimum target current*
t_{DELAY}	350	ns	*Propagation delay, comparator-to-VDRV is 290-460 ns*
Calculate using "Formulas > Calculate Now"			
t_{CHARGE}	352.27	ms	*Total time to complete precharge*
$I_{PK\ ACTUAL}$	~~10.22~~	A	*Peak current after 350 ns comparator delay*
$I_{PK\ TARGET}$	7.11	A	*Target peak current. Set by V_{REF+}/R_{SENSE}*
$I_{MIN\ TARGET}$	2.35	A	*Target minimum current. Set by V_{REF-}/R_{SENSE}*
$I_{AVG\ TARGET}$	4.73	A	*Target average current*
$I_{AVG\ ACTUAL}$	4.54	A	*Actual average current*
$F_{SW\_MAX\_PEAK\ (delayed)}$	352.04	kHz	*Calculated max switching frequency with t_{DELAY}*
$P_{SW\_MAX\_PEAK}$	54.21	mW	*Computed max switching power. Recommend ≤ POUT (55 mW)*



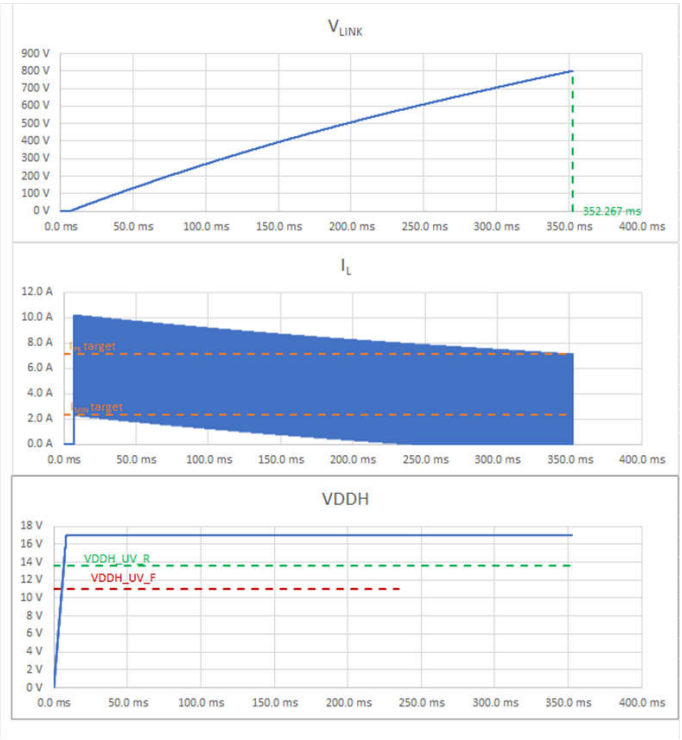


Figure 2-13. Calculator Double R_{SENSE} Output

2.3 Highlighted Products

2.3.1 TPSI31P1-Q1

The TPSI31P1-Q1 is designed to be used in automotive precharge systems as an alternative to traditional passive precharge architectures that typically include costly electromechanical relays (EMR), along with bulky, high power resistors. The TPSI31P1-Q1, combined with external power switches, power inductor and diode, forms an active precharge approach. The inductor current is continuously monitored and controlled in a hysteretic mode of operation by the TPSI31P1-Q1 to linearly charge the large capacitance of the downstream system. The TPSI31P1-Q1 is an isolated switch driver that generates a secondary bias supply from power received on the primary side, therefore no isolated secondary supply is required. With a gate drive voltage of 17V with 1.5A and 2.5A peak source and sink current, a large availability of power switches can be used including SiC FET and IGBT.

2.3.2 TPS7A49

The TPS7A49 series of devices are positive, high-voltage (36V), ultra-low-noise (15.4μV_{RMS}, 72dB PSRR) linear regulators that can source a 150mA load.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware Requirements

The hardware used to evaluate this reference design consists of the following:

- TIDA-050082 reference design board
- DC power supply (N8930A) for 800V, $5A_{AVG}$
- Two DC power supplies, one for providing power to TPSI31P1-Q1 VDDP (5V), the second for driving TPSI31P1-Q1 EN/CE (5V)
- Interlocked safety box for safely testing HV
- 2mF capacitance made up of four 500µF, 2kV capacitors connected in parallel
- Resistive discharge path for the capacitance
- Oscilloscope (MSO44)
- Two HV differential probes for measuring up to 800V across link capacitance and SW node to HV ground
- Current probe capable of measuring up to 20A

3.2 Test Setup

The following test results were collected using the setup shown in Figure 3-1 using a 10kW, 1kV DC supply on the input and output to 2mF capacitance with a 20kΩ discharge resistance. A system with battery input and shorter cables does not always require as much input capacitance.

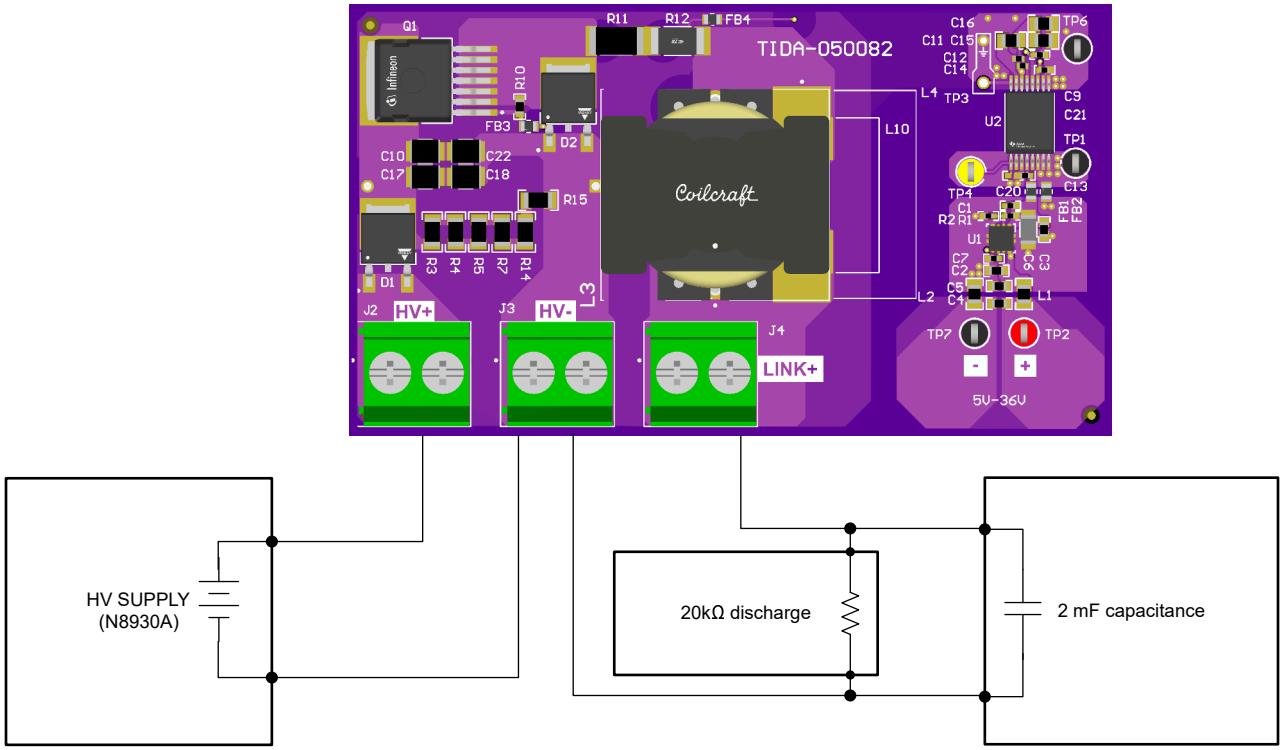


Figure 3-1. Active Precharge Setup

3.3 Test Results

With bootstrap capacitance C_{DIV1} = 10µF and C_{DIV2} = 32µF, the secondary rails of the driver (VDDM and VDDH) require approximately 30ms to power up before precharge starts. Lower bootstrap capacitance yields a quicker driver secondary rail power up time but affords less margin for the rails to droop if the driver outputs power beyond maximum capability.

The 400V and 800V precharge waveforms (Figure 3-2 and Figure 3-3) show the active precharge circuit charging behavior once the driver secondary rails are powered up.

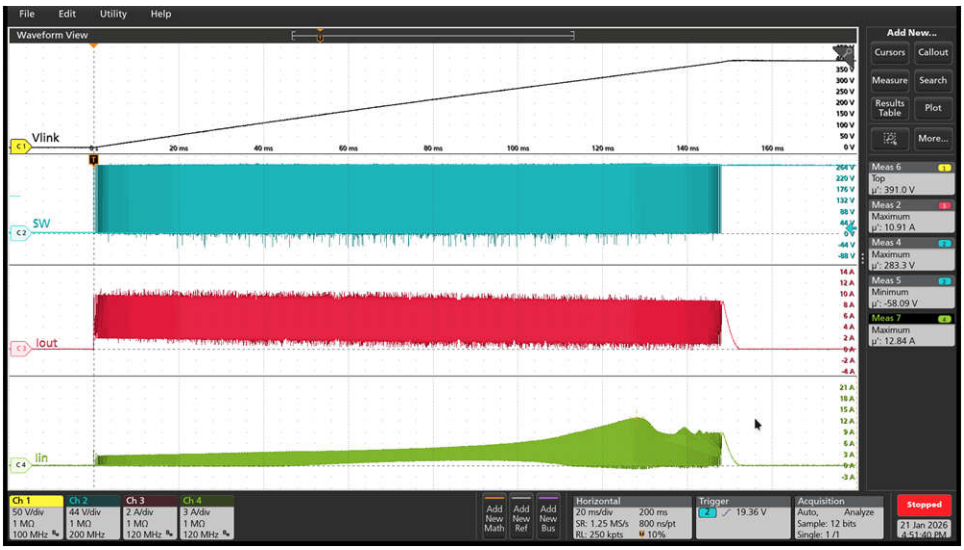


Figure 3-2. 400V V_{IN}

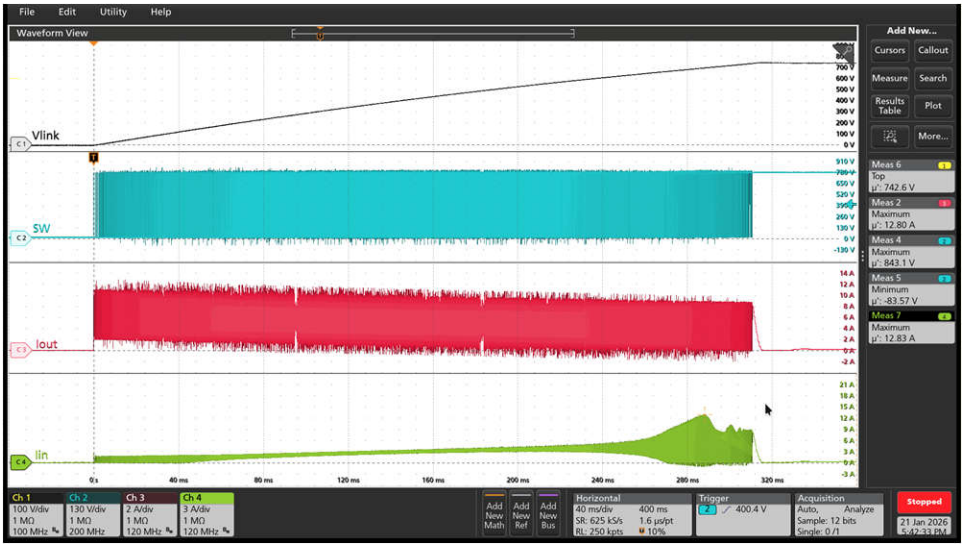


Figure 3-3. 800V V_{IN}

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematics

To download the schematics, see the design files at TIDA-050082.

4.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-050082.

4.1.3 PCB Layout Recommendations

Layout becomes critical for minimizing parasitic elements that require additional components to compensate or, in extreme cases, render a design non-functional. The following PCB layout considerations help develop a functional high-voltage (HV) active precharge design.

4.1.3.1 Use Large Return Planes to Contain Electromagnetic Fields

Electromagnetic Compatibility (EMC) often receives secondary consideration in active precharge applications because of the brief operational duration, but standard PCB best practices remain essential. Engineers need to implement large reference or ground planes for all signal and power traces to contain the electric (E-field) and magnetic (H-field) fields that moving charges generate, as Figure 4-1 shows.

Insufficient reference planes create larger E-fields and H-fields, increasing the risk of noise injection into nearby circuitry or electromagnetic interference (EMI). Trace and plane widths (w) typically follow thermal rise limits (for example IPC-2152 standards). To minimize electromagnetic interference, designers must minimize the height (h) between the trace and reference plane and the overall trace length. EMC considerations become particularly vital for the high di_L/dt loop and SW node, which represent the primary noise sources in this design.

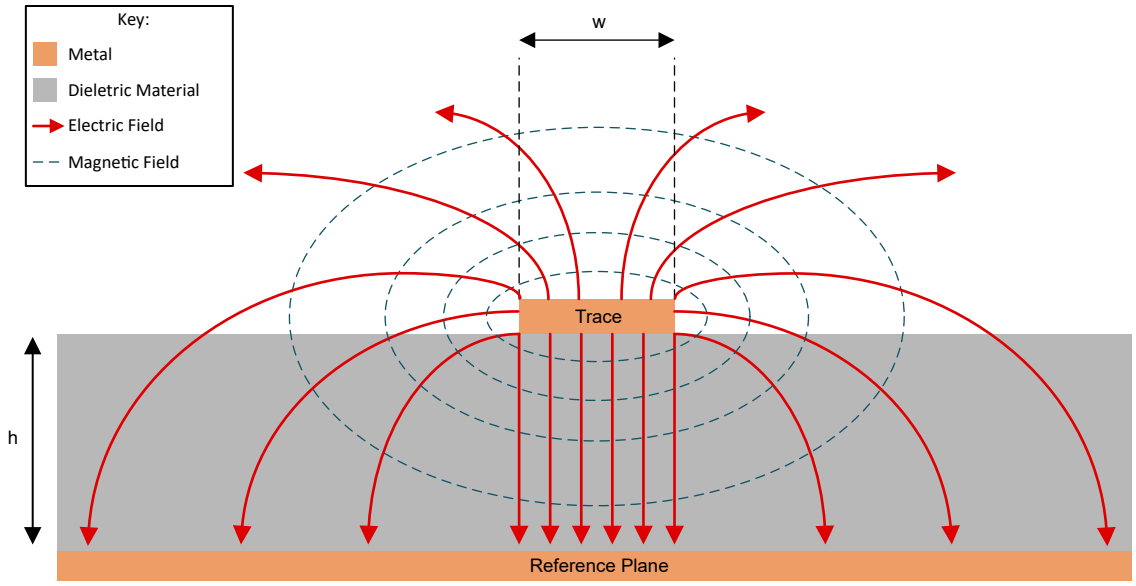


Figure 4-1. Trace Electromagnetic Cross-Sectional View

4.1.3.2 Minimize High di_L/dt Loop Length to Control Oscillations and EMI

Optimize the high di/dt loop by placing the input capacitance close to the switching circuit. Figure 4-2 illustrates the main reference design current loops using a simplified schematic and the reference design layout.

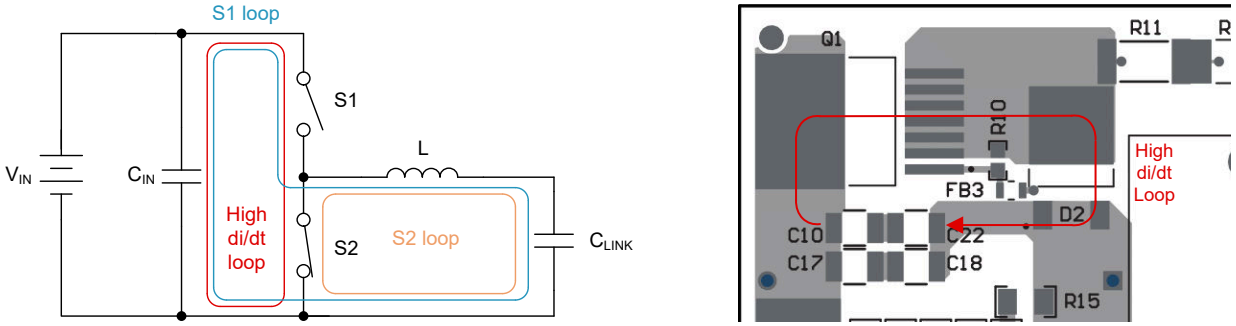


Figure 4-2. High di/dt Loop Schematic and Layout

In this circuit, S1 represents the MOSFET and S2 represents the flyback diode. Current alternates between the S1 and S2 paths; the current remains continuous where these loops overlap but is discontinuous in the non-overlapping section. This results in a high di/dt loop as the current suddenly transitions from zero to the full load current. Parasitic inductances and capacitances within this loop form resonant circuits that generate voltage oscillations during transitions, as shown in Figure 4-3. Excessive oscillations can exceed absolute maximum specifications, potentially damaging the MOSFET or flyback diode.

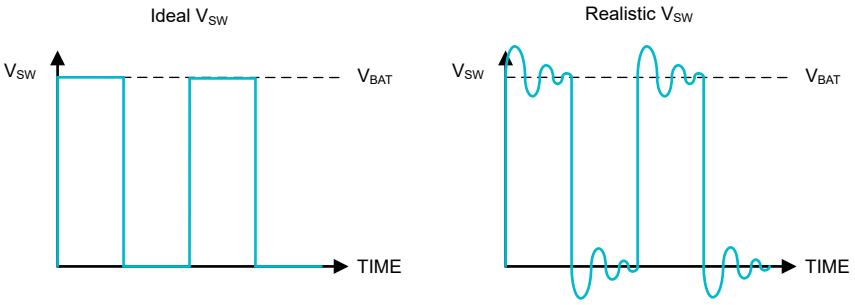


Figure 4-3. Ideal vs Realistic V_{SW} Behavior

Reducing the high di/dt loop length minimizes the energy stored and released by parasitic elements ($W_L = 0.5 \times LI^2$) and reduces voltage overshoot ($V_L = L \times di_L/dt$). Additionally, current in this loop forms a time-varying H-field which can inject current into nearby circuits through mutual inductance, causing more EMI. Minimize the high di/dt loop length and place the input capacitance as close as possible to the MOSFET drain and flyback diode anode for best performance.

If excessive V_{SW} oscillations persist, consider increasing damping by implementing:

- Increased MOSFET gate resistance to slow turn-on
- Series resistance at the sense resistor
- An RC snubber circuit across the SW node to HV−

4.1.3.3 Minimize SW Node Area to Improve Ringing and Noise

Just as high di_L/dt loops achieve best performance by minimizing length, high di_L/dt nodes achieve best performance by minimizing area. The SW node, consisting of the MOSFET source, flyback diode cathode, and inductor connection, experiences high di_L/dt during MOSFET transitions. When the MOSFET turns on, the SW node pulls high to V_{BAT}. When the MOSFET turns off, the flyback diode pulls the SW node to HV−. A large SW node creates parasitic inductances and capacitances that contribute to ringing and component stress. Additionally, a larger SW node acts as an antenna, creating larger E-fields and H-fields that result in more EMI.

For best performance, the SW node requires compact design and close positioning to the input capacitance and reference plane.

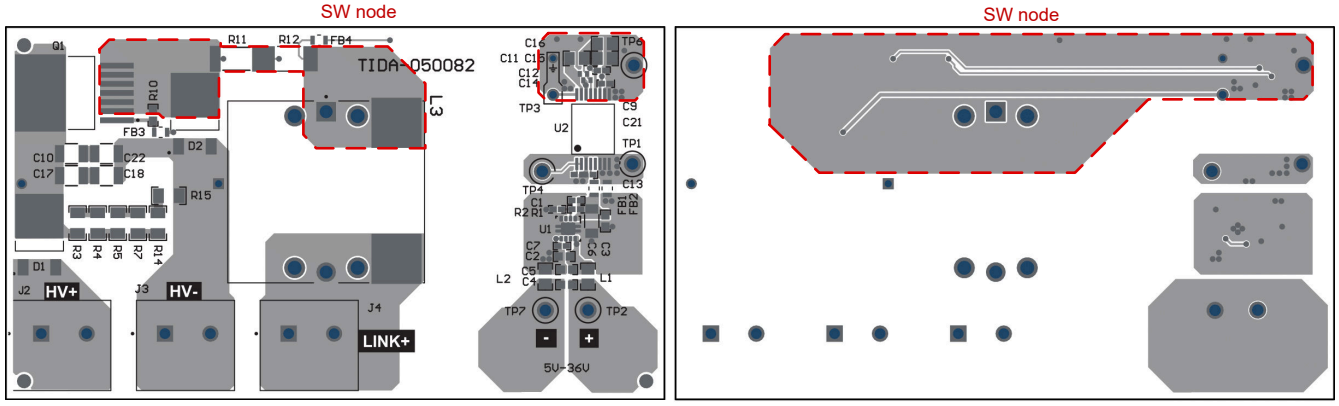


Figure 4-4. Top and Bottom View SW Node From TIDA-050082 Board

4.1.3.4 Minimize Inductor Pad to Limit Parasitic Capacitive Coupling

The initial reference design board utilized large copper layers to support multiple surface-mount inductor footprints. Although the spacing met HV creepage and clearance requirements, the excess copper created parasitic capacitive coupling (C_{PAR}) to the inductor shown in Figure 4-5. This coupling reduces the effective inductance during high-voltage switching, causing transient load current spikes during SW node transitions.

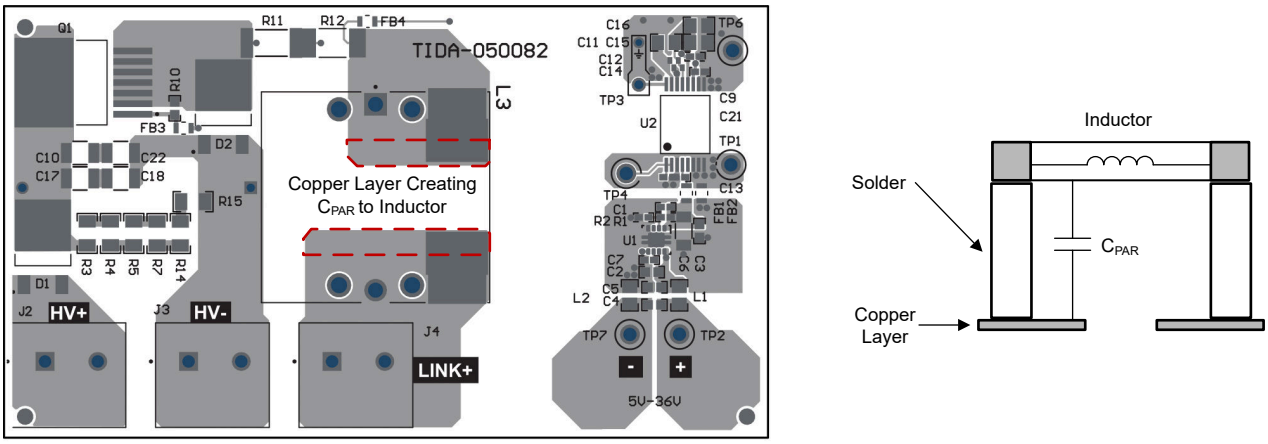


Figure 4-5. Inductor Pad Copper Layer Creating C_{PAR}

Removing the excess C_{PAR} copper layer significantly mitigates these transient spikes and improves system stability. Figure 4-6 and Figure 4-7 show before and after waveforms.

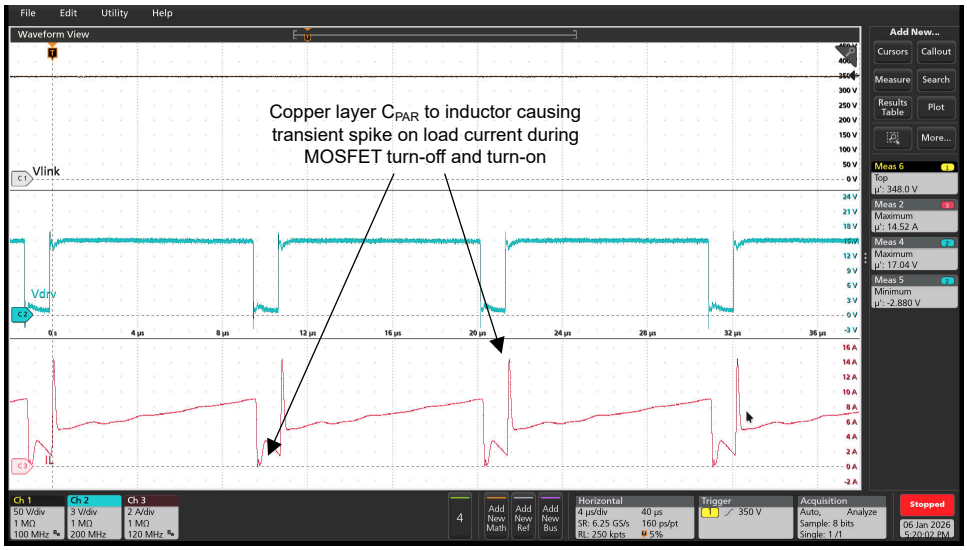


Figure 4-6. Waveform With C_{PAR} Copper

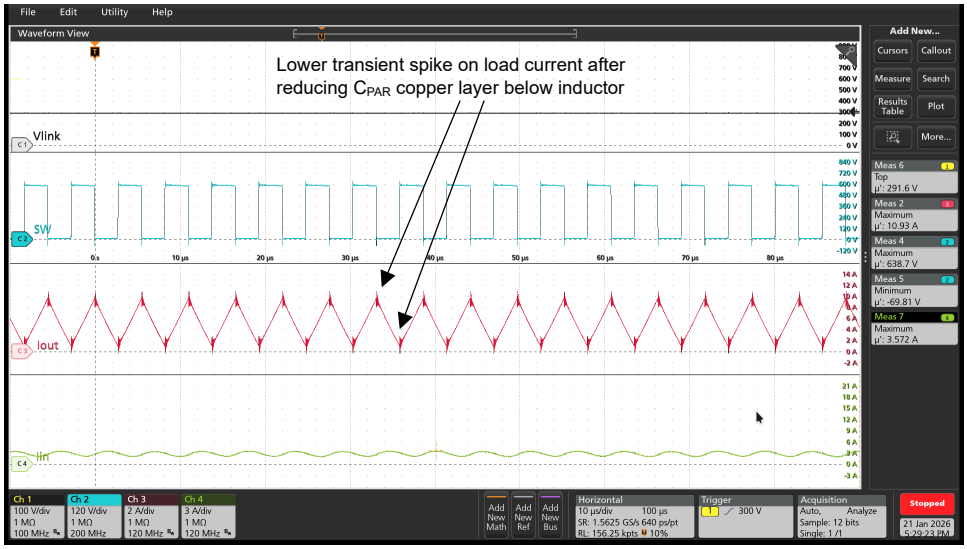


Figure 4-7. Waveform Without C_{PAR} Copper

4.1.3.5 HV Creepage and Clearance

HV designs require sufficient conductor spacing to prevent dielectric breakdown and arcing. Required spacing increases proportionally with the voltage potential between conductors. For detailed design principles, consult Demystifying Clearance and Creepage Distance for High-Voltage End Equipment. To determine specific spacing requirements according to the IPC-2221B standard, utilize the *PCB Conductor Spacing and Voltage Calculator* from Sierra Circuits®.

4.1.3.6 Layout Prints

To download the layer plots, see the design files at TIDA-050082.

Figure 4-8 through Figure 4-14 show the TIDA-050082 layout prints.

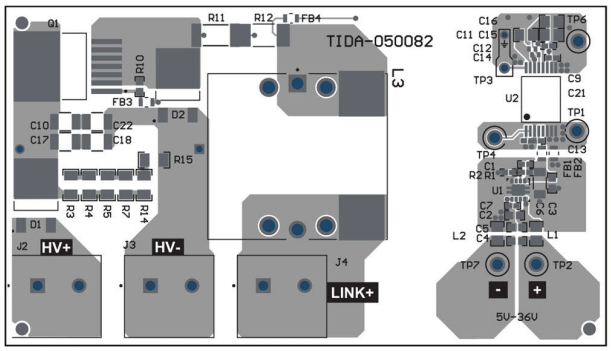


Figure 4-8. TIDA-050082 Top View Composite

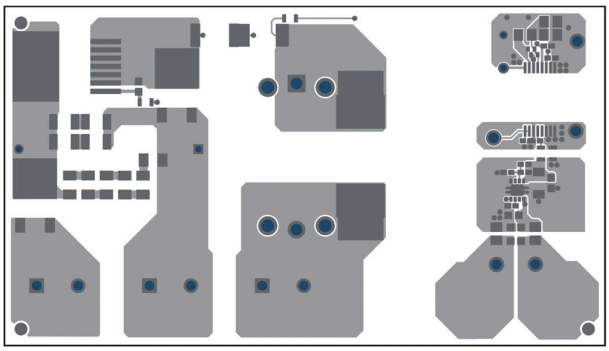


Figure 4-9. TIDA-050082 Top Outer Layer

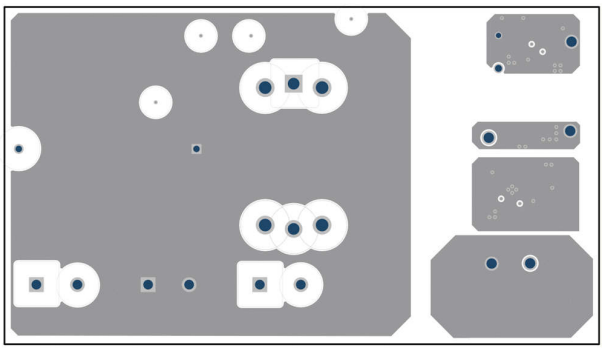


Figure 4-10. TIDA-050082 Inner Layer 1

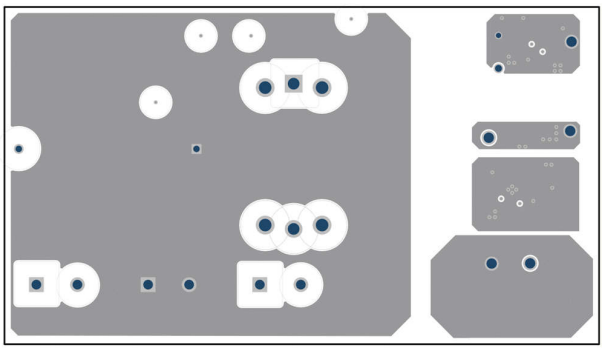


Figure 4-11. TIDA-050082 Inner Layer 2

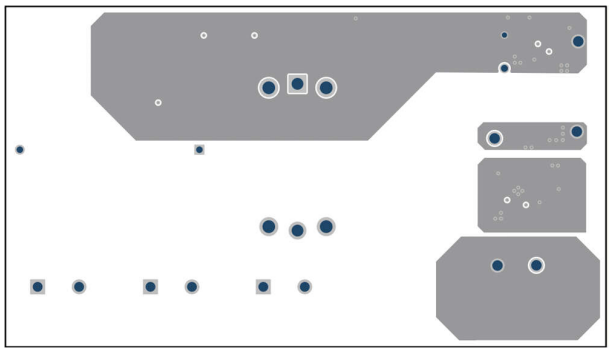


Figure 4-12. TIDA-050082 Inner Layer 3

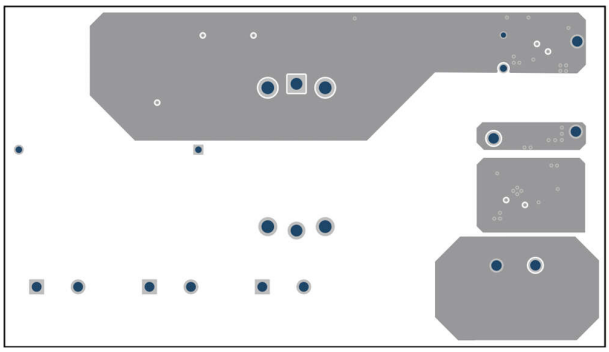


Figure 4-13. TIDA-050082 Inner Layer 4

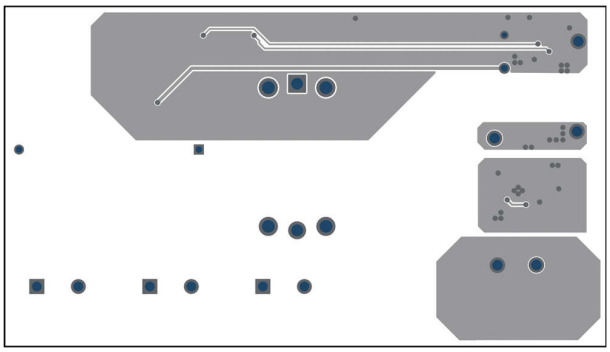


Figure 4-14. TIDA-050082 Bottom Outer Layer

4.2 Tools

TPSI31P1-SINGLE-RSENSE-CALC	Calculation tool to help calculate and simulate active precharge circuit behavior given component values.
TPSI31P1-DOUBLE-RSENSE-CALC	Calculation tool to help calculate and simulate active precharge circuit behavior given component values.

4.3 Documentation Support

1. Texas Instruments, *TPSI31P1-Q1 Automotive Active Pre-charge Controller With 17V Isolated Gate Driver and Bias Supply Datasheet*
2. Texas Instruments, *TPS7A49 36-V, 150-mA, Ultra-Low-Noise, Positive Linear Regulator Datasheet*

4.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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