**Product Overview**

**Generate a Power-On Reset Pulse**

On device start-up, some logic parts may output an invalid state until cleared. A pulse can be generated when $V_{CC}$ turns on to reset those parts to valid output states.

![Power-on reset pulse](image)

**Design Considerations**

- The pulse width is determined by $T = RC$
  - The standard configuration for a 1-ms pulse is $R = 10 \, \text{k}\Omega$, $C = 0.1 \, \mu\text{F}$
- Multiple reset pulse generators with different RCs can be used to delay the pulse to some devices, resetting some before others or triggering clock inputs
- [FAQ] How does a slow or floating input affect a CMOS device?
- [FAQ] Where do I find maximum power dissipation for a device?
- Ask a question on the TI E2E™ forum

**Recommended Parts**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>AEC-Q100</th>
<th>$V_{CC}$ Range</th>
<th>Channels</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LVC1G14</td>
<td></td>
<td>1.65 V – 5.5 V</td>
<td>Inverting buffer</td>
<td>1 channel, Schmitt-trigger inputs</td>
</tr>
<tr>
<td>SN74LVC1G14-Q1</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SN74LVC2G14</td>
<td></td>
<td>1.65 V – 5.5 V</td>
<td>Inverting buffer</td>
<td>2 channel, Schmitt-trigger inputs</td>
</tr>
<tr>
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<td></td>
<td></td>
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<tr>
<td>SN74LVC1G17</td>
<td></td>
<td>1.65 V – 5.5 V</td>
<td>Buffer</td>
<td>1 channel, Schmitt-trigger inputs</td>
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<tr>
<td>SN74LVC1G17-Q1</td>
<td>✓</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For more devices, browse through the [online parametric tool](https://www.ti.com/parametric) where you can sort by desired voltage, channel numbers, and other features.
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