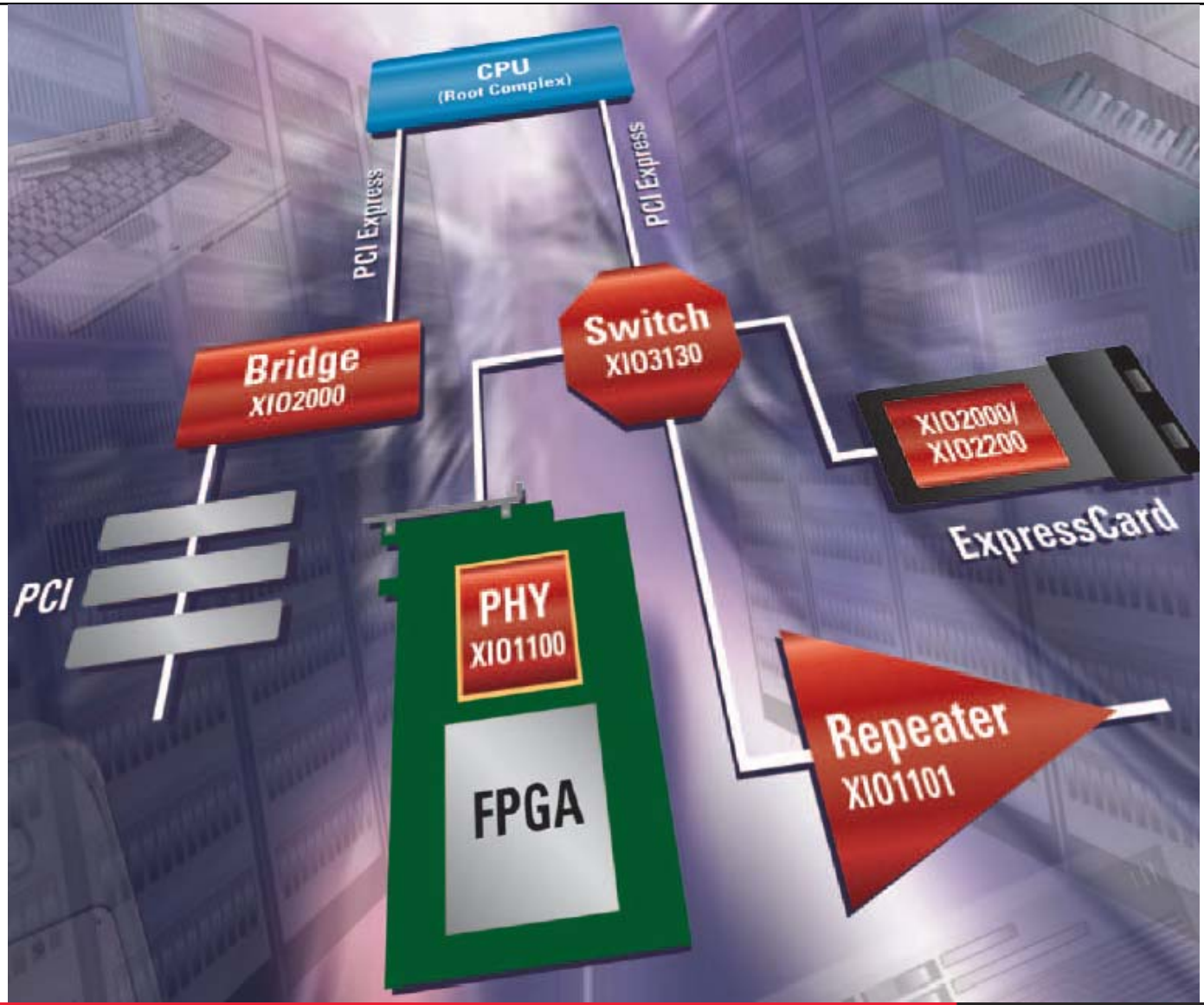
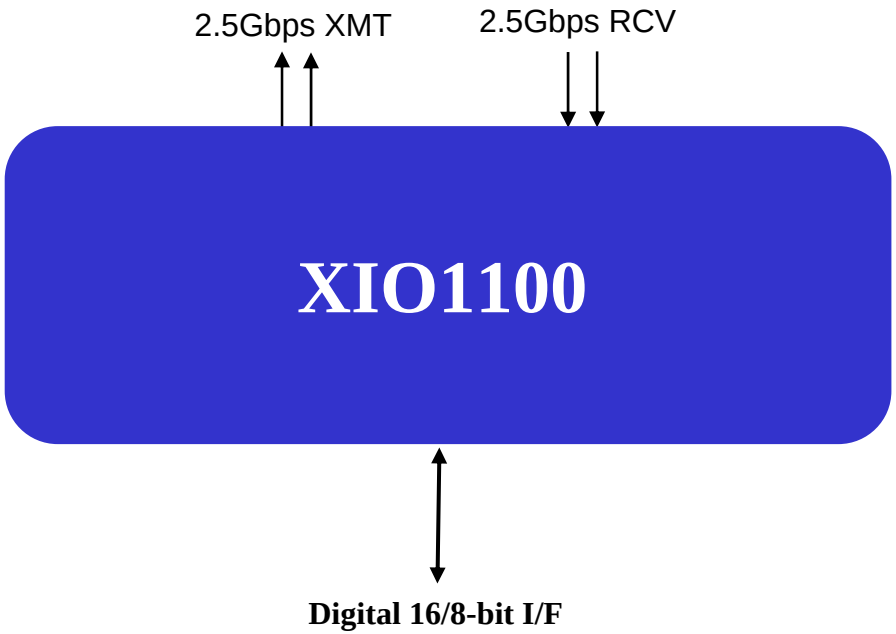
XIO1100 x1 PCIe PHY



SLLT196

XIO1100 – x1 Discrete PHY

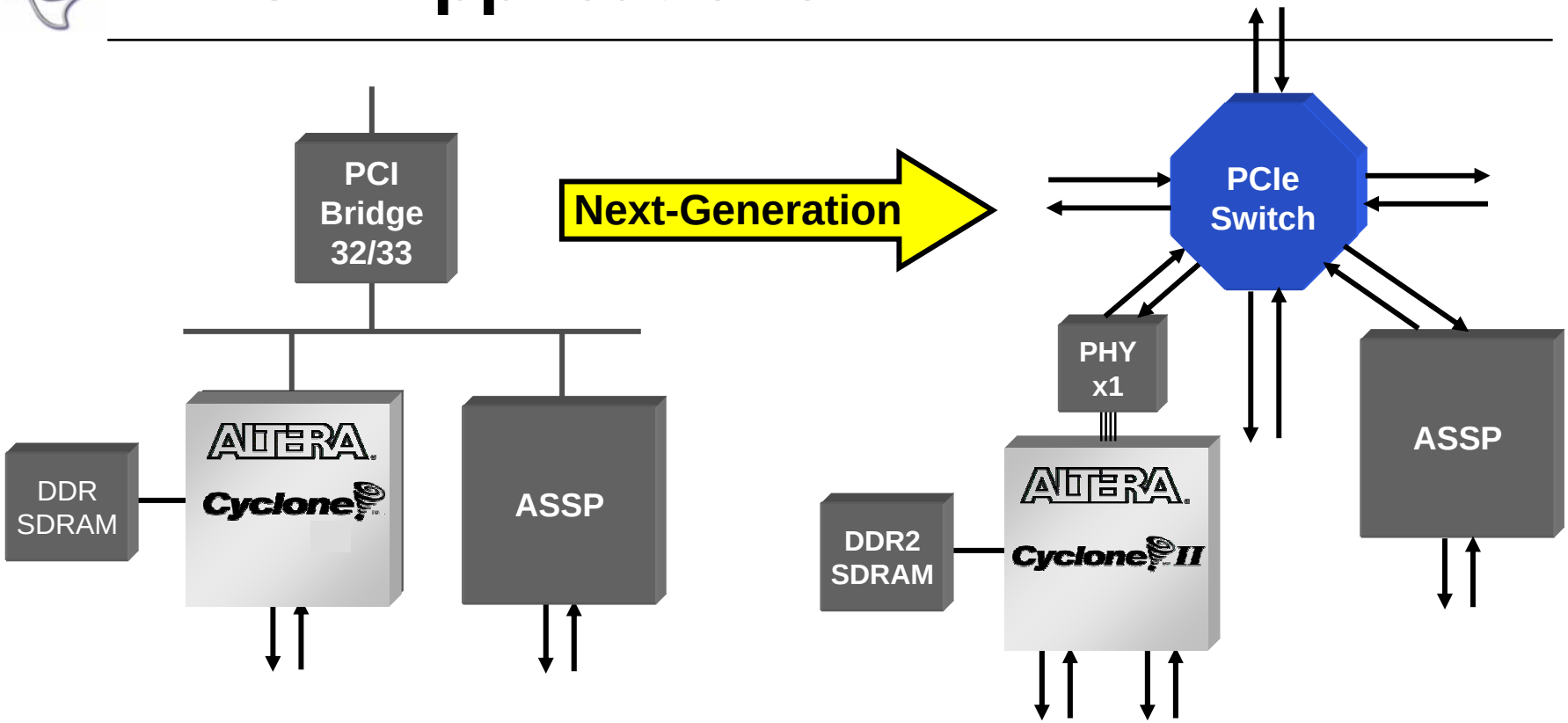


Part Number	Package	Samples	MP
XIO1100 Dev Board	100 pins	4Q05 April 06	April-06

- Discrete x1 ***PCI Express 1.1 Compliant PHY***
  - Meets tighter jitter requirements in 1.1 specification
- ***8/16 bit parallel interface based on Intel PIPE specification***
  - Enhancement of supporting source synchronous clocking on both the Tx and Rx paths that eases board Layout Constraints
  - 125 MHz Data Clock with DDR data
- ***Support for multiple PCI Express reference clocks***
  - 100 MHz Differential
  - 125 MHz Single-Ended
- Supports enhanced low power states by turning off clock in L1
- TI PCI-Express Bridge (XIO2000) and PCI-Express 1394a (XIO2200) based on this technology

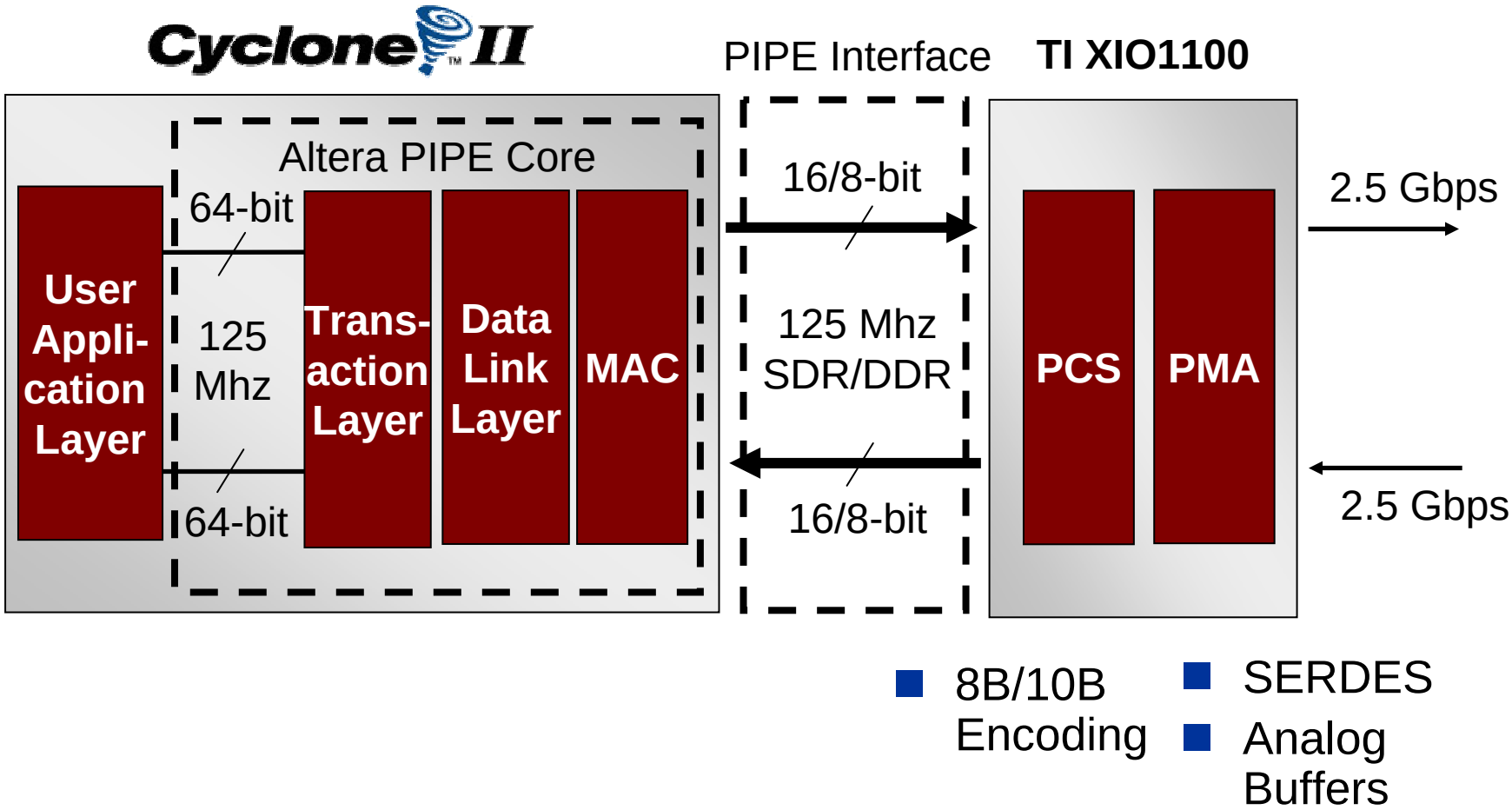
** Sample/Production date subject to change.*

FPGA Applications

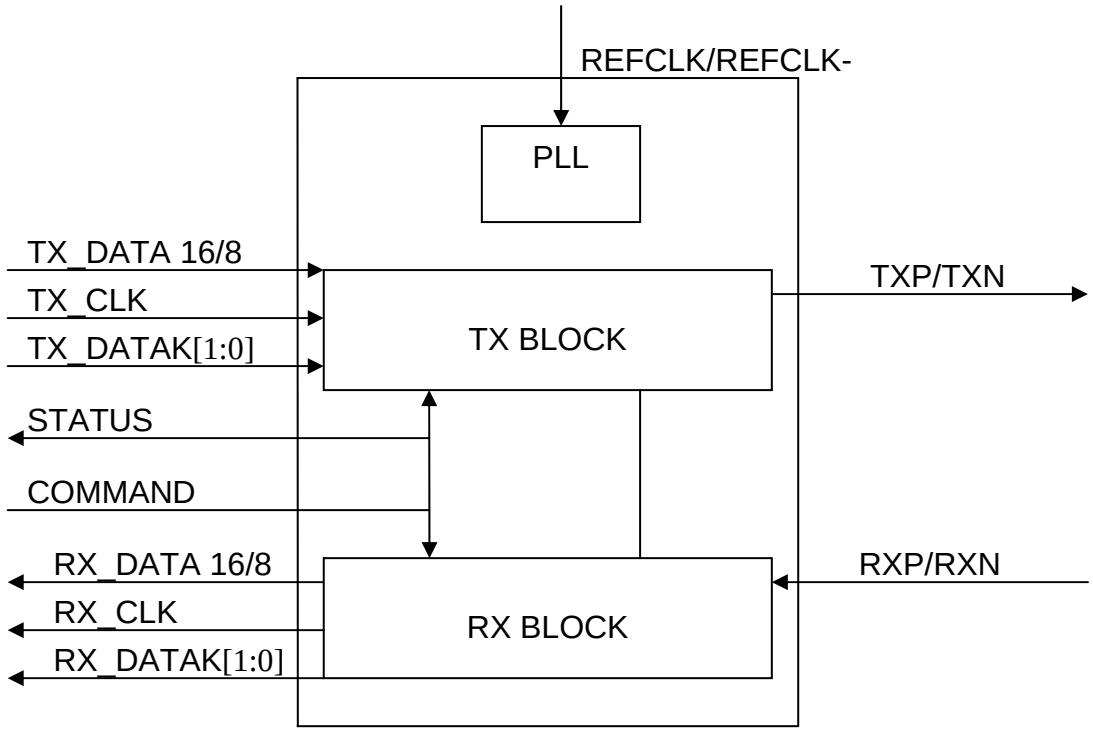


- Replace PCI Bridge Hierarchy With PCI Express Fabric
- Time-to-Market With Custom Endpoint Design in FPGA
  - Increased Performance & Scalability
  - Reduced Cost vs. System Performance

Altera TI x1 PCIe Solution



XIO1100 BLOCK DIAGRAM



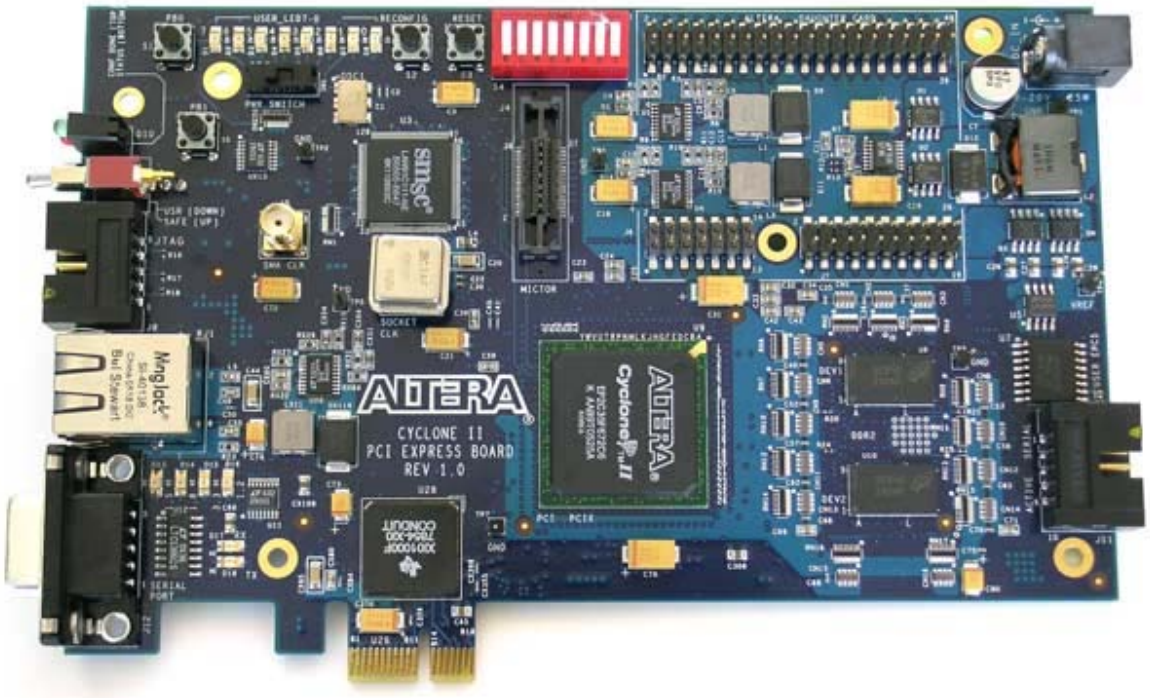
Standard Features of PHY

- 2.5Gb/s data rate
- Utilize 8 or 16-bit parallel interface
- Data/Clock recovery
- 8b/10b encode/decode and error indication
- Receiver Detection
- Supports compliance pattern transmission
- Supports Polarity Inversion of RXP/RXN.

XIO1100 PIPE SUMMARY

- PIPE is a standard defined by Intel Corp.
- XIO1100 uses a modified version of Intel Pipe Interface.
    - Source-Synchronous Clocking (RXCLK & TXCLK) to help in PCB implementations.
- Selectable 8-bit or 16-bit parallel interface.
- High-Speed PCB design techniques must be employed (125MHz and 250MHz frequencies).
    - Match trace lengths
    - Match impedance and eliminate/reduce impedance discontinuities (stubs, transitions thru vias, etc...).
- Model the transmission lines
    - IBIS models available for XIO1100

Altera-TI x1 PCIe Demo Board



XIO1100 Value Proposition

- XIO1100 is TI's third generation PHY
  - Passed PCI SIG Workshop #49 ***v1.0a and v1.1*** Compliance
  - ***Proven PCI Express compatibility and interoperability***
    - XIO1100 base design used in TI's PCI Express compliant devices XIO2000A and XIO2200A (PCIe Integrator list, also included in PCI SIG ExpressCard based Gold Suite tests)
- Flexible MAC interface
  - Selectable 8 or 16-bit parallel interface
    - 16-bit: 125MHz rising-edge clocked
    - 8-bit: 125MHz rising and falling-edge clocked (DDR).
  - Source Synchronous Clocking, i.e. both RX path and TX path have a dedicated clock (TXCLK and RXCLK)
- Support for two PCI Express reference clocks
    - 100 MHz Differential for normal system clock designs
    - 125 MHz Single-Ended for asynchronous clocking designs

XIO1100 Milestone

Deliverables	Target Completion Date
Preliminary Datasheet with Final Pin-out	Now (contact factory or your regional TI sales office)
Demonstration Board	Now
Final Datasheet	April 06
Samples	Now
Dev Kit	April 06
Plugfest (Altera-TI Solution)	PASSED v1.0a and v1.1 Compliance
MP	April 06