Product Overview

DP83TG721 1000BASE-T1 Automotive Ethernet PHY With Advanced TSN and AVB

Features

- IEEE802.3bp 1000BASE-T1 compliant
- OA TC10 compliant, <20µA sleep current
  - Local and remote wake up and wake forwarding
- Advanced TSN
  - IEEE 1588v2/802.1AS Time Synchronization
  - Hardware time-stamping with integrated Phase correction
  - Highly accurate 1pps signal (±15ns)
- Audio Clocking
  - AVB IEEE 1722 media clock generation capability
  - Phase synchronized wall clock output: 1KHz to 50MHz
  - I2S & TDM8 SCLK/FSYNC/MCLK clock generation
- Open Alliance TC12 Interoperability and EMC compliant
  - OA EMC compliant
  - SAE J2962-3 EMC Compliant
- Integrated LPF on MDI pins
- MAC Interfaces: RGMII and SGMII
- Supported I/O voltages: 3.3V, 2.5V, and 1.8V
- Pin compatible with TI's 100BASE-T1 PHYs and 1000BASE-T1 PHYs
  - Single board design for 100BASE-T1 and 1000BASE-T1 with required BOM change
- Diagnostic tool kit
  - Temperature, Voltage, ESD monitor
  - Data throughput calculator : Inbuilt MAC packet generator, counter and error checker
  - Signa Quality Indicator
  - TDR based open and short cable fault detection
  - CQI for cable degredation monitoring
  - Loopback modes
- 25MHz clock output source
- VQFN, wettable flank packaging
- AEC-Q100 Qualified
  - IEC61000-4-2 ESD : ±8-kV contact discharge
  - AECQ Grade 1: –40°C to +125°C ambient operating temperature

Applications

- Telematics control unit (TCU, TBOX)
- AVB
- ADAS: LIDAR, RADAR, Front Camera
- Zonal, Gateway, and body control

Description

The DP83TG721-Q1 device is an IEEE 802.3bp and Open Alliance compliant automotive Ethernet physical layer transceiver. The DP83TG721-Q1 provides all physical layer functions needed to transmit and receive data over unshielded/shielded single twisted-pair cables. The device provides xMII flexibility with support for RGMII and SGMII MAC interfaces.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
DP83TG721SRHARQ1	VQFN (36)	6.00mm × 6.00mm

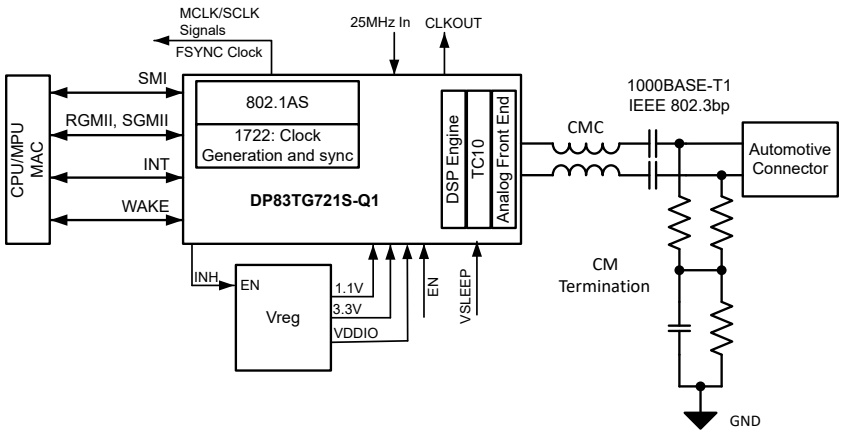

Figure 1. Simplified Schematic

Time Synchronization

The DP83TG721-Q1 integrates IEEE 1588v2/802.1AS timestamping and other additional hardware engine to offer sub 15 nanosecond synchronization accuracy.

The DP83TG721 is also capable of providing a wide range of high quality time synchronization clock (1KHz to 50MHz) and generate synchronous patterns on GPIO's. This enables the DP83TG721 to achieve system level synchronization for ADAS sensor data synchronization, Corner Radar Chirp synchronization, 1pps signal for GPS, LIDAR, V2x, etc.

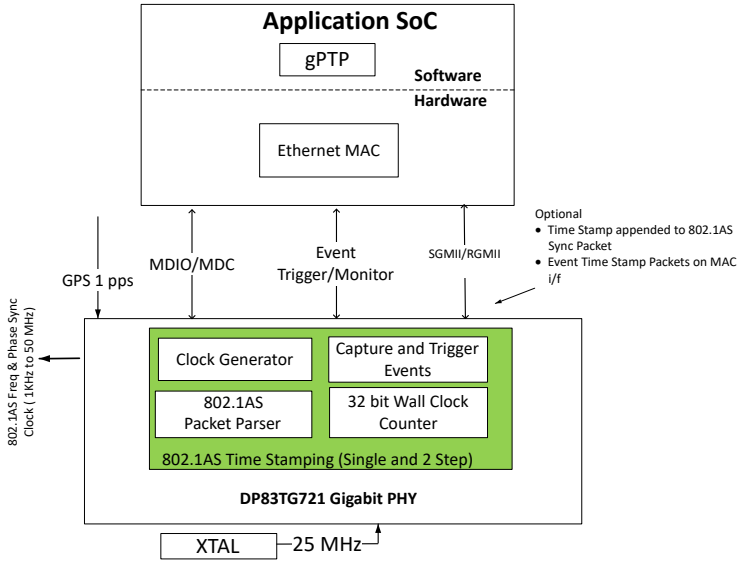

Figure 2. DP83TG721-Q1 802.1AS Time Synchronization Architecture

Integrated Audio Over Ethernet

DP83TG721 offers audio clocking designs for AVB (Audio Video Bridging) and other Audio transports protocols (IES676, IEEE 1733 RTP, Dante) by:

- Generating IEEE 1722 Media Clock with embedded CRF packet decode
- Synchronized clocks (FSYNC, BCLK, MCLK) for Audio interface I2S and TDMx.

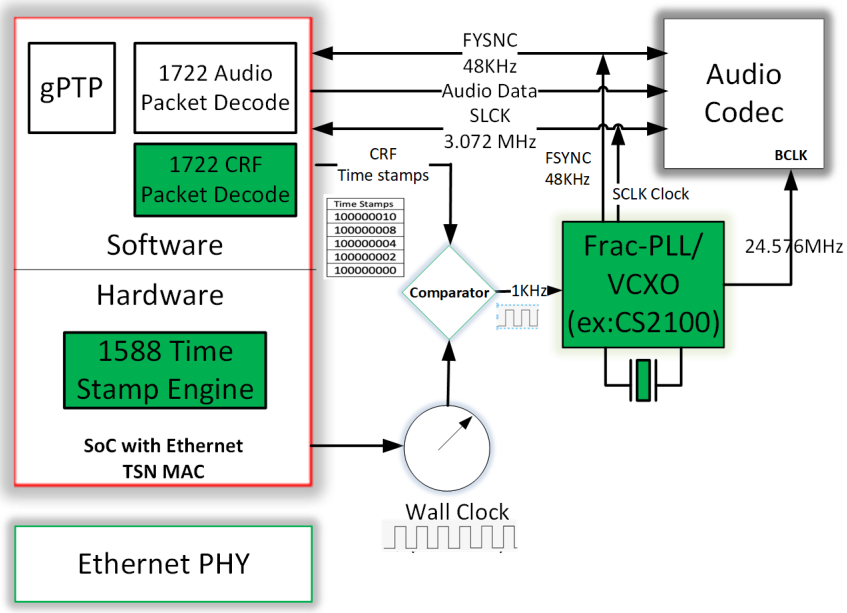

Figure 3. Typical Audio Over Ethernet Architecture

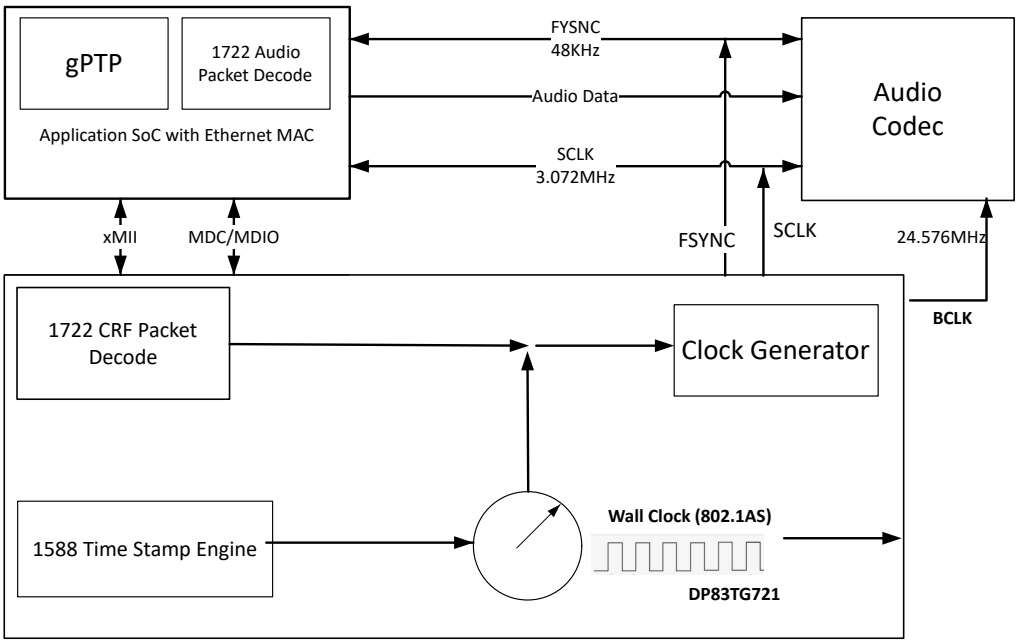

Figure 4. Audio Over Ethernet Architecture with DP83TG721

TC10 Sleep/Wake-Up

DP83TG721 supports Open Alliance TC10 Sleep/Wake-up feature. DP83TG721 supports local/remote wake-up, wake-forwarding, sleep negotiation as outlined in the TC10 specification.

The block diagram of a general system implementation of TC10 is as shown below

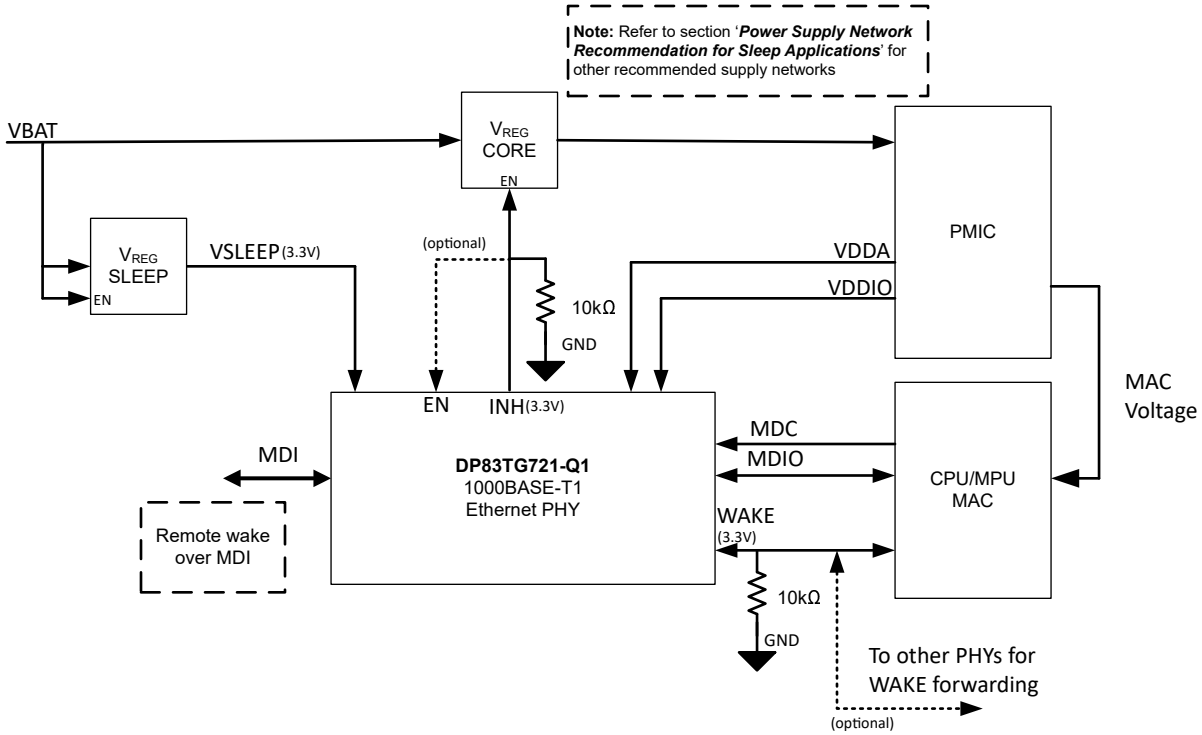

Figure 5. TC10 System Implementation Diagram

DP83TG721 EVM-MC and Software Support

The DP83TG721EVM-MC supports 1000Mbps speed and a DP83867 is provided for copper (1000BASE-T) media conversion using the RGMII MAC Interface.

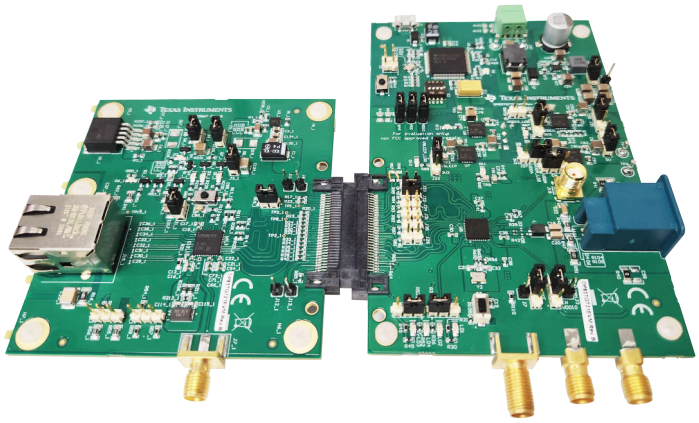

Figure 6. DP83TG721EVM-MC

The DP83TG721EVM-MC offers:

- Media Converter: 1000BASE-T to 1000BASE-T1
- IEEE802.3bp Compliant
- RGMII Back-to-Back Configuration
- On-board MSP430F5529
  - USB2MDIO/ DIEP Support
- Status LEDs
  - Link
  - Link + Activity
  - Power-On

New DIEP Debug Interface Experience

DIEP offers all your Ethernet PHY debug needs in one place including MDIO bus serial management, device control registers, access to both extended registers and standard registers, and the ability to save data read and run script text files.

- ***NEW*** restructured navigation and register display
- ***NEW*** improved text script execution

Debug Interface for Ethernet PHY's (DIEP)

Comparison of Device Features

The DP83TG721 enables very high time synchronization accuracy for automotive applications. Compared to the DP83TG720x series, the DP83TG721 offers advanced diagnostic tools, hardware time stamping, TC-10 low power sleep, and has integrated Audio Video Bridging (AVB). Table 1 provides an overview of feature differences between the two.

Table 2. Comparison Between DP83TG720x and DP83TG721

Feature	DP83TG720x-Q1	DP83TG721-Q1
Interfaces		
PMA/PMD	1000Base-T1	1000Base-T1
MAC Interface Support	RGMII only (for DP83TG720R-Q1) RGMII, SGMII (for DP83TG720S-Q1)	RGMII only (for DP83TG721R-Q1) RGMII, SGMII (for DP83TG721S-Q1)
Features Supported		
Sleep/Wake functionality	Custom Sleep/Wake Implementation	OA TC10 Compliant Implementation
Internal Power Shutdown	No	Supported with EN pin
Diagnostics	Signal Quality Indicatior (SQI) Time Domain Reflectometry (TDR) Built-In Self Test (BIST) Compliance Test Modes	Signal Quality Indicatior (SQI) Time Domain Reflectometry (TDR) Built-In Self Test (BIST) Compliance Test Modes Cable Quality Indicator (CQI)
802.1AS Support	No	PTP Wall Clock Tranmsit and Receive Packet Parsing and Timestamping Event Triggering and Timestamping
AVB Clock Generation	No	IEEE1722 CRF packet decode Media, Bit and Codec Clock Generation
Power Supply		
VDDA3P3V	3.3V +/- 10%	3.3V +/- 10%
VDDIO	1.8V +/- 10% 2.5V +/- 10% 3.3V +/- 10%	1.8V +/- 10% 2.5V +/- 10% 3.3V +/- 5%
VSLEEP	3.3V +/- 10%	3.3V +/- 10%
VDD	0.95V - 1.1V	1.05V - 1.21V

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