

# TMS320TCI6484

## DSP for MAC and PHY layer processing in femtocell and macro wireless base stations plus other high-performance applications



### Product Bulletin

#### Higher system performance at lower costs

The TCI6484 offers a high-performance, low power per channel, digital signal processor (DSP) capable of supporting both MAC and PHY layer processing for 2G, 3G and 4G wireless base stations. By eliminating the need for a RISC processor dedicated to MAC-layer processing and by improving its data throughput capabilities, the TCI6484 is an ideal platform for a higher density, lower cost system. With the use of just one instead of two distinct processors, latencies stemming from inter-processor communication are eliminated and the system's software architecture is simplified, thereby increasing the efficiency of the system and reducing development costs. As a result, base station manufacturers

can accelerate their development processes, delivering new features and systems to market faster.

With the support of two TCP2 accelerators, the TCI6484 can support symbol processing rates as high as 34 Mbps. Higher throughput gives base station manufacturers the opportunity to either lower system costs by deploying fewer DSPs for the same system performance or increasing system density with a greater number of carriers or channels per card.

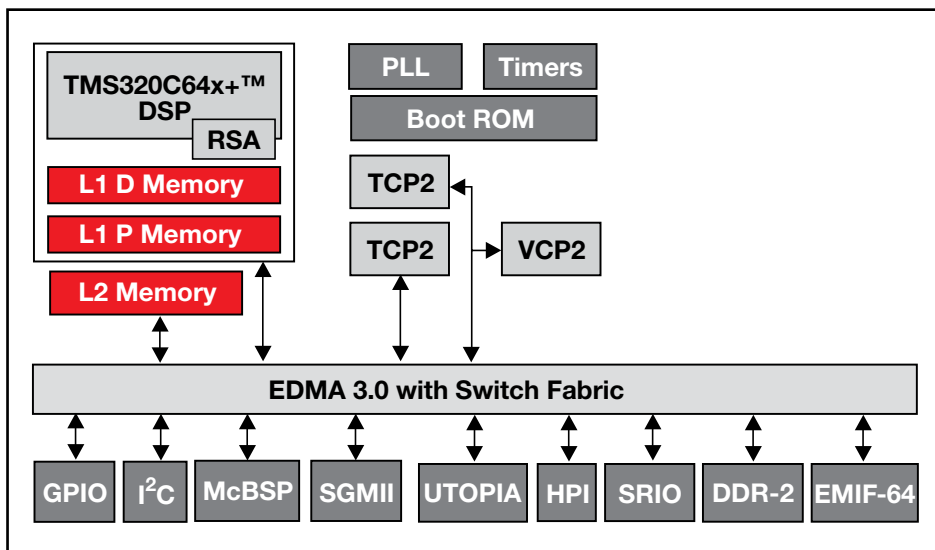
#### Multiple standards, multiple applications

The TCI6484 leverages TI's leading 65-nm process technology to integrate greater functionality, including additional high-performance

#### Key Features

- Programmable platform can support multiple standards: GSM-EDGE, EDGE Evolution, TD-SCDMA, WCDMA, HSPA, HSPA+, LTE and WiMAX
- Scalable across multiple form factors: macro, micro, pico and femtocell base stations
- Support for MAC and PHY layers on a single platform eliminates the need for a RISC coprocessor
- Enhanced memory and cache performance for efficient MAC-layer processing:
  - Increased L2 cache size to 1 MB; total L2 memory of 2 MB
  - Increased 32-bit DDR memory speed to 667 MHz
- Industry-leading, 65-nm process technology allows for greater integration
- Increased symbol rate processing with up to 34 Mbps of performance with two turbo accelerators (TCP2)
- Full selection of peripherals: Serial Rapid IO, sGMII for 10/100/1000 Ethernet, HPI, I<sup>2</sup>C, two McBSP ports and UTOPIA

▼ A detailed block diagram of the TCI6484



accelerators and new peripheral interfaces. This breakthrough in integration and the small space-saving device size allows manufacturers to increase the channel and carrier capacity of their base station systems.

The versatility and high-performance capabilities of the TCI6484 make the device an ideal processing engine for a wide range of wireless standards, including GSM-EDGE, EDGE Evolution, TD-SCDMA, WCDMA, HSPA, HSPA+, LTE and WiMAX. In addition, the TCI6484 is easily scalable into designs that target the most prevalent base station configurations, such as macro, micro, pico and femtocell applications.

### MAC-layer processing

The many enhancements to the TCI6484 DSP make it an excellent platform for MAC-layer processing in wireless base stations. New features of the memory subsystem include expanding the maximum size of the Level 2 (L2) cache memory by a factor of four over the previous generation device. As a result, the size of the L2 cache has increased from 256 KB to 1 MB. The larger on-chip cache memory space for storing frequently used instructions and data improves the overall processing performance of the device by reducing the likelihood that it must access data stored in slower external memory.

The speed at which the TCI6484 accesses data stored in external memory has also been greatly increased. The DDR2 memory interface on the device has been enhanced with faster data transfer speeds

that are 25 percent higher than the previous generation C64x+ DSP-based device. This reduces the latencies that could develop when data is transferred between the external memory and the TCI6484 DSP's core. Internally, the interface to DDR2 memory has been enhanced with improved internal buffering capabilities and a wider bus width to increase the throughput of data within this memory space.

### Increased data throughput

With its ability to process symbol data at a rate of 34 Mbps, the TCI6484 is an ideal platform for higher density, lower cost base station systems such as femtocells. The device supports the symbol processing rates needed for multiple sectors or carriers for applications like GSM-EDGE, EDGE Evolution, WCDMA, HSPA, HSPA+ and TD-SCDMA. The TCI6484 is also an excellent platform for 4G applications like WiMAX Wave 2 and initial LTE deployments.

### Faster peripherals

For efficient, high-density base station systems, the TCI6484 DSP features a full set of the high-performance peripheral interfaces for communicating with networks, external memory, switching devices and other processors that may be present on the channel card. The on-chip interfaces include the sGMII interface, which is capable of supporting 10/100/1000 Ethernet connectivity through a serial interface, and four lanes of the Serial Rapid IO (SRIO) interface, which are capable of data rates of 1.25, 2.5 and 3.125 Gbps.

The SRIO interface can be configured either as a four-lane bus or as a set of four single-lane high-speed links. The TCI6484 also incorporates an HPI interface, I<sup>2</sup>C connectivity, two McBSP ports and a UTOPIA interface.

### Shortened development cycles

The TCI6484 DSP uses the same 1-GHz C64x+ DSP core found in the TCI6482 device. In addition, the TCI6484 DSP core is upward code-compatible to the C64x™ DSP processing core of the TCI100, TCI100Q and other C641x+ DSPs. By reusing the software developed on the previous generations of C64x+ and C64x DSPs, equipment manufacturers can reduce their overall development time and cost.

The TCI6484 is supported by the user-friendly Code Composer Studio™ integrated development environment and a hardware development card that supports two TCI6484 DSPs. Base station manufacturers and other high-performance application developers can also leverage TI's extensive network of third-party developers who can provide a wealth of tools, software solutions and hardware development cards.

### For more information

To learn more about the TMS320TCI6484 DSP or other solutions for wireless infrastructures, contact your local TI field sales office or visit [www.ti.com/tci6484](http://www.ti.com/tci6484).

High-performance TCI6484 features	TCI100Q	TCI6482	TCI6484
<b>Processing</b>	850 MHz Single TCP1	1 GHz Single TCP2	1 GHz Dual TCP2
<b>Memory subsystem</b>	Total of 1 MB L2 Max cache size 256 KB	Total of 2 MB L2 Max cache size 256 KB	Total of 2 MB L2 Max cache size 1 MB
<b>Peripherals</b>	No RapidIO lanes No Ethernet No DDR	4x Serial Rapid IO Ethernet: RGMII DDR2 @ 533 MHz	4x Serial Rapid IO Ethernet: SGMI DDR2 @ 667 MHz

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