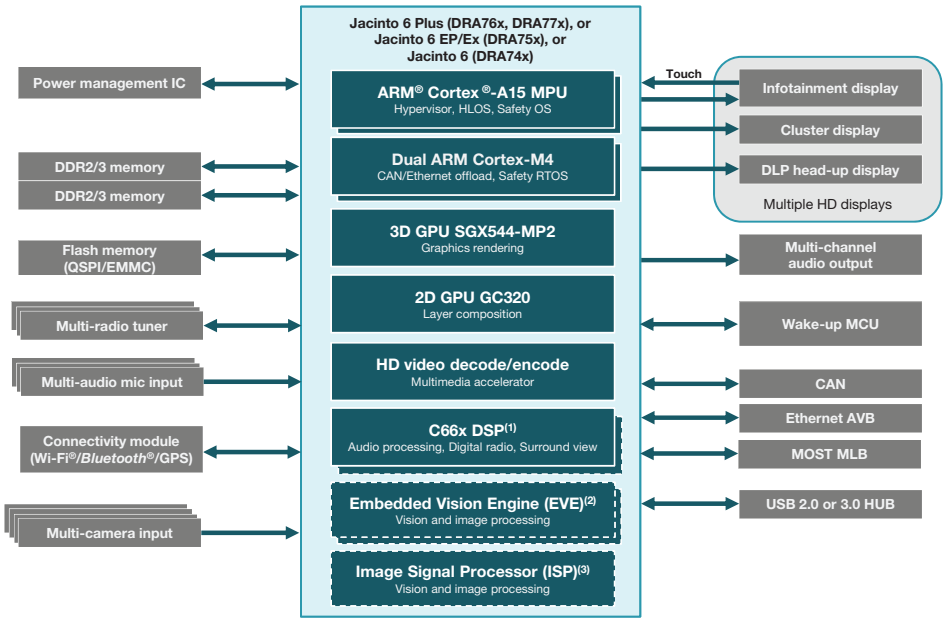
Overview – “Jacinto 6” SoCs for automotive digital cockpit

The powerful “Jacinto 6” SoC family enables automotive digital cockpit solutions where functionality from several vehicle Electronic Control Units (ECUs) are integrated into a single powerful “Jacinto 6” SoC that can support all of the user interface and communications functions, including: head unit, digital instrument cluster, heads-up display, rear-seat entertainment, informational ADAS–rear camera and surround view, telematics.



(1) Second DSP available on Jacinto 6 EP/Ex (DRA75x) and Jacinto 6 Plus EP/Ex (DRA77x)
(2) Dual embedded vision engine (EVE) available on Jacinto 6 Ex (DRA75x) and Jacinto 6 Plus Ex (DRA77x)
(3) ISP available on Jacinto 6 Plus family (DRA76x/DRA77x)

Features and benefits: TI “Jacinto 6” value proposition

Features	Benefits
Performance provided by heterogeneous architecture	“Jacinto 6” supports multiple digital cockpit applications, including those with safety requirements, without compromising performance. In addition to the main ARM® Cortex®-A15 core, 3D Graphical Processing Unit and multimedia accelerators enable multiple use cases and functionalities such as: • In-vehicle infotainment • Digital instrument cluster • Multi-OS/Multi-domain • Navigation and routing • Voice recognition and control • Smartphone projection • High-performance graphics and display • Fast boot/Early boot • Safety certifiable systems • Hardware and software sSecurity
Signal, image and vision processing	“Jacinto 6” SoC family integrates digital signal processor (C66x DSP), image signal processor (ISP) and embedded vision engine (EVE) coprocessors to offload all the heavy signal, image and vision processing to enable integration of following cockpit features: • Software-defined digital radio • Audio processing • Driver monitoring and identification • Robust rear-view camera and surround view • Image processing
Integration of automotive peripherals to optimize system BOM	“Jacinto 6” SoCs provide right set of peripherals to enable cockpit integration and optimized system BOM including: • Multi-HD display support • Multi-HD camera input interfaces • Automotive peripherals including eAVB, CAN and MOST • Rich set of high-speed and connectivity interfaces including PCIe, USB, etc.
Software platforming	All “Jacinto 6” processors share a common core platform and architecture, allowing software to be reused as developers scale their design from entry to premium segments and reducing time to market.

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