“Jacinto 6 Plus”
Automotive Processors

Device Overview

TI’s new “Jacinto 6 Plus” processors are an extension of the current “Jacinto 6” family of devices with improved performance and additional features. Using the same common core platform and heterogeneous architecture as the existing “Jacinto 6” family enables software platforming, allowing for maximum reuse of investments and reduced time to market.

- **“Jacinto 6 Plus”** – Improved performance in the main processing units (MPUs), TMS320C66x digital signal processor (DSP), graphics processing unit (GPU), and memory speed allows for concurrencies of infotainment and digital cluster features, emerging analytics and image manipulation, as well as multi-OS capabilities. The integration of an image signal processor (ISP), CSI-2 ports, and CAN-FD1 enable an optimized system bill-of-materials (BOM) while supporting innovation.
- **“Jacinto 6 EP Plus”** - Adds a second TMS320C66x digital signal processor (DSP) core for image manipulation technologies such as dynamically stitching multiple cameras into a single, surround view; additional multi-radio tuner configurations; complex post processing algorithms for audio and speech processing and a variety of other differentiated technologies like driver monitoring system (DMS).
- **“Jacinto 6 Ex Plus”** - Further extends performance and integration possibilities from the “Jacinto 6 EP” by offering the TI Vision AccelerationPac including two embedded vision engines (EVEs) enabling simultaneous informational advanced driver assistance systems (ADAS) and infotainment functionalities without compromising the performance of either system.

Introduction

The DRA74xP, DRA75xP, DRA76xP, and DRA77xP automotive applications processors are built to meet the intense processing needs of the modern digital cockpit automobile experiences.

Device Features

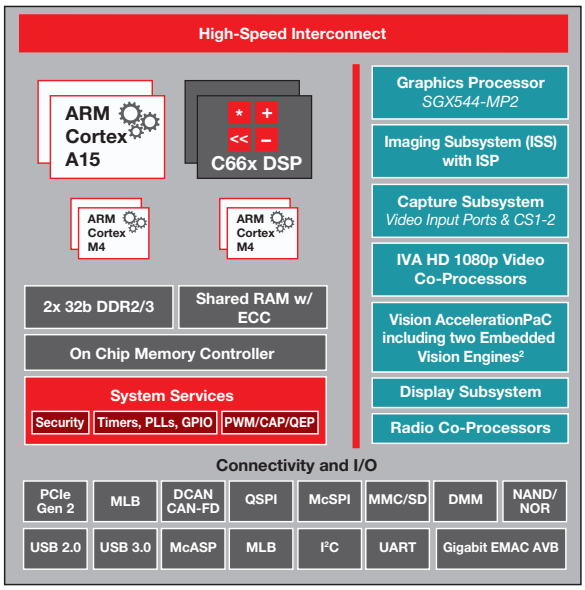
- The device is composed of the following subsystems:
  - Two ARM® Cortex®-A15 microprocessor units (MPUs)
  - Two digital signal processors (DSP C66x subsystem)
  - Imaging Subsystem (ISS), including an image signal processor (ISP)
  - Image and video accelerator high definition (IVA-HD) subsystem
  - Two ARM Cortex-M4 processing subsystems, each including two ARM Cortex-M4 microprocessors
  - Vision AccelerationPac including two embedded vision engines (EVEs)[2]
  - Display subsystem (DSS)
  - Video Processing subsystem (VPE)
  - MIPI® CSI-2 camera serial interface[1]
  - Video Input Capture (VIP)
  - Dual-core POWERVR™ SGX544-MPx 3D GPU
  - 2D-graphics accelerator (BB2D) subsystem, including Vivante™ GC320 core
  - Three pulsewidth modulation (PWM) subsystem
  - Real-time clock (RTCsubsystem
  - Debug subsystem

Package

- The “Jacinto 6 Plus” devices are offered in two packages:
- DRA74xP and DRA75xP are available in a 760-ball, 23x23mm, 0.8mm pitch ball grid array (BGA) package, allowing for pin-to-pin compatibility with existing “Jacinto 6” devices.
- DRA76xP and DRA77xP are available in a 784-ball, 23x23mm, 0.8mm pitch ball grid array (BGA) package to take full advantage of Jacinto 6 Plus capability and performance.

1: CSI-2 and CAN-FD available on DRA76xP and DRA77xP only

2: Vision AccelerationPac for Jacinto 6 Ex Plus only



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