TPS50601-SP Total Ionizing Dose (TID) Radiation Report

This report discusses the results of the *Total Ionizing Dose* (TID) testing the *Radiation Hardness Assured* (RHA), QML Class V - TI's TPS50601-SP (5962R1022101VSC). The RHA version of the TPS50601-SP passes up to 100 krad (Si) *Low Dose Rate* and 100 krad (Si) *High Dose Rate* TID, and does not exhibit *Enhanced Low Dose Rate Sensitivity* (ELDRS).

NOTE: For questions or comments, contact hirelmarketing@list.ti.com.

Contents

List of Figures

List of Tables

1 Applicable and Reference Documents

1.1 Applicable Documents

- TPS50601-SP data sheet (SLVSD45)
- TPS50601-SP Dual Evaluation Module (http://www.ti.com/tool/tps50601spevm-d)
- TPS50601-SP Single Evaluation Module (http://www.ti.com/tool/TPS50601SPEVM-S)
- *TPS50601SPEVM, 6-A/12-A, SWIFT™ Regulator Evaluation Module* (SLVU499)
- TPS50601-SP PSpice Average Model (http://www.ti.com/lit/zip/slvm776)
- TPS50601-SP PSpice Transient Model (http://www.ti.com/lit/zip/slvm760)

1.2 Reference Documents

TI's TID radiation (total dose) test procedure follows the standards put forth in MIL-STD-883 TM 1019. The document is found at the DLA website:
http://www.landandmaritime.dla.mil/programs/milspec/ListDocs.aspx?BasicDoc=MIL-STD-883

2 Device Information

2.1 Product Description

The TPS50601-SP is a radiation-hardened 1.6- to 6.3-V_{IN}, 6-A synchronous step-down converter, which is optimized for small footprint designs through integrating the high- and low-side MOSFETs. Further space savings is achieved through current mode control, which reduces component count, and a high switching frequency, reducing the footprint of he inductor. Optimal packaging provides an excellent power efficiency in an ultra-small footprint.

The TPS50601-SP has been RHA qualified to 100 krad (Si) under both low-dose rate (LDR) and high-dose rate (HDR). It is orderable under SMD 5962R1022101VSC in our thermally enhanced 20-pin ceramic, dual in-line flat pack package.

2.2 Device Details

Table 1 lists the device information used in the initial RHA TID characterization and qualification of HDR tests. Current production lot RLAT data is always found in the Group E report shipped. The process for pulling the group E report from TI is described in *TI QML Class V/Q Lot Documents* (SBOA140).

Table 1. Device and Exposure Details

TID HDR/LDR Details: Up to 150 krad (Si)	
TI Device Number	TPS50601-SP (5962R1022101VSC)
Package	20-pin ceramic flatpack (HKH)
Technology	LBC7x
Die Lot Number	2108506TI1
A/T Lot Number / Date Code	lot # 3002141 (1311B, W15), lot# 3002142 (1311A, W16), lot# 3002147 (1311C, W14)
Quantity Tested	48 device including 1 control device
Lot Accept/Reject	Devices passed 3 krad (Si), 10 krad (Si), 30 krad (Si), 50 krad (Si), 100 krad (Si)(1), and 150 krad (Si)(2)
HDR Radiation Facility	Texas Instruments SVA Group, Santa Clara, CA
LDR Radiation Facility	RAD/Aeroflex in Colorado Springs, Colorado
HDR Dose Level	3 krad (Si), 10 krad (Si), 30 krad (Si), 50 krad (Si), 100 krad (Si), and 150 krad (Si)(2)
HDR Dose Rate	65 rad / s
LDR Dose Level	3krad (Si), 10 krad (Si), 30 krad (Si), 50 krad (Si), 100 krad (Si)
LDR Dose Rate	0.01 rad / s
HDR Radiation Source	Gammacell 220 Excel (GC-220E) Co-60
LDR Radiation Source	Gammacell JLSA 81-24 Co-60
Irradiation Temperature	Ambient, room temperature

(1) 100 krad (Si) units pass total ionization dose irradiation for application environments with dose rate less than 0.05 rad (Si) / s, per MIL-STD-883 1019.9, Condition A and section 3.11 extended room temperature anneal test.
(2) 150 krad (Si) units pass, per MIL-STD-883 1019.9, Condition A and section 3.12 MOS acceleration annealing test.

Figure 1. TPS50601-SP Device Used in Exposure

3 Total Dose Test Setup

3.1 Test Overview

The TPS50601-SP was tested according to MIL-STD-883, Test Method 1019.9. For this testing, Condition A and D was used. For Condition A, the product was irradiated up to 1.5 × the rated radiation level and then put through full electrical parametric testing on the production *Automated Test Equipment* (ATE). The device was functional and passed all electrical parametric tests with the readings within (guard bands) of the *Standard Microcircuit Drawing* (SMD) electrical specification limits.

The TPS50601-SP Linear BiCMOS (LBC7) process technology contains CMOS and Bipolar components. Due to the use of Bipolars in the design, an ELDRS study was performed to determine if the device has an LDR sensitivity.

3.2 Test Description and Facilities

The TPS50601-SP LDR exposure was performed on biased and unbiased devices in a Co60 gamma cell under a 10 mrad (Si) / s exposure rate. The dose rate of the irradiator used in the exposure ranges from < 10 mrad (Si) / s to a maximum of approximately 100 krad (Si) / s, determined by the distance from the source. For the LDR (10 mrad (Si) / s) exposure, the test box was positioned approximately 2 m from the source. The exposure boards are housed in a lead-aluminum box (as specified in MIL-STD-883 TM 1019.9) to harden the gamma spectrum and minimize dose enhancement effects. The irradiator calibration is maintained by *Longmire Laboratories* using *Thermoluminescence Dosimeters* (TLDs) traceable to the *National Institute of Standards and Technology* (NIST) and the dosimetry was verified using TLDs prior to the radiation exposures. After exposure, the devices were packed in dry ice (per MIL-STD-883 Method 1019.9 section 3.10) and returned to TI Dallas for a full post-radiation electrical evaluation using TI's production Automated Test Equipment (ATE). ATE guard band test limits are set within SMD electrical limits to ensure a minimum Cpk and test error margin based on initial qualification and characterization data. Post-radiation measurements were taken within 30 minutes of removal of the devices from the dry ice container. The devices were allowed to reach room temperature prior to electrical post-radiation measurements.

The TPS50601-SP HDR exposure was performed on biased and unbiased devices in a Co60 gamma cell at TI's SVA facility in Santa Clara California. The un-attenuated dose rate of this cell is 65 rad (Si) / s. After exposure, the devices were packed in dry ice (per MIL-STD-883 Method 1019.9 section 3.10) and returned to TI Dallas for a full post-radiation electrical evaluation using TI's ATE. ATE guard band test limits are set within SMD electrical limits to ensure a minimum Cpk and test error margin based on initial qualification and characterization data. Post-radiation measurements were taken within 30 minutes of removal of the devices from the dry ice container. The devices were allowed to reach room temperature prior to electrical post-radiation measurements.

3.3 Test Setup Details

The devices under HDR and LDR exposure were tested in both biased and unbiased conditions as described in the following:

(A) **Unbiased** – For the unbiased LDR conditions, the exposure was with grounded outputs. The unbiased exposure was not performed for HDR.

(B) **Biased** – Figure 2 shows the biased diagram that was used for HDR and LDR exposure for the RHA characterization.

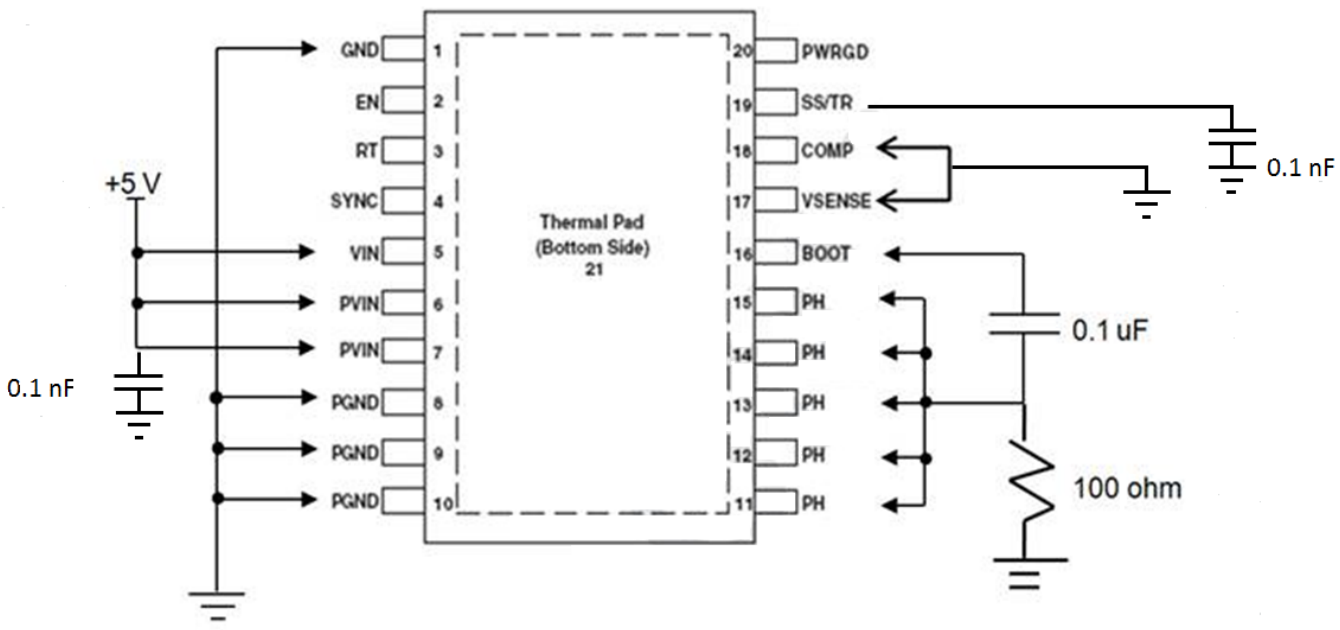

Figure 2. Bias Diagram Used in TID Exposure

3.4 Test Configuration and Condition

A step-stress (3 k, 10 k, 30 k, 50 k, 100 krad) test method was used to determine the TID hardness level. That is, after a predetermined TID level was reached, an electrical test was performed on a given sample of parts to verify that the units where within SMD electrical test limits. MIL-STD-883, Test Method 1019.9, Condition A and D was used in this case. If this passes, then the wafer lot can be certified as an RHA wafer lot.

Table 2 and Table 3 list the samples used during the RHA characterization.

Table 2. HDR Biased Device Information

HDR = 65 rad (Si) / s					
Total Samples: 5 biased / TID level					
Exposure Level					
3 k	10 k	30 k	50 k	100 k (RLAT included)	150 k
01 (wafer 14) 03 (wafer 14) 02 (wafer 15) 03 (wafer 15) 60 (wafer 16)	06 (wafer 14) 10 (wafer 14) 04 (wafer 15) 49 (wafer 16) 51 (wafer 16)	09 (wafer 14) 12 (wafer 15) 06 (wafer 15) 47 (wafer 16) 48 (wafer 16)	13 (wafer 14) 10 (wafer 15) 11 (wafer 15) 44 (wafer 16) 45 (wafer 16)	15, 19, 27, 28, 29, 30, 32 (wafer 14) 17, 19, 23, 25, 26, 29, 30 (wafer 15) 16, 17, 21, 22, 27, 30, 31, 32 (wafer 16)	14 (wafer 14) 12 (wafer 15) 14 (wafer 15) 36 (wafer 16) 43 (wafer 16)

Control Unit
1

Table 3. LDR Device and Exposure Information

LDR = 10 mrad (Si) / s	
Total Samples: 5 biased / TID level	
Exposure Level	
50 k	100 k (RLAT included)
Unit 09 (W19 → Q1, Q2, Q3, Q4, Q5)	Unit 11 (W19 → Q1, Q2, Q3, Q4, Q5) 43, 44, 45, 53, 55, 59, 60 (wafer 14) 34, 37, 39, 43, 45, 49, 53 (wafer 15) 03, 04, 05, 09, 10, 11, 14, 15 (wafer 16)

LDR = 10 mrad (Si) / s				
Total Samples: 10 Unbiased / TID level				
Exposure Level				
3 k	10 k	30 k	50 k	100 k
01 (W19 → Q1) 01 (W19 → Q2) 01 (W19 → Q3) 01 (W19 → Q4) 01 (W19 → Q5) 02 (W19 → Q1) 02 (W19 → Q2) 02 (W19 → Q3) 02 (W19 → Q4) 02 (W19 → Q5)	03 (W19 → Q1) 03 (W19 → Q2) 03 (W19 → Q3) 03 (W19 → Q4) 03 (W19 → Q5) 04 (W19 → Q1) 04 (W19 → Q2) 04 (W19 → Q3) 04 (W19 → Q4) 04 (W19 → Q5)	05 (W19 → Q1) 05 (W19 → Q2) 05 (W19 → Q3) 05 (W19 → Q4) 05 (W19 → Q5) 06 (W19 → Q1) 06 (W19 → Q2) 06 (W19 → Q3) 06 (W19 → Q4) 06 (W19 → Q5)	01 (W19 → Q1) 01 (W19 → Q2) 01 (W19 → Q3) 01 (W19 → Q4) 01 (W19 → Q5) 02 (W19 → Q1) 02 (W19 → Q2) 02 (W19 → Q3) 02 (W19 → Q4) 02 (W19 → Q5)	03 (W19 → Q1) 03 (W19 → Q2) 03 (W19 → Q3) 03 (W19 → Q4) 03 (W19 → Q5) 04 (W19 → Q1) 04 (W19 → Q2) 04 (W19 → Q3) 04 (W19 → Q4) 04 (W19 → Q5) 12 (W19 → Q1) 12 (W19 → Q2) 12 (W19 → Q3) 12 (W19 → Q4) 12 (W19 → Q5)

Control Unit
3, 7, 14, 15, 16, 17

4 Total Ionizing Dose (RHA) Characterization Test Results

4.1 Total Ionizing Dose RHA Characterization Summary Results

The parametric data for the TPS50601-SP passes up to 100 krad (Si) LDR and 100 krad (Si) HDR TID.

The 150 krad (Si) HDR units were parametrically tested on ATE and then put through 100ºC anneal for 168 hours. The units were then put through parametric testing on the ATE and passed all tests to the specified SMD test limits. These units do not exhibit time-dependent effects (TDE) degradation after Rebound test, per MIL-STD-883 1019 Condition A and section 3.12 accelerated annealing test. Rebound testing is applicable for devices containing MOS components.

The drift of SMD electrical parameters including critical parameters through LDR is within experimental error to the drift at HDR. The device is tested to a maximum total dose of 100 krad (Si) per MIL-STD-883, TM1090 Condition A and Condition D.

The TPS50601-SP passed post-electrical testing over all the conditions below ensuring that the wafer lot is certifiable as 100 krad RHA. Samples were assembled and included from all five sections (top, bottom, middle, right, and left) from one wafer level variability regarding TID drift through post-electrical test on ATE after HDR and LDR exposure.

NOTE: HDR biased and LDR unbiased is generally worst case for MOS devices.

- HDR (100 rad / s) biased: Post 3 krad (Si), 10 krad (Si), 30 krad (Si), 50 krad (Si), 100 krad (Si) [(1)], 150 krad (Si) [(2)]
- LDR (0.01 rad / s) unbiased: Post 3 krad (Si), 10 krad (Si), 30 krad (Si), 50 krad (Si), 100 krad (Si)
- LDR (0.01 rad / s) biased: 50 krad (Si), 100 krad (Si)

4.2 Group E Full RHA Radiation Lot Acceptance (RLAT) Report

The Group E RHA RLAT summary is shipped with each TI RHA QMLV product. To see the list of all documents shipped with TI QMLV products, review our *TI QML Class V/Q Lot Documents* (SBOA140). This document also has instructions on how to pull the full RHA (Group E) report.

NOTE: TI may provide technical, applications or design advice, quality characterization, and reliability data or service providing these items shall not expand or otherwise affect TI's warranties as set forth in the Texas Instruments Incorporated Standard Terms and Conditions of Sale for Semiconductor Products and no obligation Semiconductor Products and no obligation or liability shall arise from TI's provision of such items.

(1) 100 krad (Si) units pass, per MIL-STD-883 1019.9, Condition A, section 3.11 extended room temperature anneal test.
(2) 150 krad (Si) units pass, per MIL-STD-883 1019.9, Condition A, section 3.12 accelerated annealing test.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265