

Total Ionizing Dose (TID) Report

Impact of Reference Voltage on the ELDRS
Characteristics of the LM4050 Shunt Voltage
Reference



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Impact of Reference Voltage on the ELDRS Characteristics of the LM4050 Shunt Voltage Reference

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Abstract-- Two different reference voltage options (2.5V and 5.0V) of National Semiconductor's LM4050WGxxRLQV shunt voltage reference were put through Total Ionizing Dose (TID) testing at High Dose Rate (HDR) and Low Dose Rate (LDR) with different biasing conditions during irradiation and showed different sensitivities to the different dose rates and bias conditions. Another product, DS16F95WxFQMLV, that uses the same wafer fabrication process had a different TID response.

I. INTRODUCTION

THE LM4050WGxxRLQV (SMD 5962R09235xxVZA) is a precision shunt voltage reference with different reference voltage options (Fig. 1) [1][2], where the "xx" is a wildcard for the different voltage options. The reference voltage (V_R in Fig. 1) is set internally in the chip by the resistor ratios of the resistors shown in the block diagram in Fig. 2. High Dose Rate (HDR) and Low Dose Rate (LDR) Total Ionizing Dose (TID) testing and an Enhanced Low Dose Rate Sensitivity (ELDRS) characterization of the 2.5V reference option were presented at the NSREC 2010 Data Workshop [3]. The 5.0V reference option recently went through a similar ELDRS characterization and unexpectedly showed different sensitivities to dose rate and bias conditions. The differences in radiation response between the two voltage options will be presented here.

The LM4050 is fabricated on National Semiconductor's LFAST wafer process, which is a standard, junction isolated bipolar structure on a lightly doped substrate. This is the same process as used for the DS16F95WxFQMLV (SMD 5962F8961501VxA) [4][5] RS-485 transceiver, which also had ELDRS data presented at the NSREC 2010 Data Workshop [6]. Although the products share the same process, the radiation response was different. The differences in the products and the impact on radiation performance will also be discussed.

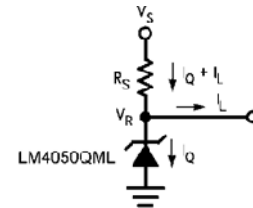


Fig. 1 LM4050 application diagram. The reference voltage (V_R) is factory set by adjusting the ratios of the internal resistors (see Fig. 2).

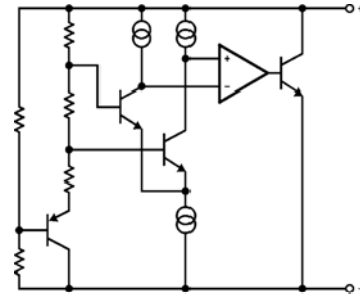


Fig. 2 LM4050 block diagram. The resistor ratios are adjusted to set the reference voltage.

II. PRODUCT TESTED

The complete National Semiconductor product name, the DLA Land and Maritime (formerly known as DSCC) Standard Microcircuit Drawing Product Identification Number (SMD PIN), reference voltage for the LM4050 and the wafer lot number of the products discussed here are listed in TABLE I.

TABLE I
PRODUCTS AND LOT NUMBERS

National Part Number	DLA SMD PIN Number	V_R	Wafer Lot Number
LM4050WG5.0RLQV	5962R0923562VZA	5.0V	JM09CX06D
LM4050WG2.5RLQV	5962R0923561VZA	2.5V	JM09CX06A
DS16F95WFQMLV	5962F8961501VHA		JP09342

The LM4050-2.5 and LM4050-5 wafers came from the same parent wafer lot and were processed together up until metal mask where the resistor ratios are defined. The test results for the LM4050-5 are covered in detail here. These results are compared to previously reported test results for the LM4050-2.5 which are covered in detail in [3]. For the

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DS16F95, the units tested at HDR came from the same wafer lot as those tested at LDR, but it is not known if they were from the same wafer. The LDR testing of the DS16F95 is covered in detail in [6].

III. TEST METHOD

The ELDRS characterization of the LM4050 was performed per MIL-STD-883, Test Method 1019 section 3.13.1.1 [7]. A four way split was run with units biased and unbiased during irradiation at low dose rate (LDR) and high dose rate (HDR). All units tested came from the same wafer for each reference voltage. The HDR testing was performed on separate dates for the two different voltage options at National Semiconductor’s radiation facility in Santa Clara, California. Dose rate was 152 rad(Si)/s. Both the 2.5V and 5.0V options went through LDR testing at the same time. Irradiation was done at 10 mrad(Si)/s at Radiation Assured Devices (now Aeroflex RAD) in Colorado Springs, Colorado [8]. The unbiased units had all pins grounded during irradiation. For the biased units, the negative pin was connected to ground and the positive pin (V_R) was connected to a power supply through an 866 Ω resistor (R_S in Fig. 1). The supply voltage was set so that the operating current (I_Q in Fig. 1) was 15 mA, (15 V for the 2.5V option and 17 V for the 5.0V option).

Electrical testing was done on an Eagle ETS500 test system at National Semiconductor’s Santa Clara radiation facility. All datasheet parameters were tested. For the HDR legs testing was done at 0, 3, 10, 30, 50 and 100 krad(Si) levels. The LDR splits were pulled at close to the same levels. The LDR splits had an additional data point taken at 150 krad(Si). For the HDR splits, electrical testing was completed within an hour of being removed from the gamma radiation. The LDR legs were shipped overnight from the test facility at RAD to National for testing, and shipped back overnight to RAD to resume irradiation in accordance with MIL-STD-883, TM1019.

The LDR test method for the DS16F95 is covered in [6]. The HDR testing was performed at National Semiconductor’s South Portland, Maine radiation test facility. Testing was done only with the units biased during irradiation, with the supply voltage at 5.75 V, the control pins held high at 5 V and the bus pins terminated with a 1 k Ω resistor. Electrical testing was performed on an MCT tester, which groups test types. Each parameter is tested under different operating conditions, but the different operating conditions are grouped for calculating statistics. This resulted in a delta between the LDR and HDR testing at 0 rad. The HDR readings were normalized to LDR 0 rad readings in the following figures.

IV. LM4050-5 TEST RESULTS

The parametric drift between 0 rad and 100 krad(Si) was analyzed for each of the test splits. The LM4050 is a simple shunt reference and there are only 2 parametric tests: minimum operating current and reference voltage at various current loads (Table II). The minimum operation current,

which has a specification limit of 60 μ A did not show any significant drift through irradiation. For TID qualification, the reference voltage is expressed in terms of percentage drift from the 0 rad reading. Measureable drift was detected on this parameter through irradiation (Table II). As the operating current (I_Q in Fig. 1) increased there was a slight amount of increase in the parametric drift, with the 15 mA I_Q being the worst case. The worst case irradiation condition resulting in the most parametric drift was at LDR with the units biased during irradiation. The condition with the least amount of drift was HDR biased. For 15 mA I_Q , V_R is plotted in Fig. 3 and % drift is plotted in Fig. 4.

TABLE II
ELDRS CHARACTERIZATION TABLE THROUGH 100 KRAD FOR LM4050-5

Parameter	Units	Median Drift				LDR/HDR	
		LDR		HDR		Drift Ratio	
		Bias	Unbias	Bias	Unbias	Bias	Unbias
Min Op Current	μ A	-0.674	-0.577	-0.744	-0.797	0.9	0.7
V_R $I_Q=60 \mu$ A	% drift	0.548	0.581	0.217	0.214	2.5	2.7
V_R $I_Q=100 \mu$ A	% drift	0.549	0.582	0.217	0.213	2.5	2.7
V_R $I_Q=1$ mA	% drift	0.550	0.582	0.218	0.217	2.5	2.7
V_R $I_Q=10$ mA	% drift	0.555	0.587	0.223	0.226	2.5	2.6
V_R $I_Q=15$ mA	% drift	0.557	0.590	0.225	0.229	2.5	2.6

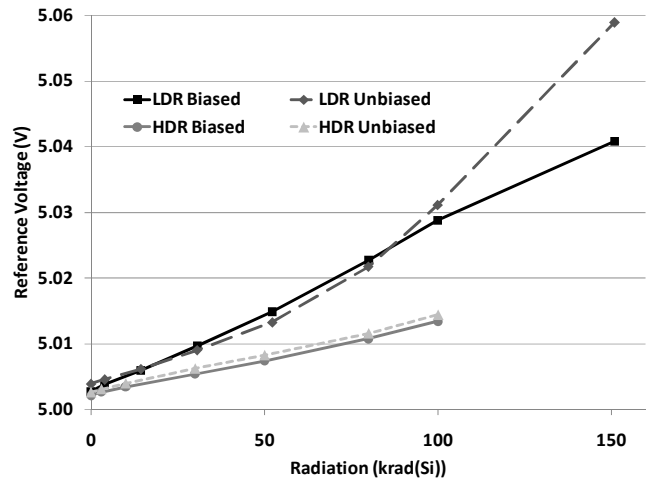


Fig. 3 LM4050-5 reference voltage (V_R) with a 15 mA operating current (I_Q) vs. radiation exposure level.

Per the ELDRS characterization method in MIL-STD-883, TM1019, section 3.13.1.1, the median parametric drift for each test condition was compared (Table II). If any parameters show significant drift and the ratio of the median LDR drift to the median HDR drift is greater than 1.5, the “part is considered to be ELDRS susceptible”. With the units biased during irradiation, the reference voltage LDR/HDR drift ratio was 2.6, indicating that the LM4050WG5.0RLQV has ELDRS under the definition in MIL-STD-883.

To qualify a part defined as having ELDRS for low dose rate environments, MIL-STD-883 TM1019 requires that the part is tested at a dose rate of 10 mrad(Si)/s and an overtest factor of 1.5X is used. For the LM4050WG5.0RLQV to be

qualified to 100 krad(Si), it must pass qualification testing to 150 krad(Si) at a dose rate of 10 mrad(Si)/s with all parameters inside the post irradiation test limits. The post irradiation drift limit for reference voltage is 1.5%. Fig. 5 shows a plot of the median parametric drift in percent for the reference voltage with a 15 mA load. The maximum, average, minimum and the standard deviations of the drift are shown in Table III.

TABLE III
LM4050-5 Vr DRIFT AT LDR WITH LOAD CURRENT AT 15 mA (% DRIFT)

TID Level krad(Si)	30.6	52.3	102	151.7
Biased				
Maximum	0.15	0.26	0.56	0.81
Average	0.14	0.24	0.52	0.76
Minimum	0.10	0.19	0.40	0.61
Standard Deviation	0.04	0.06	0.10	0.13
Unbiased				
Maximum	0.11	0.20	0.65	1.31
Average	0.10	0.19	0.54	1.10
Minimum	0.08	0.15	0.40	0.82
Standard Deviation	0.03	0.05	0.13	0.24

V. 2.5V vs. 5.0V DRIFT

Tables IV and V list the reference voltage drift through 100 and 150 krad(Si) in terms of voltage and percentage drift from the pre irradiation value, a scaling factor for drift between the 5.0V and. 2.5V options and a scaling factor for drift between LDR and HDR for each voltage option. If the drift scaled perfectly with the reference voltage, the scaling factor would be 2. There was some scaling in the magnitude of the drift with reference voltage, but it varied by dose rate and condition. This is illustrated in Figs. 4 and 5 with the drift expressed in terms of percent change from the pre irradiation reading. For three of the splits, the scaling factor of the drift between the 2.5V and 5.0V part was 1.3 to 1.6. For the LDR unbiased split, the scaling factor was 2.

TABLE IV
LM4050-2.5 AND LM4050-5 Vr DRIFT THROUGH 100 KRAD (Si)

Dose Rate	Condition	Drift through 100 krad(Si)				Scaling Factors		
		2.5V mV	5.0V mV	2.5V %	5.0V %	5.0V/2.5V	LDR/HDR	5.0V
LDR	Biased	18	28	0.68	0.56	1.56	2.57	2.55
LDR	Unbiased	15	30	0.60	0.59	2.00	1.88	2.73
HDR	Biased	7	11	0.29	0.23	1.57		
HDR	Unbiased	8	11	0.33	0.23	1.38		

TABLE V
LM4050-2.5 AND LM4050-5 Vr DRIFT THROUGH 100 KRAD (Si)

Dose Rate	Condition	Drift through 150 krad(Si)				Scaling Factor 5.0V/2.5V
		2.5V mV	5.0V mV	2.5V %	5.0V %	
LDR	Biased	27	40	1.09	0.81	1.48
LDR	Unbiased	26	59	1.02	1.18	2.27

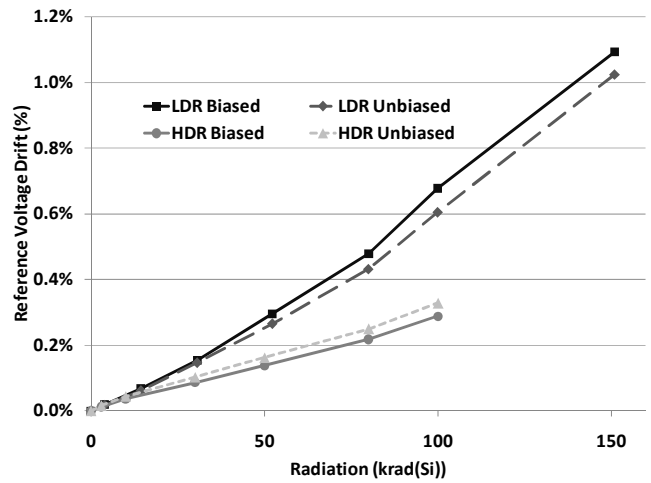


Fig. 4 LM4050-2.5 Vr drift in percent at 15 mA IQ.

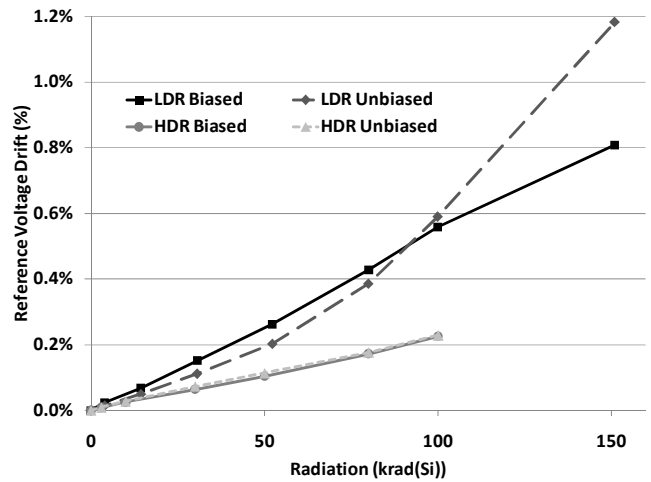


Fig. 5 LM4050-5 Vr drift in percent at 15 mA IQ.

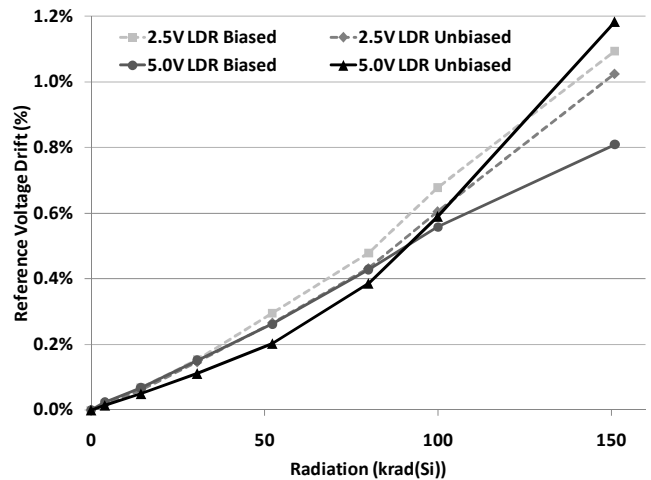


Fig. 6 LM4050-2.5 and LM4050-5 Vr drift in percent at 15 mA IQ at LDR.

For the 2.5V part, the worst case condition causing the most parametric drift was at LDR with the units biased during irradiation (Fig. 4) while for the 5.0V part the worst case condition was with the units unbiased during irradiation (Fig. 5). In all cases but one, the output drift is approximately

linear with radiation exposure. For the 5.0V part under the LDR unbiased condition, the drift begins to diverge from a linear function after 50 krad(Si).

VI. LM4050 VS. DS16F95 PARAMETRIC DRIFT

The DS16F95WFQMLV is an RS-485 transceiver, rated to 300 krad(Si) at high dose rate (Fig. 7) [5]. Although it uses the same process, LFAST, as the linear reference LM4050, it is a digital product, converting between single-ended and differential digital signals, along with some digital control logic functions. Per MIL-STD-883 TM1019, ELDRS testing may be omitted if “devices are known not to contain any linear circuit functions by design” [7].

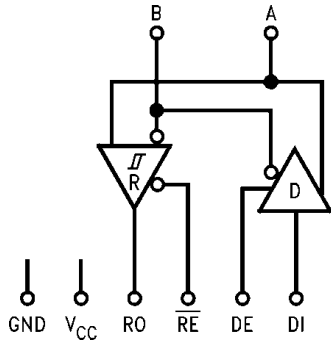


Fig. 7 Block diagram of the DS16F95. Although it is a digital product, it shares the same wafer fab process with the LM4050.

At HDR, the only parameters on the DS16F95 with detectable parametric shifts through 300 krad(Si) were supply current, the input currents to the control logic and output short circuit current. The parametric drift for all parameters was less than 10% through 300 krad(Si) except for the input currents to the control logic pins, which were 30%. Since these currents were small to begin with compared to the spec limit (minimum reading was greater than $-10\mu\text{A}$ with a minimum limit of $-50\mu\text{A}$) the actual drift through irradiation (not more than $2\mu\text{A}$) was insignificant.

The control logic currents and supply currents on the DS16F95WFQMLV were tested at an LDR of 10 mrad(Si)/s to 30 krad(Si) in [6]. Supply current actually decreased at both LDR and HDR and the change through 30 krad(Si) was less than 1% (Fig 8). The control logic pins showed a parametric drift of up to 10% for the HDR biased and LDR unbiased conditions and up to 40% for the LDR biased condition through 30 krad(Si) (Fig. 9). The absolute value of the drift ($2\mu\text{A}$ worst case) is insignificant when compared to the specification range ($50\mu\text{A}$) at 4% of the specification range.

The data presented here indicates that the 300 krad(Si) rating of the DS16F95 cannot be applied to the LM4050, even though the two products share the same process. This has to do with the function of the products and which elements are crucial for the correct operation of the products. For the DS16F95, the critical elements are the switching

levels and speeds of the transistors, which do not show significant sensitivity to ionizing radiation. For the LM4050, the V_{BE} of the pnp transistor is the most crucial element in setting the reference voltage and the V_{BE} of a planar pnp transistor is typically sensitive to ionizing radiation and can show ELDRS. Increased leakage in the npn transistors and parasitic surface devices can also impact the reference voltage, but may not be significant enough to change the switching characteristics of the DS16F95.

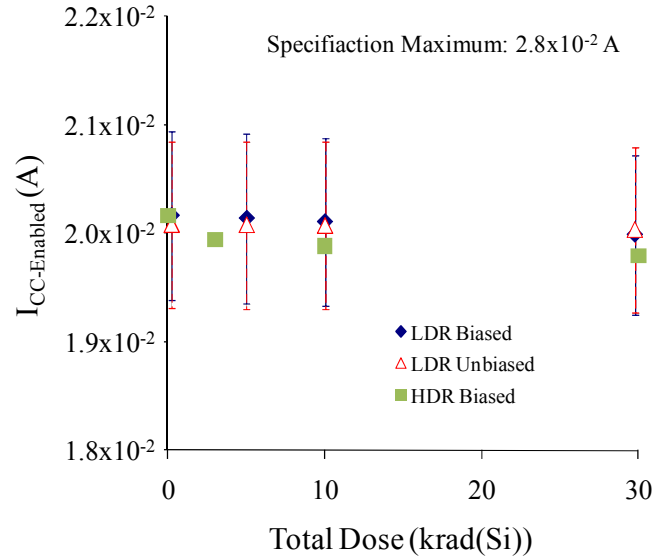


Fig. 8 DS16F95 supply current with the driver and receiver enabled. Maximum limit is 28 mA and supply current decreases with radiation exposure. Plot from [4] with HDR data normalized to 0 rad LDR readings added.

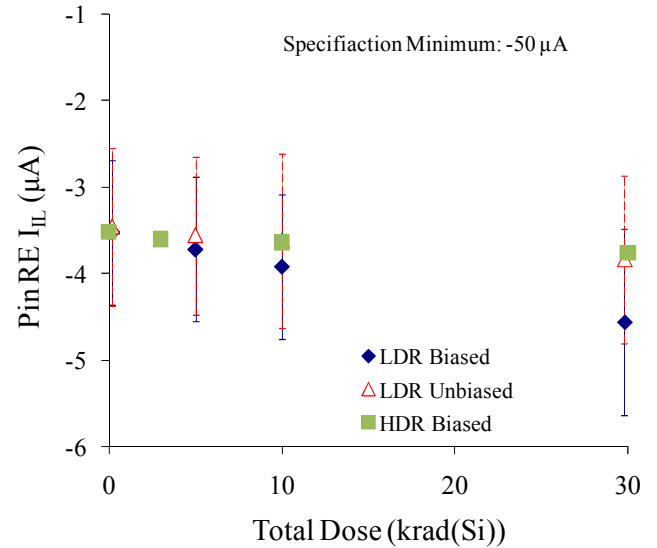


Fig. 9 DS16F95 RE-bar current. The minimum limit for this parameter is 50 μA . Plot from [4] with HDR data normalized to 0 rad LDR readings added.

VII. CONCLUSIONS

The LM4050WG5.0RLQV is considered to have ELDRS under the definition in MIL-STD-883 TM1019. To qualify

the product at 100 krad(Si) for low dose rate environments, the part is tested at a dose rate of 10 Mrad(Si)/s to a TID of 150 krad(Si), with all parameters inside the specification limits at 150 krad(Si).

The radiation performance characteristics of one product cannot always be applied to another product using the same process. Even the different voltage options of the same product may behave differently. For the LM4050, a simple resistor ratio change changed the product's sensitivity to radiation under different biasing conditions. As the LDR data on the LM4050-5 show, the parametric drift cannot always be extrapolated out to higher doses.

VIII. REFERENCES

- [1] National Semiconductor, Santa Clara, CA, "LM4050QML Precision Micropower Shunt Voltage Reference", Oct. 4, 2010. [Online]. Available: <http://www.national.com/ds/LM/LM4050QML.pdf>
- [2] DLA Land and Maritime, Columbus OH, Standard Microcircuit Drawing, 5962-09235, "MICROCIRCUIT, LINEAR, 2.5 V PRECISION MICROPOWER SHUNT VOLTAGE REFERENCE, MONOLITHIC SILICON", Oct. 18, 2010 [Online]. Available: <http://www.dsccl.dla.mil/Downloads/MilSpec/Smd/09235.pdf>
- [3] K. Kruckmeyer, E. Morozumi, R. Eddy, T. Trinh, T. Santiago, P. Maillard, "Single event transient and ELDRS test results for LM4050QML 2.5V precision reference," in Proc. IEEE Rad. Effects Data Workshop Rec., Jul. 2010, pp. 164-169.
- [4] A. T. Kelly, R. D. Brown, F. Wong, and P. R. Fleming, "Single event and low dose-rate effects in the DS16F95 RS-485 transceiver", in Proc. IEEE Rad. Effects Data Workshop Rec., Jul. 2010, pp. 94-99.
- [5] National Semiconductor, Santa Clara, CA, "DS16F95QML EIA-485/EIA-422A Differential Bus Transceiver", Oct. 27, 2010. [Online]. Available: <http://www.national.com/ds/DS/DS16F95QML.pdf>
- [6] DLA Land and Maritime, Columbus OH, Standard Microcircuit Drawing, 5962-09235, "MICROCIRCUIT, LINEAR, RS-485 DIFFERENTIAL BUS TRANSCEIVER, MONOLITHIC SILICON", Mar. 22, 2010 [Online]. Available: <http://www.dsccl.dla.mil/Downloads/MilSpec/Smd/89615.pdf>
- [7] *Test Method Standard, Microcircuits*, MIL-STD-883, Dept. Defense, Defense Supply Center, Columbus, OH, Jun. 18, 2004 [Online]. Available: <http://www.dsccl.dla.mil/Downloads/MilSpec/Docs/MIL-STD-883/std883.pdf>
- [8] Aeroflex, Denver, CO, "Aeroflex RAD," 2011. [Online]. Available: <http://www.aeroflex.com/ams/pagesproduct/prods-radinc-services.cfm>

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