

TMS570LC4357-EP Production Flow and Reliability Report

ABSTRACT

The TMS570LC4357-EP device is part of the Hercules TMS570 series of high-performance automotive-grade ARM® Cortex®-R-based MCUs. The TMS570LC4357-EP device has onchip diagnostic features including: dual CPUs in lockstep, Built-In Self-Test (BIST) logic for CPU, the N2HET coprocessors, and for on-chip SRAMs; ECC protection on the L1 caches, L2 flash, and SRAM memories. The device also supports ECC or parity protection on peripheral memories and loopback capability on peripheral I/Os.

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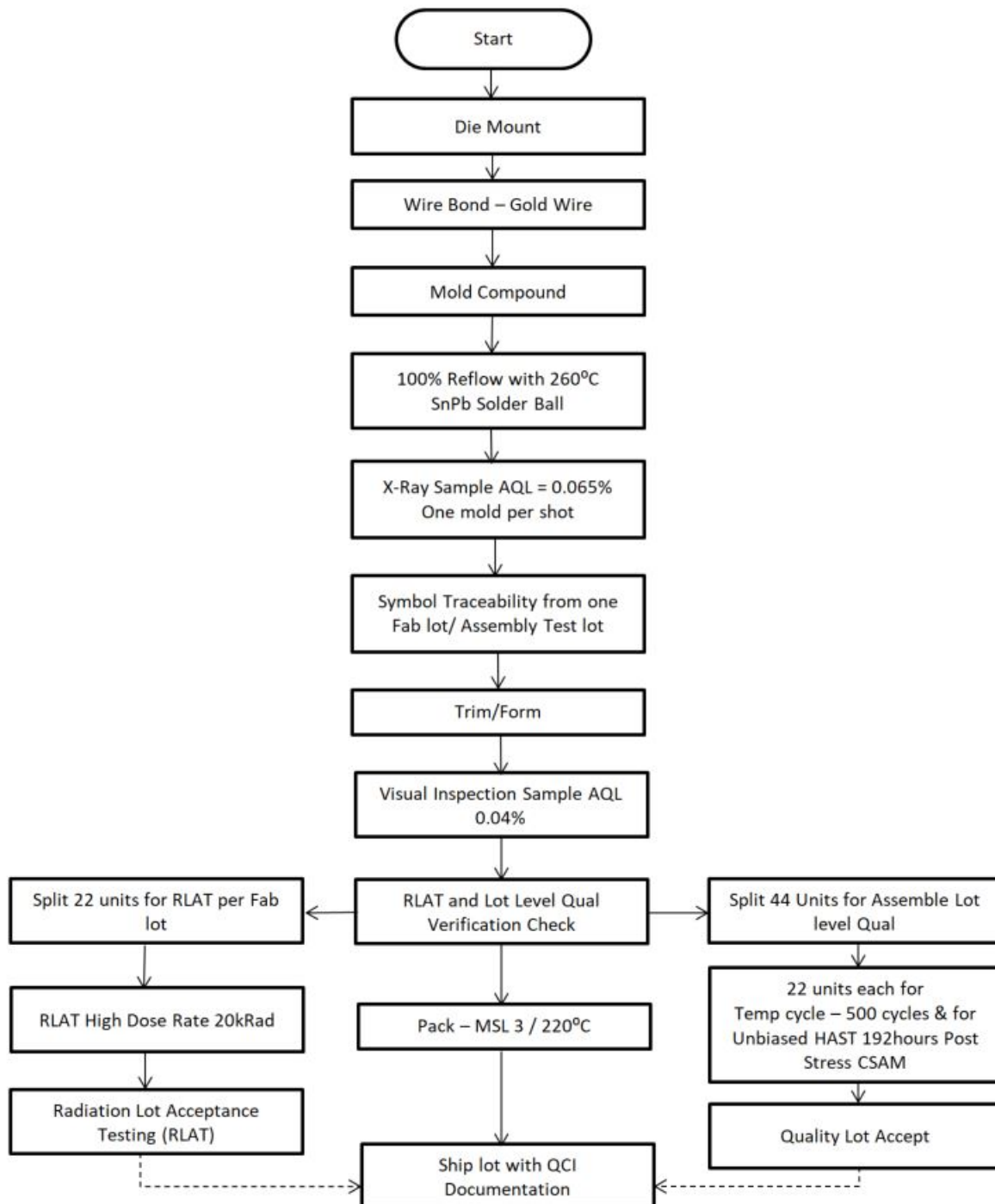
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1 Device Introduction

TMS570LC4357-EP is a Radiation Hardened device in plastic package which allow this device to be use in a space application. The device was verified immune to 43 MeV·cm²/mg at 125°C for single event latchup. Each Fab lot was tested according to MIL-STD-883 for Radiation Lot Acceptance Tested (RLAT) up to 20 krad(Si) and each Assembly and Test lot will follow the process flow shown in [Section 2](#). To ensure the quality of TMS570LC4357-EP, it is qualified with EP requirements. See [Section 3](#) for further details.

2 TMS570LC4357-EP Production Flow


3 Device Qualification

The following is the device qualification summary:

Qualification by Similarity (Qualification Family)

A new device can be qualified either by performing full scale quality and reliability tests on the actual device or using previously qualified device(s) through "Qualification by Similarity" (QBS) rules. By establishing similarity between the new device and those qualified previously, repetitive tests will be eliminated, allowing for timely production release. When adopting QBS methodology, the emphasis is on qualifying the differences between a previously qualified product and the new product under consideration. The QBS rules for a technology, product, test parameters or package shall define which attributes are required to remain fixed in order for the QBS rules to apply. The attributes which are expected and allowed to vary will be reviewed and a QBS plan shall be developed, based on the reliability impact assessment above, specifying what subset of the full complement of environmental stresses is required to evaluate the reliability impact of those variations. Each new device shall be reviewed for conformance to the QBS rule sets applicable to that device. See JEDEC JESD47 for more information.

Device Baseline ⁽¹⁾			
<i>TI Device:</i>	TMS5704357BGWTEP	<i>Assembly Site:</i>	TIPI - (Philippines)
<i>DLA VID:</i>		<i>Test Site:</i>	TIPI - (Philippines)
<i>Wafer Fab:</i>	TSMC-14	<i>Pin/Package Type:</i>	nFBGA (GWT) ! 337
<i>Fab Process:</i>	F021	<i>Leadframe:</i>	Cu
<i>Fab Technology:</i>	F021	<i>Termination Finish:</i>	NiPdAu
<i>Die Revision:</i>	B	<i>Bond Wire:</i>	20.3 μm Au
<i>Die Name:</i>	YF771693BM	<i>Moisture Sensitivity:</i>	MSL 3 / 220°C
<i>ESD CDM:</i>	±500 V		
<i>ESD HBM:</i>	±2000 V		

⁽¹⁾ Baseline information in effect as of the date of this report.

Enhanced Product New Device Qualification Matrix				
Note that qualification by similarity ("qualification family") per JEDEC JESD47 is allowed				
Description	Condition	Sample Size Used/ Rejects	Lots Required	Test Method
<i>Electromigration</i>	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules
<i>Wire Bond Life</i>	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules
<i>Electrical Characterization</i>	TI Data Sheet	10	3	N/A
<i>Electrostatic Discharge Sensitivity</i>	HBM	3 units/voltage	1	EIA/JESD22-A114
	CDM			EIA/JESD22-C101
<i>Latch-up</i>	Per Technology	6/0	1	EIA/JESD78
<i>Physical Dimensions</i>	TI Data Sheet	5/0	1	EIA/JESD22- B100
<i>Thermal Impedance</i>	Theta-JA on board	Per Pin-Package	N/A	EIA/JESD51
<i>Bias Life Test</i>	125°C / 1000 hours or equivalent	77/0	3	JESD22-A108 ⁽¹⁾
<i>Biased HAST</i>	130°C / 85% / 96 hours	77/0	1	JESD22-A110 ⁽¹⁾
<i>Extended Bias HAST</i>	130°C / 85% / 250 hours (for reference)	77/0	3	JESD22-A110 ⁽¹⁾
<i>Unbiased HAST</i>	130°C / 85% / 96 hours	77/0	3	JESD22-A.118 ⁽¹⁾
<i>Temperature Cycle</i>	-65°C to +150°C nonbiased for 500 cycles	77/0	3	JESD22-A104 ⁽¹⁾
<i>Solder Heat</i>	260°C for 10 seconds	22/0	1	JESD22-B106
<i>Resistance to Solvents</i>	Ink symbol only	12/0	1	JESD22-B107
<i>Solderability</i>	Condition A (steam age for 8 hours)	22/0	1	ANSI/J-STD-002-92
<i>Flammability</i>	Method A / Method B	5/0	3	UL-1964
<i>Bond Shear</i>	Per wire size	5 units x 30/0 bonds	3	JESD22-B116
<i>Bond Pull Strength</i>	Per wire size	5 units x 30/0 bonds	3	ASTM F-459
<i>Die Shear</i>	Per die size	5/0	3	TM 2019
<i>High Temp Storage</i>	150°C / 1,000 hours	15/0	3	JESD22-A103-A ⁽¹⁾
<i>Moisture Sensitivity</i>	Surface Mount Only	12	1	J-STD-020-A ⁽¹⁾
<i>Radiation Response Characterization</i>	Total Ionization Dose, and Single-Event Latchup	5 units/dose level	1	MIL-STD-883/Method 1019
<i>Outgassing Characterization</i>	TML (Total Mass Lost), CVCM (Collected Volatile Condensable material), WVR (Water vapor recorded)	5	1	ASTM E595

⁽¹⁾ Precondition performed per JEDEC Std. 22, Method A112/A113.

4 Outgas Report

Outgassing test was performed on 5 units. A total mass loss (TML) of 1.00% and collected volatile condensable material (CVCM) of 0.10% were used as screening levels for rejection of spacecraft materials. The outgas test was performed in a vacuum environment of less than 5×10^{-5} torr according to ASTM E 595, for a duration of 24 hours at 125°C. The TML, CVCM, and the amount of Water Vapor Recovered (WVR) were measured after the test.

Table 1: Outgas test results.

Sample	TML (%)	CVCM (%)	WVR (%)
TMS5704357BGWTPSEP	0.09	0.04	0.05

Quality and Reliability Data Disclaimer

The attached quality and reliability information is specific to the TI Enhanced Plastic product family of plastic encapsulated commercial-off-the-shelf (COTS) semiconductor products and components. Due to possible differences in product assembly and test baselines, this information is NOT APPLICABLE to TI standard, industrial, or automotive catalog commercial products.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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