

# Product Clip

Standard Linear and Logic

## NanoStar™ and NanoFree™ The smallest industry-standard logic package

The smallest industry-standard logic package with world-class proven reliability designed for today's high-volume manufacturing environments.

### Board-Level Reliability

TI: 1,286 cycles: -40 to 125°C.  
Zero failures.

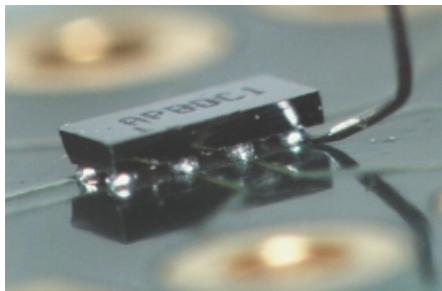
TI: 1,900 cycles: 0 to 100°C.  
Zero failures. (Modeled at 30-unit sample size.)

For optimal reliability, please review the land-pad design illustrated in the *WCSP Design Summary* available at:

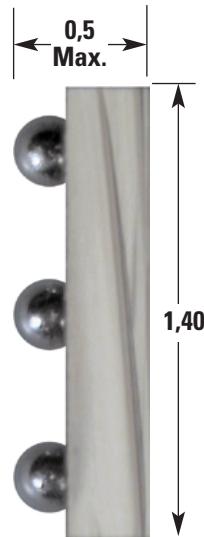
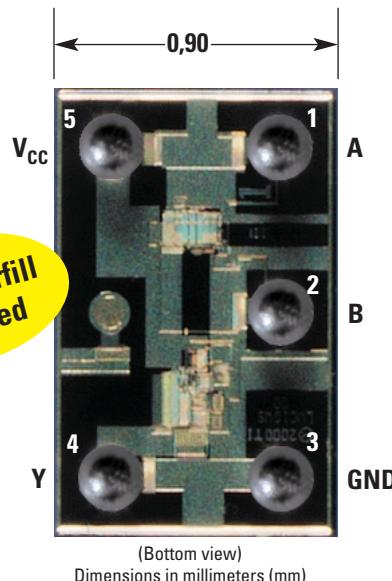
[www.ti.com/nanostar](http://www.ti.com/nanostar)

### Solder Bumps Provide Easy Testability

Due to the ideal placement of the solder bumps along the outside of the package along with sufficient bump height, probe tips can easily create a dedicated contact to the individual pins.



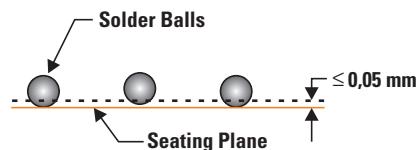
No Underfill  
Required



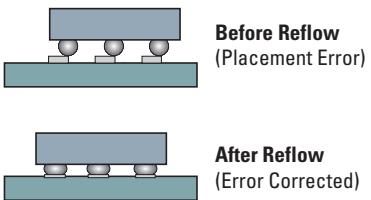
Alternate Source:  
Renesas Technology

### Placeability

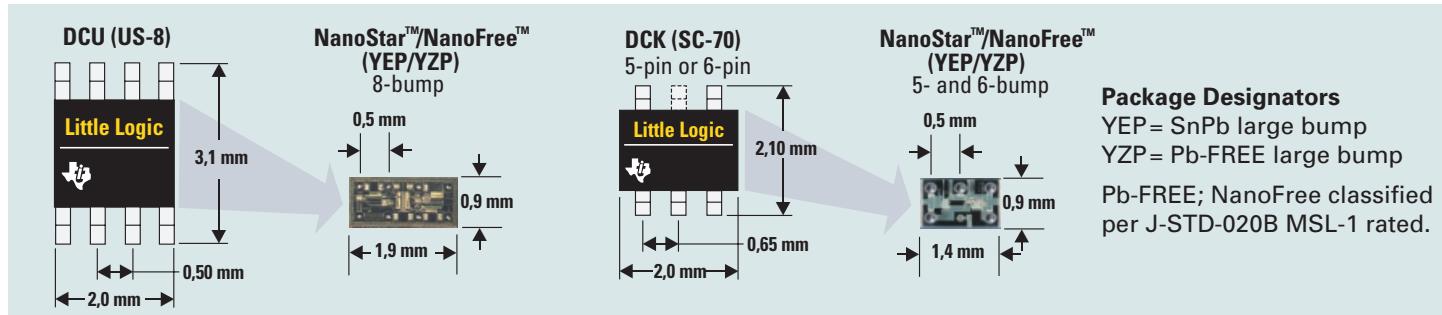
**Coplanarity:** This package meets a coplanarity of 0,05 mm as shown. Coplanarity is defined as a unilateral tolerance zone measured upward from the seating plane.



**Self-Correction:** Self-correction during reflow reduces the need for accurate placement. About 50% of ball-to-paste overlap is sufficient for the self-correction process.



### Package Comparisons



**Package Designators**  
YEP = SnPb large bump  
YZP = Pb-FREE large bump  
Pb-FREE; NanoFree classified per J-STD-020B MSL-1 rated.

## NanoStar/NanoFree Typical Characteristics

Family	Operating Voltage Range (V)	Optimized Voltage (V)	Propagation Delay (typ) (ns)	Output Drive (mA)	Input Tolerance (V)	$I_{OFF}$ Protection
AUC	0.8 to 2.7	1.8	2.0	8	3.6	Yes
LVC	1.65 to 5.5	3.3	3.5	24	5.5	Yes

## Products Available by Function

Description	3.3-V LVC			1.8-V AUC	
	Single-Gate	Dual-Gate	Triple-Gate	Single-Gate	Dual-Gate
<b>Gates</b>					
2-input NAND gate	LVC1G00	LVC2G00		AUC1G00	AUC2G00
2-input NOR gate	LVC1G02	LVC2G02		AUC1G02	AUC2G02
2-input AND gate	LVC1G08	LVC2G08		AUC1G08	AUC2G08
2-input OR gate	LVC1G32	LVC2G32		AUC1G32	AUC2G32
2-input exclusive OR gate	LVC1G86	LVC2G86		AUC1G86	
3-input exclusive OR gate	LVC1G386				
<b>Configurable Logic</b>					
Configurable multi-function gate	LVC1G57				
Configurable multi-function gate	LVC1G58				
Configurable multi-function gate	LVC1G97				
Configurable multi-function gate	LVC1G98				
<b>Buffers</b>					
Buffer driver w/open drain output	LVC1G07	LVC2G07	LVC3G07	AUC1G07	AUC2G07
Schmitt-trigger buffer	LVC1G17	LVC2G17		AUC1G17	
Bus buffer gate	LVC1G125	LVC2G125		AUC1G125	
Bus buffer gate	LVC1G126	LVC2G126			
Buffer driver w/3-state outputs	LVC1G240	LVC2G240		AUC1G240	
Buffer gate		LVC2G34	LVC3G34		
<b>Inverters</b>					
Inverter gate	LVC1G04	LVC2G04	LVC3G04	AUC1G04	AUC2G04
Inverter unbuffered gate	LVC1GU04	LVC2GU04		AUC1GU04	
Inverter buffer/driver	LVC1G06	LVC2G06	LVC3G06	AUC1G06	AUC2G06
Schmitt-trigger inverter	LVC1G14	LVC2G14	LVC3G14	AUC1G14	
<b>Analog Switches</b>					
Analog switch	LVC1G66	LVC2G66		AUC1G66	
Analog MUX/deMUX		LVC2G53			
Single-pole, double-throw analog switch	LVC1G3157				
<b>Flip-Flops</b>					
Positive-edge-triggered D-type flip-flop	LVC1G79			AUC1G79	
Positive-edge-triggered D-type flip-flop	LVC1G80			AUC1G80	
Positive-edge-triggered D-type flip-flop w/clear and preset		LVC2G74			
<b>Multiplexers</b>					
Single 2-line to 1-line data selector/multiplexer		LVC2G157			
1-of-2 noninverting demultiplexer with 3-state deselected output	LVC1G18				
1-of-2 decoder/demultiplexer	LVC1G19				

## For More Information About NanoStar and NanoFree

Visit the NanoStar home page for application reports, product samples and the *NanoStar Design Summary*:

[www.ti.com/nanostar](http://www.ti.com/nanostar)  
[www.ti.com/littlelogic](http://www.ti.com/littlelogic)

Reliable. Logic. Innovation.; the red/black banner; NanoStar and NanoFree are trademarks of Texas Instruments.

© 2003 Texas Instruments Incorporated

Printed in the U.S.A. by Texoma Business Forms, Colbert, OK

 Printed on recycled paper.

### Safe Harbor Statement

This publication contains forward-looking statements that involve a number of risks and uncertainties. These "forward-looking statements" are intended to qualify for the safe harbor from liability established by the Private Securities Litigation Reform Act of 1995. These forward-looking statements generally can be identified by phrases such as TI or its management "believes," "expects," "anticipates," "foresees," "forecasts," "estimates" or other words or phrases of similar import. Similarly, such statements herein that describe the company's products, business strategy, outlook, objectives, plans, intentions or goals also are forward-looking statements. All such forward-looking statements are subject to certain risks and uncertainties that could cause actual results to differ materially from those in forward-looking statements. Please refer to TI's most recent Form 10-K for more information on the risks and uncertainties that could materially affect future results of operations. We disclaim any intention or obligation to update any forward-looking statements as a result of developments occurring after the date of this publication.