Maximizing signal integrity with M-LVDS backplanes

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As the demand for higher clock and data transfer rates across backplane systems continues to grow, fundamental elements of high-speed printed circuit board design become essential. This article identifies issues associated with high-speed multipoint backplane design and provides recommendations that include the use of multipoint low-voltage differential signaling (M-LVDS) (TIA/EIA-899) technology. M-LVDS provides multipoint communication with up to 32 M-LVDS circuits connected to the same media. Test results demonstrating the use of M-LVDS across a custom-designed backplane will be presented along with development guidelines for aiding the design of a high-performance system.

Backplane signaling technologies

The good news is that there are many choices available for transferring information within a backplane environment, but this can also make it difficult to decide which technology should be used in a particular application. The key to selecting the right signaling technology for a backplane is having a good understanding of the system requirements such as signaling rate, power, topology, EMI, transmission distance, and loading conditions.

Some of the single-ended signaling technologies available include transistor-transistor logic (TTL), low-voltage TTL (LVTTL), backplane transceiver logic (BTL), gunning transceiver logic (GTL), and GTL plus (GTLP) (see Table 1). Single-ended transmission occurs when information is sent over a single line referenced to ground, helping to keep the costs lower for cabling or connectors. However, single-ended signal transmission is also more susceptible to noise, crosstalk, and ground offsets, all of which can result in receiving false data.

TTL and LVTTL standard logic devices abound, providing not only many choices for signal transmission across the backplane but also the cost advantage of single-ended transmission. However, TTL standard logic devices have large voltage swings that typically translate into EMI. Maintaining these large voltage swings becomes a problem in heavily loaded systems, and TTL is susceptible to signal integrity issues associated with single-ended data transmission (noise, crosstalk, and ground offsets).

BTL also uses single-ended transmission but lowers the voltage swing to 1.1 V, which can lead to higher transmission rates and reduced EMI radiation relative to TTL. This reduced voltage swing is achieved by an open-collector output with the bus terminated through a resistor to 2.1 V. When the driver is activated, the bus is pulled down to the saturation point of the driver plus the voltage drop across a series diode, resulting in a 1-V low. The value of the termination resistor should match the characteristic impedance of the signal path.

GTL uses an open drain but, unlike BTL, does not use a series diode. This results in an active-low condition of only 0.4 V. The bus termination voltage is reduced to 1.2 V, providing a total voltage swing of 0.8 V. This lower voltage swing can further reduce EMI and provide for higher transmission rates relative to BTL. However, the sink current is reduced to 40 mA, which is acceptable for onboard chip-to-chip applications but limits the capabilities for driving a heavily loaded backplane. GTL is primarily recommended for point-to-point technologies. GTLP is much better suited for multipoint (backplane) environments than GTL.

GTLP is similar to GTL, with slight variations in output voltage and termination levels (see Table 1) that were introduced to improve the noise margin relative to ground. More significantly, GTLP offers two drive options (50 mA or 100 mA) that can accommodate a more heavily loaded backplane. GTLP also features output edge control and internal precharge circuitry enabling live insertion, further improving performance within the backplane environment.

Table 1. Single-ended signaling technologies

PARAMETER	TTL (LVTTL)	BTL	GTL	GTLP
V_{IN}, high (V)	2.0	1.62	0.85	1.05
V_{IN}, low (V)	0.8	1.47	0.75	0.95
V_t, V_{REF} (V)	1.4	1.55	0.8	1.0
V_{OUT}, high (V)	2.4	2.1	1.2	1.5
V_{OUT}, low (V)	0.4	1	0.4	0.55
Standard driver load (Ω)	—	11	11	11
Drive sink current (mA)	—	100	40	50 or 100
Standard	JESD8-1	IEEE 1194.1	JESD8-3	—

When information is transmitted within a system, it is possible for the ground reference on the transmission end to be offset relative to the ground reference on the receiving end. For single-ended transmission, the signal is referenced to ground; so this ground offset could result in receiving the wrong information. Also, noise within the backplane environment can couple onto the signal path, which again can lead to receiving corrupt information.

Differential signaling provides several benefits over single-ended transmission. For instance, the issue of ground offset within the application is diminished since the signals are referenced to each other rather than to ground. Further, noise within a backplane environment can be alleviated if careful consideration is given to the board layout. If the signal path of the differential pair is routed closely together, noise coupled onto one signal will likely couple onto the other signal of the differential pair. Since these signal pairs are referenced to each other, the noise is effectively canceled out. It is important to note that the magnitude of the resulting offset voltage cannot exceed the input signal range of the receiver. If it does, the information will be corrupt, even with differential signaling.

Of course, with differential signaling, two signal paths per channel will increase the number of cables or connector pins in the system. This must be weighed against the benefits associated with differential signaling and the needs of the applications. Some of the differential signaling technologies available include RS-485, positive emitter-coupled logic (PECL), low-voltage PECL (LVPECL), low-voltage differential signaling (LVDS), BusLVDS, and multipoint LVDS (M-LVDS) (see Table 2).

RS-485 employs the advantages associated with differential signaling and is ideally suited for transmitting data over long distances (up to 1200 m) or noisy environments. Multiple drivers and receivers can share the same transmission pair (see Figure 1), which is accomplished by properly terminating each end of the signal path. RS-485 is widely accepted in industrial applications, providing an economic and robust solution.

PECL and LVPECL provide reduced voltage swings and faster transition times than RS-485, making them capable of much higher speeds. PECL transmission may require a separate supply terminating the load resistor to $V_{CC} - 2$ V.

LVDS, with reduced voltage swings and faster transition times, is also capable of much higher speeds than RS-485. LVDS has an added benefit of using less power than PECL and does not require a separate supply for terminating the load resistor at the end of the transmission line. However, LVDS is not intended to support multipoint configurations.

BusLVDS has characteristics similar to those of LVDS, except that it is intended to support multipoint configurations. Since the multipoint configuration requires termination at both ends of the transmission path, the equivalent resistance is half that of a point-to-point configuration.

Figure 1. Multipoint configuration

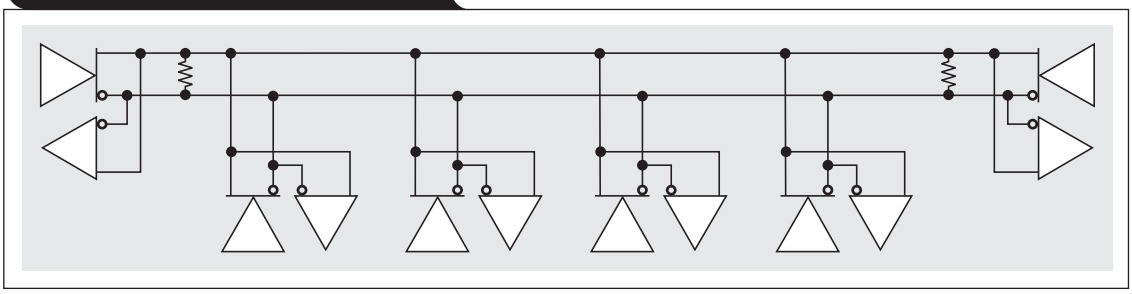


Table 2. Differential signaling technologies

PARAMETER	RS-485	PECL (LVPECL)	LVDS	BusLVDS	M-LVDS
V_{IN}, high	$V_{DIFF} > 200$ mV	$V_{DIFF} > 100$ mV	$V_{DIFF} > 100$ mV	$V_{DIFF} > 100$ mV	$V_{DIFF} > 50$ mV*
V_{IN}, low	$V_{DIFF} < -200$ mV	$V_{DIFF} < -100$ mV	$V_{DIFF} < -100$ mV	$V_{DIFF} < -100$ mV	$V_{DIFF} < -50$ mV*
V_{IN} range (V)	–7 to 12	Varies	0 to 2.4	0 to 2.4	–1.4 to 3.8
V_{OUT}, high**	1.5 V < V_{DIFF}	800 mV	350 mV	300 mV	550 mV
V_{OUT}, low**	–1.5 V > V_{DIFF}	–800 mV	–350 mV	–300 mV	–550 mV
Common-mode output	–1 V < V_{OS} < 3 V	3.6 V (1.95 V)	1.125 V < V_{OS} < 1.375 V	1.1 V < V_{OS} < 1.5 V	0.3 V < V_{OS} < 2.1 V
Standard driver load (Ω)	60	50†	100	27	50
Drive current (mA)	> 25	16	3.5	11	11
Standard	TIA/EIA-485-A	—	TIA/EIA-644-A	—	TIA/EIA-899

* Type 1 receiver threshold is –50 mV < V_{ID} < 50 mV. Type 2 receiver threshold is 50 mV < V_{ID} < 150 mV.
** These are nominal differential output voltage levels relative to the common-mode voltage and may vary with the vendor.
† Each line is terminated with 50 Ω or a Thevenin equivalent.

BusLVDS addresses this issue by increasing the drive current so that, even though the equivalent resistance is cut in half, the desired differential signal level is still maintained.

M-LVDS is a technology designed specifically for heavily loaded backplanes to transfer clock or data signals. The PCI Industrial Computer Manufacturers Group (PICMG®) 3.0 AdvancedTCA™ specification identifies M-LVDS for clock signaling sources across the backplane. M-LVDS provides the following features and benefits (refer to TIA/EIA-899):

- Lower voltage swings relative to RS-485, which can translate into reduced EMI
- Controlled transition times (>1 ns) that help to hide stubs and also reduce EMI
- Receivers that can typically withstand up to ±2 V of ground offset and have common-mode noise immunity
- Support for multipoint configuration
- No need for a separate supply voltage for termination

The standards and corresponding signaling technologies are designed to accommodate certain speeds, transmission lengths, and loading conditions. However, actual performance is highly dependent on how well the overall system is designed. Board layout, effective impedance, proper termination, and stub effects can all degrade signal integrity. Careful system-level design is necessary to optimize performance of the chosen signaling technology. These considerations will be discussed next.

M-LVDS backplane design considerations

According to TIA/EIA-899, M-LVDS is intended for use in point-to-point applications, multidrop clock or data distribution applications, and multipoint data bus applications with multiple drivers sharing the same bus. The receiver input thresholds that are tighter than standard LVDS and the controlled edge rates are added qualities of M-LVDS that can contribute to the success of a high-performance system design.

A backplane test system was constructed with 8-, 19-, and 30-slot bus lengths to demonstrate the capabilities of M-LVDS in several backplane loading scenarios. The guidelines presented here describe high-performance system design practices for success with using M-LVDS in a backplane environment.

The backplane design was a collaborative effort between Texas Instruments (TI) and North East Systems Associates (NESA). The system is based on the CompactPCI® 6U standard with an 0.8″ slot pitch, standard 6U cards, and a 21-slot backplane (2 slots are reserved for power and 19 are used for test cards) that fits into a standard chassis for a 19″ rack. NESA built several multipoint backplane models for the purpose of simulating 8-, 19-, and 30-slot buses. Different edge rates, card and connector stub lengths, backplane differential impedance, termination resistance, and number of slots loaded for each bus length were also variables included in the simulations. IBIS and H-SPICE models of TI M-LVDS devices were provided to NESA and incorporated into the modeling and simulation stage of the backplane system to ensure the accuracy of the final system.

The physical system was constructed based on the simulation results NESA provided. Measurements of active M-LVDS devices operating on the multidrop buses were performed for verification of those simulation results. NESA also simulated and measured the passive backplane traces to ensure that the impedance and other signal integrity parameters specified in the backplane design rules were met. The result of this effort was a controlled impedance design consisting of 10 FR-4 layers, including 4 controlled impedance layers, 2 power layers, and continuous ground layers. Each slot on the backplane uses differentially fed, standard 2-mm HM connectors. This optimized M-LVDS backplane system operates at a data rate of >200 Mbps and a clock rate of >100 MHz across the 8-, 19-, and 30-slot designed bus systems.

The differential M-LVDS bus paths on the backplane were designed to meet a 130-Ω differential impedance, as this was the recommended backplane impedance suggested by the simulation results. A 100-Ω differential impedance is normally used in standard differential bus and backplane design, but the higher impedance helps to alleviate the effect of low effective path impedance created from the close slot pitch and large card load. In simulation, the raw backplane impedance and connector stub lengths were varied to aid in optimizing the former. As connector stub lengths increase, so does the overall capacitance of the loaded backplane bus, lowering the system differential impedance. Keeping connector stub lengths to a minimum will maximize the loaded impedance of the system bus. Results of the time domain reflectometry (TDR) and time domain transmission (TDT) simulations performed by NESA are shown in Table 3 and Table 4, respectively. The PICMG 3.0 AdvancedTCA base specification also recommends using a 130-Ω differential trace impedance to help increase the effective impedance of the clock bus in a heavily loaded backplane.

Table 3. Simulated TDR results from fully loaded 30-slot backplane*

RAW BACKPLANE IMPEDANCE (Ω)	MINIMUM IMPEDANCE LOADED (Ω)	MAXIMUM IMPEDANCE LOADED (Ω)	APPROXIMATE AVERAGE IMPEDANCE LOADED (Ω)
100	45.1	50.2	46
130	52.7	58.8	54
150	57.3	63.9	58

*1″ stubs; TDR rise time = 1 ns.

Table 4. Simulated TDT results from fully loaded 30-slot backplane

RAW BACKPLANE IMPEDANCE (Ω)	RISE TIME INPUT (ns)	RISE TIME OUTPUT (ns)	PROPAGATION DELAY (ns)	PER UNIT DELAY (ps/in)
100	1.07	3.07	9.63	388
130	1.07	2.98	10.6	427
150	1.07	3.01	11.2	452

With a raw impedance of 130 Ω, the effective differential impedance of the fully loaded 30-slot backplane is raised to 54 Ω from the 46 Ω provided by a standard 100-Ω raw impedance. This reduces the load on the device driving the bus and increases the differential voltage of the bus. The drawback of the 130-Ω differential impedance is that it increases the delay from 388 ps/in to 427 ps/in. Based on the results in Table 3, using a 150-Ω differential impedance would further increase the effective impedance of the backplane. However, a 150-Ω differential impedance is not easily manufactured, which increases the difficulty of providing a reliable and repeatable printed circuit board.

A trade-off between slot pitch and daughtercard stub length had to be accounted for during the backplane design. As pitch between slots is decreased, the "per unit" distributed loading on the backplane increases and the effective backplane impedance is reduced. The plug-in card stubs can significantly lower the effective impedance due to their capacitive effect on the backplane traces. As the card stub lengths increase, their capacitance increases and the effective impedance of the backplane is reduced, signal rise times are slowed, and propagation delay through the backplane is increased. If slot pitch is increased, the card stubs can be longer for a particular effective backplane impedance and vice versa. Table 5 and Table 6 show simulation results of TDR and TDT, respectively, on a 130-Ω raw impedance differential trace with 0.8″ slot pitch and different daughtercard stub lengths. Based on the correlated simulation and empirical results, a 1″ or shorter stub length is recommended to prevent the effective backplane impedance from falling below 54 Ω.

Except for delay differences, the 8-, 19-, and 30-slot backplane buses look very similar in passive testing. This is because they all share the same parameters, including 0.8″ slot spacing, identical connectors, and identical card stub lengths. The impedance and transmission profiles are similar to the 30-slot case presented.

Passive and active simulations along with empirical measurements were completed for the various backplane cases with 8-, 19-, and 30-slot buses. As mentioned earlier, the distributed load is similar for all the backplane buses, but actual driver and receiver waveforms can look quite different due to the distance to the terminations and the slot driving the bus. The resistor value used to terminate either end of the multipoint bus was chosen as a good compromise between the heavily and lightly loaded backplane configurations. Through analysis of the passive simulations and empirical results, 80 Ω was chosen to terminate the bus at either end; and all active simulation and empirical results were gathered with the 80-Ω terminations. Ringing, overshoot, and undershoot can be improved by using termination resistors closer to the effective bus impedance for the loading condition being tested.

Table 5. Simulated TDR results from fully loaded 30-slot backplane*

STUB LENGTH (in)	MINIMUM IMPEDANCE LOADED (Ω)	MAXIMUM IMPEDANCE LOADED (Ω)	APPROXIMATE AVERAGE IMPEDANCE LOADED (Ω)
0.5	57.5	62	58
1.0	52.8	58.8	54
1.5	45.9	56.6	50
2.0	40.3	55	48
2.5	35.9	53.6	45
3.0	32.3	52.3	43

*Raw impedance = 130 Ω; TDR rise time = 1 ns.

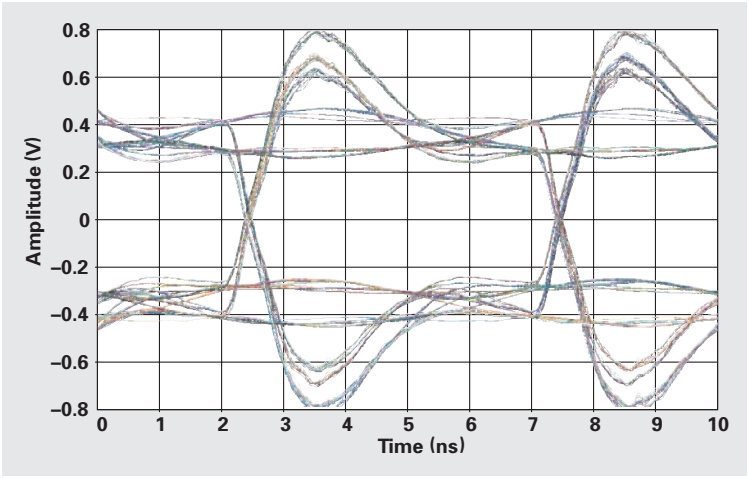
Table 6. Simulated TDT results from fully loaded 30-slot backplane

STUB LENGTH (in)	RISE TIME INPUT (ns)	RISE TIME OUTPUT (ns)	PROPAGATION DELAY (ns)	PER UNIT DELAY (ps/in)
0.5	1.07	2.60	9.68	390
1.0	1.07	2.98	10.6	427
1.5	1.07	3.40	11.5	464
2.0	1.07	3.84	12.3	496
2.5	1.07	4.28	13.1	528
3.0	1.07	4.78	13.8	556

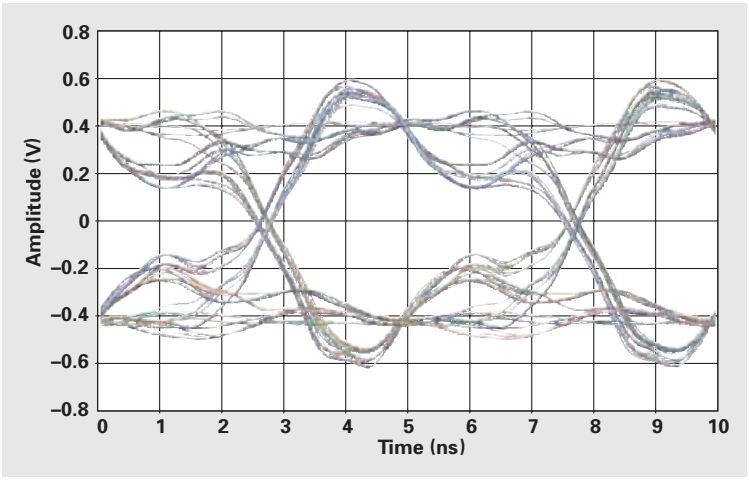
Figure 2 shows simulated 200-Mbps eye patterns at the driver output pins of slot 1 and the receiver inputs of slots 10 and 19 when slot 1 is driving a fully loaded 19-slot backplane bus. The differential voltage drops at slot 10 because it is in the middle of the bus, far away from the termination resistors, but it is still at acceptable levels. Slot 19 shows an improvement in differential voltage because the termination resistor is nearby.

Figure 2. Simulated 200-Mbps eye patterns when slot 1 drives 19-load bus

(a) At slot 1 driver output



(b) At slot 10 receiver input



(c) At slot 19 receiver input

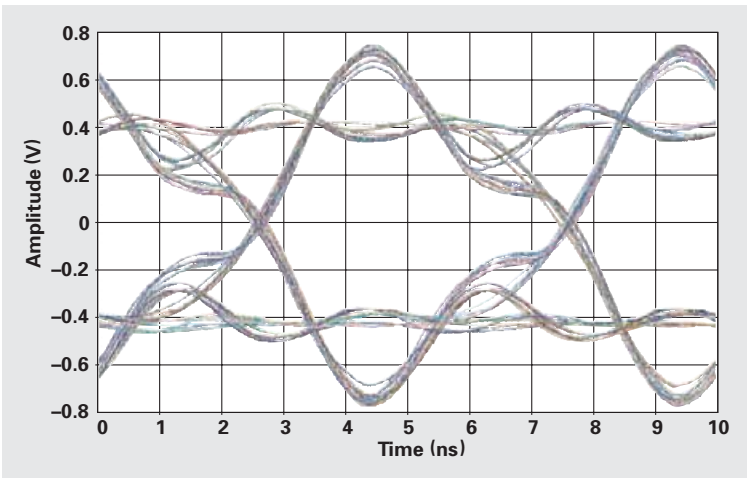
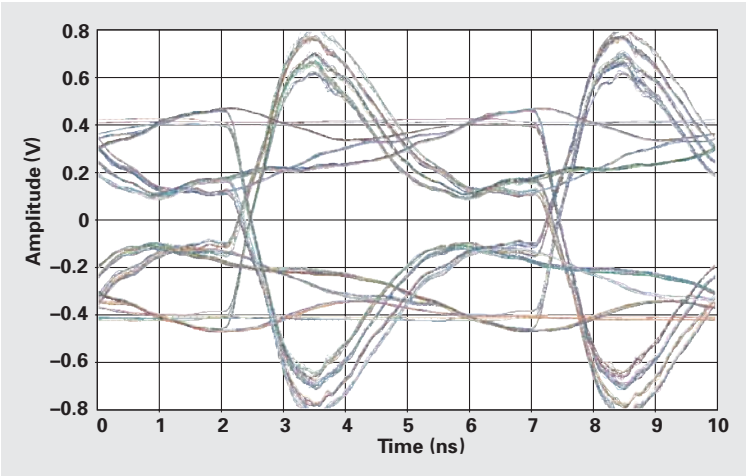


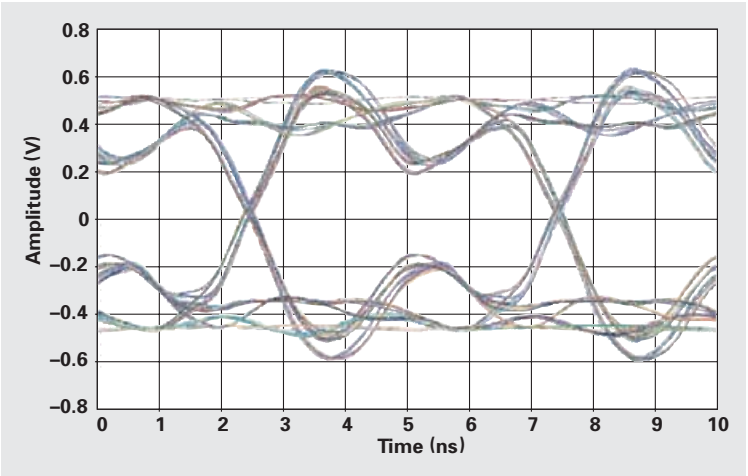
Figure 3 shows simulated 200-Mbps eye patterns at the driver output pins of slot 10 and the receiver inputs of slots 15 and 1 when slot 10 is driving a fully loaded 19-slot backplane bus. The effects of driving into the middle of a heavily loaded bus are evident in the jitter displayed in Figure 3a. However, by the time the signals reach slots 15 and 1, the initial amount of jitter at the driver output pins is masked by the increased rise and fall times. This effect is due to the capacitance encountered at each connector along the backplane by the signals from the driver at slot 10.

Figure 3. Simulated 200-Mbps eye patterns when slot 10 drives 19-load bus

(a) At slot 10 driver output



(b) At slot 15 receiver input



(c) At slot 1 receiver input

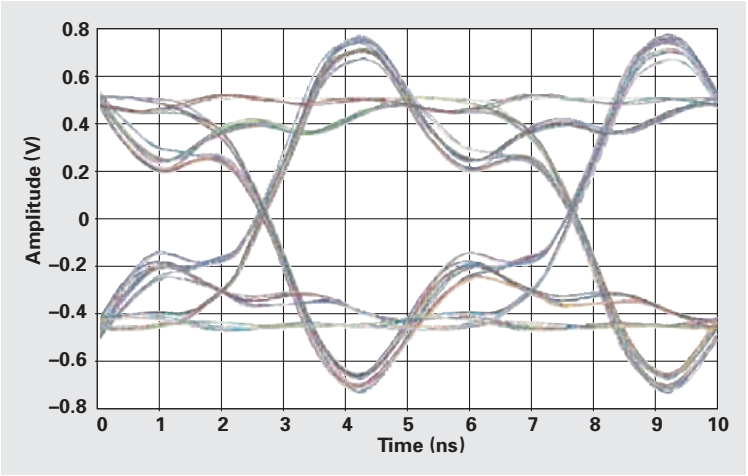
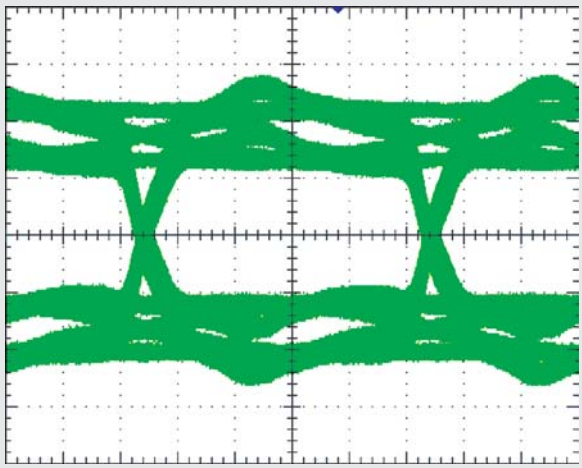
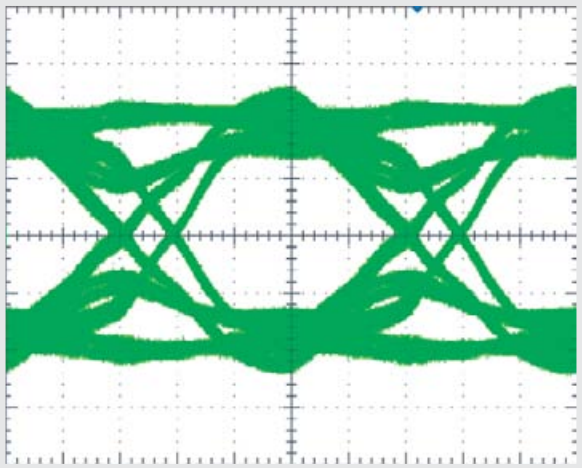


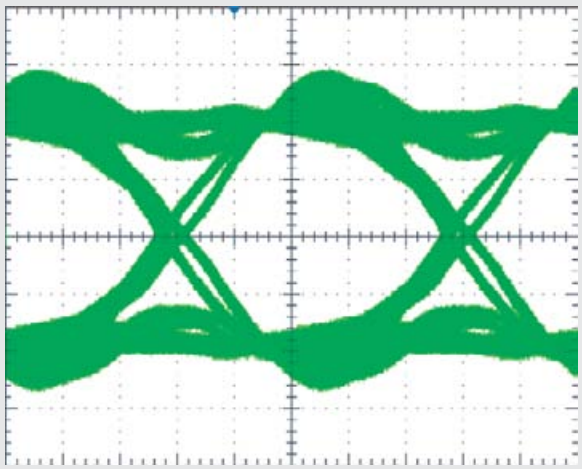
Figure 4. Measured 200-Mbps eye patterns when slot 1 drives 19-load bus



(a) At slot 1 driver output



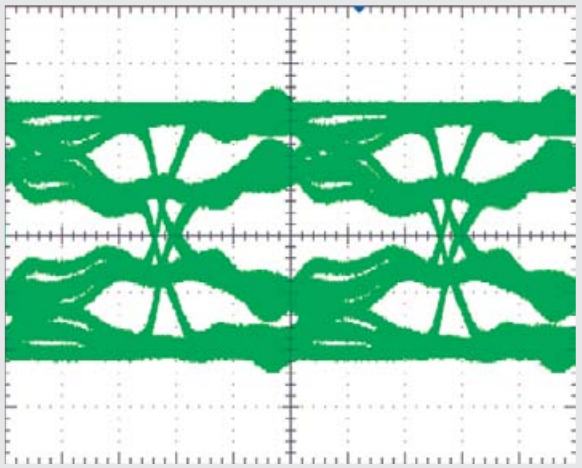
(b) At slot 10 receiver input



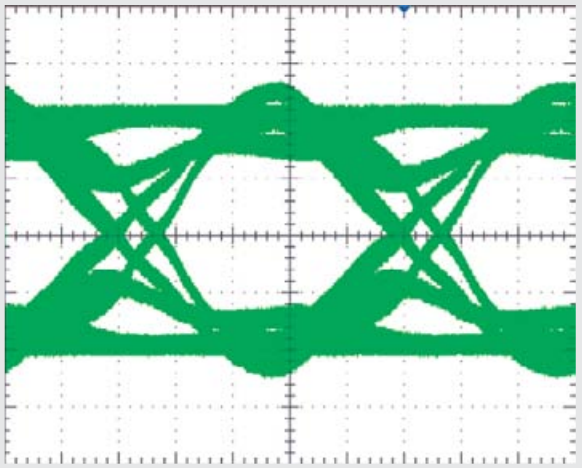
(c) At slot 19 receiver input

Figures 4 and 5 depict the measured results of the simulated waveforms in Figures 2 and 3. Comparing the simulation data to the measured data reveals that the modeling and simulation efforts in predicting the actual signal behavior on the bus are fairly accurate. For instance, the actual 200-Mbps eye pattern at the slot 1 driver output in Figure 4a has a lower amount of overshoot and more jitter than the simulation of the same case in Figure 2a. Because the voltage overshoot in the actual system is more dampened than that in the simulations, the signals in the actual

Figure 5. Measured 200-Mbps eye patterns when slot 10 drives 19-load bus



(a) At slot 10 driver output



(b) At slot 1 receiver input

system fall sooner than those in the simulated system. This causes the simulated results to predict a lower amount of jitter than that measured in the actual results. The simulated results, however, do accurately predict the minimum differential voltage in the measured eye pattern. Similar comparisons of overshoot, jitter, and differential voltage can be made between all of the simulated and actual results.

In conclusion, it is important to consider all aspects of backplane system design. As pitch between slots is decreased, the "per unit" distributed loading on the backplane increases and the effective backplane impedance is reduced. This can be mitigated by using a 130-Ω differential trace impedance, which helps increase the effective impedance in a heavily loaded backplane. Stub lengths should be kept short to minimize associated capacitance. The differential signal path should be carefully considered to help preserve data transmission within a noisy environment.

Each of the signaling technologies mentioned will satisfy certain needs. M-LVDS incorporates a controlled edge rate with LVDS-compatible signal levels. With the design guidelines previously discussed, implementing M-LVDS in a point-to-point, multidrop, or multipoint system can be successfully achieved. The 30-slot system demonstrates the robustness of M-LVDS drivers and the low capacitance of M-LVDS receivers supporting large bus systems up to and beyond 200-Mbps data rates (100-MHz clock rates). The PICMG 3.0 AdvancedTCA base specification calls for the use of M-LVDS for synchronization clocks across the backplane.

References

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