

A novel approach to narrowband matching high-speed RF ADCs

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For applications that don't require wideband sampling (1GHz to 2GHz or more), it can be challenging to design a narrowband (NB) match (requiring only hundreds of megahertz) with a balun or transformer front-end circuitry for an analog-to-digital converter (ADC). This challenge is magnified in systems with high intermediate frequencies that are digitized in modern communications or radar systems to perform signal processing in the digital domain.

In this article, I'll describe a simple process to maximize your ADC without a lot of simulation downtime. In a few simple steps, this process resolves hundreds of megahertz of bandwidth (BW) at any baseband or intermediate frequency location, as long as it sits within the ADC's own rated bandwidth.

Choosing the ADC and balun

Understanding the application requirements upfront is crucial when selecting the right type of ADC and ultimately determining the front-end development approach. Assume that there is a defined sampling rate, number of channels, digital output interface type and useful internal digital features that you could use or that are necessary for the application. I'll use the ADC3669 converter throughout this narrowband front-end example.

To begin, you must first understand the analog input characteristics of your chosen ADC. If you scroll down to the analog input parameters section of any converter datasheet, you should see the parallel $R||C$ specified in the specification tables. If not, check whether there is a simplified analog input model. As a final option, use

the ADC's S-parameters, which are typically listed on the product's webpage. For example, the ADC3669 data sheet lists a model input with a resistor (R) = 100Ω and a capacitor (C) = approximately 1.85pF (aggregated) differential impedance terms. See Figure 1.

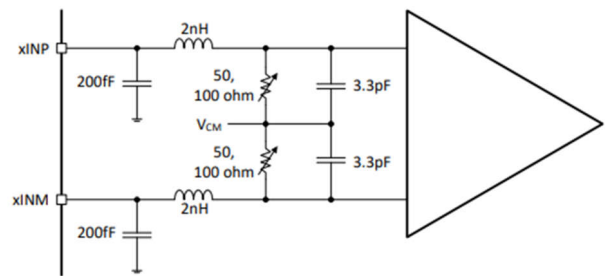


Figure 1. Analog input model in the ADC3669 datasheet

The next step is to choose the proper transformer or balun for the ADC, which include comparing these specifications between vendors: the return loss (RL), insertion loss, and phase and magnitude imbalance. If these parameters are not specified on the data sheet, ask the manufacturer, or measure them using a vector network analyzer or VNA.

Choosing between a standard flux-coupled transformer or balun will depend on the BW requirements. Standard transformers are often $<1\text{GHz}$, whereas a balun can achieve much higher BW. Reference [1] describes transformer and balun parametric and ADC requirements in detail.

For NB matching, the example calls for a reactive resistor-capacitor-inductor (RCL) match with the last component in shunt; see Figure 2 and References [2] and [3] for information about matching pads and topologies. Collecting and understanding the application

requirements will enable you to select the front-end BW and balun. For the example, I selected the TCM2-33WX+ balun from Mini-Circuits with a 1:2 impedance ratio and 3GHz of BW after measuring and understanding this balun's capabilities from previous examples used on the

ADC3669 evaluation module (EVM). The TCM2-33WX+ provides a relatively low input drive in order to reach ADC's full scale input range.

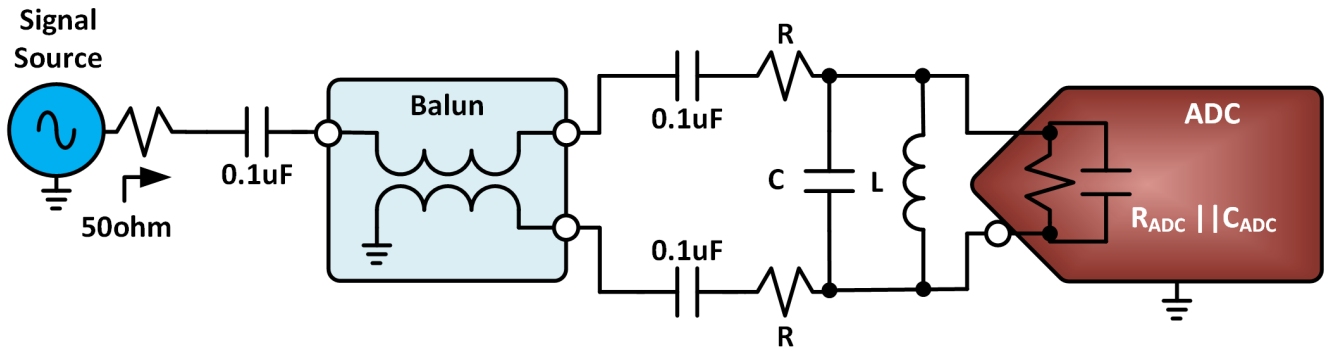


Figure 2. Front-end interface and component placement

Solving for R

To conduct an RCL reactive match, first determine the R value of the front end. You could split the termination between the primary and secondary of the balun, but in this example we only terminate the secondary of the balun in order to minimize the number of components required. Depending on the application and signal-chain lineup, a split termination across the balun's primary and secondary may make more sense.

As shown below, the calculations reveal how to solve the R value which completes the differential termination required by the secondary of the balun. A good starting point for setting up the secondary differential termination is to use the ideal case, 100Ω, since this balun has an 1:2 impedance ratio. The balun does have losses and parasitics that change over frequency. So, to start the calculation and obtain a more proper R value termination, use the balun's RL number at the specified center frequency (940MHz in the example) to calculate the characteristic impedance (Z_o) to which the balun needs to be properly matched for optimized signal power transfer to the load.

The example illustrates how to calculate the secondary termination of the balun chosen. The TCM2-33WX+ data sheet specifies -16.3dB at 940MHz. Using this value, solve for the characteristic impedance as reflected from the balun's secondary (Equation 1):

$$RL = -16.3dB \text{ at } 940MHz = 20 \log \left(\frac{50 - Z_o}{50 + Z_o} \right) = 10^{\left(\frac{-16.3}{20} \right)} = \left(\frac{50 - Z_o}{50 + Z_o} \right) \quad (1)$$

Therefore, $Z_o = 36.72\Omega$ (primary impedance).

In an ideal 1:2 impedance balun, 100Ω on the secondary should equal 50Ω on the primary; see Figure 3. This is not the case in actuality, however, as shown in the calculation. To determine the actual impedance reflected back to the primary, use the value of Z_o found in the previous step, and back-calculate to get the proper termination on the secondary side (Equation 2):

$$\frac{Z(\text{Primary Reflected})}{Z(\text{Secondary Ideal})} = \frac{Z(\text{Primary Ideal})}{Z(\text{Secondary Reflected})} \quad (2)$$

Therefore, $\left(\frac{36.72}{100} \right) = \left(\frac{50}{X} \right)$, where solving for X = 136.1Ω.

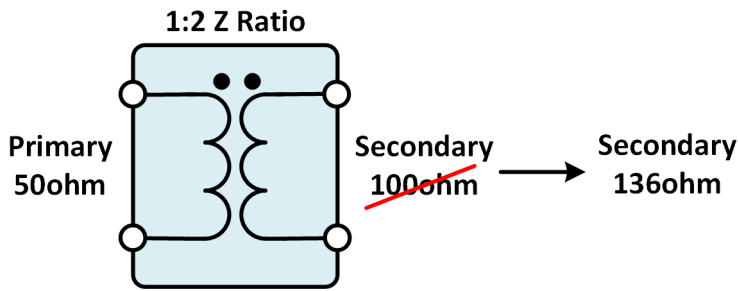


Figure 3. A 1:2 impedance balun or transformer

Because the balun has some unaccounted losses at this frequency, the 136Ω secondary termination helps compensate for these losses and provides a better termination value to start with on the secondary, reflecting back the correct impedance at this specific intermediate center frequency onto the primary of the balun. Proper impedance matching will achieve a closer 50Ω match on the primary to yield the maximum signal power transferred from the source.

The 136Ω secondary termination is an aggregate termination. Because the ADC itself already has a 100Ω differential termination inside, place one series 33Ω resistor on each side of the secondary. Review Figure 2 again. You have now solved for the R value required.

A -16dB RL at 940MHz may allow you to use smaller resistor values or possibly eliminate them altogether. I recommend keeping resistors in the design, however, as the ADC's internal differential impedance has a ±10% tolerance range from process variations; the RL of the balun will have tolerances as well. Adding in a small amount of extra resistance helps keep the overall impedance more accurate, as you will notice when looking closely at the ADC's S-parameter values at 940MHz.

Solving for L

The next step is to “resonate out” the ADC's internal C to determine an equivalent shunt inductor or L value for the

match. To choose this value, first find the internal C value of the ADC using one of two methods:

- Use the ADC model given in the data sheet (Figure 1) to determine the aggregate parasitic internal front-end capacitance or C value, estimated as approximately 1.85pF.
- Use the S-parameters from the ADC3669 webpage. See reference [4].

The second approach offers a more precise capacitive number at the frequency of interest, as the capacitive value found at 940MHz will be more absolute versus the first approach, where the C value in the model covers the full range of the ADC's input BW. Let's review both approaches in order to understand the trade-offs.

In both methods, the idea is to simply set the two reactive elements to be equal (Equation 3):

$$X_C = \frac{1}{(2\pi \times f \times C)} \text{ and } X_L = 2\pi \times f \times L \quad (3)$$

Next, set f to the resonate center frequency of your NB application. For the example, I will use 940MHz.

In the first method, if f = 940MHz,

$$\frac{1}{(2\pi \times 940M \times 1.85p)} = 2\pi \times 940M \times L \quad (4)$$

Then, solving for L = 15.5nH.

In the second method, you need to use the S-parameters and plot them in a simulator in order to determine the C value at 940MHz; see Figure 4.

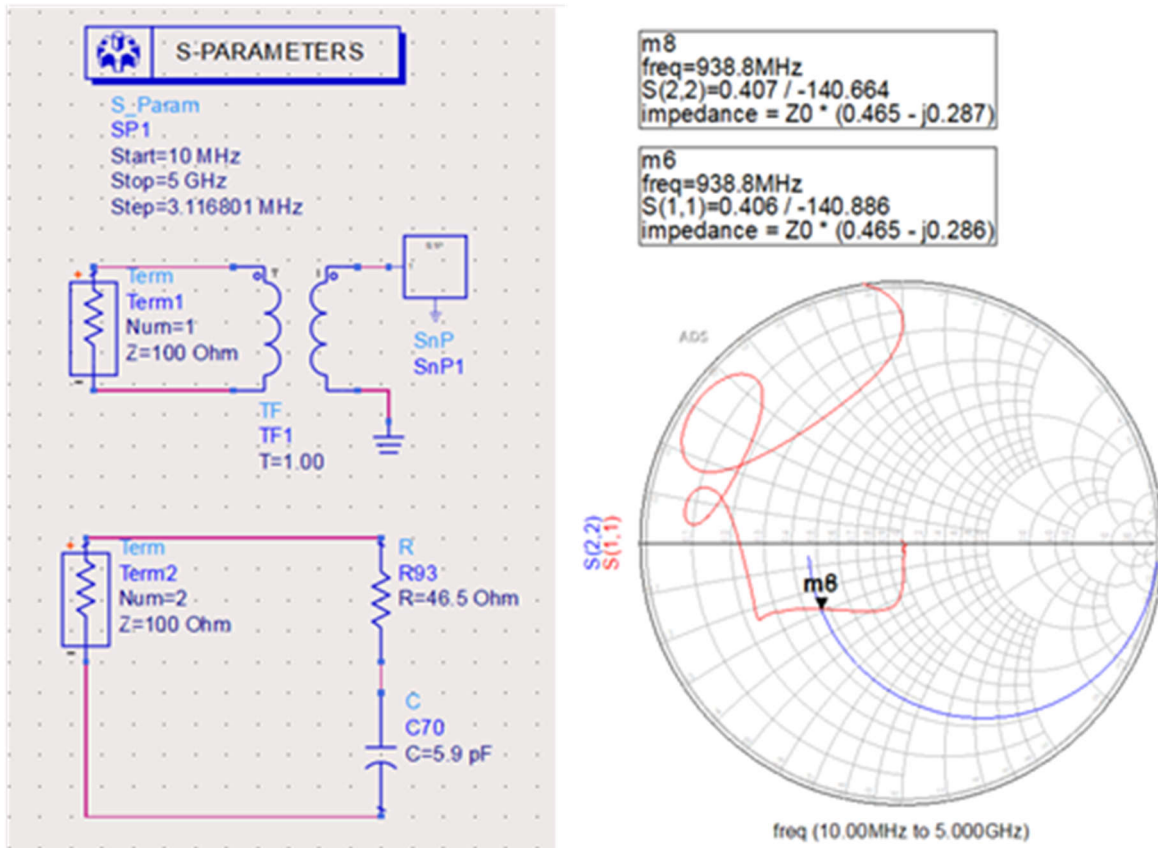


Figure 4. Smith chart plot of the ADC3669 analog input at 940MHz

The second method is a bit more involved; the Smith chart plots the S-parameters in a series R + jXc configuration. The R + jXc needs to be parallel-transformed so that the R and Xc are in parallel, or R||Xc. See Figure 5 and Equation 4:

$$Impedance = Z_o \times (R + jX_c) \text{ or } 100 \times (0.465 - j0.287) = 46.5 - j28.7 \quad (5)$$

Use Equation 5 to obtain the parallel transformation:

$$R_p = \left(\frac{46.5^2 + (-28.7)^2}{46.5} \right) = 64.2\Omega \quad (6)$$

Recalling the two inflated 33Ω resistors used to set the R value in the previous section brings the aggregate resistive termination seen by the balun to 130.2Ω, which is closer to 100Ω differential that the balun would see ideally with a smaller or no R value at all.

Next, solve for the parallel capacitor at 940MHz, see Equation 6:

$$C_p = \frac{\frac{-28.7}{(46.5^2 + (-28.7)^2)}}{\frac{2}{\pi \times (-28.7 \times 10^6)}} = 1.62pF \quad (7)$$

Now use the same equation as above in order to find the appropriate shunt L value. If f = 940MHz, C = 1.62pF,

$$\frac{1}{(2\pi \times 940M \times 1.62p)} = 2\pi \times 940M \times L \quad \text{. Solving for } L = 18.1nH.$$

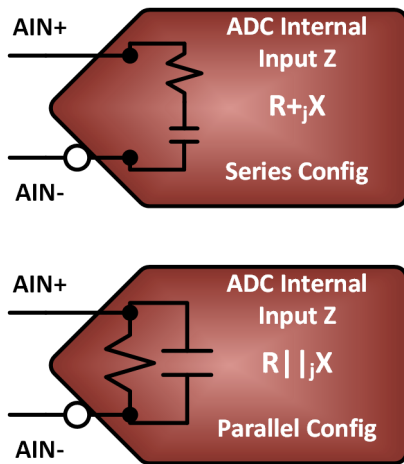


Figure 5. ADC internal R and C series to parallel representations

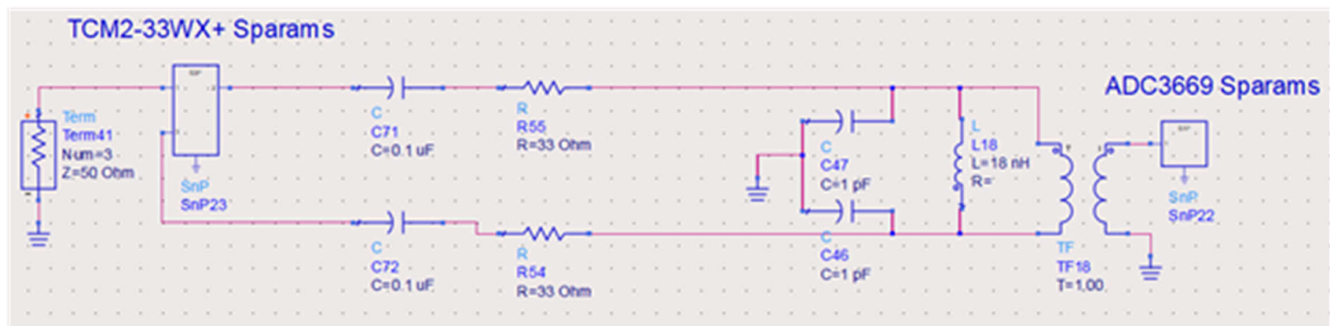


Figure 6. ADS simulation front-end mockup with 18nH shunt match

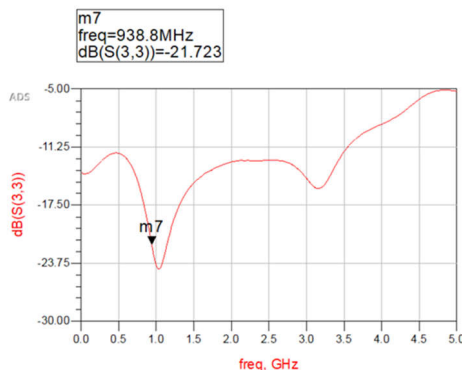


Figure 7. Simulated RL (S11) plot of 18nH shunt-matched response

Next, let's compare our simulated results against some measured data in the lab. Figure 8 illustrates the use of the ADC3669 EVM to implement the front-end match to measure a passband flatness response. The resonant point is centered, but the match is a bit more wideband than expected. This is where simulation can be inadequate. A 3D electromagnetic simulation solver

These two C values found in the two methods above (eg: 1.85pF and 1.62pF) are on the order of the same magnitude; therefore, you need to consider the internal inductive L parasitics, as well as the external L parasitics that get added in, based on your layout.

It is also possible to simulate the entire frontend in ADS simulator package, as shown in Figure 6, which uses the S-parameters of the TCM2-33WX+ balun and the ADC3669. The simulation results shown in Figure 7 show very good RL (<-15 dB), indicating that 18nH is a good match at 940MHz.

might be able to capture all of the board parasitics in order to get a closer 1:1 match between the simulation and lab measurements. There are a few second- and third-order nuances to uncover, however. Next, we will add in a shunt C to complete the RCL reactive match to make the lab measurement narrower, as expected.

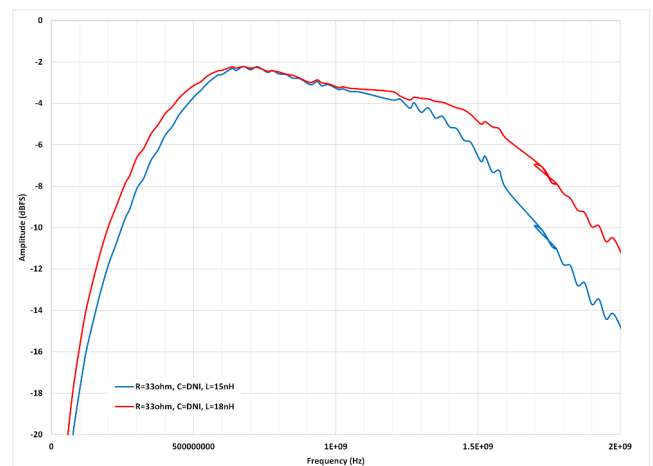


Figure 8. Passband flatness sweep with L value installed

Solving for C

To further improve the narrowband width match (in other words, make it narrower), add the last component in the RCL reactive match from Figure 2. Placing the C term in parallel with the inductor creating an LC tank. It seems counterintuitive to add capacitance back into the front-end match after placing the 18nH inductor to combat the ADC's internal capacitance, but it tightens the filter match. In order to solve for a parallel C value to complete the LC tank, use Equation 7:

$$f_o = \frac{1}{(2\pi \times \sqrt{LC})} \text{ or } 940\text{MHz} = \frac{1}{(2\pi \times \sqrt{18\text{nH} \times C})} \quad (8)$$

Solving for C = 1.6pF.

Let's put this value (1.6pF capacitor or nearest standard value) in the front-end design and rerun the passband BW sweep; see Figure 9.

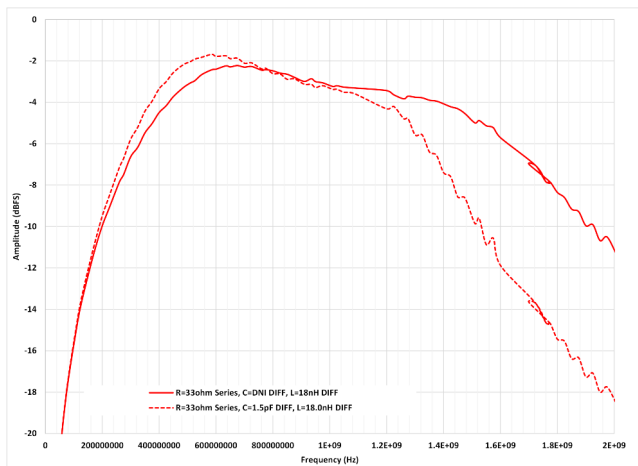


Figure 9. Passband flatness sweep with L and C values installed

As can be seen, adding in the additional 1.5pF capacitor in parallel with the 18nH inductor, creating that LC tank, doesn't really improve or narrow the match (see mini-dashed curve).

The LC tank method will work, but with a few considerations. Removing the internal C by solving the external L value (18nH) will help but may not entirely prove to be the end solution. To implement

this accurately, you need to use a much larger C value to completely remove any internal and residual external C parasitics. You are competing with balun and trace parasitics, as well as the ADC's internal sampling capacitor, which is dynamic in nature as the sample switch opens and closes quickly.

Let's choose a higher value for C, such as 9.1pF, re-solve for L in using Equation 7 again:

$$f_o = \frac{1}{(2\pi \times \sqrt{LC})} \text{ or } 940\text{MHz} = \frac{1}{(2\pi \times \sqrt{L \times 9.1\text{p}})} \quad (9)$$

Solving for L = 3nH.

With these values in place of the front-end design, Figure 10 shows the results after re-running the passband BW sweep.

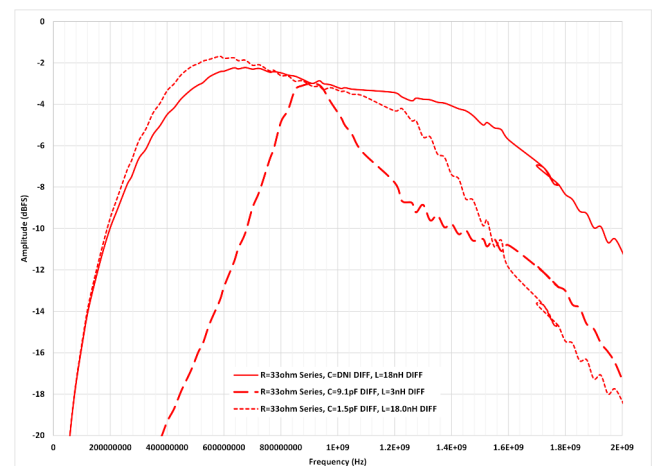


Figure 10. Passband flatness sweep with new L and C values installed

As you can see, there is a considerable improvement when narrowing the bandwidth match to 350MHz wide (the thick dashed curve) by increasing the external C in order to further improve the NB match response. Typically, it's good to use at least twice the value of C based on the aggregate ADC's internal sampling network as a good starting point. Adding this term externally will only further improve RL in the band of choice.

You can then adjust the L value, the C value, or both to help widen or narrow or shift the BW needed to match

for your application needs. You will need to remember these values for the layout, balun and ADC input model; it is not possible to simulate all parasitic nuances, and some empirical experience might be necessary in order to gauge the match properly.

Figure 11 illustrates the signal-to-noise ratio (SNR) and second- and third-order harmonics (HD2 and HD3) collected over the NB application example to further verify the ADC's performance within the 940MHz band.

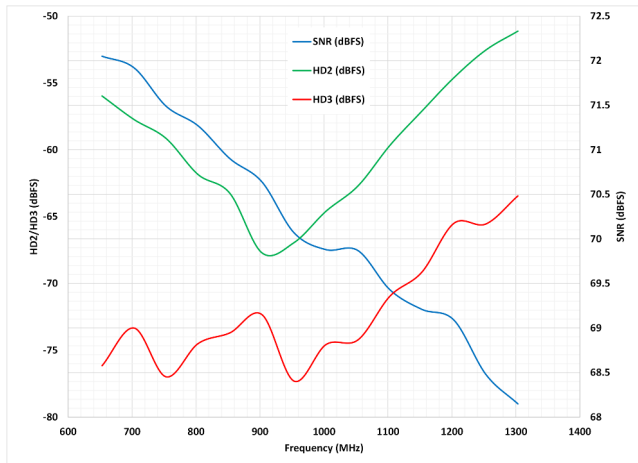


Figure 11. Resulting AC performance of SNR, HD2 and HD3 vs. the NB match frequency range

An analog input center frequency of 940MHz is a bit outside the ADC datasheet measurement specification. The collected values do follow the correct trend for all the collected measurements, SNR, HD2 and HD3, however, and degradation will continue to occur as the input RL degrades >940MHz for this particular ADC.

Conclusion

You do not have to be an expert simulator when developing a narrowband matching application to your particular high-speed RF sampling ADC. This NB matching approach can be used to help strengthen any upstream filtering in the RF signal chain. First, address the resistive part of the NB matching effort by using the chosen balun's return loss values from its datasheet to will help improve the input front-end network's return loss. Next, use the ADC's given S-parameters, datasheet input model or lumped element

R||C values in the specification tables as a starting point to your NB match, at your frequency band of interest. Keep in mind, the balun and pcb layout contribute to the passive components needed to complete the match. Make sure these are factored in as well as a starting point.

With a little simulation to provide direction and some simple math, you can accelerate your next high-speed RF converter design in no time.

References

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