EVM User's Guide: SK-AM62, SK-AM62B, SK-AM62B-P1

AM62x SK Evaluation Modules

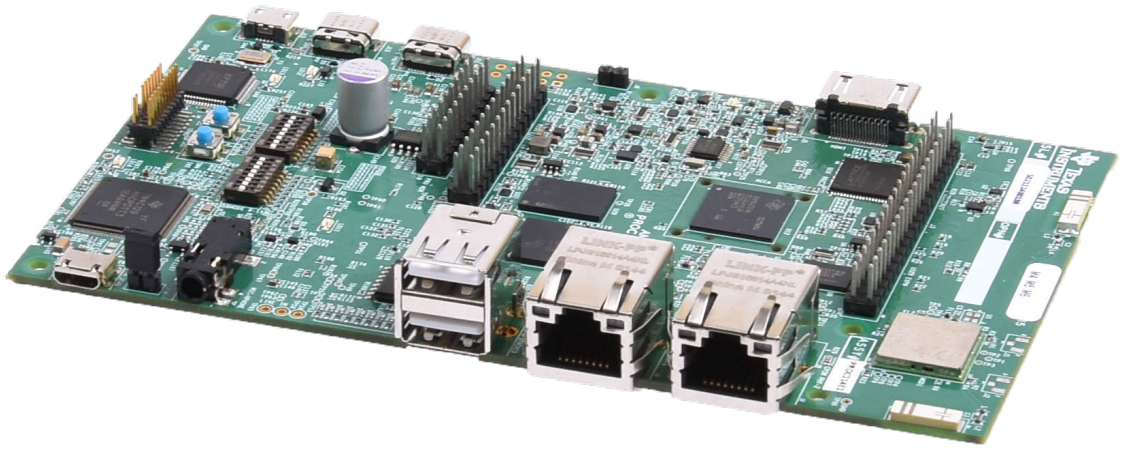
Description

The AM62x starter kit (SK) evaluation module (EVM) is a stand-alone test and development platform built around the AM62x system-on-a-chip (SoC). AM62x processors are comprised of a quad-core 64-bit Arm®-Cortex®-A53 microprocessor, single-core Arm®-Cortex®R5F microcontroller (MCU) and an Arm®-Cortex®-M4F MCU.

The SK-AM62 is the version of the AM62x starter kits for general purpose applications utilizing a discrete power design. SK-AM62B is the newest version of SK-AM62 and includes high-security field-securable (HS-FS) silicon to customize keys and encryption for security applications. SK-AM62B-P1 is the newest version of SK-AM62, which includes the TPS64219 and TPS64220 PMIC onboard that is designed to enable power efficient portable and stationary applications. Additionally, the SK-AM62B-P1 is security enabled which allows for secure boot, debug security and firewalls.

Features

- Processing: AM6254 with four Arm Cortex-A53, 3D graphics processing unit (GPU), one Cortex-M4F, two PRU-SS
- Display: Dual display support, up to 2K display resolution. One dual-channel LVDS. One HDMI connector over DPI or RGB444 with audio codec TLV320AIC3106.
- M.2 key E interface support for Wi-Fi® and *Bluetooth*® modules; two RJ-45 Ethernet 1000/100 Mbps with TSN support
- Connectivity: One Type-A USB 2.0, one Type-C dual-role device (DRD) USB 2.0 supports USB booting, onboard XDS110 joint test action group (JTAG) emulator, four niversal asynchronous receiver-transmitters (UARTs) by USB 2.0-B
- Storage: 2-GB DDR4; bootable interfaces on SK, removable microSD, USB, quad serial peripheral interface (QSPI), Ethernet, UART
- Software: TI processor SDK Linux®, RT-Linux, TI processor SDK Android™ AM62x, out-of-box demonostrations including Wi-Fi



This design incorporates HDMI® technology.

Copyright © 2026 Texas Instruments Incorporated

Table of Contents

Description 1
Features 1
1 Evaluation Module Overview 4
1.1 Introduction 4
1.2 Kit Contents 4
2 Hardware 5
2.1 System Description 5
3 Additional Information 66
3.1 EVM Revisions and Assembly Variants 66
3.2 Known Issues and Modifications 66
3.3 Trademarks 70
4 Compliance and Certifications 71
4.1 EMC, EMI and ESD Compliance 71
Regulatory Compliance 71
5 References 72
6 Revision History 72

List of Figures

Figure 2-1. SK-AM62 Top View 5
Figure 2-2. SK-AM62B-P1 Rev B Top View 6
Figure 2-3. SK-AM62 Back View 7
Figure 2-4. SK-AM62B-P1 Rev B Bottom View 8
Figure 2-5. Functional Block Diagram of the SK-AM62 Board 10
Figure 2-6. Functional Block Diagram of the SK-AM62B Board 11
Figure 2-7. Functional Block Diagram of the SK-AM62-P1 Board with TPS65219 PMIC 12
Figure 2-8. Functional Block Diagram of the SK-AM62B-P1 Board with TPS65219 PMIC 13
Figure 2-9. SD Bootmode Switch Setting Example (From E2) 15
Figure 2-10. SD Bootmode Switch Setting Example (E1) 15
Figure 2-11. Clock Architecture of AM62x SKEVM 17
Figure 2-12. SoC WKUP Domain 17
Figure 2-13. MMC2 - Wilink Interface on SK-AM62 and SK-AM62-P1 36
Figure 2-14. MMC2 - M.2 Connector Interface on SK-AM62B and SK-AM62B-P1 37
Figure 2-15. Power Supply Block Diagram 47
Figure 2-16. Power Up Sequence 48
Figure 2-17. Power Down Sequence 49
Figure 2-18. Power Sequence Block Diagram 50
Figure 2-19. Bootmode Switch Configuration for SD Boot (From E2) 52
Figure 2-20. Bootmode Switch Configuration for SD Boot (E1) 53
Figure 3-1. PRU Connector Missalignment on E1 Boards 67
Figure 3-2. Schematic of I2C Buffer Section 69
Figure 3-3. Location on AM62x SK E3 (Bottom Side) 69
Figure 3-4. OLDI Display RESET Logic Circuit 70
Figure 3-5. PCBA Bottom Image 70

List of Tables

Table 2-1. Interface Mapping 14
Table 2-2. Power Test Points 16
Table 2-3. Clock Table 18
Table 2-4. Display Connector Pinout (As used by display and the E3 EVM) 19
Table 2-5. Display Connector Pinout (E1/E2) 20
Table 2-6. CSI Camera Connector J19 Pin-out 21
Table 2-7. JTAG Connector (J17) Pin-out 24
Table 2-8. Test Automation Connector (J23) Pin-out 26
Table 2-9. UART Port Interface 27
Table 2-10. IO Expander Signal Detail 40
Table 2-11. GPIO Mapping 42
Table 2-12. Type-C port Power roles 44
Table 2-13. Recommended External Power Supply 44
Table 2-14. SoC Power Supply 50
Table 2-15. INA I2C Device Address (E1) 51

Copyright © 2026 Texas Instruments Incorporated

Table 2-16. INA I2C Device Address (E2)..... 51
Table 2-17. BOOT-MODE Pin Mapping..... 53
Table 2-18. PLL Reference Clock Selection BOOTMODE [2:0]..... 53
Table 2-19. Boot Device Selection BOOT-MODE [6:3]..... 54
Table 2-20. Backup Boot Mode Selection BOOT-MODE [12:10]..... 54
Table 2-21. Primary Boot Media Configuration BOOT-MODE [9:7]..... 54
Table 2-22. Backup Boot Media Configuration BOOT-MODE [13]..... 55
Table 2-23. User test LEDs 55
Table 2-24. PRU Header (J10) Pin-out..... 56
Table 2-25. 40 Pin User Expansion Connector..... 57
Table 2-26. Pin MCU Connector (J9)..... 59
Table 2-27. EVM Push Buttons..... 61
Table 2-28. I2C Mapping Table (SK-AM62 E3 and SK-AM62-P1 Variants)..... 62
Table 2-29. I2C Mapping Table (SK-AM62 E2)..... 64
Table 3-1. SK EVM PCB Design Revisions and Asssembly Variants..... 66
Table 3-2. AM62x SK EVM Known Issues and Modifications..... 66

Copyright © 2026 Texas Instruments Incorporated

1 Evaluation Module Overview

1.1 Introduction

The SKEVM allows the user to experience great dual display feature through HDMI® (over DPI) and LVDS, and industrial communication methods using serial, Ethernet, USB and other interfaces.

The SKEVM can be used for your display application(for example a HMI or control panel) with either a HDMI display or an external LVDS panel, up to 2K resolution. It's high performance (up to) Quad-A53 ARM cores at 1.4GHz, with rich industrial interfaces, offer control and communication capabilities for a wide ranges of applications, such as PLC, automation control and monitor/supervisor systems. In addition, SKEVM can communicate with other processors or systems, and act as a communication gateway. The embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ from TI.

This technical User's Guide describes the hardware architecture of the AM62x SKEVM, a low cost Starter Kit built around the AM62x SoC. The AM62x processor comprises of a Quad-Core 64-bit Arm®-Cortex® A53 microprocessor, Single-core Arm Cortex-R5F MCU and an Arm Cortex-M4F MCU.

Note

This evaluation board is a pre-production release and has several known issues that must not be copied into a production system. E1 EVM Shown in product photos.

Note

The maximum length of the IO cables shall not exceed 3 meters.

1.2 Kit Contents

- EVM
- Quick Start Guide

Copyright © 2026 Texas Instruments Incorporated

2 Hardware

2.1 System Description

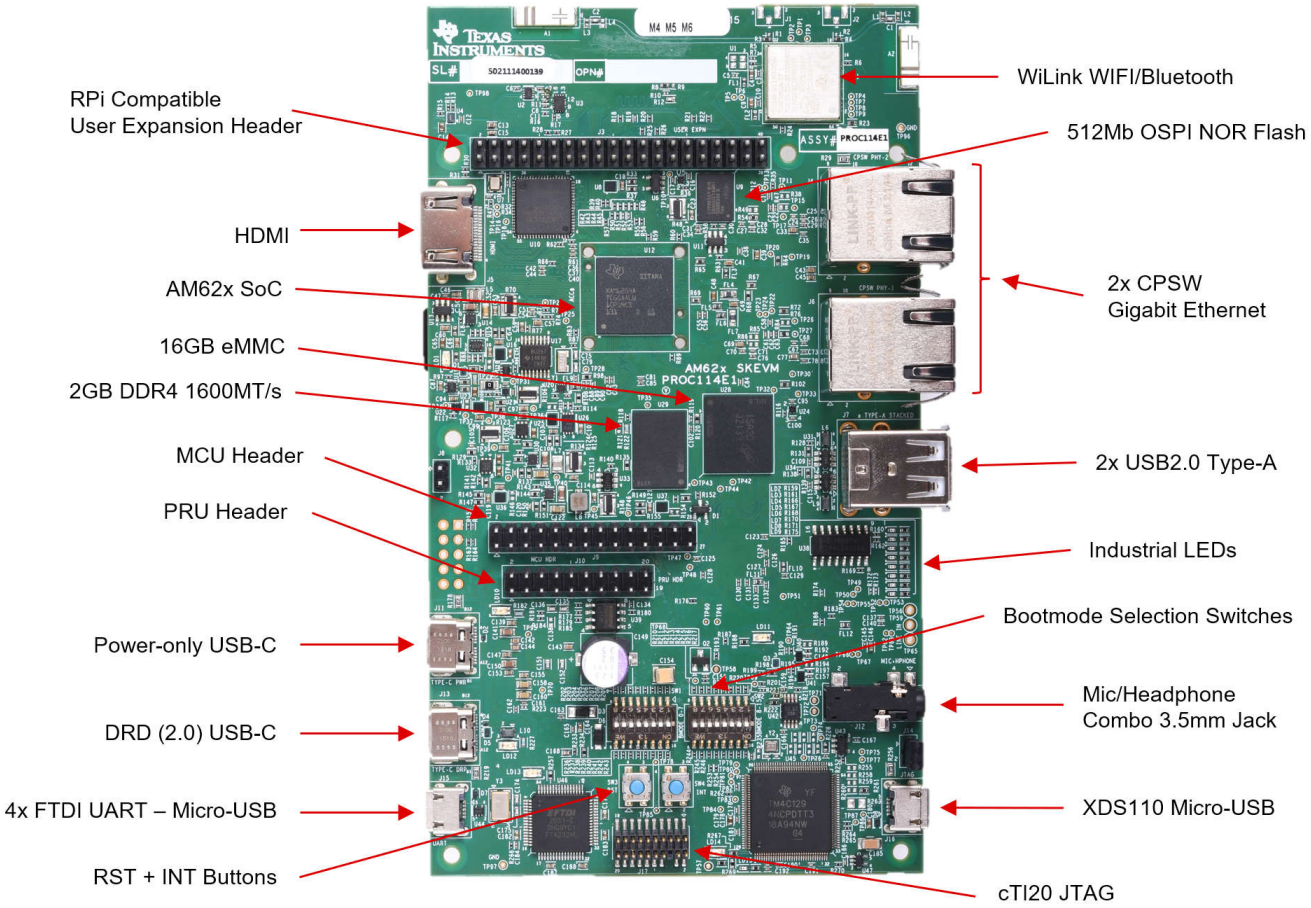


Figure 2-1. SK-AM62 Top View

Copyright © 2026 Texas Instruments Incorporated

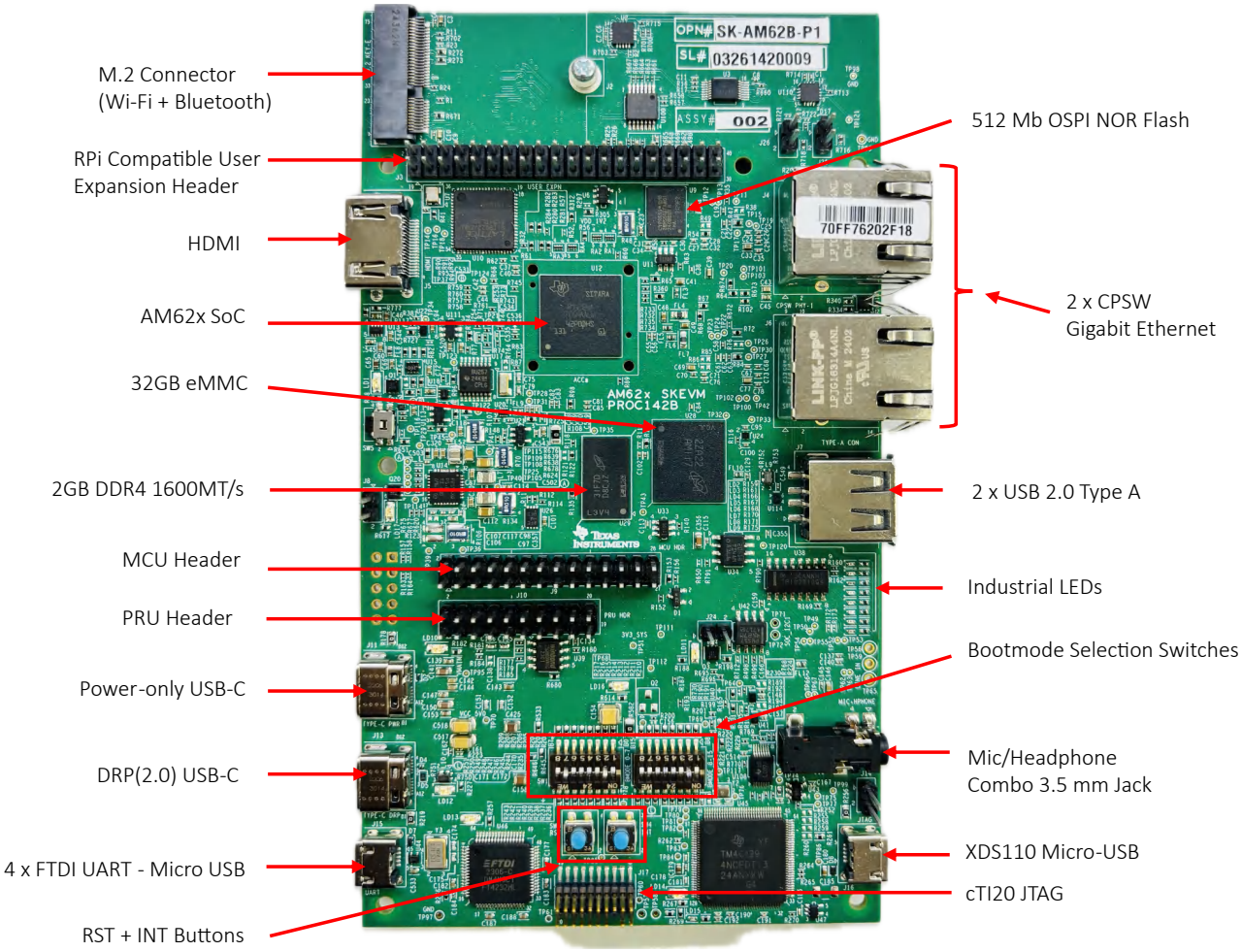


Figure 2-2. SK-AM62B-P1 Rev B Top View

Copyright © 2026 Texas Instruments Incorporated

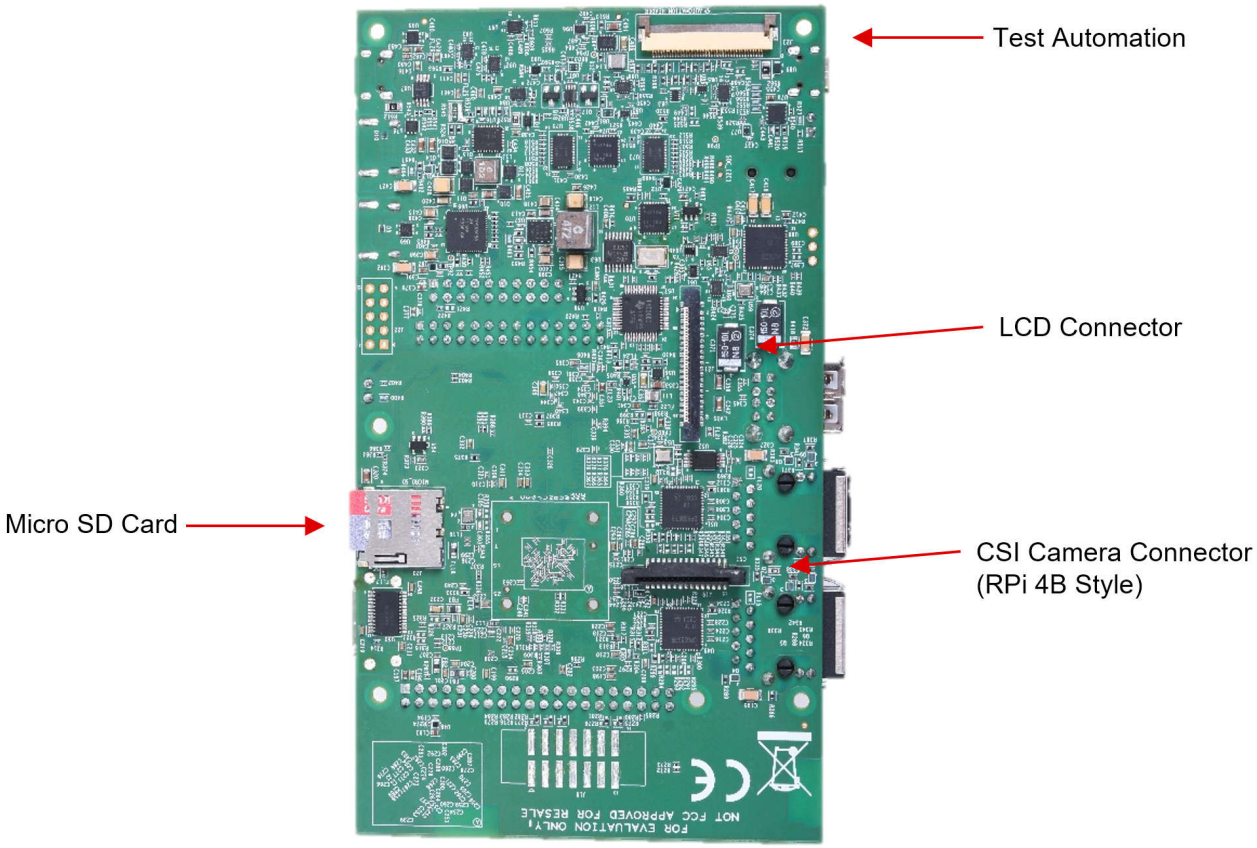


Figure 2-3. SK-AM62 Back View

Copyright © 2026 Texas Instruments Incorporated

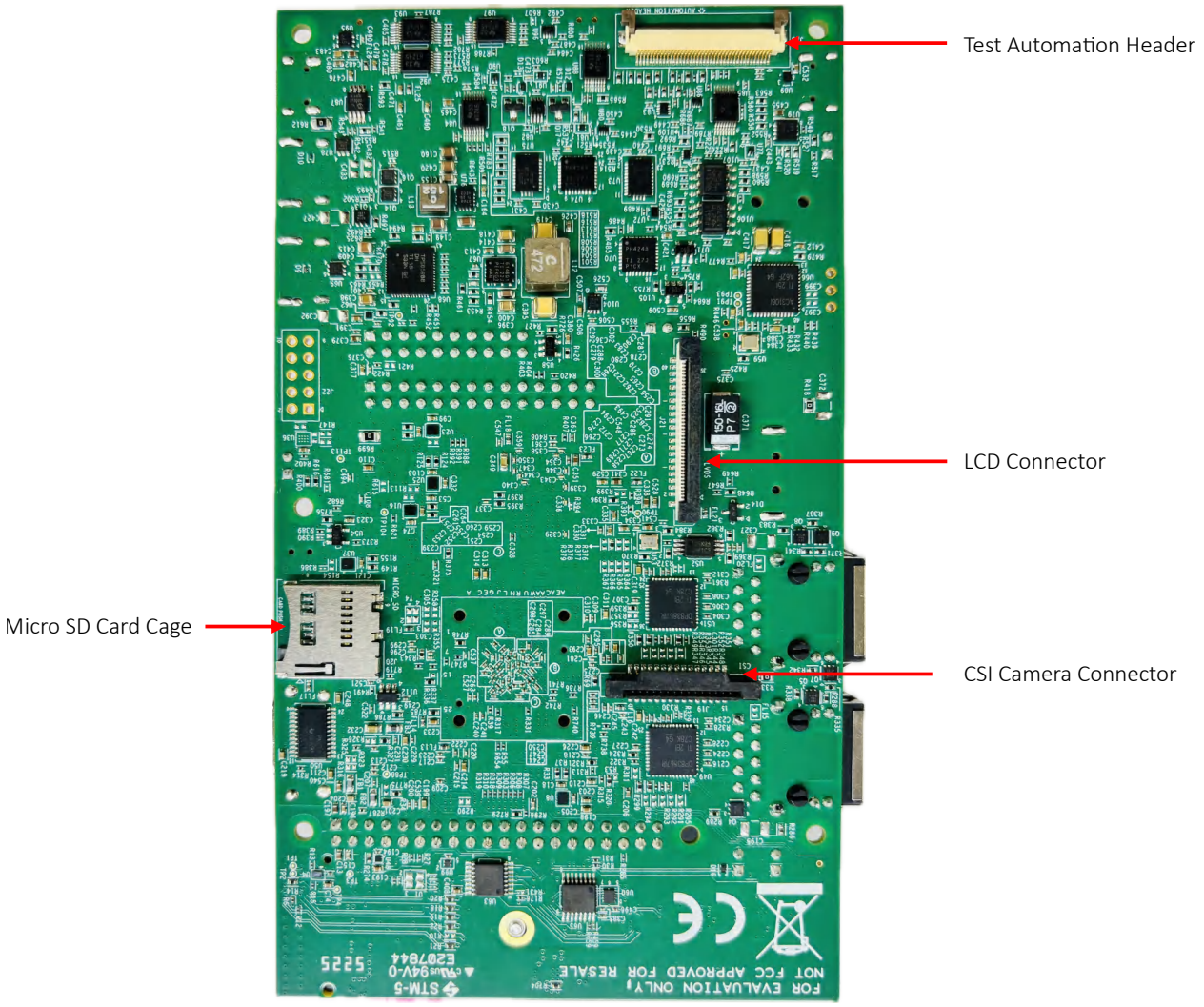


Figure 2-4. SK-AM62B-P1 Rev B Bottom View

2.1.1 Key Features

The AM62x SKEVM is a high performance, standalone development platform that enables users to evaluate and develop industrial applications for the Texas Instrument's AM62x System-on-Chip (SoC).

The following sections discuss the SKEVM's key features.

2.1.1.1 Thermal Compliance

There is elevated heat on the processor, use caution particularly at elevated ambient temperatures! Although the processor is not a burn hazard, caution should be used when handling the EVM due to increased heat in the area of the SoC.

	Caution	Caution Hot surface. Contact may cause burns. Do not touch!

2.1.1.2 Processor

- AM62x SoC, 13 mm x 13 mm, 0.5 mm pitch, 423-pin VCA FBGA

2.1.1.3 Power Supply

- Two USB Type-C ports (5V-15V input range)
- Optimized Power Solution with Discrete Regulators and LDOs for the Processor and Peripherals

Copyright © 2026 Texas Instruments Incorporated

2.1.1.4 Memory

- 2GB DDR4 supporting data rate up to 1600MT/s.
- Micro SD Card slot with UHS-1 support
- 512Mbit Octal SPI Flash memory
- 512 Kbit Inter-Integrated Circuit (I2C) board ID EEPROM
- 16GB eMMC Flash

2.1.1.5 JTAG/Emulator

- XDS110 On-Board Emulator
- Supports 20-pin JTAG connection from external emulator

2.1.1.6 Supported Interfaces and Peripherals

- 1x USB2.0 Type C Interface, support DFP and UFP roles
- 1x USB2.0 Host Interface, Type A
- 1x HDMI Interface
- Audio Line in and Mic + Headphone out
- Wilink WL1837 Module with support for Wi-Fi and Bluetooth
- 2x Gigabit Ethernet ports supporting 10/100/1000 Mbps data rate on two RJ45 connectors.
- Quad port UART to USB circuit over microB USB connector
- Industrial Ethernet LEDs
- INA devices for current monitoring
- 2x Temperature Sensors near SoC and DDR4 for thermal monitoring

2.1.1.7 Expansion Connectors/Headers to Support Application Specific Add-On Boards

- CSI Camera Header
- LVDS Display connector
- User Expansion connector
- PRU Header
- MCU Header

Copyright © 2026 Texas Instruments Incorporated

2.1.2 Functional Block Diagram (SK-AM62 and SK-AM62B)

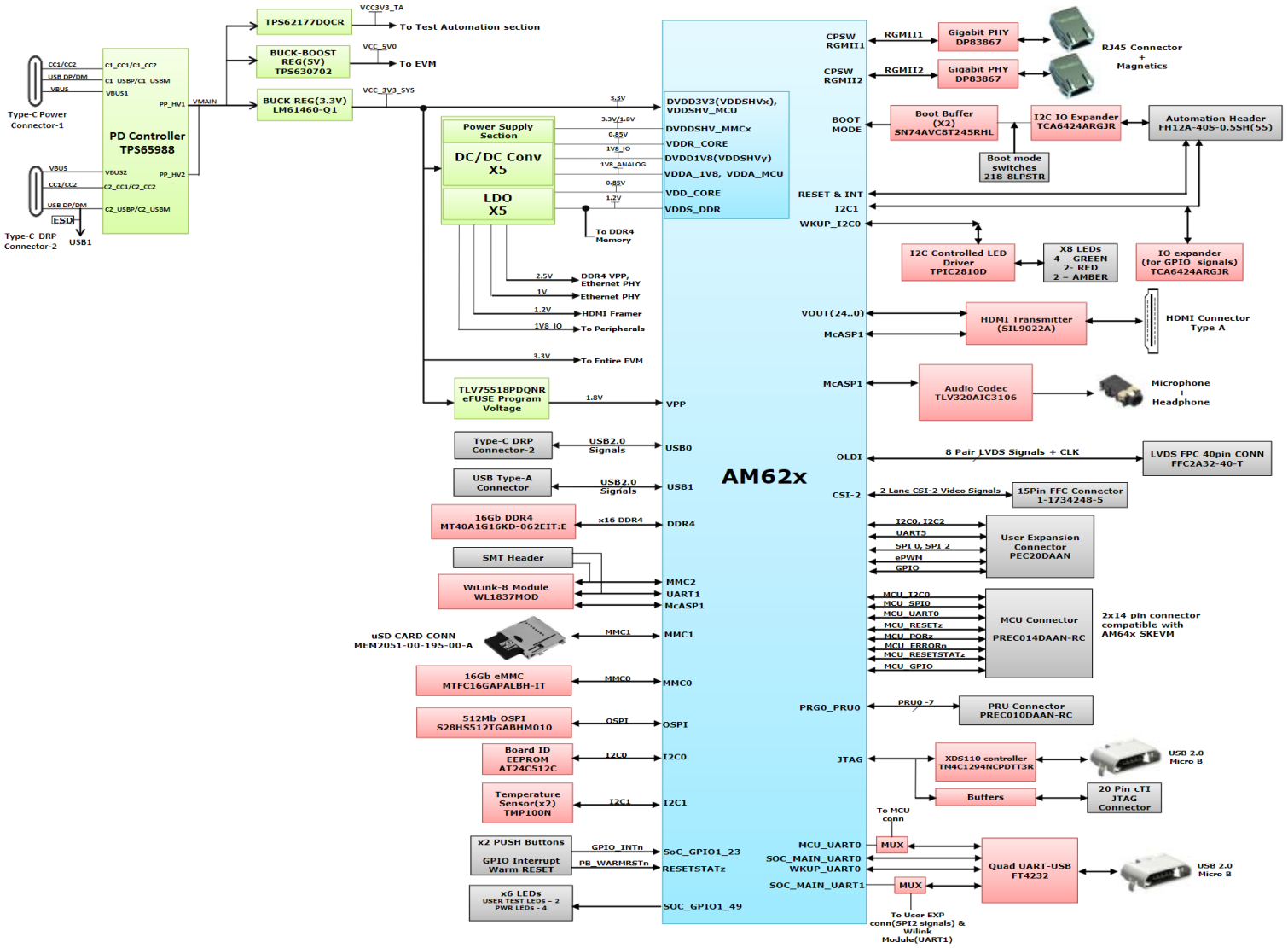


Figure 2-5. Functional Block Diagram of the SK-AM62 Board

Copyright © 2026 Texas Instruments Incorporated

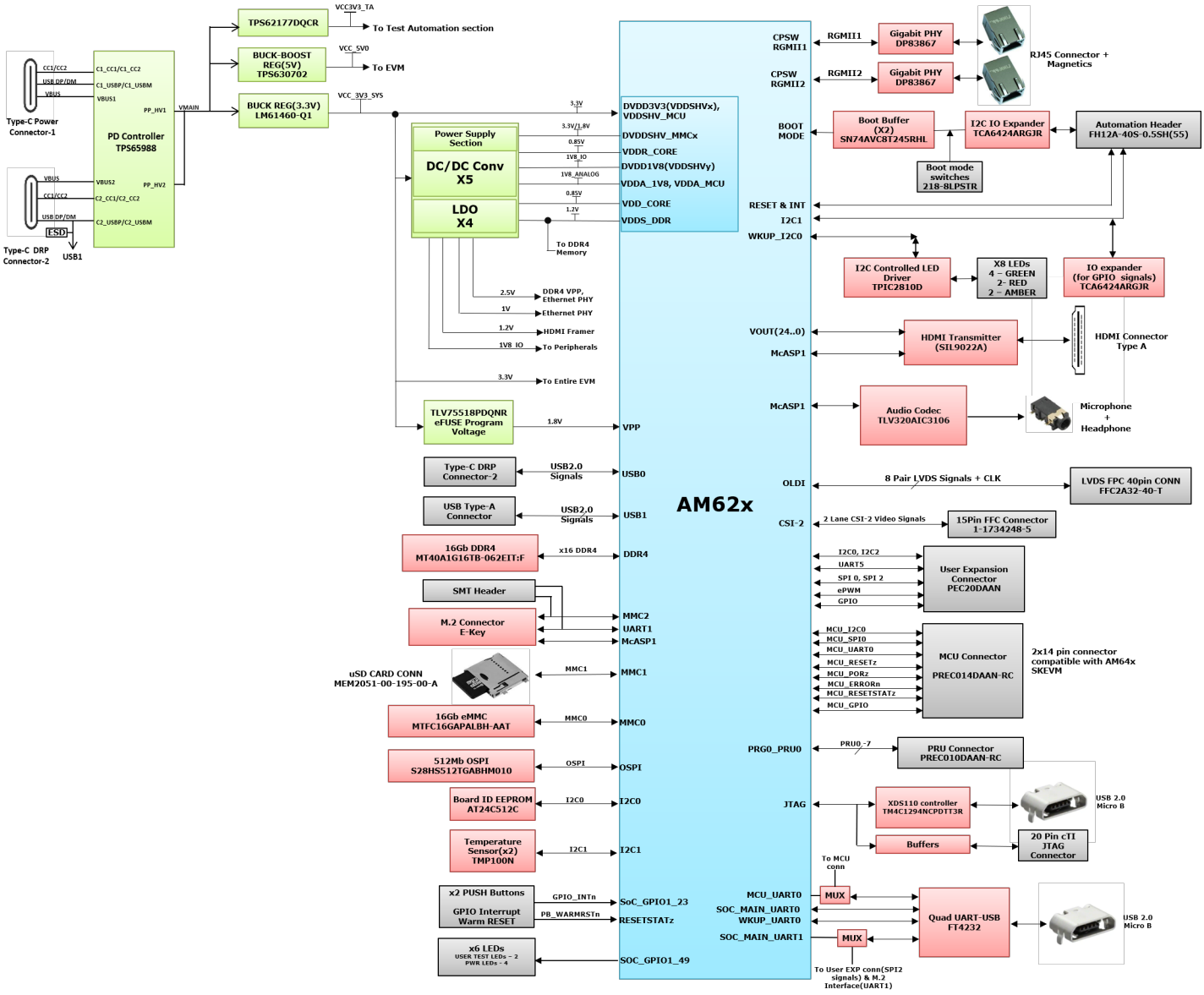


Figure 2-6. Functional Block Diagram of the SK-AM62B Board

Copyright © 2026 Texas Instruments Incorporated

2.1.3 Functional Block Diagram (SK-AM62-P1 and SK-AM62B-P1)

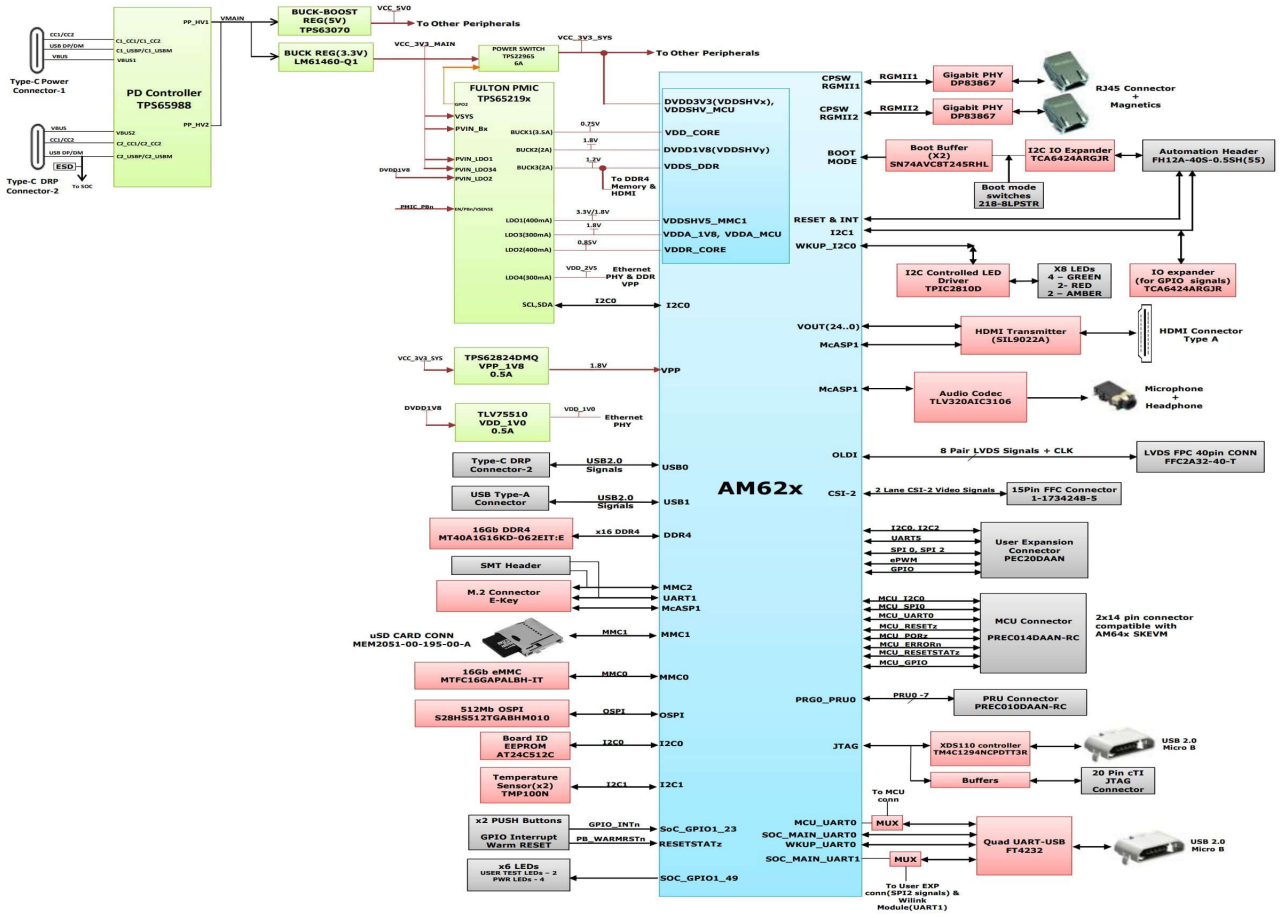


Figure 2-7. Functional Block Diagram of the SK-AM62-P1 Board with TPS65219 PMIC

Copyright © 2026 Texas Instruments Incorporated

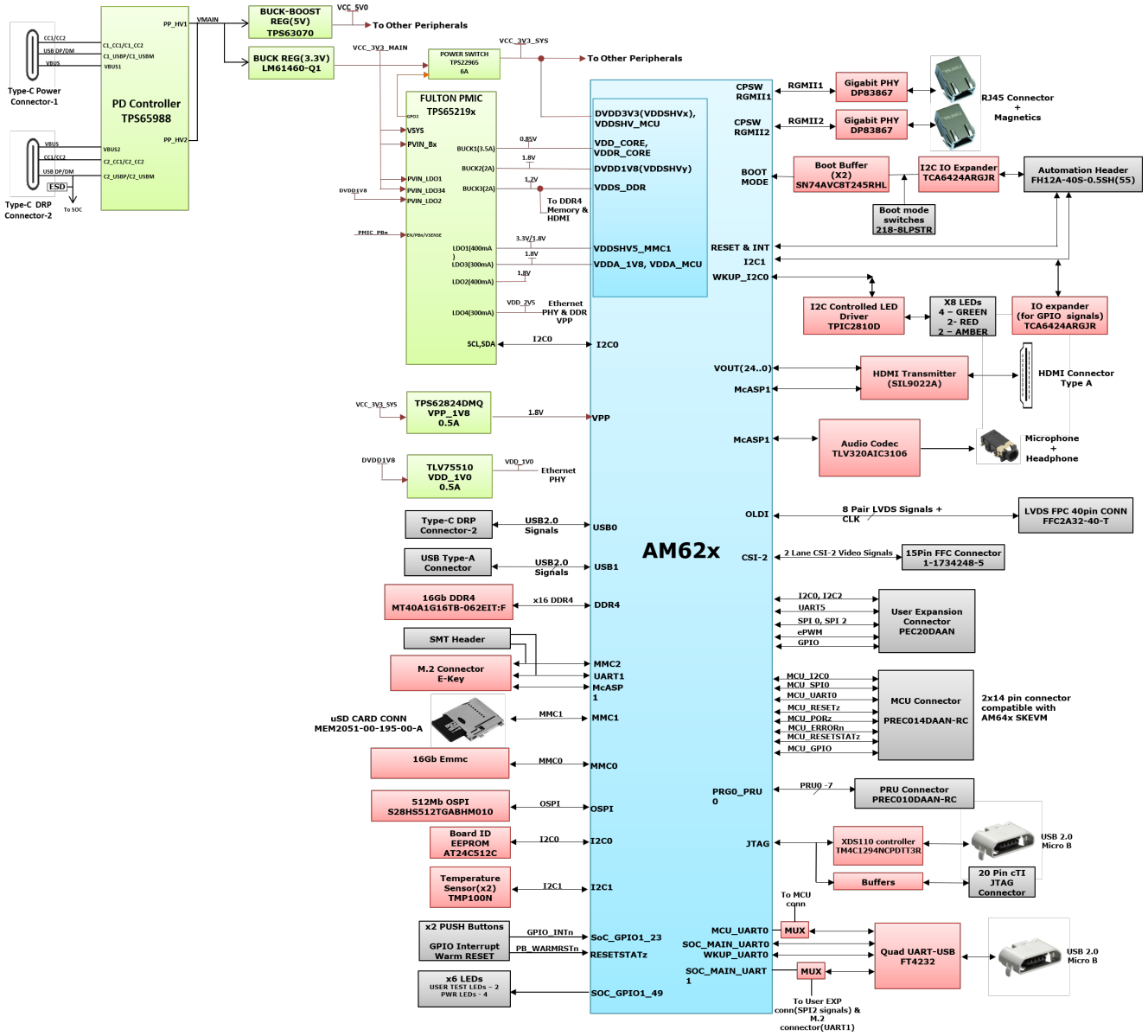


Figure 2-8. Functional Block Diagram of the SK-AM62B-P1 Board with TPS65219 PMIC

Copyright © 2026 Texas Instruments Incorporated

2.1.4 AM62x SKEVM Interface Mapping

Table 2-1 is provided below.

Table 2-1. Interface Mapping

Interface Name	Port on SoC	Device Part Number
Memory – DDR4	DDR0	MT40A1G16KD-062E:E
Memory – OSPI	OSPI0	S28HS512TGABHM010
Memory – Micro SD Socket	MMC1	MEM2051-00-195-00-A
Memory – eMMC	MMC0	MTFC16GAPALBH-IT
Memory – Board ID EEPROM	SoC_I2C0	AT24C512C-MAHM-T
Ethernet 1 – RGMII	SoC_RGMII1	DP83867IRRGZ
Ethernet 2 – RGMII	SoC_RGMII2	DP83867IRRGZ
LED Driver – 8 Communication LEDs	WKUP_I2C0	TPIC2810D
PRU Header – 2x10 HDR	PR0_PRU0_GPO and SoC_I2C0	PREC010DAAN-RC
User Expansion Connector – 2x20 HDR	SPI0, SPI2, UART5, SoC_I2C0, SoC_I2C2 and GPIOs	PEC20DAAN
MCU Header – 2x14 HDR	MCU_UART0, MCU_MCAN0, MCU_SPI0, MCU_I2C0 and MCU GPIOs	PREC014DAAN-RC
USB – 2.0 Type C	USB0	TUSB4020BIPHP + AU-Y1008-2
USB – 2.0 Type A	USB1	-
LVDS Display Connector	OLDI0	FFC2A32-40-T
CSI Interface	CSI0	1-1734248-5
HDMI	VOUT0	SiI9022ACNU + TPD12S016PWR + 10029449-001RLF
Audio Codec	McASP2 and SoC_I2C1	TLV320AIC3106IRGZT + SJ-43514-SMT
GPIO Port Expander	SoC_I2C1	TCA6424ARGJR
UART Terminal (UART-to-USB)	SoC_UART [1:0], WKUP_UART0 and MCU_UART0	FT4232HL + 629105150521
Test Automation Header	SoC_I2C1	FH12A-40S-0.5SH
Temperature Sensors	SoC_I2C1	TMP100NA/3K
Current Monitors	SoC_I2C1	INA231AIYFDR
Connectivity – Wilink Module	MMC2, McASP2 and SoC_UART2	WL1837MODGIMOCT

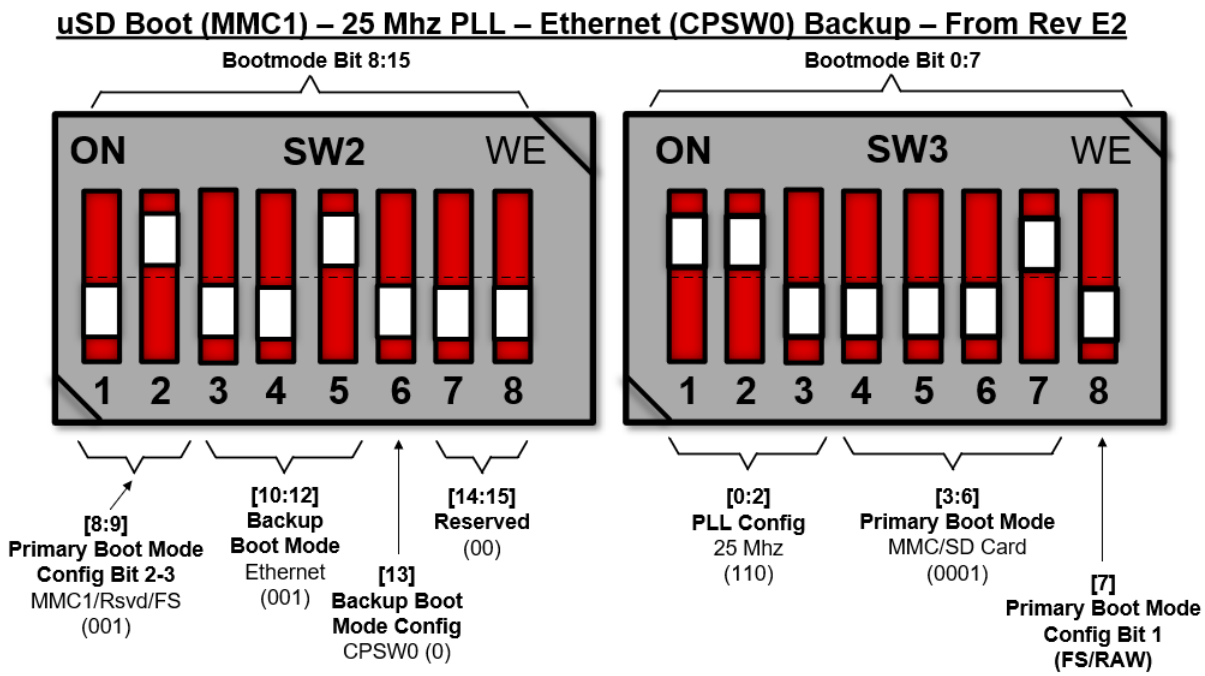
2.1.5 Power ON/OFF Procedures

Power to the EVM is provided through an external power supply providing PD voltage and current to the either of the two USB Type-C Ports.

2.1.5.1 Power-On Procedure

1. Place the SKEVM boot switch selectors (SW1, SW2) into selected boot mode. Example boot-modes for SD card and no-boot are shown below.
2. Connect your boot media (if applicable).
3. Attach the PD capable USB Type-C cable to the SKEVM Type-C (J11 or J13) Connector.
4. Connect the other end of the Type-C cable to the source, either AC Power Adapter, or Type C source device (such as a Laptop computer).
5. Visually inspect that either LD10 or LD12 LED are illuminated.
6. XDS110 JTAG and UART debug console output are routed to micro-USB ports J16 and J15, respectively.

Copyright © 2026 Texas Instruments Incorporated



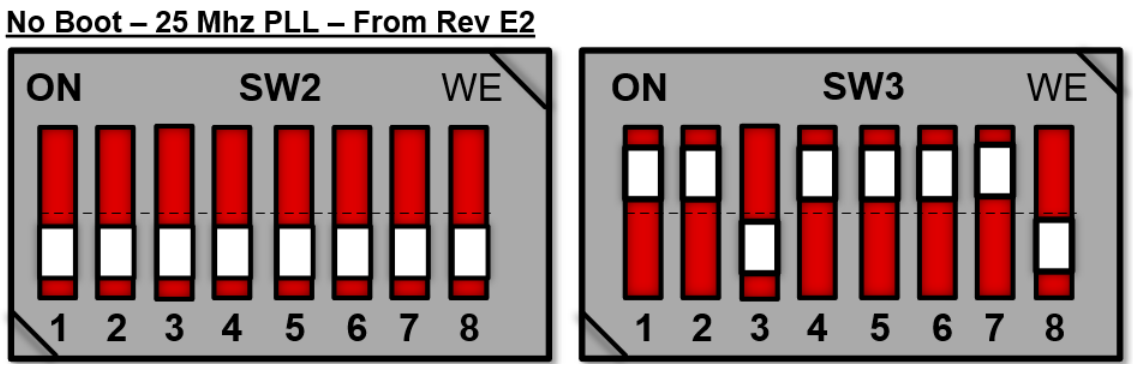


Figure 2-9. SD Bootmode Switch Setting Example (From E2)

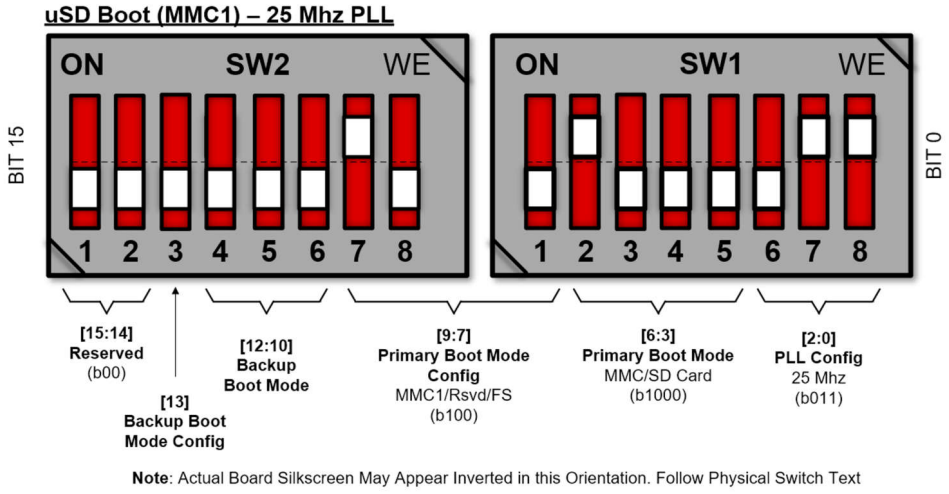


Figure 2-10. SD Bootmode Switch Setting Example (E1)

2.1.5.2 Power-Off Procedure

1. Disconnect AC power from AC/DC converter.

Copyright © 2026 Texas Instruments Incorporated

2. Remove the USB Type-C cable from the SKEVM.

2.1.5.3 Power Test Points

Test points for each power output on the board is mentioned in Table 2-2.

Table 2-2. Power Test Points

Sl #	Power Supply	Test Point	Voltage
1	VBUS_TYPEC1	C398.1	5V-15V
2	VBUS_TYPEC2	C415	5V-15V
3	VMAIN	TP95	5V-15V
4	VCC_5V0	TP70	5V
5	VCC_3V3_SYS	TP51	3.3V
6	VDD_2V5	TP42	2.5V
7	VPP_1V8	TP31	1.8V
8	VDD_1V0	TP33	1.0V
9	VDD_1V1	TP44	1.1V
10	VDD_1V2	TP10	1.2V
11	VDDA1V8	TP36	1.8V
12	VCC_1V8	TP41	1.8V
13	VDDSHV_SDIO	TP29	1.8V/3.3V
14	VCC1V2_DDR	TP40	1.2V
15	VCC_CORE	TP45	0.85V
16	VDD_CORE	TP46	0.85V
17	VCC_0V85	TP39	0.85V
18	VDDR_CORE	TP38	0.85V
19	DDR_VREFCA	TP43	0.6V
20	VCC3V3_TA	TP87	3.3V
21	VCC3V3_XDS	TP77	3.3V
22	VCC_3V3_FT4232	C482.1	3.3V

2.1.6 Peripheral and Major Component Description

The following sections provide an overview of the different interfaces and circuits on the AM62x SK EVM.

2.1.6.1 Clocking

Figure 2-11 shows the clock architecture of AM62x SKEVM.

Copyright © 2026 Texas Instruments Incorporated

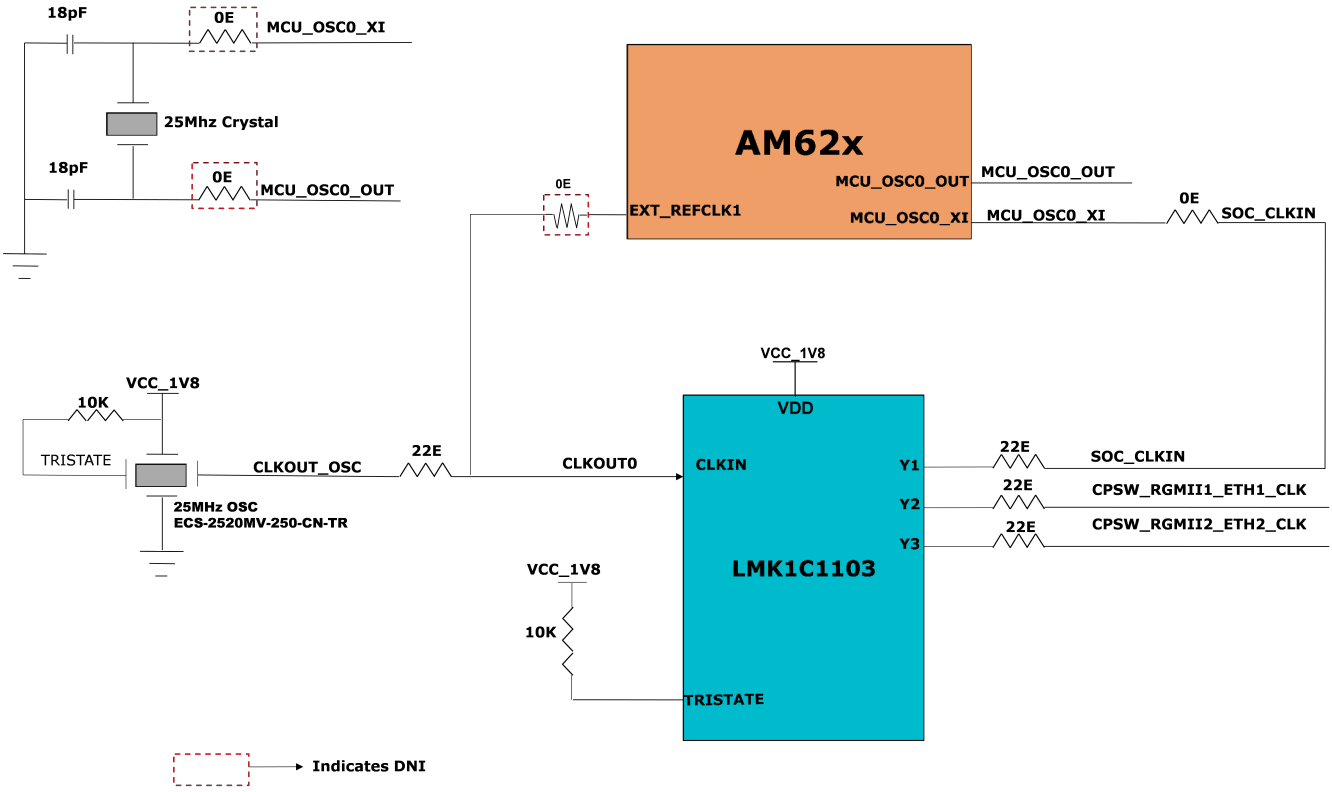


Figure 2-11. Clock Architecture of AM62x SKEVM

A clock generator of part number LMK1C1103PWR is used to drive the 25 MHz clock to the SoC and two Ethernet PHYs. LMK1C1103PWR is a 1:4 LVCMOS clock buffer, which takes the 25 MHz crystal/LVCMOS reference input and provides three 25 MHz LVCMOS clock outputs. The source for the clock buffer shall be either the CLKOUT0 pin from the SoC or a 25 MHz oscillator, the selection is made using a set of resistors. By default, an oscillator is used as input to the clock buffer on the AM62x SKEVM. Output Y2 and Y3 of the clock buffer are used as reference clock inputs] for two Gigabit Ethernet PHYs.

There is one external crystal attached to the AM62x SoC to provide clock to the WKUP domain of the SoC (32.768 KHz).

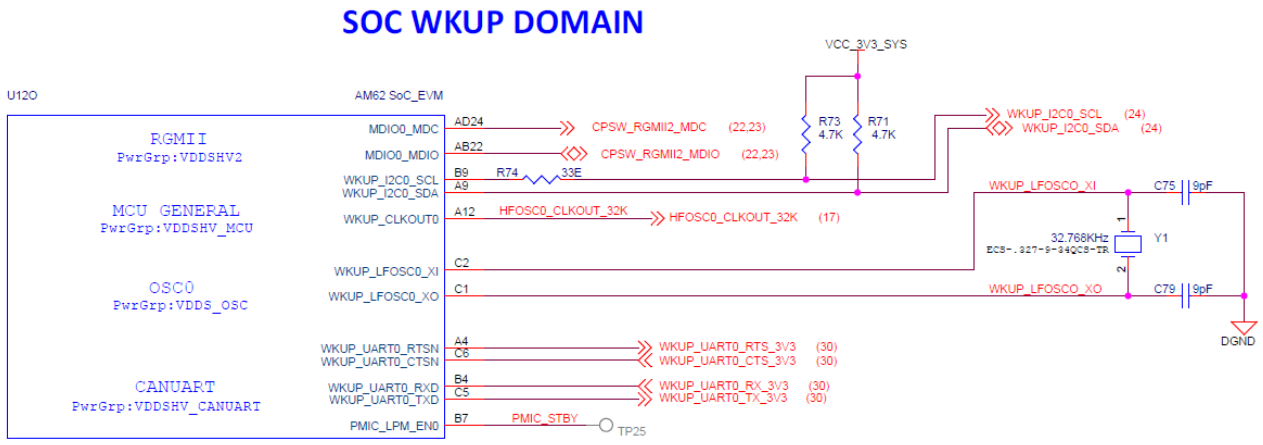


Figure 2-12. SoC WKUP Domain

Copyright © 2026 Texas Instruments Incorporated

2.1.6.1.1 Peripheral Ref Clock

Clock inputs required for peripherals such as XDS110, USB HUB, FT4232, HDMI Transmitter and Audio Codec are generated locally using separate crystals or oscillators. Crystals or Oscillators used to provide the reference clocks to the EVM peripherals are shown in the table bellow.

Table 2-3. Clock Table

Peripheral	Mfr. Part No.	Description	Frequency
XDS110 emulator	ECS-.327-9-34QCS-TR	CRY 32.768 KHz 9pF SMD	32.768 KHz
FT4232 Bridge	ECS-120-18-30B-AGN-TR	CRY 12.000 MHz 18pF SMD	12.000 MHz
Audio Codec	KC2520Z12.2880C1KX00	OSC 12.288 MHz CMOS SMD	12.288 MHz
USB HUB (E1 Only)	ECS-240-20-30B-AGL-TR	CRY 24.000 MHz 20pF SMD	24.000 MHz
HDMI Transmitter	KC2520Z12.2880C1KX00	OSC 12.288 MHz CMOS SMD	12.288 MHz

The clock required by the HDMI Transmitter can be provided by either the on board oscillator or the SoC's AUDIO_EXT_REFCLK1, which can be selected through a resistor mux. SoC's EXT_REFCLK1 is used to provide clock to the User Expansion Connector on the SKEVM. The 32 KHz clock to the Wilink module is provided by WKUP_CLKOUT0 of AM62x SoC through a voltage translational buffer.

2.1.6.2 Reset

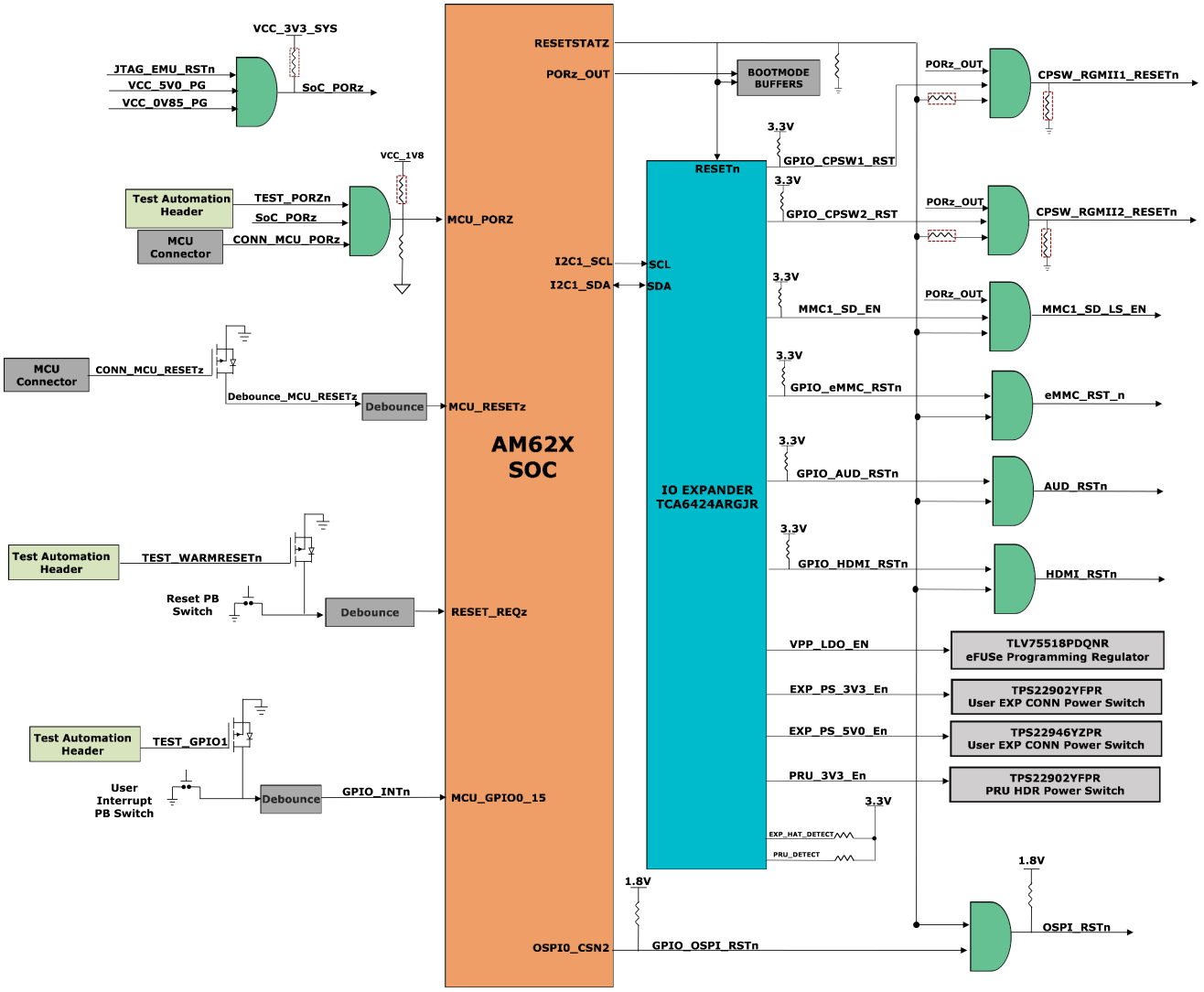
The Reset Architecture of AM62x SKEVM is shown below.

The SoC has the following resets:

- RESETSTATz is the Main domain warm reset status output
- PORz_OUT is the Main domain power ON reset status output
- RESET_REQz is the Main domain warm reset input
- MCU_PORz is the MCU domain power ON/ Cold Reset input
- MCU_RESETz is the MCU domain warm reset input
- MCU_RESETSTATz is the MCU domain warm reset status output

Upon Power on Reset, all peripheral devices connected to the main domain get reset by RESETSTATz.

Copyright © 2026 Texas Instruments Incorporated



2.1.6.3 OLDI Display Interface

The OLDI0 Display interface of the AM62x SoC is connected to a 40 pin LVDS display connector (J21) Mfr Part# FFC2A32-40-T from GCT. The OLDI Interface supports dual channel 8 bit LVDS output.The pinout and connector orientation is common between E1 and E2 boards but differs from the future 'final' E3 boards. Adapters are available to update the E1/E2 wiring to E3. Do not attempt to connect a display designed for E3 EVMs to the E1/E2 EVM without this adapter.

The Pin-out details of the Display connector are given in Table 2-5.

Table 2-4. Display Connector Pinout (As used by display and the E3 EVM)

Pin no.	Signal	Pin no.	Signal
1	VCC_3V3_SYS(EEPROM_VDD)	21	CH1_LVDS_A2P
2	SoC_I2C0_SCL	22	GND
3	SoC_I2C0_SDA	23	CH1_LVDS_A3N
4	NC	24	CH1_LVDS_A3P
5	NC	25	GND
6	GND	26	CH1_LVDS_A0N
7	GND	27	CH2_LVDS_A0P
8	OLDI_RESETn	28	GND
9	TS_INT#	29	CH2_LVDS_A1N
10	GND	30	CH2_LVDS_A1P

Copyright © 2026 Texas Instruments Incorporated

Table 2-4. Display Connector Pinout (As used by display and the E3 EVM) (continued)

Pin no.	Signal	Pin no.	Signal
11	CH1_LVDS_A0N	31	GND
12	CH1_LVDS_A0P	32	CH2_LVDS_CLKN
13	GND	33	CH2_LVDS_CLKP
14	CH1_LVDS_A1N	34	GND
15	CH1_LVDS_A1P	35	CH2_LVDS_A2N
16	GND	36	CH2_LVDS_A2P
17	CH1_LVDS_CLKN	37	GND
18	CH1_LVDS_CLKP	38	CH2_LVDS_A3N
19	GND	39	CH2_LVDS_A3P
20	CH1_LVDS_A2N	40	GND

Table 2-5. Display Connector Pinout (E1/E2)

Pin no.	Signal	Pin no.	Signal
40	VCC_3V3_SYS(EEPROM_VDD)	20	CH1_LVDS_A2P
39	GND	19	GND
38	SoC_I2C0_SCL	18	GND
37	SoC_I2C0_SDA	17	CH1_LVDS_A3N
36	NC	16	CH2_LVDS_A0N
35	NC	15	CH1_LVDS_A3P
34	NC	14	CH2_LVDS_A0P
33	TS_INT	13	GND
32	TS_RST	12	GND
31	GND	11	CH2_LVDS_A1N
30	GND	10	CH2_LVDS_CLKN
29	CH1_LVDS_A0N	9	CH2_LVDS_A1P
28	CH1_LVDS_A1N	8	CH2_LVDS_CLKP
27	CH1_LVDS_A0P	7	GND
26	CH1_LVDS_A1P	6	GND
25	GND	5	CH2_LVDS_A2N
24	GND	4	CH2_LVDS_A3N
23	CH1_LVDS_CLKN	3	CH2_LVDS_A2P
22	CH1_LVDS_A2N	2	CH2_LVDS_A3P
21	CH1_LVDS_CLKP	1	GND

2.1.6.4 CSI Interface

The CSI-2 interface from the AM62x SoC is terminated to a 15 pin Camera FPC connector 1-1734248-5 compatible with the RPi Camera Modules. These modules support 2 Lane CSI RX signals. While the SoC supports 4 CSI RX Lanes, only two are pinned out on the SKEVM

The CSI connector pin-out is compatible with the RPi camera connector. The Table 2-6 contains 15 pin CSI Connector pin-out. SoC I2C1 signals are also connected to the CSI Header. IO Expander GPIO signals are connected to the camera GPIO's.

Copyright © 2026 Texas Instruments Incorporated

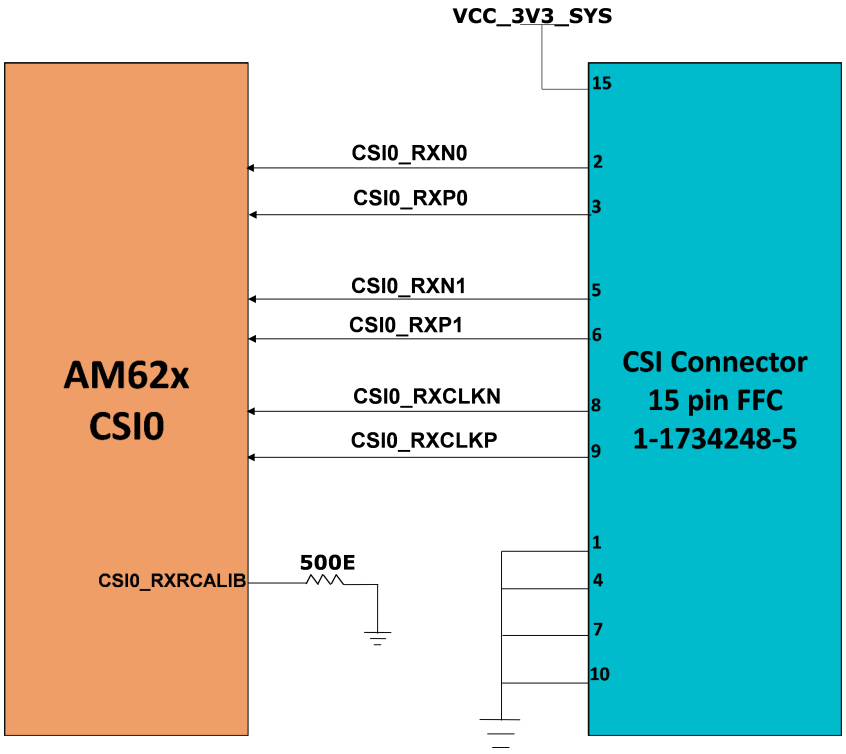


Table 2-6. CSI Camera Connector J19 Pin-out

Pin No	Pin Description
1	Ground
2	CSI0_RXN0
3	CSI0_RXP0
4	Ground
5	CSI0_RXN1
6	CSI0_RXP1
7	Ground
8	CSI0_RXCLKN
9	CSI0_RXCLKP
10	Ground
11	CSI_GPIO1
12	CSI_GPIO2
13	SoC_I2C1_SCL
14	SoC_I2C1_SDA
15	VCC_3V3_SYS

2.1.6.5 Audio Codec Interface

AM62x SKEVM has TI‘s Low-Power TLV320AIC3106 Stereo Audio Codec to interface with AM62x via McASP.

TLV320AIC3106 is a low-power stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single ended or fully differential configurations. The record path of the TLV320AIC3106 contains integrated microphone bias, digitally controlled stereo microphone preamplifier and automatic gain control (AGC) with mix/Mux capability among the multiple analog inputs. The stereo audio DAC supports sampling rates from 8 kHz to 96 kHz.

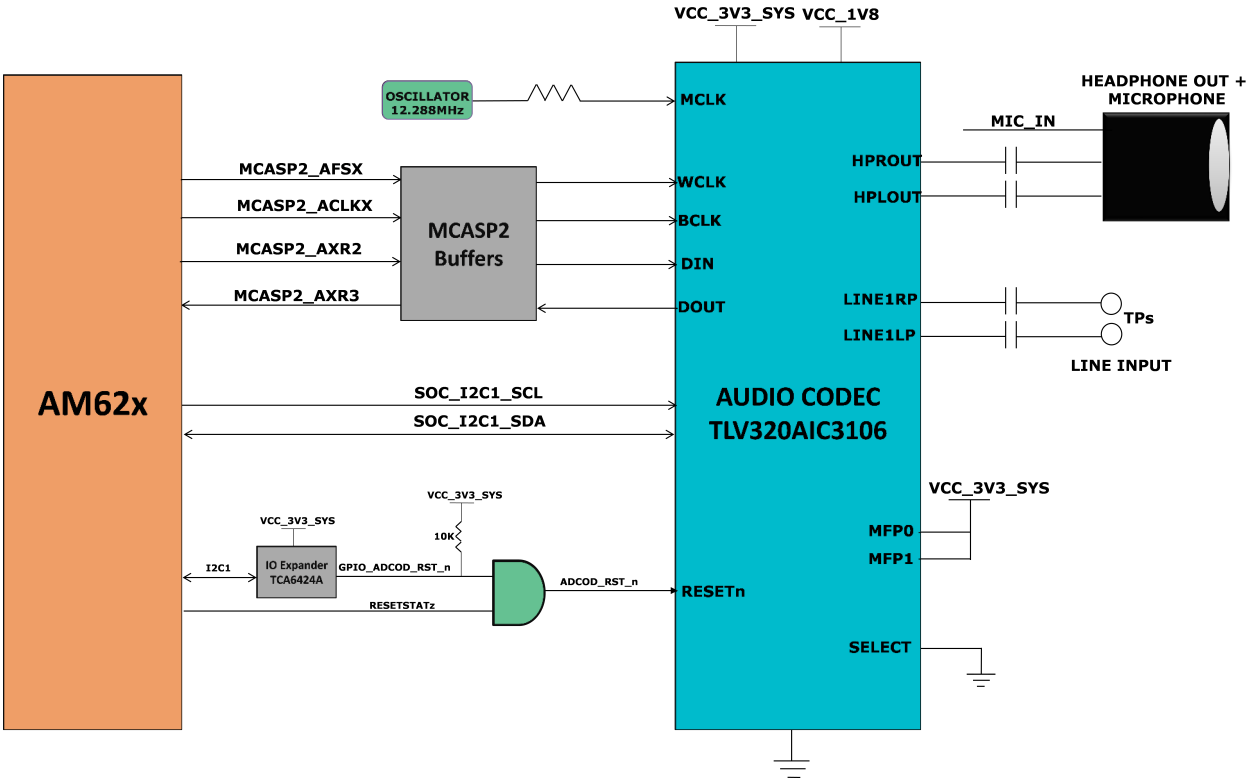
1x Standard 3.5 mm TRRS Audio Jack connector Mfr. Part# SJ-43514 shall be provided for MIC and Headphone output. Audio Codec’s Line inputs are terminated to Testpoints.

Copyright © 2026 Texas Instruments Incorporated

SELECT pin shall be held LOW to select I2C as control interface. Codec can be configured over I2C interface, where I2C address can be set by driving pins MFP0 and MFP1 pin either high or low. Both these pins are set to high, so the Device address is set to 0x1B. Unused inputs and outputs of the Audio Codec are connected to ground.

The Controller Clock input, MCLK to the Audio Codec is provided through a 12.288MHz Oscillator. Audio serial data bus bit clock BCLK of \the codec is driven by the AM62x SoC through a buffer. Audio serial data bus input and output DIN, DOUT are connected to SoC's MCASP2_AXR2 and MCASP2_AXR3 through buffers. An AND output of RESETSTATz and a GPIO sourced via IO expander are used to reset the Audio codec.

The TLV320AIC3106 is powred by an analog supply of 3.3 V, a digital core supply of 1.8 V, and a digital I/O supply 3.3 V.



2.1.6.6 HDMI Display Interface

The DSS (Display Sub system) interface from AM62x SoC is used on the SKEVM to provide a HDMI Interface through a standard Type-A Connector. The SKEVM features a SiI9022A HDMI Transmitter from Lattice semiconductors to convert the 24bit Parallel RGB DSS output stream as well as a McASP to a HDMI-compliant digital audio and video signal.

The Data mapping format used is RGB888. The data bus width is 24-bits.

SoC_I2C1 is connected to the HDMI Transmitter to access the compatible mode registers, the TPI registers, and the CPI registers. In order to use the SiI9022A, the SoC needs to setup the device. This is done via the I2C interface between the SoC and the SiI9022A. Audio Data is sent from SoC to HDMI transmitter through the McASP1 instance. HDMI_I2C Bus accesses the EDID and HDCP data on an attached sink device.

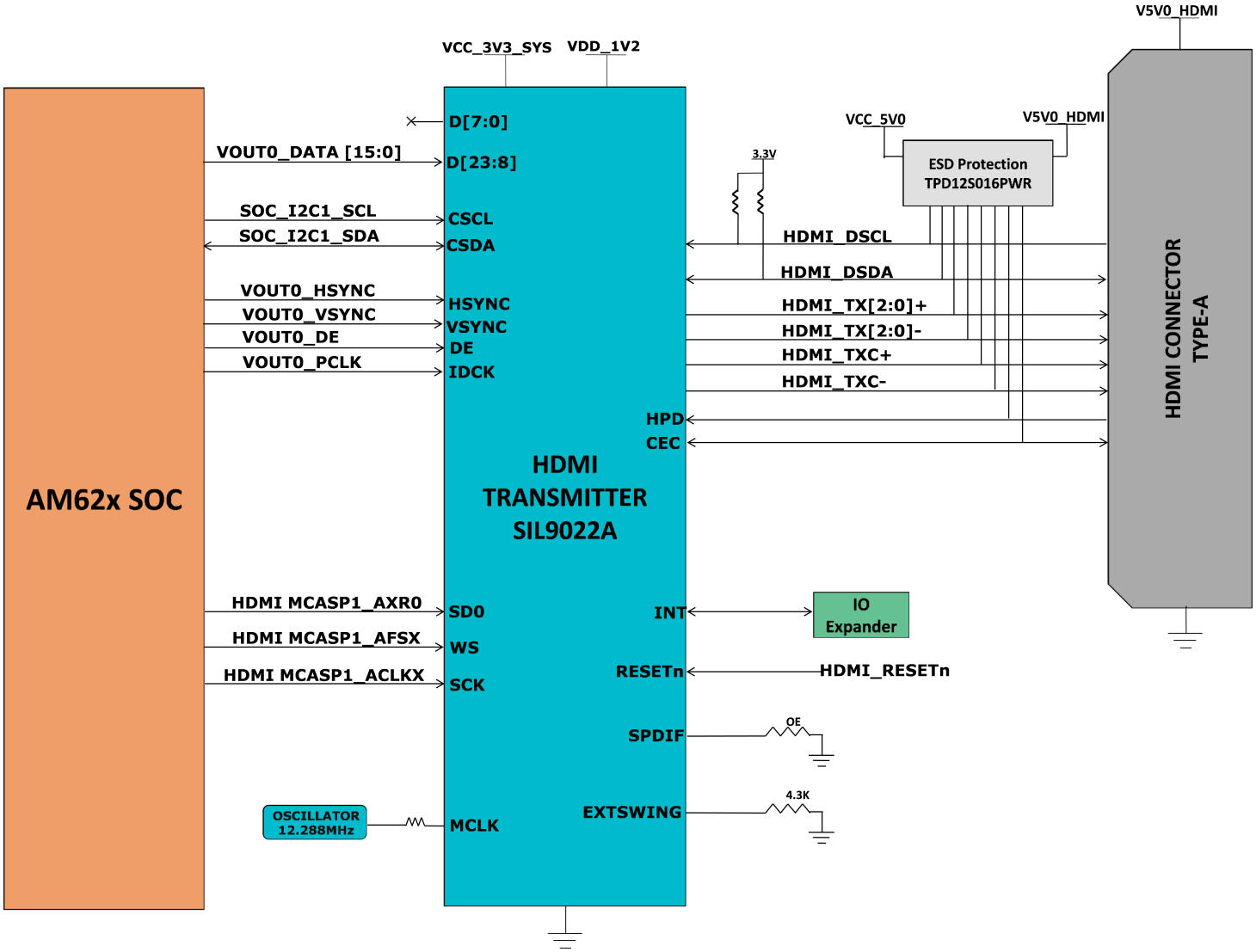
TMDS Differential data pairs along with the differential clock signals from the transmitter are connected to the HDMI connector through HDMI ESD device Mfr Part# TPD12S016PWR which also acts as a load switch to limit current supplied to the HDMI connector from board 5 V supply.

The HDMI Framer is powered using 3.3 V Board IO Supply and 1.2 V by a dedicated LDO Mfr Part# TLV75512PDQNR.

Copyright © 2026 Texas Instruments Incorporated

Note

Please see the Known Issues section of this document. The SK-AM62 E1 board was intended to feature 16bit YUV 422 video output but was wired incorrectly. E2 and newer variants of SK-AM62 as well as all variants of SK-AM62-P1 feature the full 24 bit Parallel RGB888 Interface.

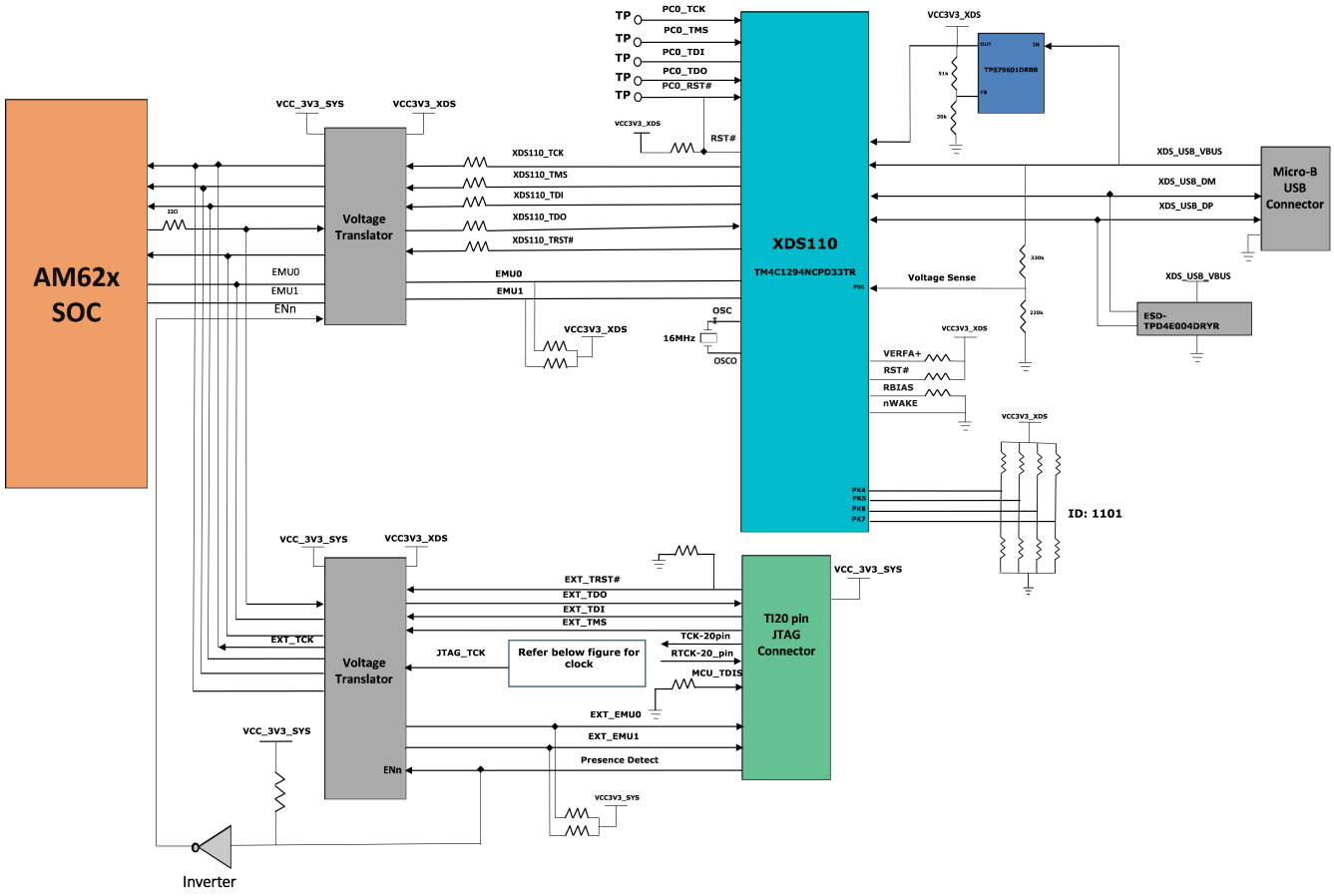


2.1.6.7 JTAG Interface

AM62x SKEVM board include XDS110 class on board emulation. The connection for the emulator uses an USB 2.0 micro-B connector and the circuit acts as a Bus powered USB device. The VBUS power from the connector will be used to power the emulation circuit such that connection to the emulator is not lost when the power to the SKEVM is removed. Voltage translation buffers are used to isolate the XDS110 circuit from the rest of the SKEVM.

Optionally, JTAG Interface on SKEVM is also provided through 20 Pin Standard JTAG cTI Header J17. This allows the user to connect an external JTAG Emulator Cable. Voltage translation buffers are used to isolate the JTAG signals from cTI header from the rest of the SKEVM. The output from the voltage translators from XDS110 Section and cTI Header Section are muxed and connected to AM62x JTAG Interface. If a connection to the cTI 20 Pin JTAG connector is sensed using a presence detect circuit, the mux will be set to route the 20 pin signals from the cTI connector to the AM62x SoC in place of the on-board emulation circuit.

Copyright © 2026 Texas Instruments Incorporated



The pin-outs of the cTI 20 pin JTAG connector are given in Table 2-7. A ESD protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ±15-kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8-kV contact discharge and ±12- kV air-gap discharge.

Table 2-7. JTAG Connector (J17) Pin-out

Pin No.	Signal
1	JTAG_TMS
2	JTAG_TRST#
3	JTAG_TDI
4	JTAG_TDIS
5	VCC3V3_SYS
6	NC
7	JTAG_TDO
8	SEL_XDS110_INV
9	JTAG_cTI_RTCK
10	DGND
11	JTAG_cTI_TCK
12	DGND
13	JTAG_EMU0
14	JTAG_EMU1
15	JTAG_EMU_RSTn

Copyright © 2026 Texas Instruments Incorporated

Table 2-7. JTAG Connector (J17) Pin-out (continued)

Pin No.	Signal
16	DGND
17	NC
18	NC
19	NC
20	DGND

2.1.6.8 Test Automation Header

AM62x SKEVM has a 40 pin test automation header (FH12A-40S-0.5SH) to allow an external controller to manipulate some basic operations like Power Down, POR, Warm Reset, Boot Mode control, and so forth.

The Test Automation Circuit is powered by the 3.3 V supply generated by a dedicated regulator Mfr. Part# TPS62177DQCR. The SoC's I2C1 is connected to the test automation header. Another I2C instance (BOOTMODE_I2C) from the Test Automation Header is connected to the 24-bit I2C boot mode IO Expander of Mfr. Part# TCA6424ARGJR to allow control of the boot modes for the AM62x SoC.

The test automation circuit has voltage translation circuits so that the controller is isolated from the IO voltages used by the AM62x. Boot mode for the AM62x must be controlled by either the user using DIP Switches or the test automation header through the I2C IO Expander. Boot Mode Buffers are used to isolate the Boot Mode controls driven through DIP Switches or I2C IO Expander. The boot mode is controlled by the user using two 8-bit DIP switches on the board, which will connect a pull-up resistor to the output of a buffer when the switch is set to the ON position and to weaker pull-down resistor when set to the OFF position. The output of the buffer is connected to the boot mode pins on the AM62x SoC and the output is enabled when the boot mode is needed during a reset cycle.

When boot mode is to be set through Test Automation header, the required switch values are set at the I2C IO expander output, which overwrites the DIP switch values to give the desired boot values to the SoC. The pins used for boot mode also have other functions which will be isolated by disabling the boot mode buffer during normal operation.

The power down signal from the Test automation header instructs the SKEVM to power down all the rails except for dedicated power supplies on the board. Similarly PORZn signal is also provided to give a hard reset to the SoC and WARM_RESETn for warm reset of the SoC. One Interrupt signal from the Test Automation header is going to the SoC GPIO (MCU_GPIO0_15) for providing an external Interrupt.

Copyright © 2026 Texas Instruments Incorporated

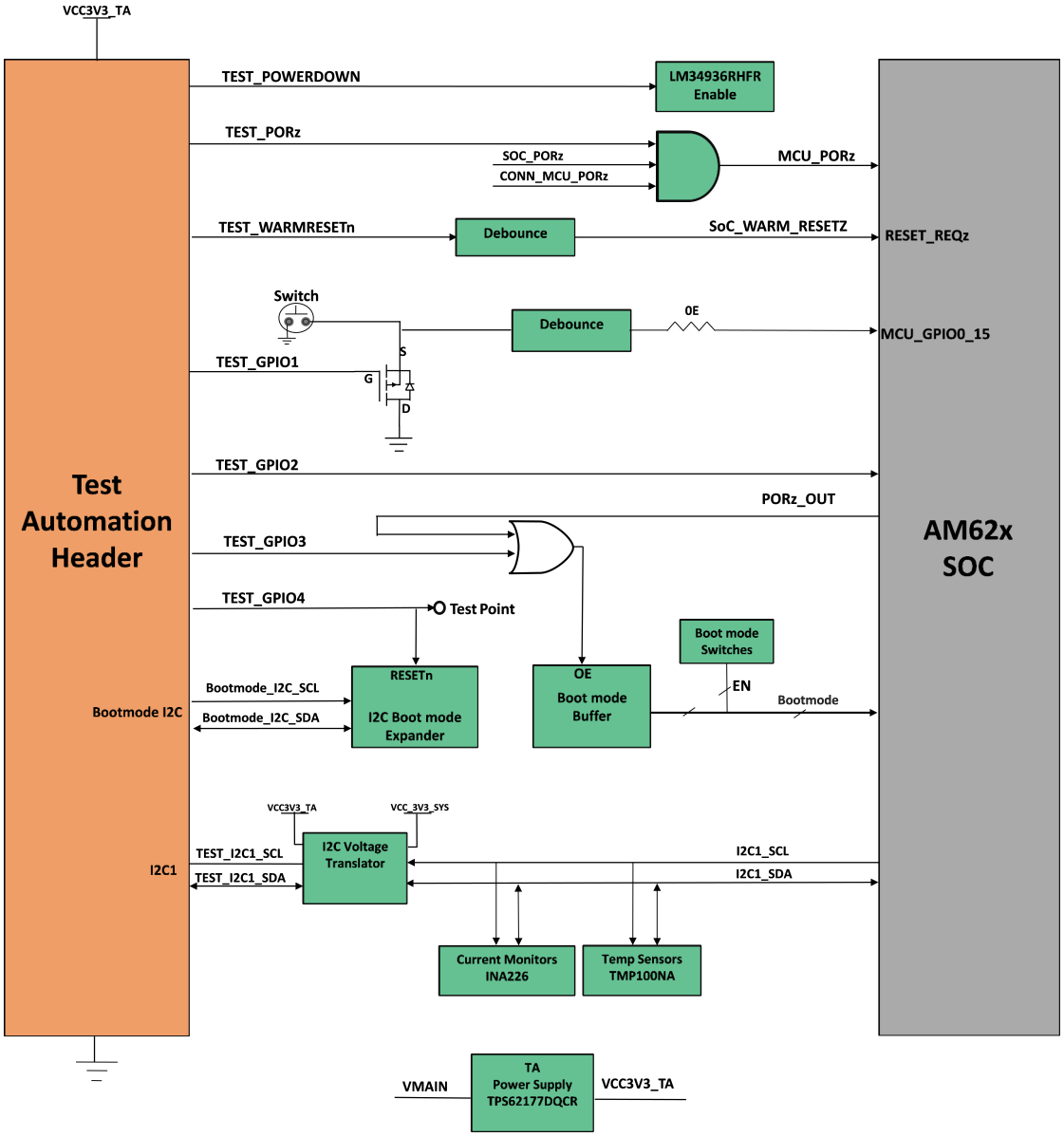


Table 2-8. Test Automation Connector (J23) Pin-out

Pin No.	Signal	IO Direction	Pin No.	Signal	IO Direction
1	VCC3V3_TA	Power	21	NC	NA
2	VCC3V3_TA	Power	22	NC	NA
3	VCC3V3_TA	Power	23	NC	NA
4	NC	NA	24	NC	NA
5	NC	NA	25	DGND	Power
6	NC	NA	26	TEST_POWERDOWN	Input
7	DGND	Power	27	TEST_PORZn	Input
8	NC	NA	28	TEST_WARMRESETn	Input
9	NC	NA	29	NC	NA
10	NC	NA	30	TEST_GPIO1	Bidirectional
11	NC	NA	31	TEST_GPIO2	Bidirectional
12	NC	NA	32	TEST_GPIO3	Input
13	NC	NA	33	TEST_GPIO4	Input

Copyright © 2026 Texas Instruments Incorporated

Table 2-8. Test Automation Connector (J23) Pin-out (continued)

Pin No.	Signal	IO Direction	Pin No.	Signal	IO Direction
14	NC	NA	34	DGND	Power
15	NC	NA	35	NC	NA
16	DGND	Power	36	SoC_I2C1_TA_SCL	Bidirectional
17	NC	NA	37	BOOTMODE_I2C_SCL	Bidirectional
18	NC	NA	38	SoC_I2C1_TA_SDA	Bidirectional
19	NC	NA	39	BOOTMODE_I2C_SDA	Bidirectional
20	NC	NA	40	DGND	Power

2.1.6.9 UART Interface

The four UART ports of the SoC (MCU UART0, WKUP UART0, SoC UART0 and SoC UART1) provided by the AM62x are interfaced with an FTDI FT4232HL for UART-to-USB functionality and terminated on a USB micro-B connector (J15) on board. When the AM62X SKEVM is connected to a Host using USB cable, the computer can establish a Virtual Com Port which can be used with any terminal emulation application. The FT4232HL is bus powered.

Since the circuit is powered through BUS power, the connection to the COM port will not be lost when the SKEVM power is removed.

Table 2-9. UART Port Interface

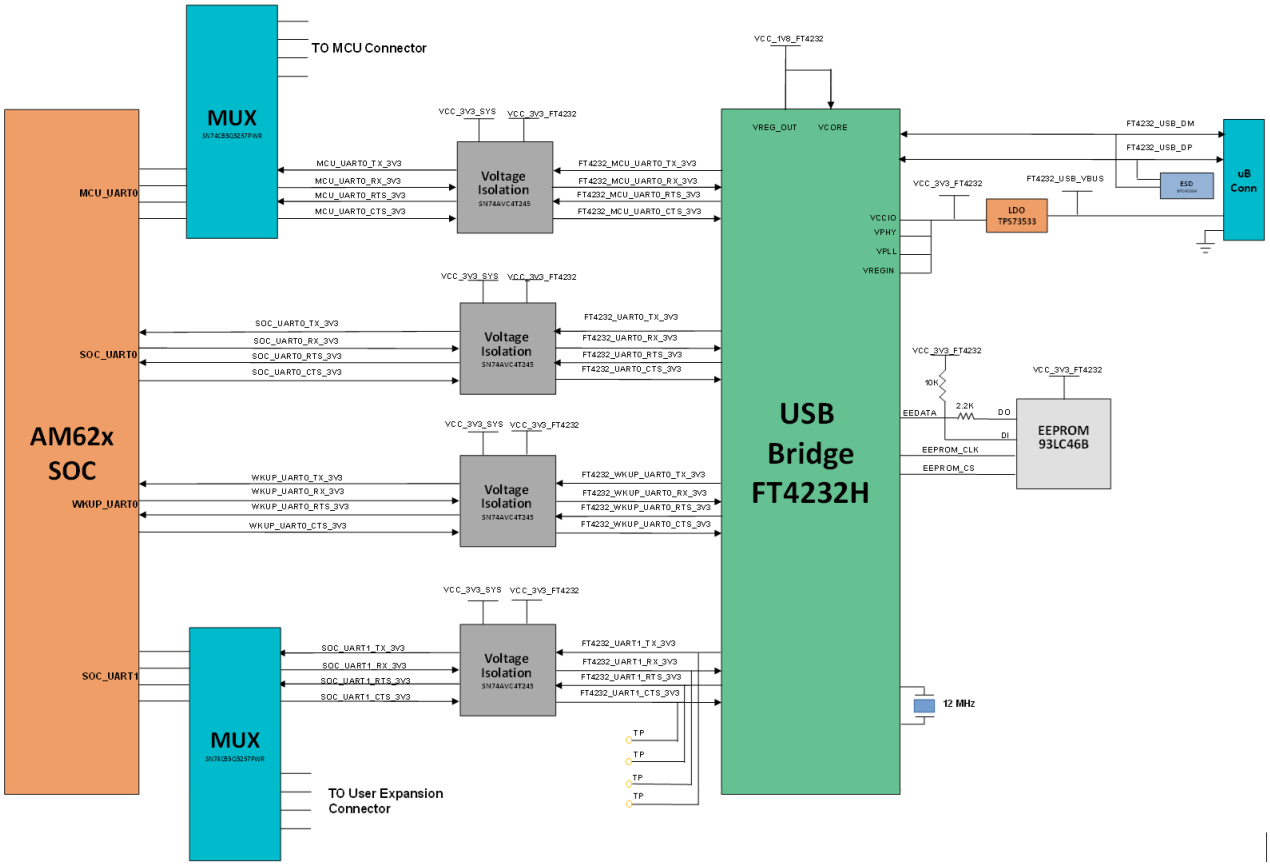
UART Port	USB to UART Bridge	USB Connector	COM Port
SoC_UART0	FT4232HL	J15	COM1
SoC_UART1			COM2
WKUP_UART0			COM3
MCU_UART0			COM4

The FT4232 chip is configured to operate in ‘Single chip USB to four channel UART’ mode and will take the configuration file from the external SPI EEPROM connected to it. The EEPROM (93LC46B) supports 1Mbit/s clock rate. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from FTDI's web site. The FT_PROG is also used for programming the board serial number for users to identify the connected COM port with board serial number when one or more boards are connected to the computer.

Note

Starting with version E2 of the SK-AM62 EVM (and all revisions of SK-AM62-P1), SoC UART0 is no longer connected for Hardware Flow Control as the CTS/RTS pins were re-purposed for other uses. Additionally, UART1 is selectable between the Expansion Connector, the FT4232 (Default) or the Wilink Bluetooth UART.

Copyright © 2026 Texas Instruments Incorporated



2.1.6.10 USB Interface

2.1.6.10.1 USB 2.0 Type A Interface

The USB 2.0 HOST Interface is offered through a USB Type-A Port on the USB1 controller on the AM62x SoC.

The USB Signals are connected on E1 to a USB 2.0 HUB Mfr Part# TUSB4020BI to provide two USB 2.0 Host ports. TUSB4020BI is a two port USB 2.0 HUB, which provides USB high-speed/full-speed connections on the upstream port and provides USB high-speed, full-speed, or low-speed connections on the downstream ports. On-chip 24 MHz crystal is used to provide clock to the USB HUB. USB0_DRVVBUS from SoC is connected to USB_VBUS pin of the HUB through resistor divider network to limit the voltage level below 1.155 V. The Reset to the HUB is given by SoC RESETSTATz output.

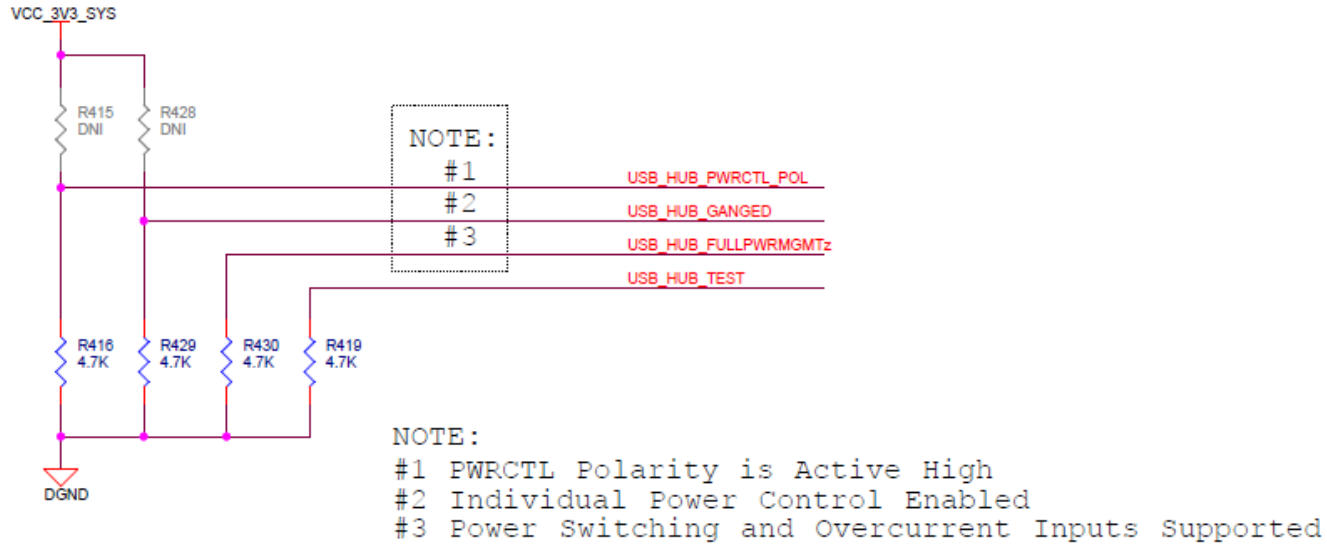
The GANGED/SMBA2/HS_UP pin and FULLPWRMGMTz/ SMBA1 pin of USB HUB are pulled down to enable individual power control of the ports when power switching is enabled. The PWRCTL_POL pin of USB HUB is pulled down to make PWRCTL polarity active high. The PWRCTL1/BATEN1 pin and PWRCTL2/BATEN2 pin of HUB is connected to enable pins of Current limit switches for VBUS supply control on downstream ports. The USB2.0 ports shall provide maximum of 500 mA, 5 V to the devices as per USB2.0 specifications. The USB HUB strapping options are provided as follows.

On E2 and future revisions, the USB Hub has been dropped in favor of connecting the onboard USB Controller directly to a single Type-A connector.

Note

Please see Section 3.2.3 for details on the differences between SK-AM62 E1 and latter implementation of the USB Subsystem.

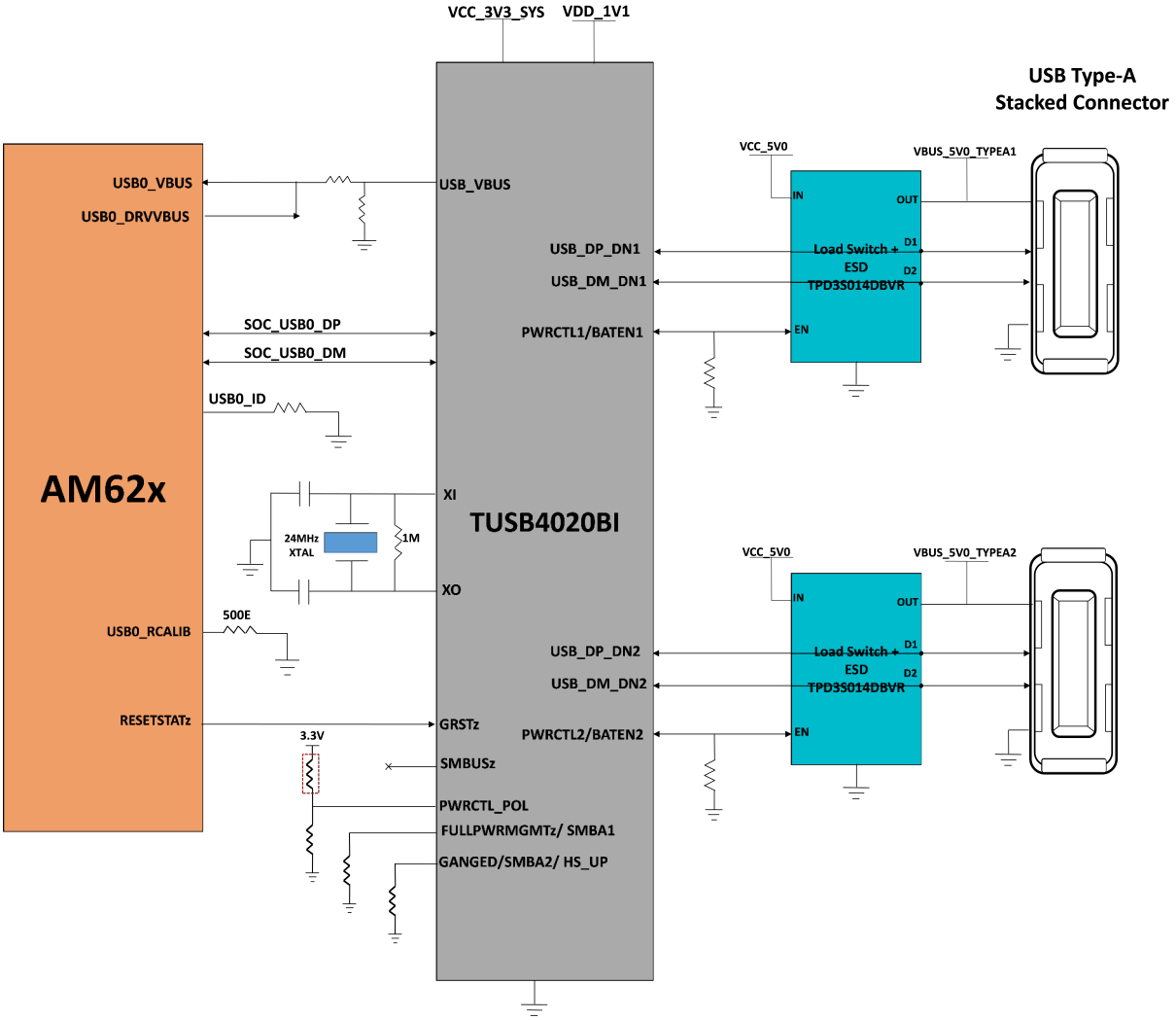
Copyright © 2026 Texas Instruments Incorporated



USB Data lines from Type-A connectors are connected to the Current Limit Load Switch and ESD Protection IC Mfr Part# TPD3S014DBVR. This switch limits the current to 500mA and dissipates the ESD strikes above the maximum level specified in the IEC 61000-4-2.

The USB HUB is powered by 3.3V from board IO supply and the 1.1V supply from Dedicated LDO Mfr Part# TLV75511PDQNR.

Copyright © 2026 Texas Instruments Incorporated



2.1.6.10.2 USB 2.0 Type C Interface

On SKEVM, USB 2.0 Interface is offered through USB Type-C Connector J13 Mfr part# 2012670005 that supports data rate up to 480 Mbps. J13 is used for Data communication and also as power connector. It is configured as DRP port using PD controller TPS65988DHRSHR IC, so it can act as either Host or Device. The role of the port depends on the type of the device getting connected on the connector and its ability to either sink or source. When the port is acting as DFP, it can source up to 5V@500mA.

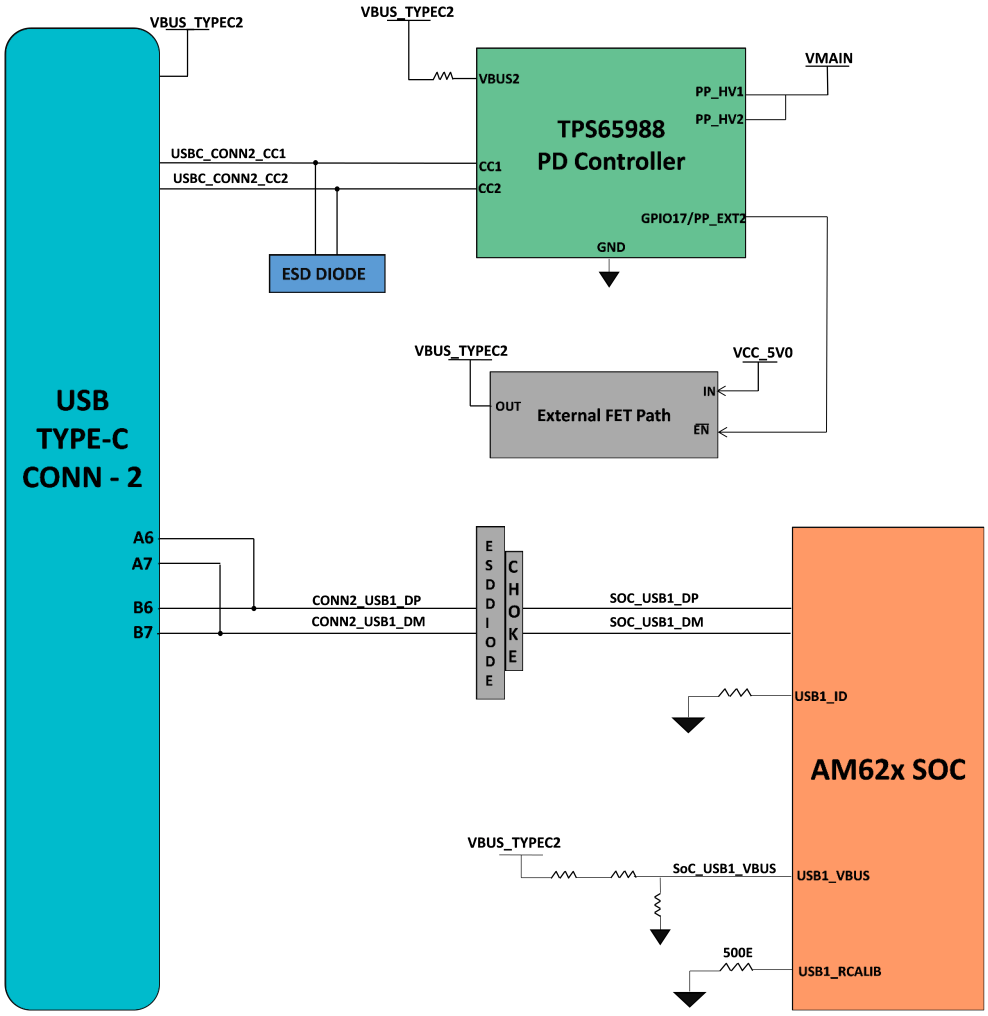
USB 2.0 Data lines DP and DM from J13 are connected to the USB0 interface of AM62x SoC via choke and ESD protection device. USB0_VBUS to the SoC is provided through a resistor divider network.

A common mode choke of Mfr Part# DLW21SZ900HQ2B is provided on USB Data lines to take care of EMI/ EMC. An ESD protection device of part number ESD122DMXR is included to dissipate ESD strikes on USB2.0 DP/DM Signals. An ESD protection device of part number TPD1E01B04DPLT is included on CC signals and TVS2200DRVR IC is included on VBUS rail of Type-C Connector J13 to dissipate ESD strikes.

Note

Please see Section 3.2.3 for details on the differences between E1 and latter implementation of the USB Subsystem.

Copyright © 2026 Texas Instruments Incorporated



Configured as DRP

2.1.6.11 Memory Interfaces

2.1.6.11.1 DDR4 Interface

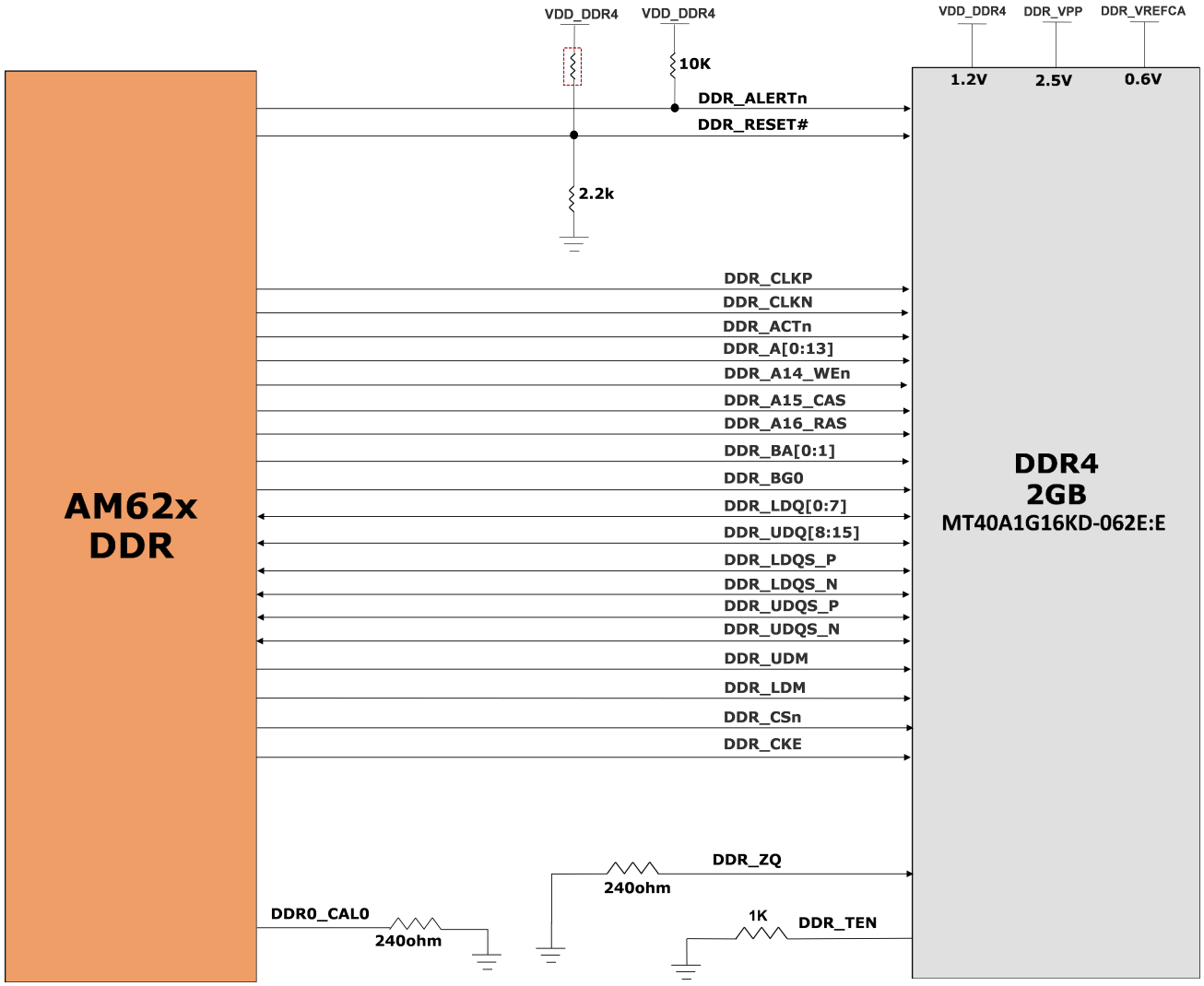
AM62x SKEVM has 2GB, 16-bit wide DDR4 memory with operating speed of up to 1600MT/s. Micron's MT40A1G16KD-062E:E is used. This uses two x8 8Gb Micron dies to make one x16 interface. The DDR memory is mounted on-board (single chip). The Placement and routing of DDR4 device is point to point.

The SK-AM62B and SK-AM62B-P1 RevA EVMs have Micron's MT40A1G16TB-062E:F part due to EOL issue.

The DDR4 requires 1.2 V and thus reduces power demand. The devices require I/O power of 1.2 V, DRAM activating power supply of 2.5 V and 0.6 V reference voltage for control, command and address pins.

DDR4 reset is an active low signal, which is controlled by SoC and the signal is pulled down to set the default active state. A footprint for pull up is also provided.

Copyright © 2026 Texas Instruments Incorporated



2.1.6.11.2 OSPI Interface

AM62x SKEVM board has a 512-Mbit OSPI memory device from Cypress Part# S28HS512TGABHM010 which is connected to the OSPI0 interface of the AM62x SoC. The OSPI interface supports single and double data rates with memory speeds up to 200 MBps SDR and 400 MBps DDR (200 MHz clock speed).

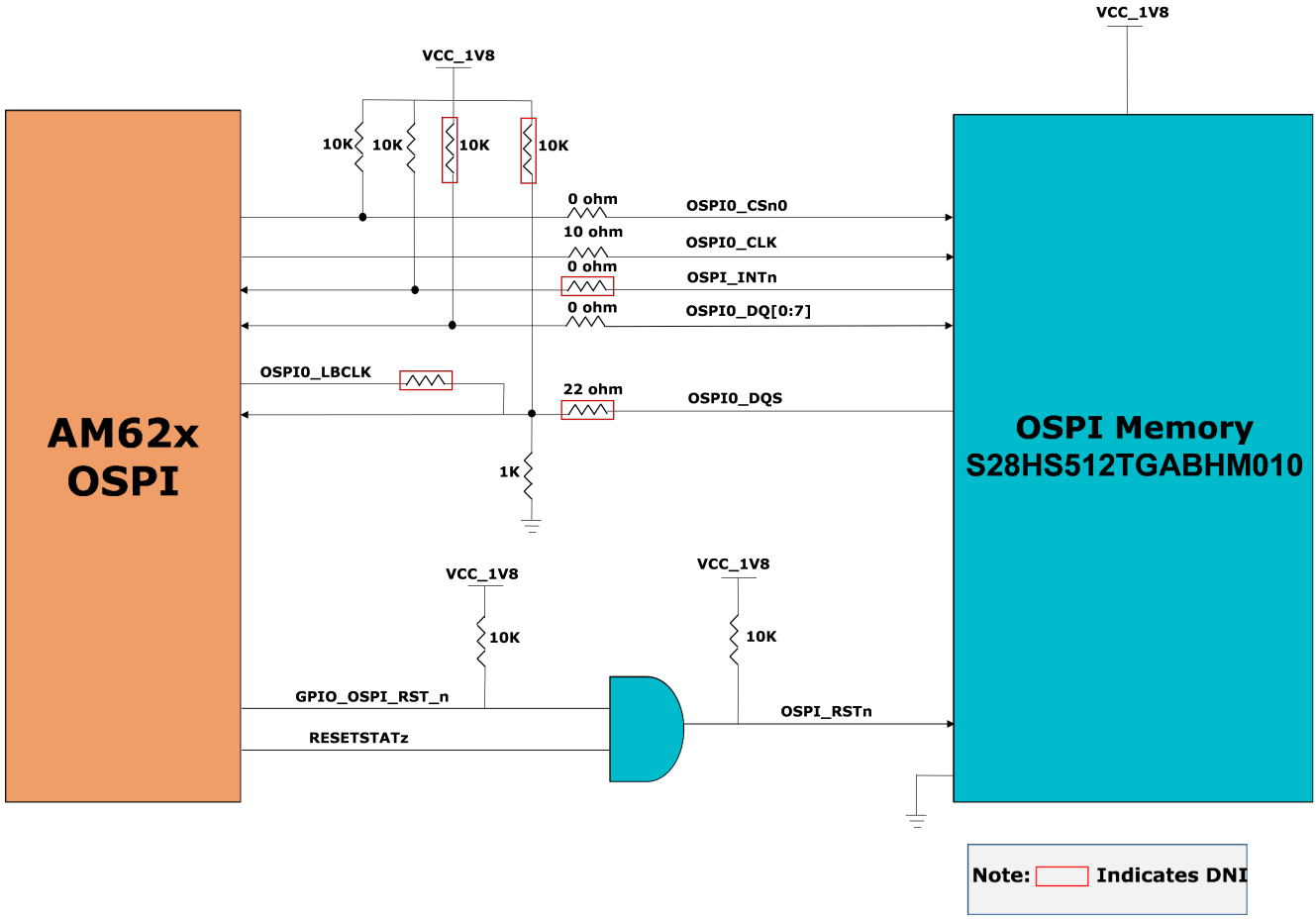
OSPI & QSPI implementation: 0 ohm resistors are provided for DATA[7:0], DQS, INT# and CLK signals. Footprints to mount external pull up resistors are provided on DATA[7:0] to prevent bus floating. The footprint for the OSPI memory also allows the installation of either a QSPI memory or an OSPI memory. The 0 ohm series resistors provided for pins OSPI_DATA[4:7] will be removed if QSPI flash is to be mounted.

Reset: The reset for the OSPI flash is connected to a circuit that ANDs the RESETSTATz from the AM62x with the signal GPIO_OSPI_RSTn from the SoC GPIO. This will apply reset for warm and cold reset. A pull-up is provided on GPIO_OSPI_RSTn coming from SoC pin to set the default active state.

Power: The OSPI flash is powered by 1.8 V IO supply. The 1.8 V supply is provided to both VCC and VCCQ pins of the OSPI flash memory.

The OSPI interface of the SoC is powered by VDDSHV1 Power group of SoC and is connected to 1.8V IO supply.

Copyright © 2026 Texas Instruments Incorporated



2.1.6.11.3 MMC Interfaces

AM62x SoC has three MMC (MMC0, MMC1 and MMC2) ports. MMC0 is connected to eMMC flash, MMC1 is interfaced with Micro SD Socket on the board and MMC2 is connected to Wilink module for WiFi Interface

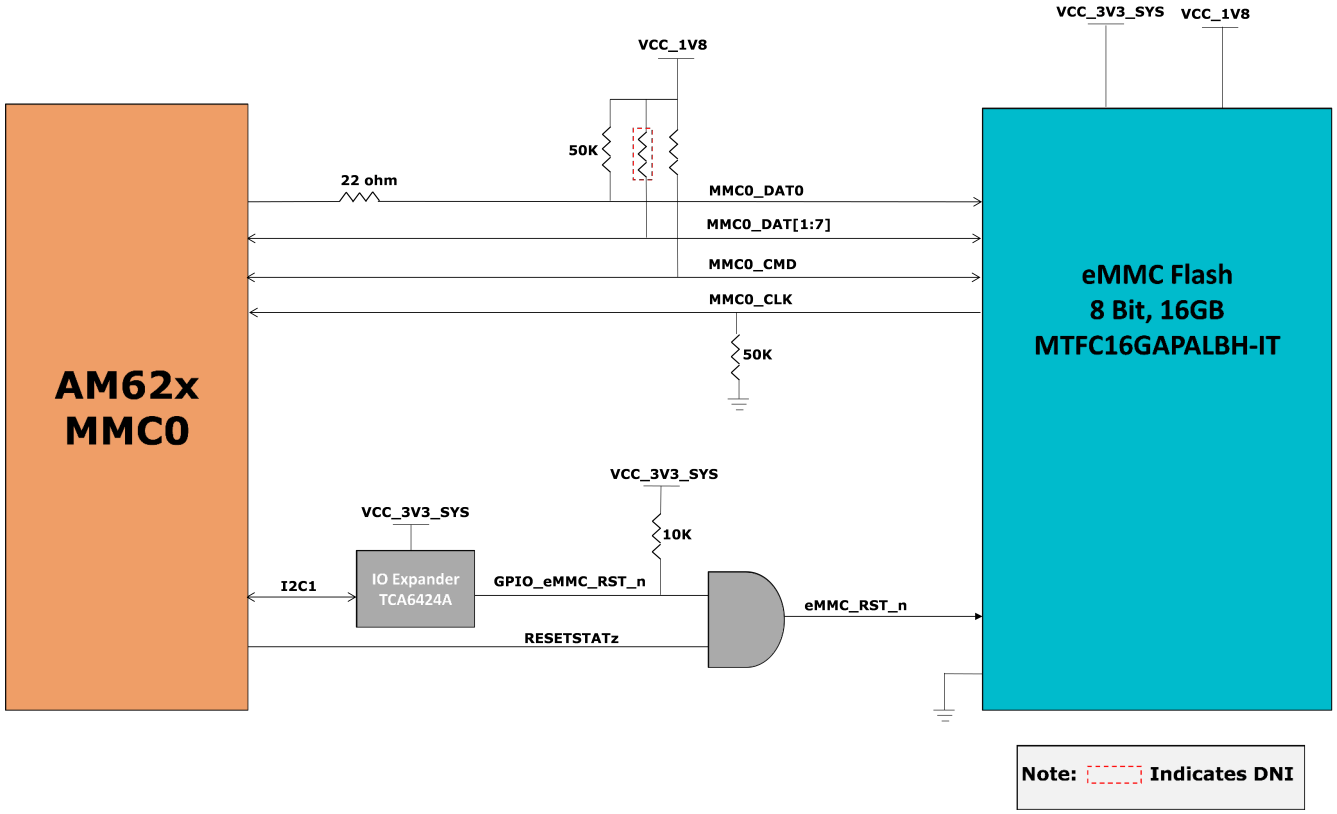
2.1.6.11.3.1 MMC0 - eMMC Interface

The SKEVM board contains 16GB of eMMC flash memory from Micron Part# MTFC16GAPALBH-IT connected to MMC0 port of the AM62x SoC. The flash is connected to 8 bits of the MMC0 interface supporting HS400 double data rates up to 200 MHz.

The SK-AM62B RevA and SK-AM62B-P1 RevA revision boards are upgraded to 32GB of eMMC flash memory from Micron Part# MTFC32GAZAQHD-IT.

The eMMC device requires two power supplies, 3.3 V for NAND memory and 1.8 V for the eMMC interface. The MMC0 interface of the SoC is powered by the VDDSHV4 power domain, which is connected to 1.8 V IO supply.

Copyright © 2026 Texas Instruments Incorporated

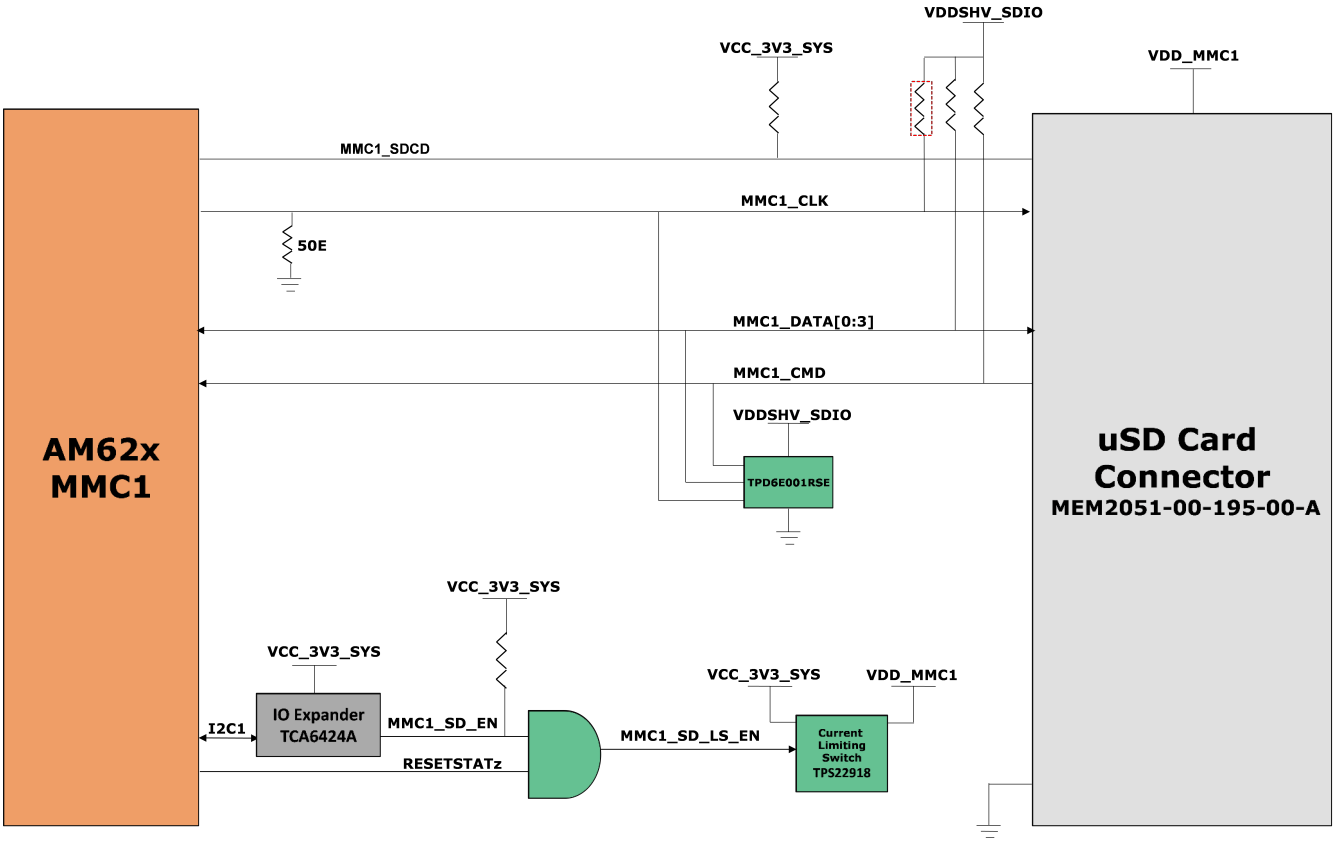


2.1.6.11.3.2 MMC1 - Micro SD Interface

The SKEVM board provides a micro SD card interface connected to the MMC1 port of the AM62x SoC. The Micro SD card socket of Mfr. Part# MEM2051-00-195-00-A is used to interface with the MMC1 port of the AM62x SoC. UHS1 operation is supported, including IO operations at both 1.8 V and 3.3 V. The Micro SD card interface is set to operate in SD mode by default. For high-speed cards, the ROM Code of the SoC attempts to find the fastest speed that the card and controller can support and can have a transition to 1.8 V.

The SD Card connector power is provided using a load switch of Mfr. Part # TPS22918DBVR, which is controlled by ANDing the output of RESETSTATz, PORz_OUT and a GPIO from an IO Expander. An ESD protection device of part number TPD6E001RSE is provided for data, clock, and command signals. TPD6E001RSE is a line termination device with integrated TVS diodes providing system-level IEC 61000-4-2 ESD protection, ± 8-kV contact discharge and ± 15kV air-gap discharge.

Copyright © 2026 Texas Instruments Incorporated



2.1.6.11.3.3 MMC2 - Wilink Interface

AM62x SKEVM has a WiLink Module of part number WL1837MODGIMOCT from TI connected to MMC2, UART2 instances and McASP2 interface through buffers. The Module is connected to 4-bit IO of the MMC2 interface supporting IEEE standard 802.11a/b/g/n data rates with 20 or 40-MHz SISO or 20-MHz MIMO. The Module requires two power supplies, 3.3V for VBAT_IN and 1.8V for VIO_IN. Power to WiLink module is supplied from on board Power supply rails.

The MMC2 interface of the SoC is powered by the VDDSHV6 power domain, which is connected to 1.8 V IO supply.

The WiLink module is removed from SK-AM62B and SK-AM62B-P1 RevA EVMs and M.2 connector is implemented expansion modules. This expansion interface is primarily used for Wi-Fi/BT modules, and supports the following interfaces: Secure Data/Secure Digital IO (SDIO), Universal Asynchronous Receiver/Transmitter (UART) and Multi-Channel Audio Serial Port (McASP).

Note: An example add-on wireless network module for this interface is the Embedded Artist EAR00388 WiFi and Bluetooth module.

Copyright © 2026 Texas Instruments Incorporated

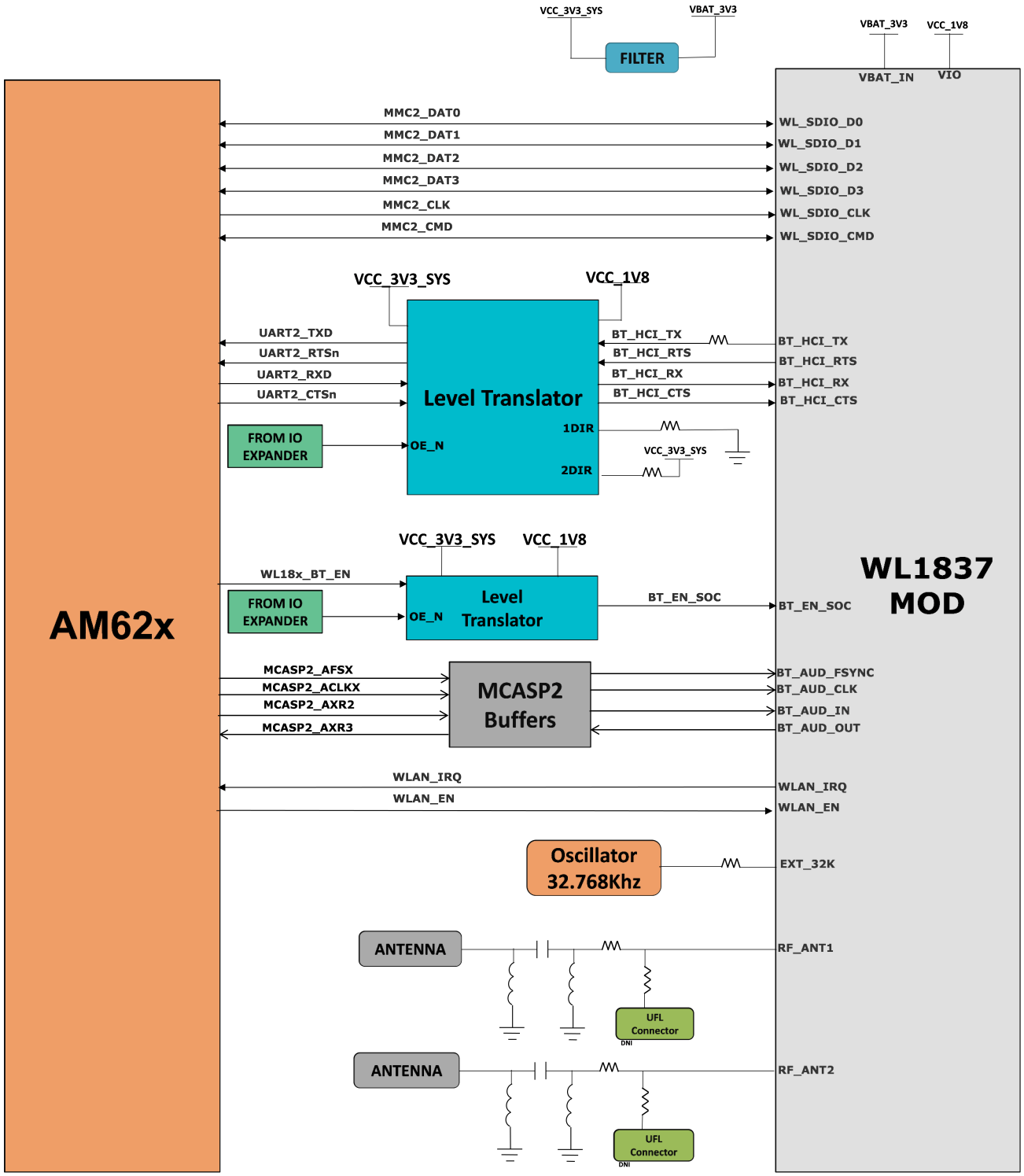


Figure 2-13. MMC2 - Wilink Interface on SK-AM62 and SK-AM62-P1

Copyright © 2026 Texas Instruments Incorporated

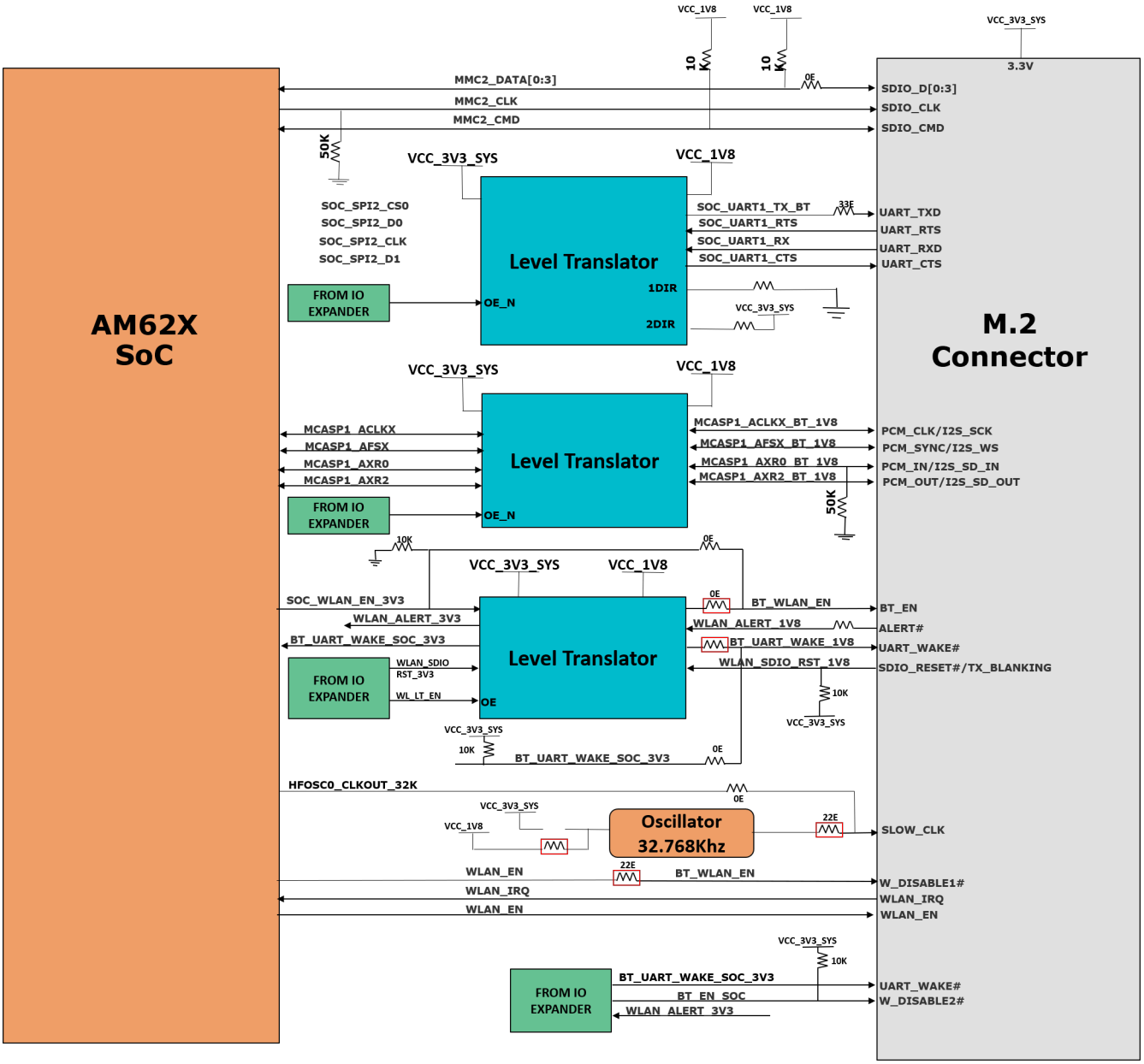


Figure 2-14. MMC2 - M.2 Connector Interface on SK-AM62B and SK-AM62B-P1

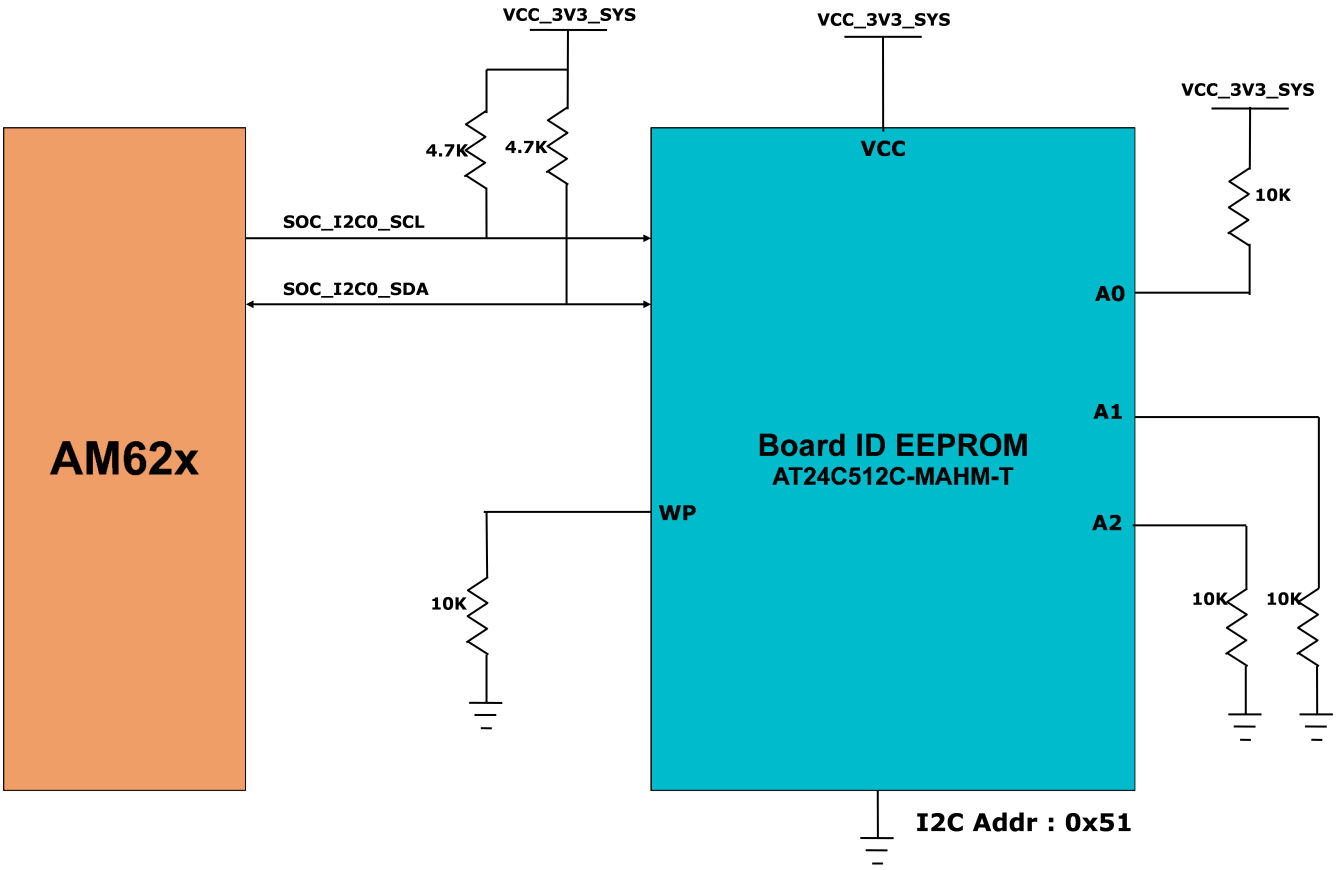
2.1.6.11.4 EEPROM

AM62x SKEVM boards are identified by their version and serial number, which are stored on the onboard EEPROM. The EEPROM is accessible from SoC I2C0 port of AM62x SoC.

The Board ID EEPROM I2C address is set to 0x51.

AM62x SKEVM includes an AT24C512C-MAHM-T 512kb EEPROM. The first 259 bytes of memory are preprogrammed with identification information for each board. The remaining 65277 bytes are available to the user for data or code storage.

Copyright © 2026 Texas Instruments Incorporated



2.1.6.12 Ethernet Interface

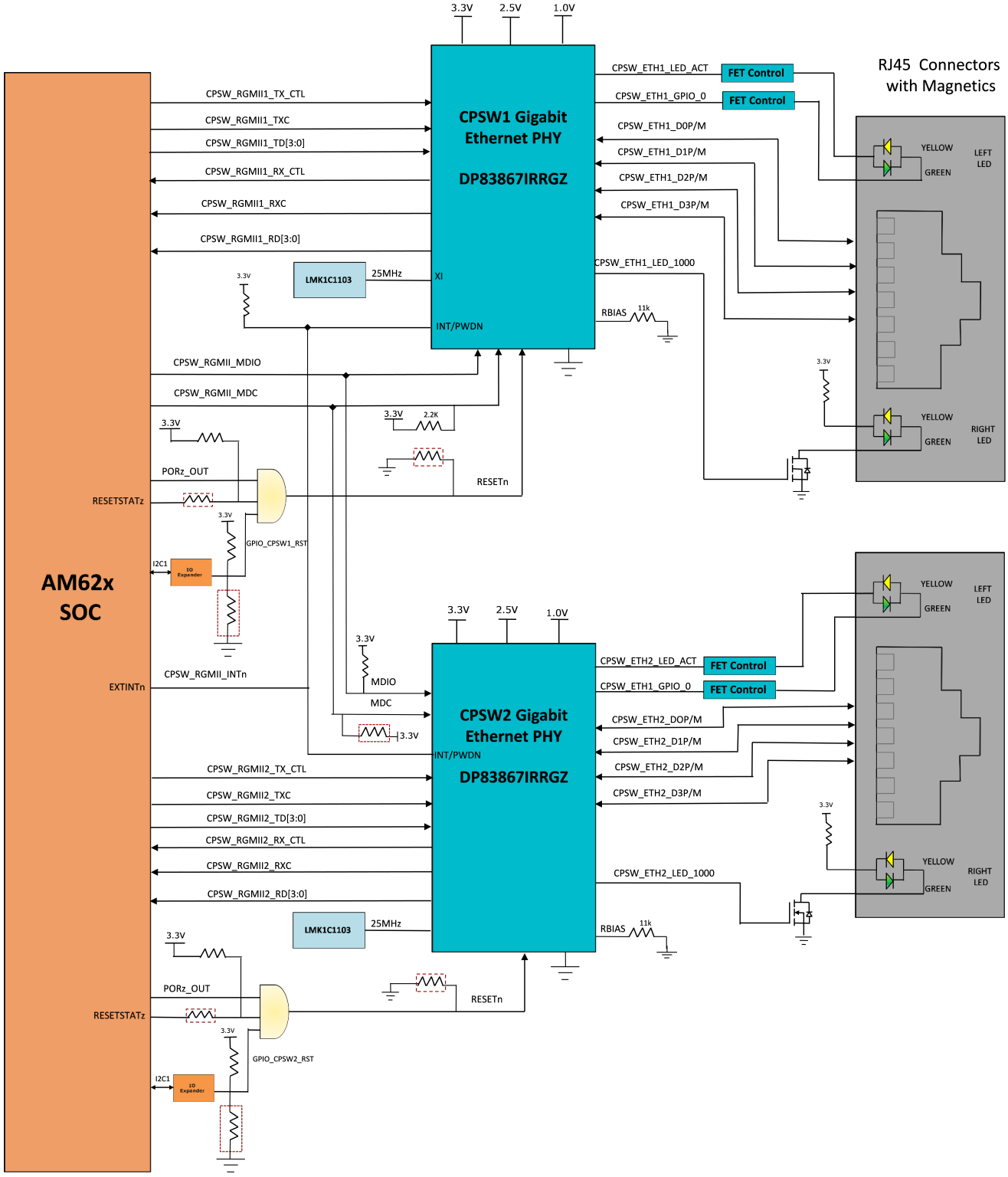
The AM62x SKEVM offers two Ethernet Ports of 1 Gigabit Speed for external Communication. Two channels of RGMII Gigabit Ethernet CPSW Ports from AM62x SoC are connected to separate Gigabit Ethernet PHY Transceivers DP83867, which are finally terminated on two RJ45 connectors with integrated magnetics.

The 48pin version of the PHY DP83867 is configured to advertise 1-Gb operation with the internal delay set to accommodate the internal delay inside the AM62x. CPSW_RGMII1 and CPSW_RGMII2 Ports share a common MDIO Bus to communicate with the external PHY Transceiver.

Two Single port RJ45 Connectors Mfr Part# LPJG16314A4NL from Link-PP are used on the board for Ethernet 10/100/1G Connectivity. RJ45 Connectors have integrated magnetics and LEDs for indicating 1000BASE-T link as well as receive or transmit Activity.

IO supply to the Ethernet PHY is set 3.3V IO level.

Copyright © 2026 Texas Instruments Incorporated



2.1.6.12.1 CPSW Ethernet PHY 2 Default Configuration

CPSW_RGMII2 port of the AM62x SoC is connected to DP83867 whose configuration is as given below:

PHY ADDR: 00001

Auto_neg: Enabled

ANGsel 10/100/1000

Copyright © 2026 Texas Instruments Incorporated

RGMII Clk skew Tx: 0ns

RGMII Clk skew Rx: 2ns

The interrupts generated from two CPSW RGMII PHYs are tied together and is connected to EXTINTn pin of AM62x SoC.

LED1 is connected to RJ45 Right LED (Green) to indicate 1000MHz link.

LED2 is connected to RJ45 Left LED (Yellow) to indicate transmit/receive activity.

GPIO_0 is connected to RJ45 Left LED (Green) to indicate 10/100MHz link.

LED Control is achieved through an external MOSFET.

2.1.6.12.2 CPSW Ethernet PHY 1 Default Configuration

The default configuration of the DP83867 is determined using a number of resistor pull-up and pull-down values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes by using the pull up and pull down options provided. The AM62x SKEVM uses the 48-pin QFN package which supports the RGMII interface.

The DP83867 PHY uses four level configurations based on resistor strapping which generate four distinct voltages ranges. The resistors are connected to the RX data and control pins which are normally driven by the PHY and are inputs to the processor. The voltage range for each mode is shown below:

Mode 1 - 0 V to 0.3 V

Mode 2 – 0.462 V to 0.6303 V

Mode 3 – 0.7425 V to 0.9372 V

Mode 4 – 2.2902 V to 2.9304 V

Footprint for both pull-up and pull-down is provided on all the strapping pins except LED_0. LED_0 is for Mirror Enable, which is set to mode 1 by default, Mode 4 is not applicable and Mode2, Mode3 option is not desired.

CPSW_RGMII1 port of the AM62x SoC is connected to DP83867 whose configuration is as given below:

PHY ADDR: 00000

Auto_neg: Enabled

ANGsel 10/100/1000

RGMII Clk skew Tx: 0 ns

RGMII Clk skew Rx: 2 ns

2.1.6.13 GPIO Port Expander

The I/O Expander used in the AM62x SKEVM is a 24-Bit I2C based I/O Expander which is used for daughter card plug-in detection and for generating resets and enable signals to various peripheral devices connected to it. The SoC_I2C1 bus of the AM62x SoC is used to interface with the I/O Expander. The I2C device address of the I/O Expander is 0x22. See Table 2-10 for the list of signals being controlled by the Expander.

Table 2-10. IO Expander Signal Detail

Pin No.	Signal	Direction	Device
P00	GPIO_CPSW2_RST	OUTPUT	CPSW Ethernet PHY-1 Reset Control GPIO
P01	GPIO_CPSW1_RST	OUTPUT	CPSW Ethernet PHY-2 Reset Control GPIO
P02	PRU_DETECT	INPUT	PRU Board Detection
P03	MMC1_SD_EN	OUTPUT	SD Card Load Switch Enable
P04	VPP_LDO_EN	OUTPUT	SoC eFuse Voltage(VPP=1.8V) Regulator Enable
P05	EXP_PS_3V3_EN	OUTPUT	EXP CONN 3.3V Power Switch Enable
P06	EXP_PS_5V0_EN	OUTPUT	EXP CONN 5V Power Switch Enable
P07	EXP_HAT_DETECT	INPUT	EXP CONN HAT Board Detection

Copyright © 2026 Texas Instruments Incorporated

Table 2-10. IO Expander Signal Detail (continued)

Pin No.	Signal	Direction	Device
P10	GPIO_AUD_RSTn	OUTPUT	Audio Codec Reset Control GPIO
P11	GPIO_eMMC_RSTn	OUTPUT	eMMC Reset control GPIO
P12	UART1_FET_BUF_EN	OUTPUT	Enable for UART1 FET Buffer
P13	WL_LT_EN	OUTPUT	Enable for Wilink Level Translators
P14	GPIO_HDMI_RSTn	OUTPUT	HDMI Transmitter Reset Control GPIO (can also be used for OLID_RSTn with resistor stuffing change)
P15	CSI_GPIO1	NA	Raspberry Pi Camera CSI0 GPIO1
P16	CSI_GPIO2	NA	Raspberry Pi Camera CSI0 GPIO2
P17	PRU_3V3_EN	OUTPUT	PRU Power Switch Enable
P20	HDMI_INTn	INPUT	HDMI Interrupt
P21	PD_I2C_IRQ	INPUT	Input interrupt from the USB-C Power Delivery Controller
P22	AUD_BUF_EN	OUTPUT	MCASP Enable and Direction Control
P23	WL_BUF_EN	OUTPUT	
P24	AUD_BUFF_CLK_DIR	OUTPUT	
P25	UART1_FET_SEL	OUTPUT	
P26	TS_INT#	OUTPUT	OLDI Display Touch Screen Interrupt
P27	IO_EXP_TEST_LED	OUTPUT	GPIO used to control USED TEST LED

Copyright © 2026 Texas Instruments Incorporated

2.1.6.14 GPIO Mapping

The Table 2-11 describes the detailed GPIO mapping of AM62x SoC with AM62x SKEVM peripherals.

Table 2-11. GPIO Mapping

Sl.No	GPIO Description	GPIO NETNAME	Functionality	GPIO Used	SoC Muxed Signal Name	Direction With Respect to Control	Default State	Active State	Voltage on SoC Side	Voltage on SK-EVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_1	MCU_SPIO_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt PRU Connector Interrupt	CPSW_RGMII_INTn/ PRu_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/User Interrupt									
10	USER Test LED 1	SOC_GPIO_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER - P00		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	CPSW Ethernet PHY-2 Reset control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P02		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER - P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFUSE Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	RPI_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	RPI_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER - P07		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P010		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P11		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

Copyright © 2026 Texas Instruments Incorporated

Table 2-11. GPIO Mapping (continued)

Sl.No	GPIO Description	GPIO NETNAME	Functionality	GPIO Used	SoC Muxed Signal Name	Direction With Respect to Control	Default State	Active State	Voltage on SoC Side	Voltage on SK-EVM
11	SOC UART1 MUX Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Rasberry Pi Cameraa CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Rasberry Pi Cameraa CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for Communications with AM62X	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Backlight Enable	VLED_ENB	ENABLE	IO EXPANDER - P26		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3

Copyright © 2026 Texas Instruments Incorporated

2.1.6.15 Power

2.1.6.15.1 Power Requirements

AM62x SKEVM can be powered through either of the two USB Type C Connectors –

- Connector 1(J11) - Power role – SINK, No Data role
- Connector 2(J13) - Power role – DRP, Data role – USB2.0 DFP or UFP

The AM62x SK EVM supports voltage input ranges of 5 V - 15 V and 3A of current. A USB PD controller Mfr. Part# TPS65988DHRSHR is used for PD negotiation upon cable detection to get necessary power required for the board. Connector 1 is configured to be an UFP Port and has no Data role. Connector 2 is configured as a DRP port, it can act as DFP only when the board is being powered by Connector 1. When both the connectors are connected to external power supply, the port with highest PD power contract will be selected to power the board.

Table 2-12. Type-C port Power roles

J11(UFP)	J13(DRP)	Board Power	Remarks
Plugged in	NC	ON - J11	J11 will be UFP and will only sink power and J13 can act as DFP if a peripheral is connected
NC	Plugged in	ON - J13	J13 will be UFP and can only sink power
Plugged in	Plugged in	ON - J11 or J13	Board will be powered by the port with highest PD power contract

The PD IC uses a SPI EEPROM to load the necessary configuration on power up so it can negotiate a power contract with a compatible power source.

The configuration file is loaded to the EEPROM using header J22. Once the EEPROM is programmed the PD obtains the configuration files via SPI communication. Upon loading the configuration files the PD negotiates with the source to obtain the necessary power requirement.

Note

The EEPROM is pre-programmed with the configuration file for the operation of the PD controller.

Power indication LEDs are provided for both the Type-C connectors for the user to identify which connector is powering the SKEVM Board.

An external power supply (Type-C output) can be used to power the EVM but is not included as part of the SKEVM kit.

The external power supply requirements (Type-C) are:

Minimum Voltage: 5 VDC, Recommended Minimum Current: 3000 mA

Maximum Voltage: 15VDC, Maximum current: 5000 mA

Table 2-13. Recommended External Power Supply

DigiKey Part No.	Manufacturer	Manufacturer Part No.
1939-1794-ND	GlobTek, Inc.	TR9CZ3000USBCG2R6BF2
Q1251-ND	Qualtek	QADC-65-20-08CB

Note

Because SK-AM62 implements USB PD for power, the device is able to negotiate to the highest Voltage/Current combination supported by both the Device and Power Adapter, as such, if the power supply exceeds the maximum voltage and current requirements listed above is acceptable as long as the power adapter is compliant with the USB-C PD specification.

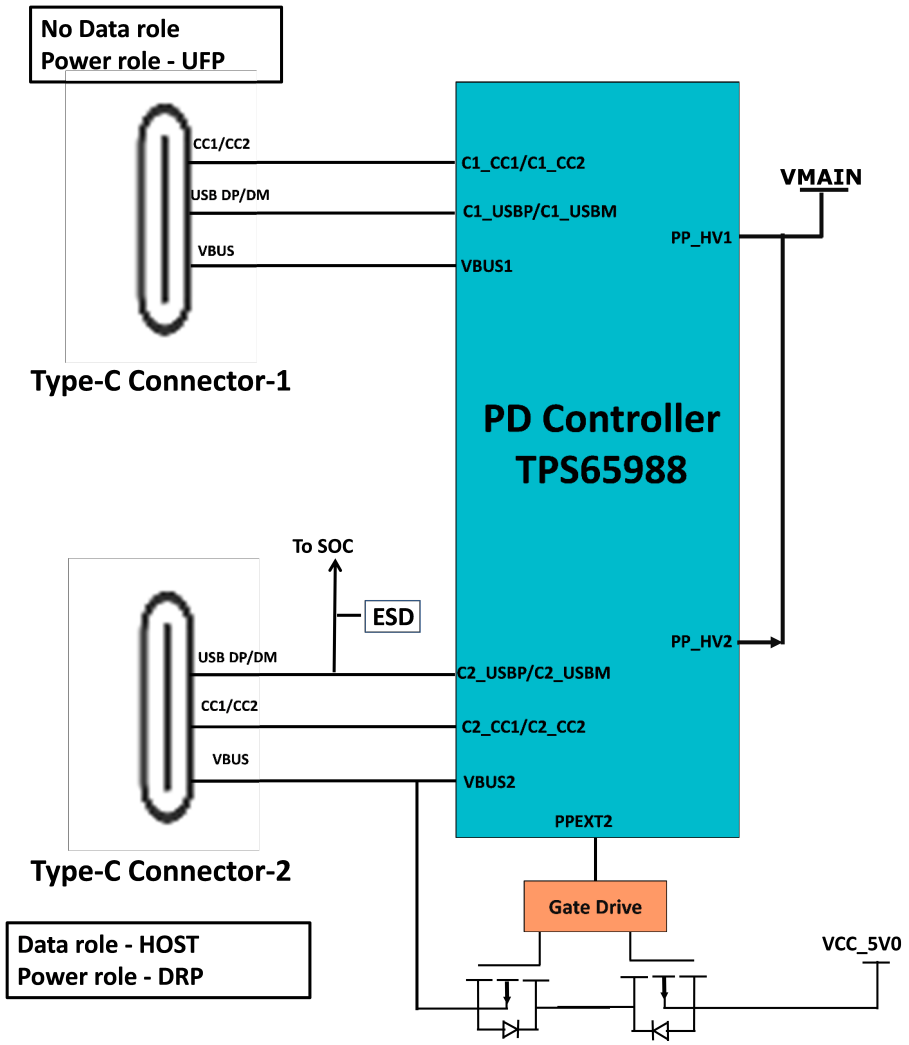
2.1.6.15.2 Power Input

Both Type-C Connectors (VBUS and CC lines) are connected to a Dual PD controller Mfr Part# TPS65988. The TPS65988 is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation

Copyright © 2026 Texas Instruments Incorporated

detection for two USB Type-C Connectors. Upon cable detection, the TPS65988 communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65988 enables the appropriate power path. The two internal power paths of TPS65988 are configured as sink paths for the two Type-C ports and an external FET path is provided for Type-C CONN 2 to source 5 V when acting as DFP. The external FET path is controlled by GPIO17/PP_EXT2 of the PD controller.

TPS65988 PD controller can provide an output of 3A (15 V max) through CC negotiation. The VBUS pins from both the Type C connectors are connected to the VBUS pins of the PD controller. The output of the PD is VMAIN which is given to on board Buck-Boost and Buck regulators to generate fixed 5 V and 3.3 V supply for the SKEVM board.



The following sections describe the power distribution network topology that supplies the SKEVM board, supporting components and reference voltages.

The AM62x SKEVM board includes a power solution based on discrete power supply components. The initial stage of the power supply will be VBUS voltage from either of the two USB Type C connectors J11 and J13. USB Type-C Dual PD controller of Mfr. Part# TPS65988DHRSHR is used for negotiation of the required power to the system.

Buck-Boost controller LM34936RHFR and Buck converter LM61460-Q1 are used for the generation of 5V and 3.3V respectively and the input to the regulators is the PD output. These 3.3 V and 5 V are the primary voltages for the AM62x SKEVM Board power resources.

Copyright © 2026 Texas Instruments Incorporated

The 3.3 V supply generated from the Buck regulator LM61460-Q1 is the input supply to the Various SoC regulators and LDOs. The 5 V supply generated from the Buck Boost regulator LM34936RHFR is used for powering the onboard peripherals

Voltage divider network is used to provide the DDR_VREFCA (0.6 V) supply for the DDR4.

Discrete regulators and LDOs used on Board are:

- TPS62824DMQR – To generate VDD_2V5 rail for PHY and DDR peripherals
- TLV75510PDQNR – To generate VDD_1V0 for Ethernet PHYs
- TLV75511PDQNR – To generate VDD_1V1 for USB HUB
- TLV75512PDQNR – To generate VDD_1V2 for HDMI Transmitter
- TPS74518PQWDRVRQ1 – To generate 1.8 V Analog supply for SoC
- TPS6282518DMQR – To generate 1.8V IO supply for SoC
- TLV7103318QDSERQ1 – To generate VDDSHV5_MMC1(SD interface) supply for SoC
- TPS62824DMQR – To generate DDR supply for SoC and DDR
- TPS62826DMQR – To generate Core supply for SoC
- TPS74501PDRVR – To generate VDDR_CORE supply for SoC

Dedicated regulators are also provided on the board for:

- TPS62177 Regulator - Powering the always on circuits of Test Automation Section
- TLV75518 LDO -e-Fuse programming of SoC
- TPS79601 LDO - XDS110 On board emulator
- TPS73533 LDO - FT4232 UART to USB Bridge

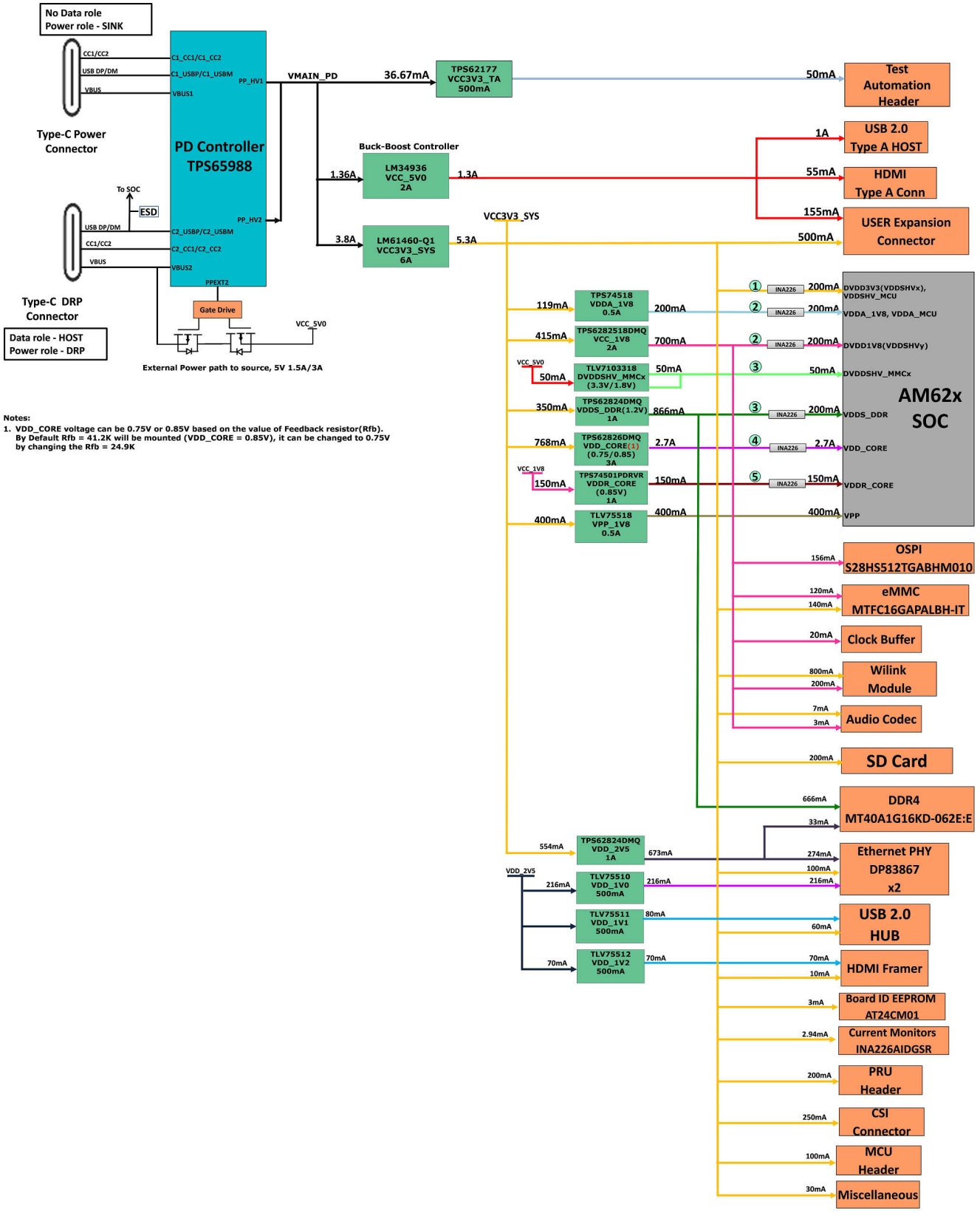
Additionally, GPIO from the test automation header is also connected to the LM34936RHFR Enable to control ON/OFF of the SKEVM via the test automation board. It only disables the VCC_5V0 output of LM34936RHFR from which all other power supplies are derived. SoC has different IO groups. Each IO group is powered by specific power supplies as given in the table below.

2.1.6.15.3 Power Supply

AM62x SKEVM utilizes an array of DC-DC converters to supply the various memories, clocks, SoC and other components on the board with the necessary voltage and the power required.

The figure below shows the various discrete regulators and LDOs used to generate power rails and the current consumption of each peripheral on AM62x SKEVM board.

Copyright © 2026 Texas Instruments Incorporated



Notes:
1. VDD_CORE voltage can be 0.75V or 0.85V based on the value of Feedback resistor(Rfb). By Default Rfb = 41.2K will be mounted (VDD_CORE = 0.85V), it can be changed to 0.75V by changing the Rfb = 24.9K

Figure 2-15. Power Supply Block Diagram

Copyright © 2026 Texas Instruments Incorporated

2.1.6.15.4 Power Sequencing

The figure below shows the Power Up and Power Down sequence of all the AM62x SKEVM Power supplies. AM62x SoC Power rails are named in red.

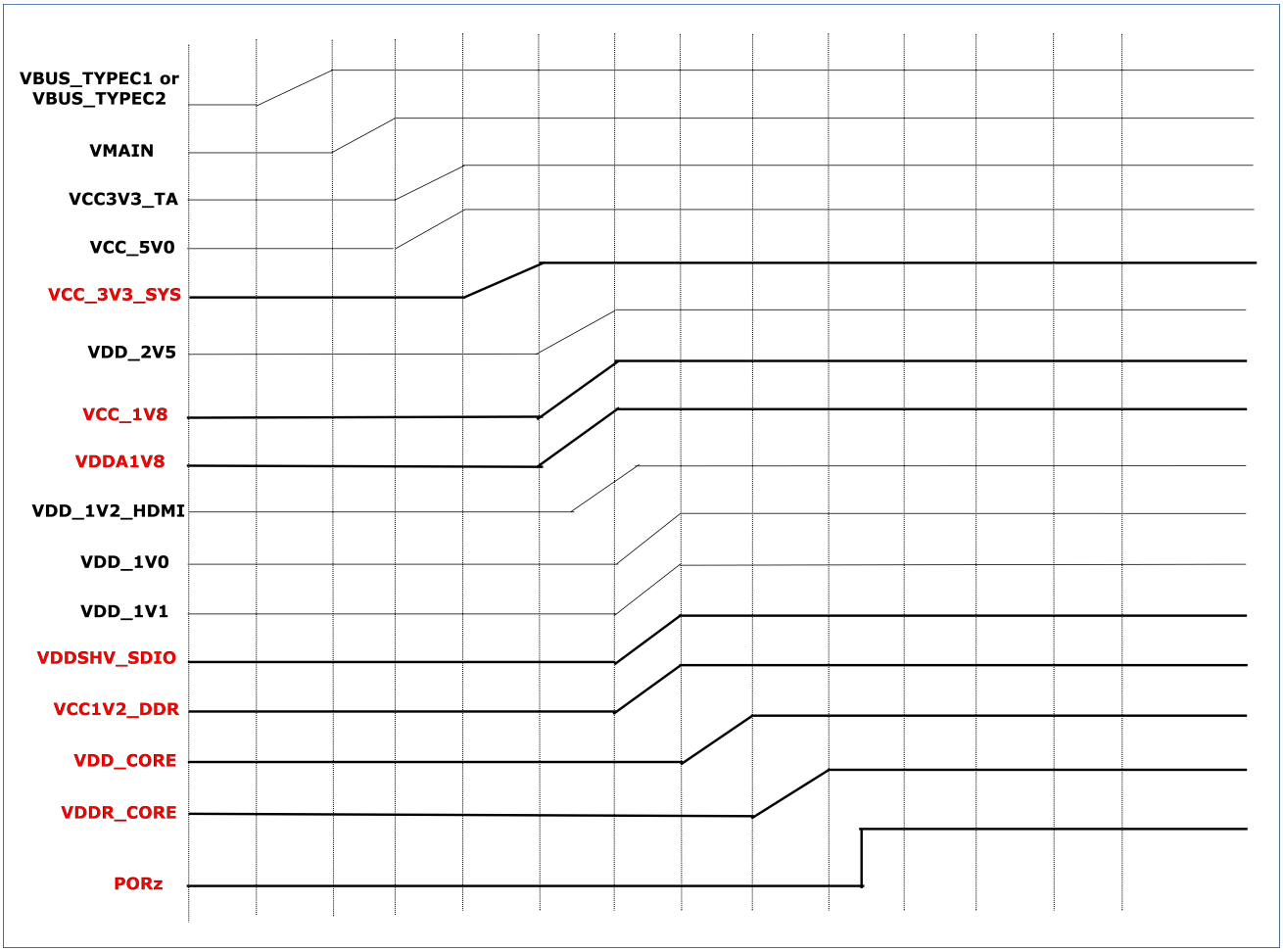


Figure 2-16. Power Up Sequence

Copyright © 2026 Texas Instruments Incorporated

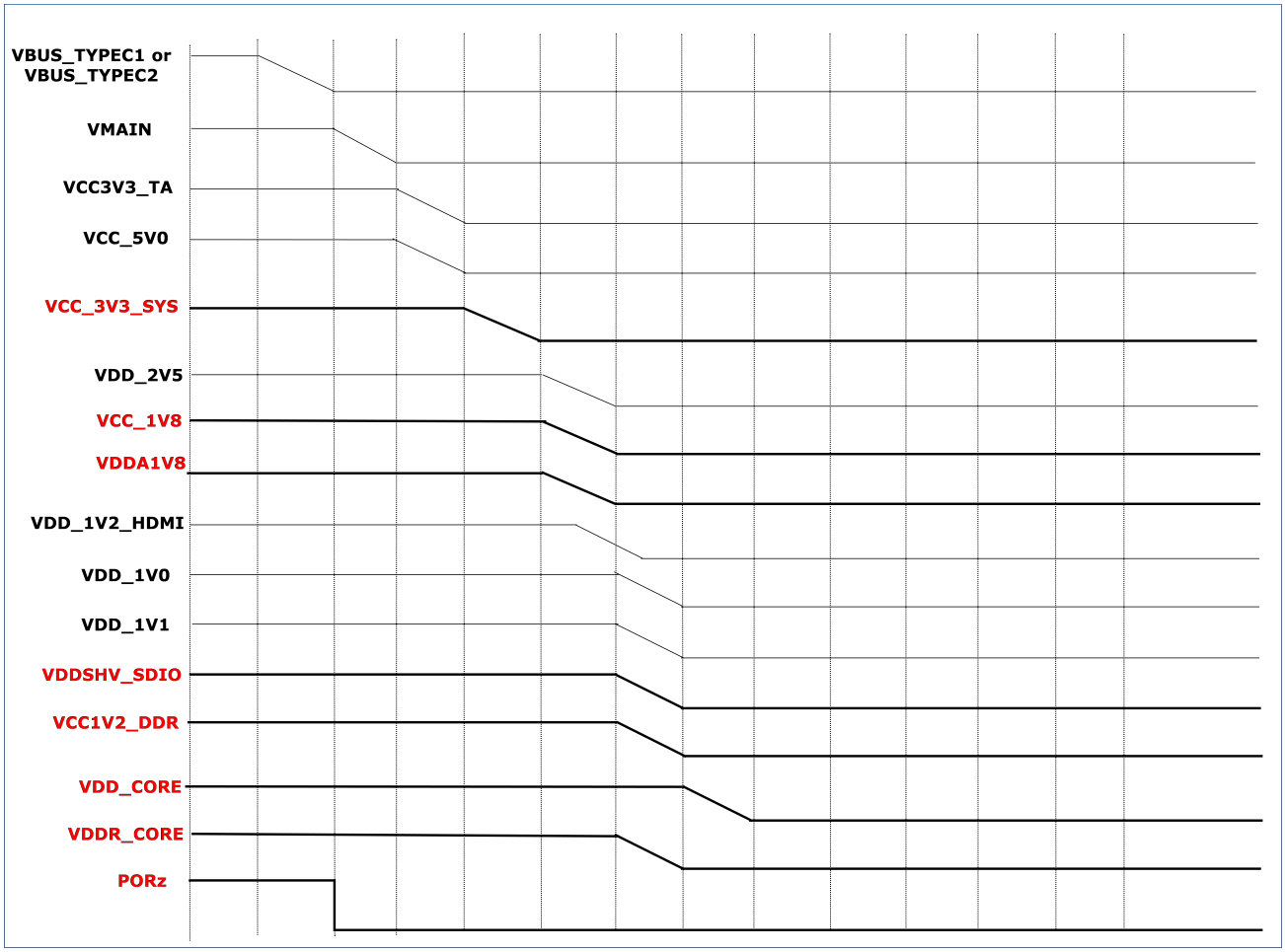


Figure 2-17. Power Down Sequence

Copyright © 2026 Texas Instruments Incorporated

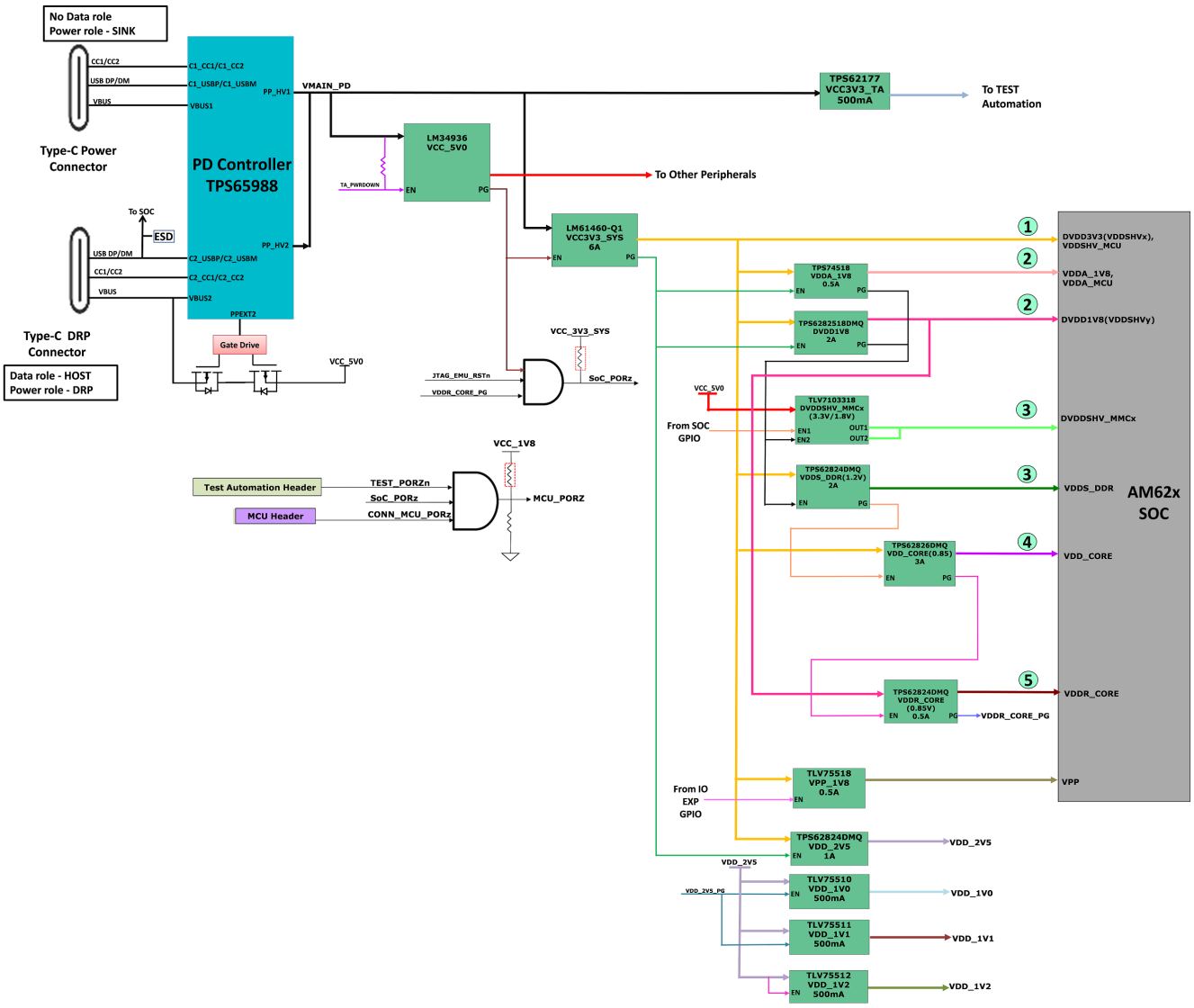


Figure 2-18. Power Sequence Block Diagram

2.1.6.15.5 AM62x SoC Power

The Core voltage of the AM62x can be 0.75 V or 0.85 V based on the Rfb(R150) Resistor value and on the power optimization requirement. By Default Rfb = 41.2K will be mounted (VDD_CORE = 0.85 V), it can be changed to 0.75 V by changing the Rfb to 24.9K. Current monitors are provided on all the SoC Power rails.

The SoC has different IO groups. Each IO group is powered by specific power supplies as shown in Table 2-14.

Table 2-14. SoC Power Supply

Sl.No	Power Supply	SoC Supply Rails	IO Power Group	Voltage
1	VDD_CORE	VDDA_CORE_USB		0.85
		VDDA_CORE_CSI		
		VDD_CANUART	CANUART	
		VDD_CORE	CORE	
2	VDDR_CORE	VDDR_CORE	CORE	0.85

Copyright © 2026 Texas Instruments Incorporated

Table 2-14. SoC Power Supply (continued)

Sl.No	Power Supply	SoC Supply Rails	IO Power Group	Voltage
3	VDDA_1V8	VDDA_1V8_CSIRX.	CSI	1.8
		VDDA_1V8_USB	USB	
		VDDA_1V8_MCU		
		VDDA_1V8_OLDI	OLDI	
		VDDA_1V8_OSCO	OSCO	
		VDDA_PLL0, VDDA_PLL1 & VDDA_PLL2		
4	VDD_DDR4	VDDS_DDR	DDR0	1.2
		VDDS_DDR_C		
5	VPP_1V8	VPP_1V8		1.8
6	SoC_VDDSHV5_SDIO	VDDSHV5	MMC1	
7	SoC_DVDD1V8	VDDSHV0	General	1.8
		VDDSHV1	OSPI	
		VDDSHV4	MMC0	
		VDDSHV6	MMC2	
		VMON_1P8_SOC		
8	SoC_DVDD3V3	VDDSHV0	General	3.3
		VDDSHV2	RGMII	
		VDDSHV3	GPMC	
		VDDSHV_MCU	MCU General	
		VMON_3P3_SOC		
		VDDA_3P3_USB	USB	

2.1.6.15.6 Current Monitoring

INA231 power monitor devices are used to monitor current and voltage of various power rails of AM62x processor. The INA231 interfaces to the AM62x through I2C interface (SoC_I2C1). Four terminal, high precision shunt resistors are provided to measure load current.

Table 2-15. INA I2C Device Address (E1)

Source	Supply Net	Device Address	Value of the Shunt Connected to the Supply Rail
VCC_CORE	VDD_CORE	0x40	10mΩ ± 1%
VCC_0V85	VDDR_CORE	0x41	10mΩ ± 1%
VCC_3V3_SYS	SoC_DVDD3V3	0x4C	10mΩ ± 1%
VCC_1V8	SoC_DVDD1V8	0x4B	10mΩ ± 1%
VDDA1V8	VDDA_1V8	0x4E	10mΩ ± 1%
VCC1V2_DDR	VDD_DDR4	0x46	10mΩ ± 1%

Table 2-16. INA I2C Device Address (E2)

Source	Supply Net	Device Address	Value of the Shunt Connected to the Supply Rail
VCC_CORE	VDD_CORE	0x40	10mΩ ± 1%
VCC_0V85	VDDR_CORE	0x41	10mΩ ± 1%
VCC_3V3_SYS	SoC_DVDD3V3	0x4C	10mΩ ± 1%
VCC_1V8	SoC_DVDD1V8	0x45	10mΩ ± 1%
VDDA1V8	VDDA_1V8	0x4E	10mΩ ± 1%
VCC1V2_DDR	VDD_DDR4	0x46	10mΩ ± 1%

2.1.6.16 AM62x SKEVM User Setup/Configuration

Copyright © 2026 Texas Instruments Incorporated

2.1.6.16.1 EVM DIP Switches

AM62x SKEVM has two 8 - position DIP Switch to set the SoC Boot mode and related parameters.

2.1.6.16.2 Boot Modes

The boot mode for the SK EVM board is defined by two banks of switches SW1 and SW2 or by the I2C buffer connected to the Test automation connector. This allows for AM62x SoC Boot mode control by either the user (DIP Switch Control) or by the Test Automation connector.

All the bits of switch (SW1 and SW2) have week pull down resistor and a strong pull up resistor as shown in below picture. Note that OFF setting provides a low logic level (‘0’) and an ON setting provides a high logic level (‘1’).

Note

The boot mode orientation has changed between E1 and future revisions. Please follow board silkscreen.

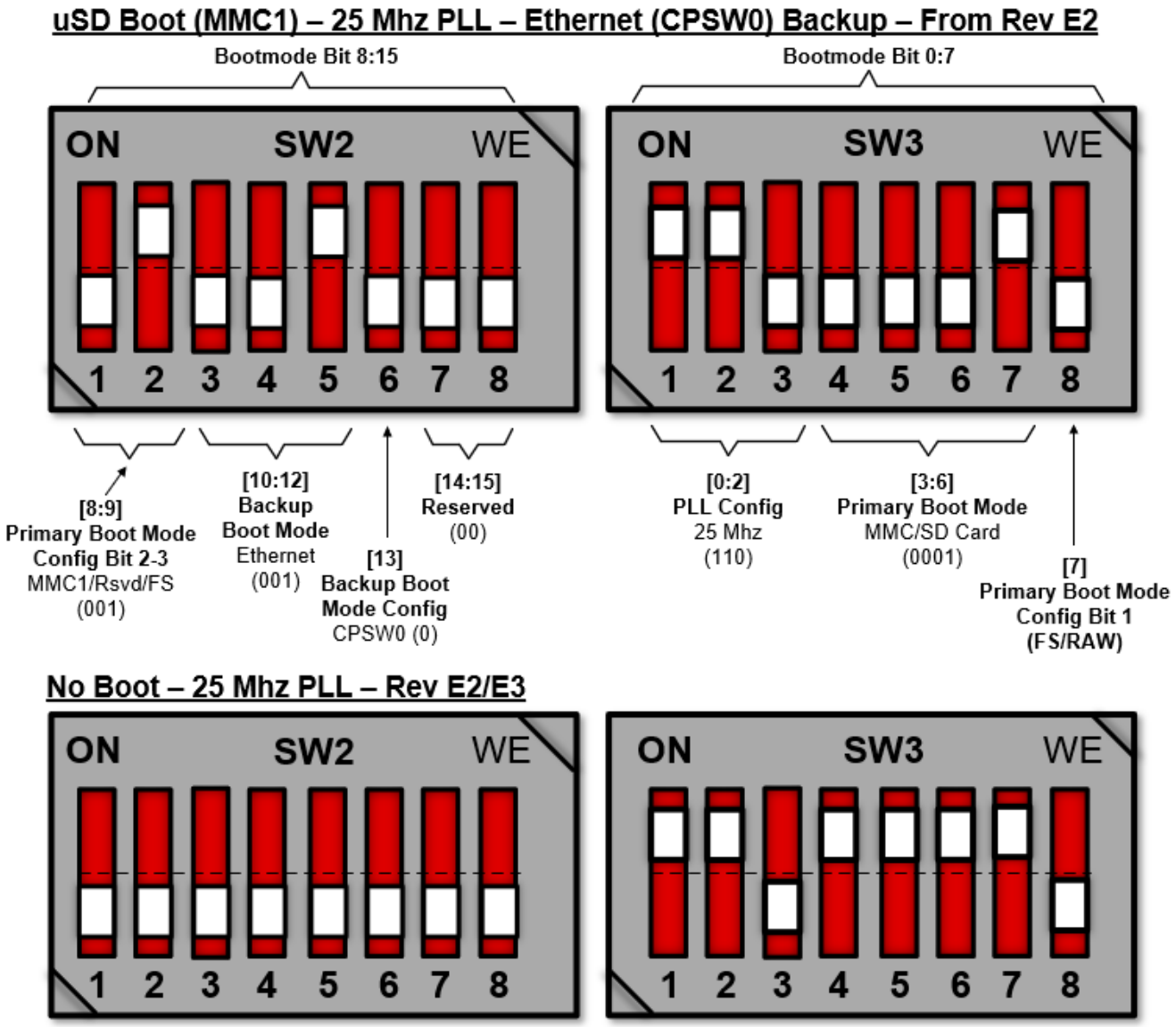


Figure 2-19. Bootmode Switch Configuration for SD Boot (From E2)

Copyright © 2026 Texas Instruments Incorporated

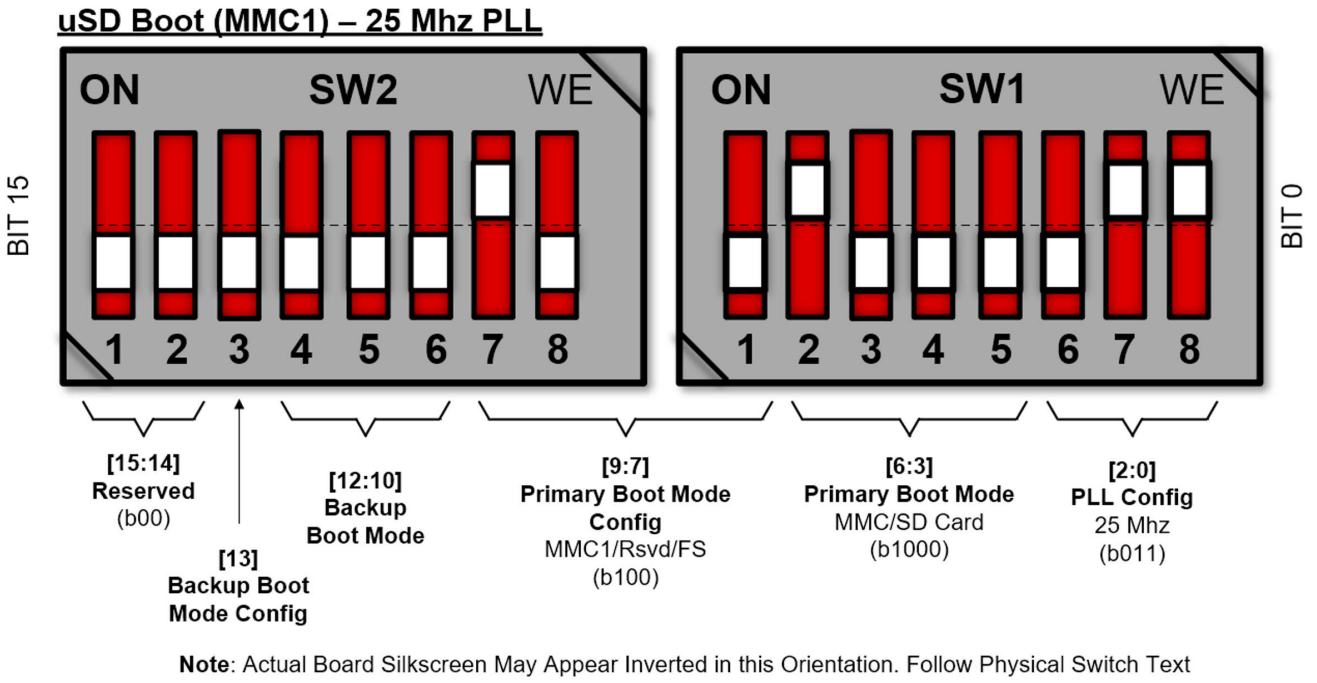


Figure 2-20. Bootmode Switch Configuration for SD Boot (E1)

The boot mode pins of the SoC have associated alternate functions during normal operation. Hence isolation is provided using Buffer IC's to cater for alternate pin functionality. The output of the buffer is connected to the bootmode pins on the AM62x and the output is enabled when the bootmode is needed during a reset cycle. The input to the buffer is connected to the DIP switch circuit and to the output of an I2C buffer set by the test automation circuit. If the test automation circuit is going to control the bootmode, all the switches will manually be set to the OFF position. The bootmode buffer should be powered by an always ON power supply to ensure that the bootmode remains present even if the SoC power is cycled.

Switch SW1 and SW2 bits [15:0] are used to set the SoC Boot mode.

The switch map to the boot mode functions is provided in the tables below.

Table 2-17. BOOT-MODE Pin Mapping

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Backup Boot Mode Configuration	Backup Boot Mode			Primary Boot Mode Configuration			Primary Boot Mode				PLL Configuration		

- BOOT-MODE [0:2] – Denote system clock frequency for PLL configuration. By default, this bits are set for 25 MHz.

Table 2-18 gives details ON PLL reference clock selection.

Table 2-18. PLL Reference Clock Selection BOOTMODE [2:0]

Bit 2	Bit 1	Bit 0	PLL REF CLK (MHz)
OFF	OFF	OFF	RSVD
OFF	OFF	ON	RSVD
OFF	ON	OFF	24
OFF	ON	ON	25
ON	OFF	OFF	26
ON	OFF	ON	RSVD

Copyright © 2026 Texas Instruments Incorporated

Table 2-18. PLL Reference Clock Selection BOOTMODE [2:0] (continued)

Bit 2	Bit 1	Bit 0	PLL REF CLK (MHz)
ON	ON	OFF	RSVD
ON	ON	ON	RSVD

- BOOT-MODE [3:6] – This provides primary boot mode configuration to select the requested boot mode after POR, that is, the peripheral/memory to boot from. Table 2-19 provides primary boot device selection details.

Table 2-19. Boot Device Selection BOOT-MODE [6:3]

Bit 6	Bit 5	Bit 4	Bit 3	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	Ethernet RGMII1
OFF	ON	OFF	ON	Ethernet RMII1
OFF	ON	ON	OFF	I2C
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMC/SD card
ON	OFF	OFF	ON	eMMC
ON	OFF	ON	OFF	USB0
ON	OFF	ON	ON	GPMC NAND
ON	ON	OFF	OFF	GPMC NOR
ON	ON	OFF	ON	Rsvd
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No boot/Dev Boot

- BOOT-MODE [10:12] – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.

Table 2-20 provides backup boot mode selection details.

Table 2-20. Backup Boot Mode Selection BOOT-MODE [12:10]

Bit 12	Bit 11	Bit 10	Backup Boot Device Selected
OFF	OFF	OFF	None (No backup mode)
OFF	OFF	ON	USB
OFF	ON	OFF	Reserved
OFF	ON	ON	UART
ON	OFF	OFF	Ethernet
ON	OFF	ON	MMC/SD
ON	ON	OFF	SPI
ON	ON	ON	I2C

- BOOT-MODE [9:7] – These pins provide optional settings and are used in conjunction with the primary boot device selected.

Table 2-21 gives primary boot media configuration details.

Table 2-21. Primary Boot Media Configuration BOOT-MODE [9:7]

Bit 9	Bit 8	Bit 7	Boot Device
Reserved	Read Mode 2	Read Mode 1	Serial NAND
Speed	Iclk	Csel	OSPI
Reserved	Iclk	Csel	QSPI

Copyright © 2026 Texas Instruments Incorporated

Table 2-21. Primary Boot Media Configuration BOOT-MODE [9:7] (continued)

Bit 9	Bit 8	Bit 7	Boot Device
Reserved	Mode	Csel	SPI
Clkout	Delay	Link stat	Ethernet RGMII
Clkout	Clk src	Reserved	Ethernet RMII
Bus Reset	Reserved	Addr	I2C
Reserved		Reserved	UART
Port	Reserved	Fs/raw	MMC/ SD card
Reserved		voltage	eMMC
Reserved	Mode	Lane swap	USB0
Reserved			GPMC NAND
Reserved			GPMC NOR
Reserved			Reserved
SFDP	Read Cmd	Mode	xSPI
Reserved		No/Dev	No boot/Dev Boot

- BOOT-MODE [13] – These pins provide optional settings and are used in conjunction with the backup boot device devices. Switch SW2.6 when ON sets 1 and sets 0 if OFF, see the device-specific TRM.
- BOOT-MODE [14:15] – Reserved.

Table 2-22 provides backup boot media configuration options.

Table 2-22. Backup Boot Media Configuration BOOT-MODE [13]

Bit 13	Boot Device
Reserved	None
Mode	USB
Reserved	Reserved
Reserved	UART
IF	Ethernet
Port	MMC/SD
Reserved	SPI
Reserved	I2C

2.1.6.16.3 User Test LEDs

The AM62x SKEVM board contains two LEDs for user defined functions.

Table 2-23 indicates the User test LEDs and the associated GPIOs used to control it.

Table 2-23. User test LEDs

Sl No.	LED	GPIO Used	SCH Net Names
1	LD1	GPIO1_49	SOC_GPIO1_49
2	LD11	U70.24(P27)	IO_EXP_TEST_LED

2.1.6.17 Expansion Headers

AM62x SKEVM features three expansion Headers, the 40 pin User expansion connector, 20 pin PRU Header and the 28 pin MCU Header.

2.1.6.17.1 PRU Connector

AM62x SKEVM has a 20 pin PRU Header which offers Low speed connection to the PRG0 Interface.

PRU_ICSSG signals from PRG0 Port (PRG0_PRU0) are connected to a 10x2 standard 0.1” spaced Receptacle connector Mfr Part # PREC010DAAN-RC. The connector features PR0_PRU0_GPO [0: 7], SoC_I2C0, +3.3V PWR and Ground reference. INTn signal from PRU Header is wired along with the CPSW PHY interrupts and connected to the EXTINTn pin of the SoC.

Copyright © 2026 Texas Instruments Incorporated

The 3.3V supply is current limited to 500mA. This is achieved by using load switch TPS22902YFPR. Enable for the load switch is controlled by IO expander. Signals routed from the PRU Connector are listed in Table 2-24

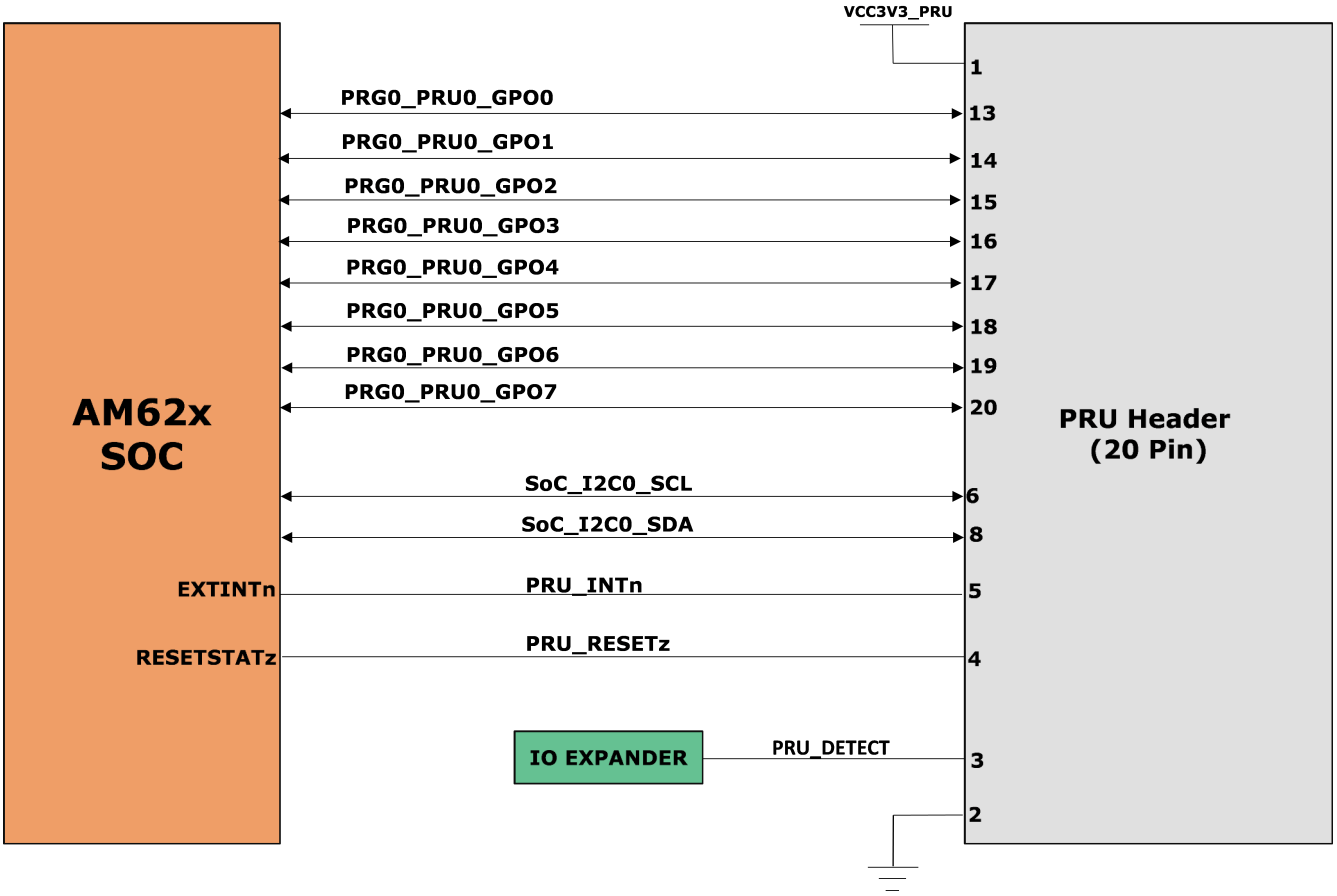


Table 2-24. PRU Header (J10) Pin-out

Pin No.	SoC Ball No.	Net name	Pin Multiplexed signal
1	-	VCC3V3_PRU	
2	-	DGND	
3	-	PRU_DETECT	
4	F22	PRU_RESETz	RESETSTATz
5	D16	PRU_INTn	EXTINTn/ GPIO1_31
6	B16	SoC_I2C0_SCL	I2C0_SCL/ PR0_IEP0_EDIO_DATA_IN_OUT30/ SYNC0_OUT/ OBSCLK0/ UART1_DCDn/ EQEP2_A EHRPWM_SOCA/ GPIO1_26/ ECAP1_IN_APWM_OUT / SPI2_CS0
7	-	NC	
8	A16	SoC_I2C0_SDA	I2C0_SDA/ PR0_IEP0_EDIO_DATA_IN_OUT31/ SPI2_CS2/ TIMER_IO5/ UART1_DSRn/ EQEP2_B/ EHRPWM_SOCB/ GPIO1_27/ ECAP2_IN_APWM_OUT
9		NC	
10	-	NC	
11	-	NC	
12	-	NC	
13	M25	PR0_PRU0_GPO0	GPMC0_AD0/ PR0_PRU1_GPO8/ PR0_PRU1_GPI8/ MCASP2_AXR4/ PR0_PRU0_GPO0/ PR0_PRU0_GPI0/ TRC_CLK/ GPIO0_15/ DDR0_IO_PLL_TESTOUT0P/ DDR0_IO_PLL_TESTOUT1P/ GPIO1_112/ LED_DIO0
14	N23	PR0_PRU0_GPO1	GPMC0_AD1/ PR0_PRU1_GPO9/ PR0_PRU1_GPI9/ MCASP2_AXR5/ PR0_PRU0_GPO1/ PR0_PRU0_GPI1/ TRC_CTL/ GPIO0_16/ DDR0_IO_PLL_REFCLK_TEST0P/ DDR0_IO_PLL_REFCLK_TEST1P/ GPIO1_113/ LED_DIO1

Copyright © 2026 Texas Instruments Incorporated

Table 2-24. PRU Header (J10) Pin-out (continued)

Pin No.	SoC Ball No.	Net name	Pin Multiplexed signal
15	N24	PR0_PRU0_GPO2	GPMC0_AD2/ PR0_PRU1_GPO10/ PR0_PRU1_GPI10/ MCASP2_AXR6/ PR0_PRU0_GPO2/ PR0_PRU0_GPI2/ TRC_DATA0/ GPIO0_17
16	N25	PR0_PRU0_GPO3	GPMC0_AD3/PR0_PRU1_GPO11/PR0_PRU1_GPI11/MCASP2_AXR7/PR0_PRU0_GPO3/ PR0_PRU0_GPI3/TRC_DATA1/GPIO0_18
17	P24	PR0_PRU0_GPO4	GPMC0_AD4/PR0_PRU1_GPO12/PR0_PRU1_GPI12/MCASP2_AXR8/PR0_PRU0_GPO4/ PR0_PRU0_GPI4/TRC_DATA2/GPIO0_19
18	P22	PR0_PRU0_GPO5	GPMC0_AD5/PR0_PRU1_GPO13/PR0_PRU1_GPI13/MCASP2_AXR9/PR0_PRU0_GPO5/ PR0_PRU0_GPI5/TRC_DATA3/GPIO0_20
19	P21	PR0_PRU0_GPO6	GPMC0_AD6/PR0_PRU1_GPO14/PR0_PRU1_GPI14/MCASP2_AXR10/PR0_PRU0_GPO6/ PR0_PRU0_GPI6/TRC_DATA4/GPIO0_21
20	R23	PR0_PRU0_GPO7	GPMC0_AD7/PR0_PRU1_GPO15/PR0_PRU1_GPI15/MCASP2_AXR11/PR0_PRU0_GPO7/ PR0_PRU0_GPI7/TRC_DATA5/GPIO0_22

2.1.6.17.2 User Expansion Connector

The AM62x SKEVM supports RPi expansion interface using a 40-pin User expansion connector Mfr. Part# PEC20DAAN. Four mounting holes must be oriented with the connector to allow for connection of these boards.

Following interfaces and IOs shall be included on to the 40 pin User Expansion connector.

- 2x SPI : SPI0 with 2 CS and SPI2 with 3 CS
- 2x I2C: SoC_I2C0 and SoC_I2C2
- 1x UART: UART5
- 2x PWM: EHRPWM0_A, EHRPWM1_B
- 1x CLK: CLKOUT0
- 9x GPI0: GPIOs from main domain
- 5V and 3.3V supply (current limited to 155mA and 500mA)

Each of the power supplies 5 V and 3.3 V are current limited to 155 mA and 500 mA, respectively. This is achieved by using two individual load switch TPS22902YFPR and TPS22946YZPR. Enable for the load switches is driven by I2C based GPIO Port expander.

Signals routed from User Expansion connector are listed in Table 2-25.

Table 2-25. 40 Pin User Expansion Connector

Pin No.	SoC Ball	Net Name	Pin Multiplexed Signals
1	-	VCC3V3_EXP	
2	-	VCC5V0_EXP	
3	K24	SoC_I2C2_SDA	GPMC0_CSN3/ GPMC0_A20/ UART4_TXD/ MCASP1_AXR5/ TRC_DATA18/ GPIO0_44/ MCASP1_ACLKR
4	-	VCC5V0_EXP	
5	K22	SoC_I2C2_SCL	GPMC0_CSN2/ MCASP1_AXR4/ UART4_RXD/ PR0_PRU0_GPO19/ PR0_PRU0_GPI19/ TRC_DATA17/ GPIO0_43/ MCASP1_AFSR
6	-	DGND	
7	A18	EXP_CLKOUT0	EXT_REFCLK1/ SYNC1_OUT/ SPI2_CS3/ SYSCLKOUT0/ TIMER_IO4/ CLKOUT0/ CP_GEMAC_CPTS0_RFT_CLK/ GPIO1_30/ ECAP0_IN_APWM_OUT
8	E15	EXP_UART5_TXD	UART5_TXD/ TIMER_IO3/ SYNC3_OUT/ UART1_RIn/ EQEP2_S/ PR0_UART0_TXD/ GPIO1_25/ MCASP2_AXR1/ EHRPWM_TZn_IN4
9	-	DGND	
10	C15	EXP_UART5_RXD	UART5_RXD/ TIMER_IO2/ SYNC2_OUT/ UART1_DTRn/ EQEP2_I/ PR0_UART0_RXD/ GPIO1_24/ MCASP2_AXR0/ EHRPWM_TZn_IN3

Copyright © 2026 Texas Instruments Incorporated

Table 2-25. 40 Pin User Expansion Connector (continued)

Pin No.	SoC Ball	Net Name	Pin Multiplexed Signals
11	B20	EXP_SPI2_CS1	MCASP0_ACLKX/ SPI2_CS1/ ECAP2_IN_APWM_OUT/ GPIO1_11/ EQEP1_A
12	E19	EXP_SPI2_CS0/EHRPWM0_A	MCASP0_AFSR/ SPI2_CS0/ UART1_RXD/ EHRPWM0_A/ GPIO1_13/ EQEP1_S
13	L21	EXP_GPIO0_42	GPMC0_CSn1/ PR0_PRU1_GPO16/ PR0_PRU1_GPI16/ MCASP2_AXR15/ PR0_PRU0_GPO18/ PR0_PRU0_GPI18/ TRC_DATA16/ GPIO0_42
14	-	DGND	
15	L23	EXP_GPIO0_32	GPMC0_ADVn_ALE/ MCASP1_AXR2/ PR0_PRU0_GPO9/ PR0_PRU0_GPI9/ TRC_DATA7/ GPIO0_32
16	V25	EXP_GPIO0_38	GPMC0_WAIT1/ VOUT0_EXTPCLKIN/ GPMC0_A21/ UART6_RXD/ GPIO0_38/ EQEP2_I
17	-	VCC3V3_EXP	
18	K25	EXP_GPIO0_39	GPMC0_WPn/ AUDIO_EXT_REFCLK1/ GPMC0_A22/ UART6_TXD/ PR0_PRU0_GPO15/ PR0_PRU0_GPI15/ TRC_DATA13/ GPIO0_39
19	B13	EXP_SPI0_D0	SPI0_D0/ CP_GEMAC_CPTS0_HW1TSPUSH/ EHRPWM1_B/ GPIO1_18
20	-	DGND	
21	B14	EXP_SPI0_D1	SPI0_D1/ CP_GEMAC_CPTS0_HW2TSPUSH/ HRPWM_TZn_IN0/ GPIO1_19
22	E24	EXP_GPIO0_14	OSPI0_CSn3/ OSPI0_RESET_OUT0/ OSPI0_ECC_FAIL/ MCASP1_ACLKR/ MCASP1_AXR3/ UART5_TXD/ GPIO0_14
23	A14	EXP_SPI0_CLK	SPI0_CLK/ CP_GEMAC_CPTS0_TS_SYNC/ EHRPWM1_A/ GPIO1_17
24	A13	EXP_SPI0_CS0	SPI0_CS0/ EHRPWM0_A/ PR0_ECAP0_SYNC_IN/ GPIO1_15
25	-	DGND	
26	C13	EXP_SPI0_CS1	SPI0_CS1/ CP_GEMAC_CPTS0_TS_COMP/ EHRPWM0_B/ ECAP0_IN_APWM_OUT/ GPIO1_16/ EHRPWM_TZn_IN5
27	A16	SoC_I2C0_SDA	I2C0_SDA/ PR0_IEP0_EDIO_DATA_IN_OUT31/ SPI2_CS2/ TIMER_IO5/ UART1_DSRn/ EQEP2_B/ EHRPWM_SOCB/ GPIO1_27/ ECAP2_IN_APWM_OUT
28	B16	SoC_I2C0_SCL	I2C0_SCL/ PR0_IEP0_EDIO_DATA_IN_OUT30/ SYNC0_OUT/ OBSCLK0/ UART1_DCDn/ EQEP2_A EHRPWM_SOCA/ GPIO1_26/ ECAP1_IN_APWM_OUT / SPI2_CS0
29	N20	EXP_GPIO0_36	GPMC0_BE1n/ MCASP2_AXR12/ PR0_PRU0_GPO13/ PR0_PRU0_GPI13/ TRC_DATA11/ GPIO0_36
30	-	DGND	
31	L24	EXP_GPIO0_33	GPMC0_OEn_REn/ MCASP1_AXR1/ PR0_PRU0_GPO10/ PR0_PRU0_GPI10/ TRC_DATA8/ GPIO0_33
32	M22	EXP_GPIO0_40/ PR0_ECAP0_IN_APWM_OUT	GPMC0_DIR/ PR0_ECAP0_IN_APWM_OUT/ MCASP2_AXR13/ PR0_PRU0_GPO16/ PR0_PRU0_GPI16/ TRC_DATA14/ GPIO0_40/ EQEP2_S
33	E18	EXP_EHRPWM1_B	MCASP0_AXR0/ PR0_ECAP0_IN_APWM_OUT/ AUDIO_EXT_REFCLK0/ PR0_UART0_TXD/ EHRPWM1_B/ GPIO1_10/ EQEP0_I
34	-	DGND	

Copyright © 2026 Texas Instruments Incorporated

Table 2-25. 40 Pin User Expansion Connector (continued)

Pin No.	SoC Ball	Net Name	Pin Multiplexed Signals
35	A19	EXP_SPI2_D1/ ECAP2_IN_APWM_OUT	MCASP0_AXR2/ SPI2_D1/ UART1_RTSn/ UART6_TXD/ PR0_IEP0_EDIO_DATA_IN_OUT29/ ECAP2_IN_APWM_OUT/ PR0_UART0_TXD/ GPIO1_8/ EQEP0_B
36	B18	EXP_SPI2_CS2	MCASP0_AXR1/ SPI2_CS2/ ECAP1_IN_APWM_OUT/ PR0_UART0_RXD/ EHRPWM1_A/ GPIO1_9/ EQEP0_S
37	M21	EXP_GPIO0_41	GPMC0_CSn0/ MCASP2_AXR14/ PR0_PRU0_GPO17/ PR0_PRU0_GPI17/ TRC_DATA15/ GPIO0_41
38	B19	EXP_SPI2_D0	MCASP0_AXR3/ SPI2_D0/ UART1_CTSn/ UART6_RXD/ PR0_IEP0_EDIO_DATA_IN_OUT28/ ECAP1_IN_APWM_OUT/ PR0_UART0_RXDGPIO1_7 EQEP0_A
39	-	EXP_HAT_DETECT	
40	A20	EXP_SPI2_CLK	MCASP0_ACLKR/ SPI2_CLK/ UART1_TXD/ EHRPWM0_B/ GPIO1_14/ EQEP1_I

2.1.6.17.3 MCU Connector

AM62x SKEVM has a 14x2 standard 0.1” spaced MCU connector which includes signals connected to the MCU Domain of SoC. 13 Signals include MCU_I2C0, MCU_UART0 (with flow control), MCU_SPI0 and MCU_MCAN0 signals are connected to the MCU Header. Additional control signals provided on the Header include CONN_MCU_RESETz, CONN_MCU_PORz, MCU_RESETSTATz, MCU_SAFETY_ERRORn, 3.3 V IO and GND. MCU_UART0 signals from AM62x SoC are connected to both MCU Header and FT4232 Bridge through MUX Mfr Part # SN74CB3Q3257PWR. The MCU Header does not include the Board ID memory interface. Allowed current limit is 100 mA on 3.3 V rail.

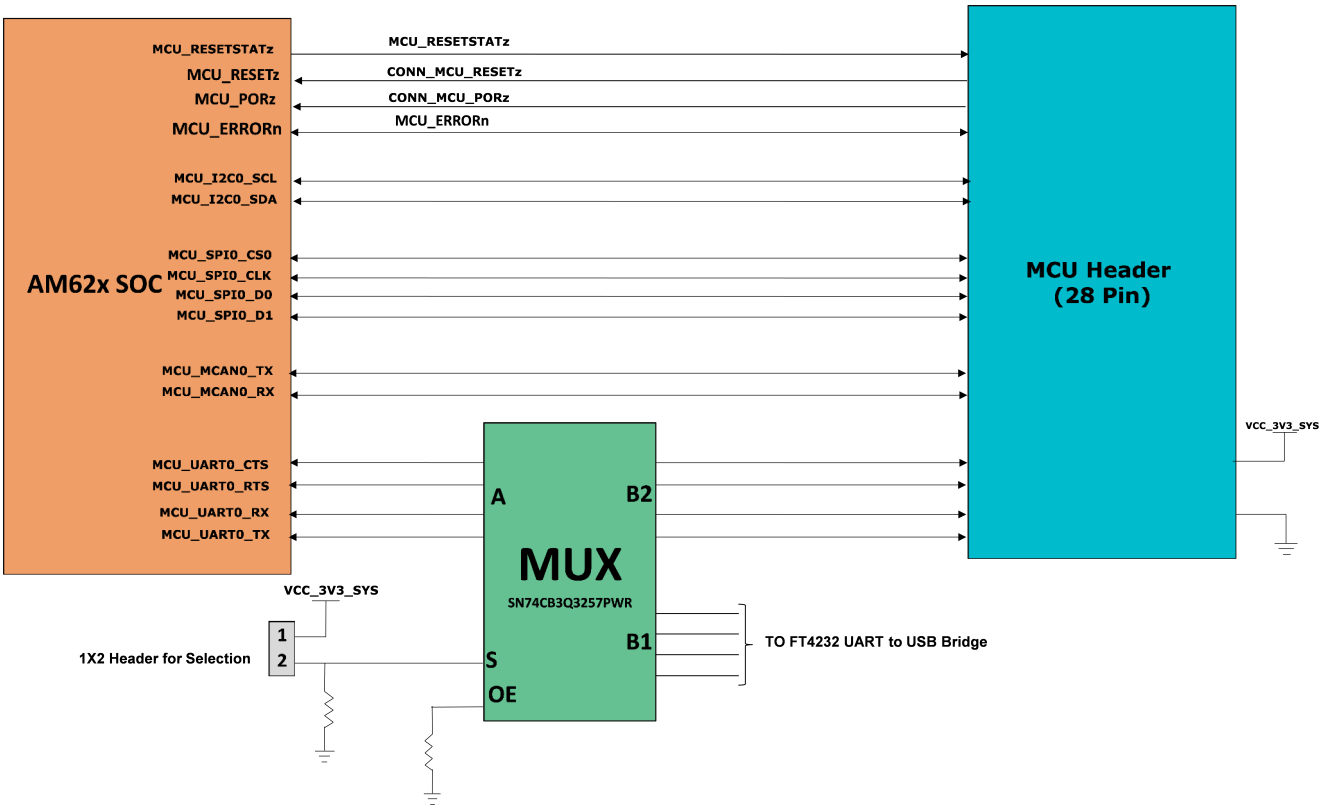


Table 2-26. Pin MCU Connector (J9)

Pin No.	SoC Ball No.	Net Name	Pin Multiplexed Signal
1	-	VCC_3V3_SYS	

Copyright © 2026 Texas Instruments Incorporated

Table 2-26. Pin MCU Connector (J9) (continued)

Pin No.	SoC Ball No.	Net Name	Pin Multiplexed Signal
2	-	DGND	
3	-	NC	
4	C9	MCU_SPI0_D1	MCU_SPI0_D1/MCU_GPIO0_4
5	-	NC	
6	D9	MCU_SPI0_D0	MCU_SPI0_D0/MCU_GPIO0_3
7	-	DGND	
8	B8	MCU_SPI0_CS1	MCU_SPI0_CS1/ MCU_OBSCLK0/ MCU_SYSCLKOUT0/ MCU_EXT_REFCLK0/ MCU_TIMER_IO1/ MCU_GPIO0_1
9	-	NC	
10	E5	MCU_GPIO0_15	MCU_MCAN1_TX/ MCU_TIMER_IO2/ MCU_SPI1_CS1/ MCU_EXT_REFCLK0/ MCU_GPIO0_15
11	D4	MCU_GPIO0_16	MCU_MCAN1_RX/ MCU_TIMER_IO3/ MCU_SPI0_CS2/ MCU_SPI1_CS2/ MCU_SPI1_CLK/ MCU_GPIO0_16
12	A6	MCU_UART0_CTS_CONN	MCU_UART0_CTSn/ MCU_TIMER_IO0/ MCU_SPI1_D0/MCU_GPIO0_7
13	B5	MCU_UART0_RXD_CONN	MCU_UART0_RXD/ MCU_GPIO0_5
14	-	NC	
15	-	DGND	
16	D6	MCU_MCAN0_TX	MCU_MCAN0_TX/ WKUP_TIMER_IO0/ MCU_SPI0_CS3/ MCU_GPIO0_13
17	B6	MCU_UART0_RTS_CONN	MCU_UART0_RTSn/ MCU_TIMER_IO1/ MCU_SPI1_D1/MCU_GPIO0_8
18	A7	MCU_SPI0_CLK	MCU_SPI0_CLK/MCU_GPIO0_2
19	A5	MCU_UART0_TXD_CONN	MCU_UART0_TXD/ MCU_GPIO0_6
20	-	DGND	
21	D10	MCU_I2C0_SDA	MCU_I2C0_SDA/ MCU_GPIO0_18
22	B3	MCU_MCAN0_RX	MCU_MCAN0_RX/ MCU_TIMER_IO0/ MCU_SPI1_CS3/ MCU_GPIO0_14
23	B12	MCU_RESETSTATz	MCU_RESETSTATz/ MCU_GPIO0_21
24	A8	MCU_I2C0_SCL	MCU_I2C0_SCL/ MCU_GPIO0_17
25	E11	CONN_MCU_RESETz	MCU_RESETz
26	D1	MCU_SAFETY_ERRORz_3V3	MCU_ERRORN
27	-	DGND	

Copyright © 2026 Texas Instruments Incorporated

Table 2-26. Pin MCU Connector (J9) (continued)

Pin No.	SoC Ball No.	Net Name	Pin Multiplexed Signal
28	D2	CONN_MCU_PORz	MCU_PORz

2.1.6.18 Interrupt

AM62x SKEVM supports two interrupts for providing Reset input and User Interrupt to the processor.

The interrupt are push buttons placed on the Top side of the Board and are listed in Table 2-27

Table 2-27. EVM Push Buttons

Sl No.	Push Buttons	Signal	Function
1	SW3	SoC_WARM_RESETZ	Main domain Warm Reset input
2	SW4	GPIO_MCU	Generates interrupt on MCU_GPIO0_15

2.1.6.19 I2C Address Mapping

There are three I2C interfaces used in SK EVM board:

- SoC_I2C0 Interface: SoC I2C [0] is connected to Board ID EEPROM, User Expansion Connector Header, USB PD controler, PRU header, and OLDI Display Touch interface.
- SoC I2C (1) Interface: SoC I2C [1] is connected to Test Automation Header, Current Monitors, Temperature Sensors, Audio Codec, HDMI Transmitter, CSI Camera Connector, GPIO Port Expander.
- SoC I2C (2) Interface: Connected I2C [2] from SoC to the User Expansion Connector Header
- MCU I2C (0) Interface: Connected MCU I2C [0] to MCU Header.
- WKUP I2C (0) Interface: Connected I2C [0] from SoC to LED Driver

The images below depict the I2C tree and the tables provide the complete I2C address mapping details on AM62x SKEVM.

Copyright © 2026 Texas Instruments Incorporated

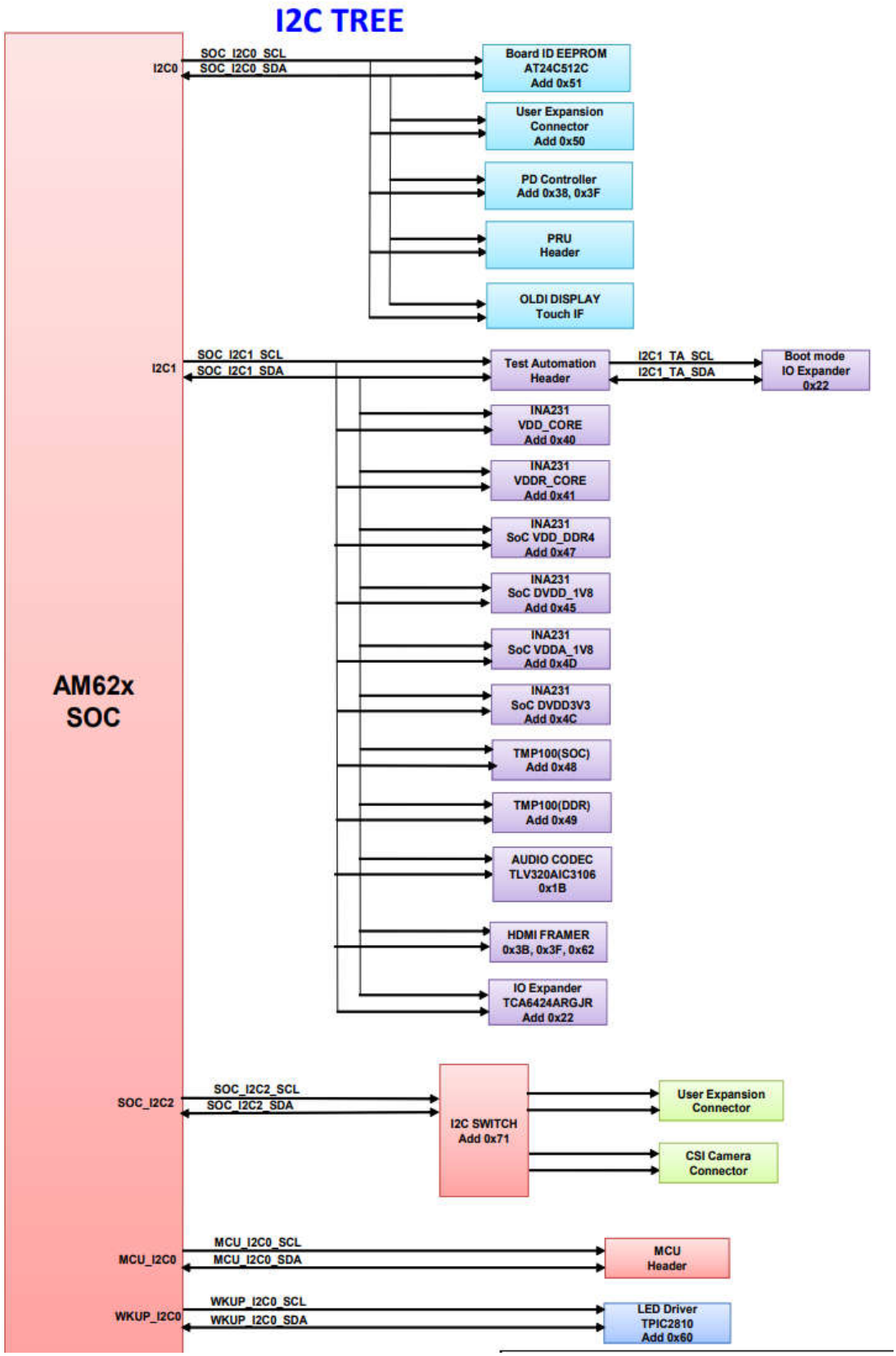


Table 2-28. I2C Mapping Table (SK-AM62 E3 and SK-AM62-P1 Variants)

I2C Port	Device/Function	Part No.	I2C Address
SoC_I2C0	Board ID EEPROM	AT24C512C-MAHM-T	0x51
SoC_I2C0	User Expansion Connector	<connector interface>	

Copyright © 2026 Texas Instruments Incorporated

Table 2-28. I2C Mapping Table (SK-AM62 E3 and SK-AM62-P1 Variants) (continued)

I2C Port	Device/Function	Part No.	I2C Address
SoC_I2C0	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
SoC_I2C0	PRU Header	<connector interface>	
SoC_I2C0	OLDI Display Touch Interface		
SoC_I2C1	Test Automation Header	<connector interface>	
SoC_I2C1	Current Monitors	INA231AIYFDR	0x40, 0x41, 0x47, 0x45, 0x4D, 0x4C
SoC_I2C1	Temperature Sensors	TMP100NA/3K	0x48, 0x49
SoC_I2C1	Audio Codec	TLV320AIC3106IRGZT	0x1B
SoC_I2C1	HDMI Transmitter	SiI9022ACNU	0x3B, 0x3F, 0x62
SoC_I2C1	GPIO Port Expander	TCA6424ARGJR	0x22
SoC_I2C2	CSI Camera Connector		
SoC_I2C2	User Expansion Connector	<connector interface>	
MCU_I2C0	MCU Header	<connector interface>	
WKUP_I2C0	LED Driver	TPIC2810D	0x60
Others			
BOOTMODE_I2C	I2C Bootmode Buffer	TCA6424ARGJR	0x22
BOOTMODE_I2C	Test Automation Header	<connector interface>	

Copyright © 2026 Texas Instruments Incorporated

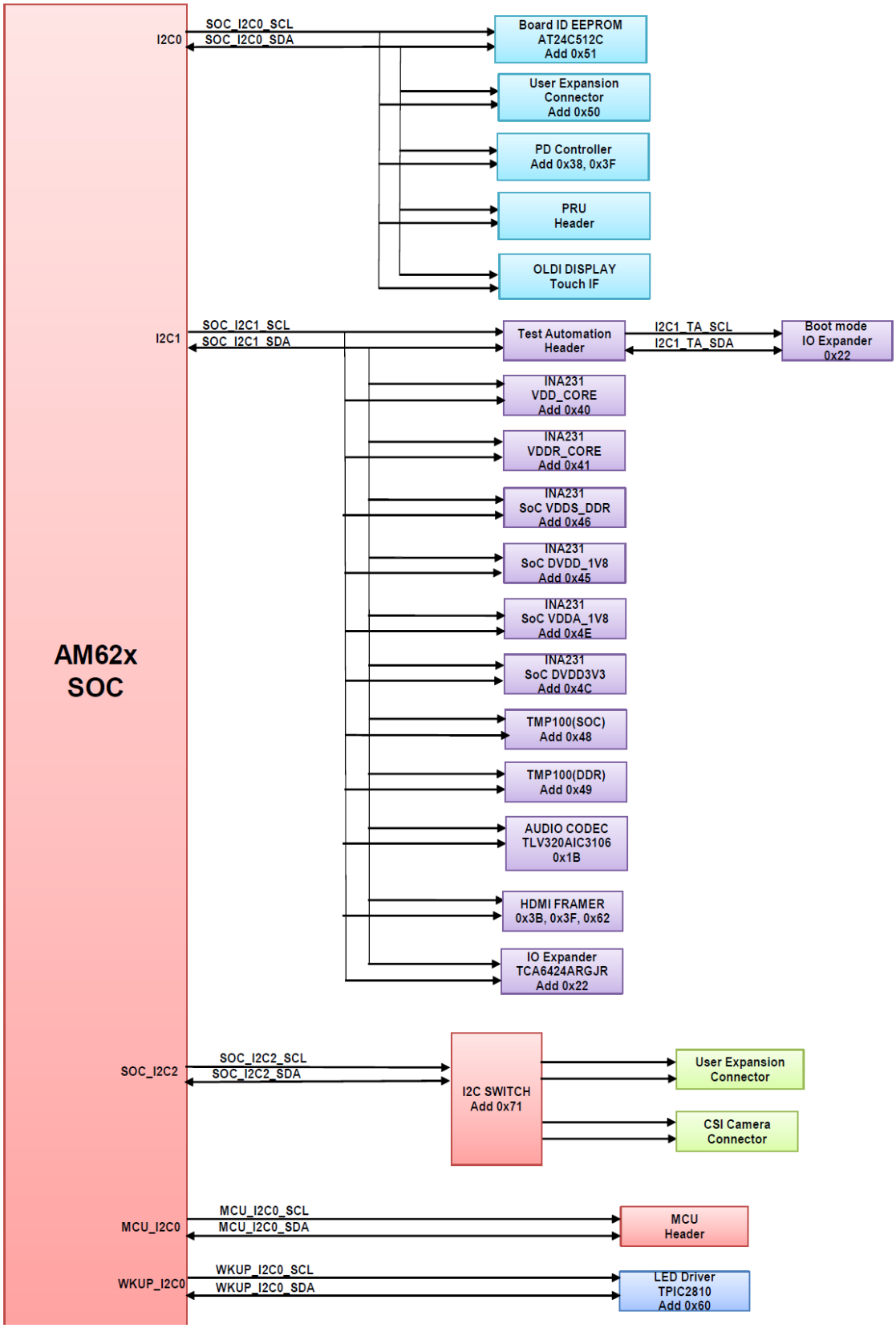


Table 2-29. I2C Mapping Table (SK-AM62 E2)

I2C Port	Device/Function	Part No.	I2C Address
SoC_I2C0	Board ID EEPROM	AT24C512C-MAHM-T	0x51
SoC_I2C0	User Expansion Connector	<connector interface>	

Copyright © 2026 Texas Instruments Incorporated

Table 2-29. I2C Mapping Table (SK-AM62 E2) (continued)

I2C Port	Device/Function	Part No.	I2C Address
SoC_I2C0	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
SoC_I2C0	PRU Header	<connector interface>	
SoC_I2C0	OLDI Display Touch Interface		
SoC_I2C1	Test Automation Header	<connector interface>	
SoC_I2C1	Current Monitors	INA231AIYFDR	0x40, 0x41, 0x46, 0x45, 0x4E & 0x4C
SoC_I2C1	Temperature Sensors	TMP100NA/3K	0x48, 0x49
SoC_I2C1	Audio Codec	TLV320AIC3106IRGZT	0x1B
SoC_I2C1	HDMI Transmitter	SiI9022ACNU	0x3B, 0x3F, 0x62
SoC_I2C1	GPIO Port Expander	TCA6424ARGJR	0x22
SoC_I2C2	CSI Camera Connector		
SoC_I2C2	User Expansion Connector	<connector interface>	
MCU_I2C0	MCU Header	<connector interface>	
WKUP_I2C0	LED Driver	TPIC2810D	0x60
Others			
BOOTMODE_I2C	I2C Bootmode Buffer	TCA6424ARGJR	0x22
BOOTMODE_I2C	Test Automation Header	<connector interface>	

Copyright © 2026 Texas Instruments Incorporated

3 Additional Information

3.1 EVM Revisions and Assembly Variants

The various AM62x SK EVM PCB design revisions, and asssembly variants are listed in the table below. Specific PCB revision is indicated in silkscreen on the PCB. Specific assembly variant is indicated with additional sticker label.

Table 3-1. SK EVM PCB Design Revisions and Asssembly Variants

OPN	PCB Revison	Assembly Variant	Revision and Assembly Variant Description
SK-AM62	PROC114E1	N/A (single variant produced)	First prototype, early release revision of the AM62x SK EVM. Implements the Sitara™ AM62x MPU with a discrete power design
SK-AM62	PROC114E2	N/A	Second prototype, early release revision of the AM62x SK EVM. Implements a number of changes and bug fixes focused on enabling 24 bit RGB output via HDMI.
SK-AM62	PROC114E3	N/A	Third prototype, early release revision of the AM62x SK EVM. Implements a number of changes around LVDS and multimedia peripherals.
SK-AM62B	PROC114A	002	Production release of AM62x SK EVM discrete version. Implements HS-FS version of SoC.
SK-AM62-P1	PROC142E1	N/A	First prototype, early release version of the AM62x SK EVM. implementing the TPS65219 PMIC.
SK-AM62B-P1	PROC142A	002	Production release of AM62x SK EVM PMIC version. Implements HS-FS version of SoC.
SK-AM62B-P1	PROC142B	002	Production release of AM62x SK EVM PMIC version, updated few designs and Known issues.

3.2 Known Issues and Modifications

This section describes the currently known issues on each EVM revision and applicable workarounds. Issues that have been patched have modification labels attached to the EVM assembly.

Table 3-2. AM62x SK EVM Known Issues and Modifications

Issue Number	Issue Title	Issue Description	Variant Affected
1	HDMI, DSS Incorrect Colors	HDMI Transmitter on E1 boards shows incorrect colors.	E1
2	J9 and J10 Header Allignment	MCU and PRU headers are missaligned on E1	E1
3	USB Boot Descoped on E1	USB Boot is not available on E1 boards	E1
4	OLDI Connector Orientation and Pinout	OLDI Connector Pinout changed and an adapter is required for E1/E2 boards.	E1, E2
5	Bluetooth Descoped on E2	Bluetooth does not work on E2 boards.	E1, E2
6	Ethernet PHY CLK Skew default Strapping	Default PHY Tx CLK Skew needs to be set to 0ns	E1, E2
7	TEST_POWERDOWN signals shorted	Resistor change required to avoid backflow from VMain	E1, E2
8	SD Card Detect Signal	MMC1_SDCD line can cause spurious interrupts to the SoC under certain conditions.	E1, E2
9	PD Controller I2C2 IRQ Not Pinned Out	I2C_IRQ signal from PD controller not pinned out resulting in problems with regard to USB Host and Device mode operation.	E1, E2
10	INA Current Monitor Adress Changes	INA adress lines changed to adress spurious address changes.	E1, E2

Copyright © 2026 Texas Instruments Incorporated

Table 3-2. AM62x SK EVM Known Issues and Modifications (continued)

Issue Number	Issue Title	Issue Description	Variant Affected
11	Test Automation I2C Buffer Changes	Issues with a buffer IC type resulted in issues accesing I2C1 bus from the Test Automation interface.	E1, E2, E3
12	ODLI Display Touch Broken	OLDI Display touch function not working after powering on the EVM	E3, Rev A

3.2.1 Issue 1 - HDMI/DSS Incorrect Colors on E1

Applicable EVM Revisions: E1

Issue Description: Due to incorrect wiring for YUV 422 of the AM62x DSS Output to the SIL9022A HDMI Transmitter, colors will appear yellow on E1 boards.

Fix: AM62x SK EVM E2 and onwards have moved to a full 24bit RGB 888 color output which also features expanded color space as a result.

3.2.2 Issue 2 - J9 and J10 Header Alignment on E1

Applicable EVM Revisions: E1

Issue Description: On revision E1 of the AM62x SK EVM, the J9 and J10 are missaligned by one set of pins, meaning that boards designed for other Sitara SK EVMs that mate to both the MCU and PRU headers will not fit on this revision.

Fix: Revisions E2 and newer align the headers as expected.

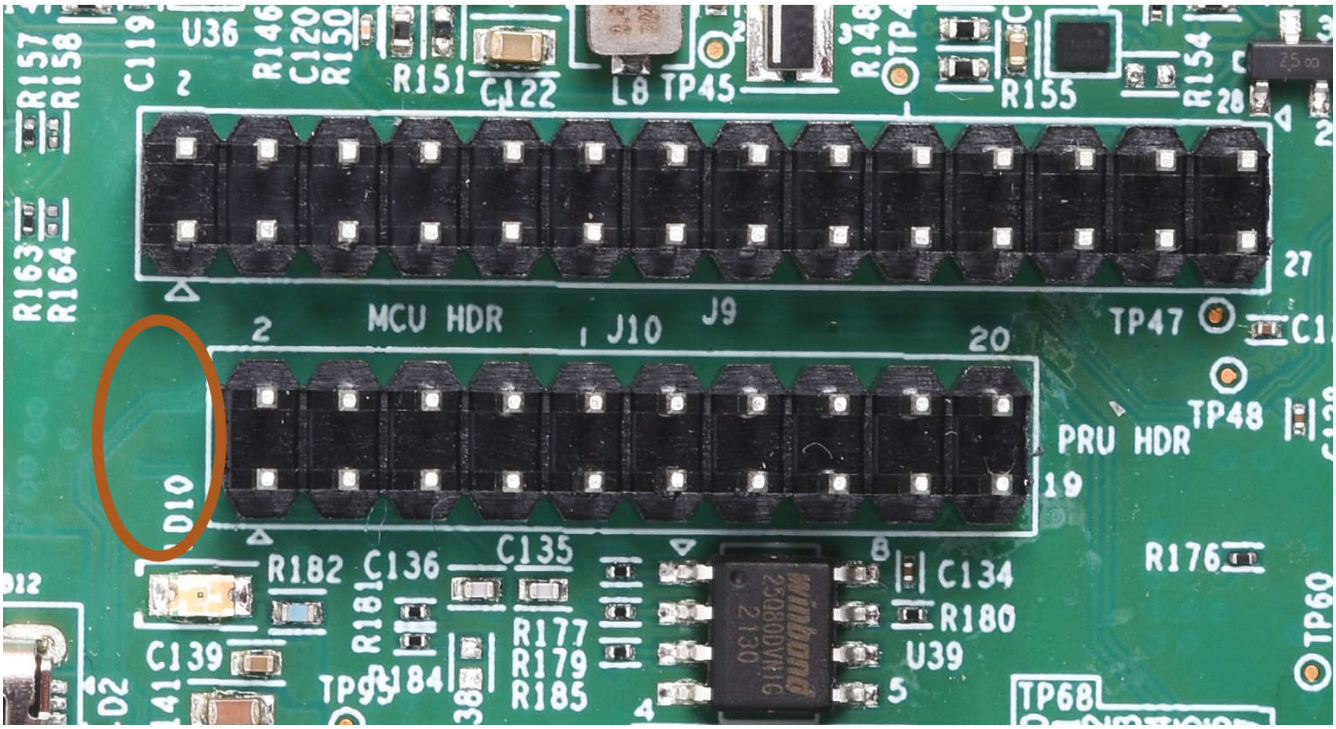


Figure 3-1. PRU Connector Missalignment on E1 Boards

3.2.3 Issue 3 - USB Boot descoped on E1

Applicable EVM Revisions: E1

Issue Description: Due to the USB0 port being routed through a Hub IC to the Type-A connector, USB boot cannot be supported on E1 boards.

Copyright © 2026 Texas Instruments Incorporated

Fix: E2 boards and newer use USB1 to the type-A connector and have moved the USB0 controller used for boot to the second USB Type-C port so that both DFU and MSC boot can be supported. The USB hub IC has also been dropped to simplify board layout and BOM.

3.2.4 Issue 4 - OLDI Connector Orientation and Pinout

Applicable EVM Revisions: E1, E2

Issue Description: The OLDI Connector Pinout was updated after version E2 in order to improve the differential routing on the cable. Please refer to Section 2.1.6.3 for the pinout change details.

Important Note: An adapter is required in order to enable E1 & E2 boards to connect to the TI recommended OLDI displays. DO NOT ATTEMPT to plug in an E1 or E2 board into such an LCD without the adapter.

3.2.5 Issue 5 - Bluetooth descoped on E2 EVMs

Applicable EVM Revisions: E2

Issue Description: Due to incorrect wiring of both RX and TX UART signals on the same channel of the U3 buffer, Bluetooth functioanlity is not supported on the E2 version of the EVM. This does not affect E1 EVMs and will be fixed on E3 and onwards.

3.2.6 Issue 6 - Ethernet PHY CLK Skew Default Strapping Changes

Applicable EVM Revisions: E1, E2

Issue Description: RGMII1 and RGMII2 PHYs (U51and U49) had strapping resistors for Tx Clock Skew = 2ns. Tx Clock skew should be set to 0ns as AM62x MAC always has internal delay enabled for Tx. Rx Clock Skew should remain 2ns.

3.2.7 Issue 7 - TEST_POWERDOWN changes

Applicable EVM Revisions: E1, E2

Issue Description: TEST_POWERDOWN (pulled up to VCC3V3_TA) and VCC_5V0_EN (pulled up to VMAIN) signals were shorted through a 0 ohm resistor. To avoid backflow from VMAIN, a pull up resistor on VCCC_5V0_EN connected to VMAIN is made DNI and R585 is mounted which is pulled to VCC3V3_TA

3.2.8 Issue 8 - MMC1_SDCD spurious interrupts

Applicable EVM Revisions: E2, E1

Issue Description: The MMC1_SDCD line was abserved to go low, causing spurious interrupts to the SoC when VDD_MMC1_SD supply went low.

Fix: VCC of the U18 ESD chip is connected to the VCC_3V3_SYS rail instead.

3.2.9 Issue 9 - PD Controller I2C2 IRQ Not Pinned Out

Applicable EVM Revisions: E2, E1

Issue Description:

The I2C_IRQ signal was required from the PD controller to read the I2C register changes of the controller with regard to USB Host and Device mode operation

Fix: I2C2_IRQ from the PD Controller is connected to IO EXP GPIO P21 (U70.18) and TEST_GPIO2 is terminated to a Test Point.

3.2.10 Issue 10 - INA Current Monitor Adress Changes

Applicable EVM Revisions: E2, E1

Issue Description:

The Adress pins of the INA devices which were tied to SDA lines could cause spurious adress changes depending on how the bus was initialized.

Fix:U23 and U25 were moved to 0x4D and 0x47 by using the remainnig combinations of VCC/GND and SCL.

Copyright © 2026 Texas Instruments Incorporated

3.2.11 Issue 11 - Test Automation I2C Buffer Changes

Applicable EVM Revisions: E1, E2, E3

Issue Description:

The buffers used for the Test Automation Interface have a special condition of not having pullups on the B side of the buffer which could not be met on the EVM due to the bus design. As such, in the current configuration, they prevent communiation from the Test Automation connector into the I2C1 bus.

Fix: Remove the TCA9801DGK buffers and bridge across pin 2 to pin 7 and pin 3 to pin 6 respectively, you will also need to remove any pull-up resistors on the SCLB side of the device since these are no longer needed. (U42 and R499, R498 on E3, please refer to inidividual scheamtics and board file for other revisions). The IC may be replaced with a **TCA9517DR** which does not have the same incomaptibiltiy. SK-AM62-P1 E2 and newer boards feature this change. If the IC is replaced, pullups on the B side should be preserved.

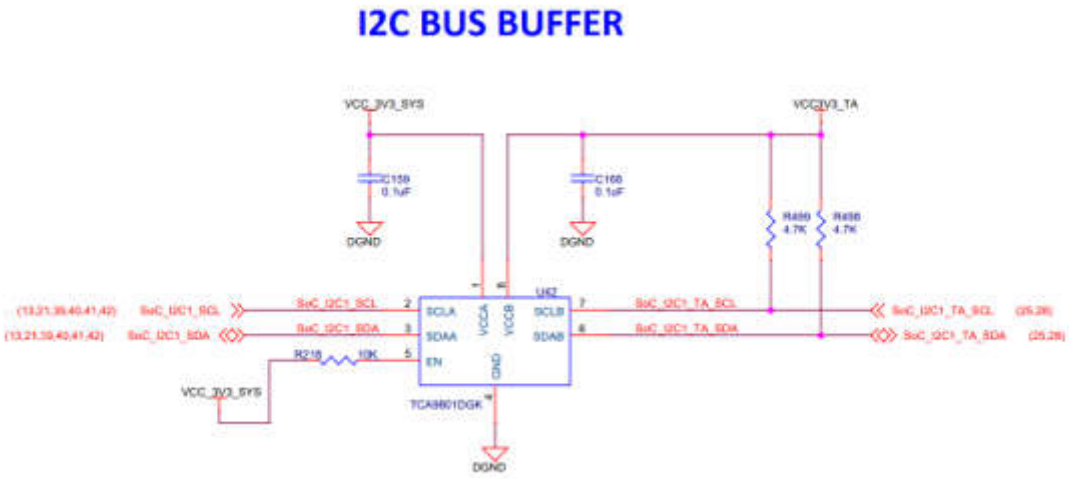


Figure 3-2. Schematic of I2C Buffer Section

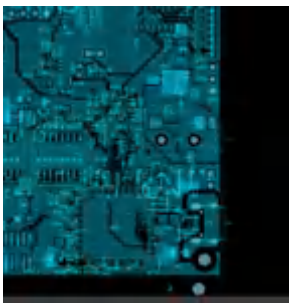


Figure 3-3. Location on AM62x SK E3 (Bottom Side)

3.2.12 Issue 12 - ODLI Display Touch Broken

Applicable EVM Revisions: E3, Rev A

Issue Description: When power on the EVM, the OLDI Display Touch function is not working.

Fix: To mitigate the issue, the resistor R684, Cap C509 and U105 power supply need to be changed to VCC_3V3_SYS, see Figure 3-4 for more information. Please follow Figure 3-5 for the rework information.

Copyright © 2026 Texas Instruments Incorporated

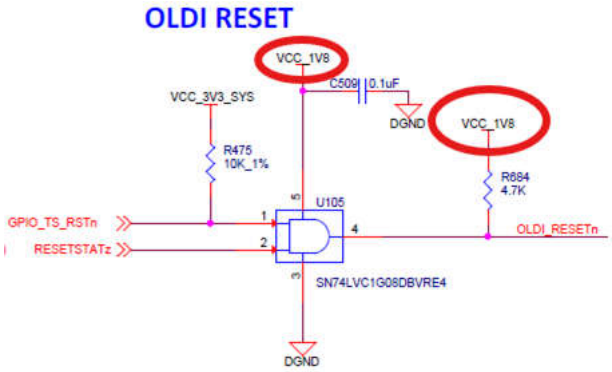


Figure 3-4. OLDI Display RESET Logic Circuit

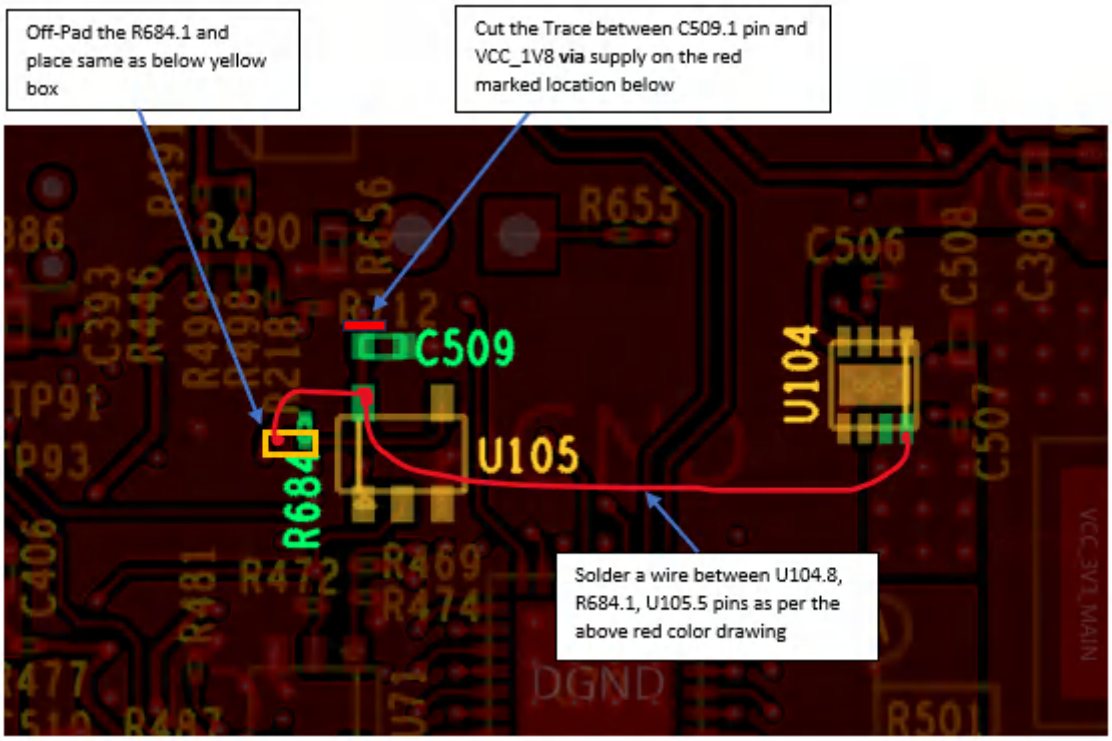


Figure 3-5. PCBA Bottom Image

3.3 Trademarks

Android™ is a trademark of Google LLC.
Sitara™ is a trademark of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
Wi-Fi® is a registered trademark of Wi-Fi Alliance.
Bluetooth® is a registered trademark of Bluetooth SIG.
Linux® is a registered trademark of Linus Torvalds.
All trademarks are the property of their respective owners.

The terms HDMI, HDMI High-Definition Multimedia Interface, HDMI trade dress, and the HDMI Logos are trademarks or registered trademarks of HDMI Licensing Administrator Inc.

Copyright © 2026 Texas Instruments Incorporated

4 Compliance and Certifications

4.1 EMC, EMI and ESD Compliance

Components installed on the product are sensitive to Electric Static Discharge (ESD). It is recommended this product be used in an ESD controlled enviorment. This may include a temperature and/or humidty controlled enviorment to limit the buildup of ESD. It is also recommended to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic enviorment as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

Regulatory Compliance

Hereby, Texas Instruments declares that the radio equipment, "AM62x Starter Kit for the Sitara Processors" is in compliance with directive 2014/53/EU.

The full text of the EU declaration of confirmity is available in the following website.

RF Exposure Information

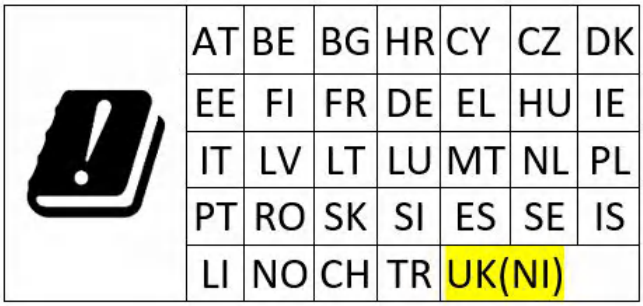
This device has been tested and meets applicable limits for Radio Frequency (RF) exposure. This equipment must be installed and operated to make sure a minimum of 20cm spacing to any person at all times.

EIRP Power

The maximum RF power transmitted in WLAN 2.4GHz band is 19dBm. The maximum RF power transmitted in WLAN 5GHz band is 19.4dBm (approximately 5150MHz-5350MHz) and 18.4dBm (approximately 5470MHz-5725MHz).

The maximum RF power transmitted in Bluetooth is 14dBm and Bluetooth Low Energy (BLE) is 8.9dBm.

The device is restricted for indoor use only within the 5.15 - 5.25GHz band. The following are the countries with restricted indoor use,



Waste Electrical and Electronic Equipment (WEEE)

This symbol means that according to local laws and regulations your product or the battery shall be disposed of separately from household waste. When this product reaches the end of life, take to a collection point designated by local authorities. Proper recycling of the product protects human health and the environment.

Copyright © 2026 Texas Instruments Incorporated

5 References

- Collaterals for reference during different phases of custom board design, self-review, and bring-up: https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1596731/faq-am625-am623-am620-q1-am625-q1-am625sip---collaterals-for-reference-during-different-phases-of-custom-board-design-self-review-and-bring-up
- Master list related to custom board design for all Sitara processor families; could be used along with other available design collaterals: https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1395812/faq-custom-board-hardware-design---master-complete-list-of-faqs-for-all-sitara-processor-am62x-am62ax-am62d-q1-am62px-am62l-am64x-am243x-am335x-families
- FAQs related to Processor collaterals, functioning, peripherals, interface, and Starter kit: https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1280721/faq-am625-am623-am620-q1-am625-q1-am625sip-custom-board-hardware-design---faqs-related-to-processor-collaterals-functioning-peripherals-interface-and-starter-kit
- Custom board schematics self-review: https://e2e.ti.com/support/processors-group/processors/f/processors-forum/1455706/faq-am625-am623-am620-q1-am625-q1-am625sip-design-recommendations-custom-board-hardware-design---custom-board-schematics-self-review

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from August 31, 2025 to February 28, 2026 (from Revision D (August 2025) to Revision E (February 2026)) **Page**

- Added SK-AM62B-P1 Rev B Top View image....5
- Added SK-AM62B-P1 Rev B Bottom View image....5
- Updated SK EVM PCB Design Revisions and Asssembly Variants table....66
- Added Issue 12 - ODLI Display Touch Broken....69
- Added References section....72

Copyright © 2026 Texas Instruments Incorporated

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025