**TLC5940 Programming Flow Chart v0.1**

9/29/05

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**DC Input Cycle**

- **Use DC EEPROM data?**
  - **YES**: Set DCPRG = High, Set DCPRG = Low.
  - **NO**: Set DC Correction Input (VPRG = High).

- **Set dot correction input (VPRG = High)?**
  - **YES**: Reset Counter = 0.
  - **NO**: Set VPRG = Low, Set FirstCycleFlag = 1.

- **Is VPRG = High?**
  - **YES**: Reset Data_Counter = 0.
  - **NO**: Set BLANK = Low (Turn LED's On).

- **Increment Counter (Counter = Counter +1)?**
  - **YES**: Set DC data to EEPROM?
    - **YES**: Set DCPRG = Low, Set VPRG = 22 Volts.
    - **NO**: Set VPRG = High.
  - **NO**: Pulse XLAT to latch in GS data.

- **Is GSCLK_Counter > 4095?**
  - **YES**: Set BLANK = High.
  - **NO**: Set BLANK to GS Data[Data_Counter].

- **FirstCycleFlag is set to high for first GS cycle after DC input cycle to add one additional SCLK pulse?**
  - **YES**: Pulse SCLK.
  - **NO**: Increment GSCLK_Counter (GSCLK_Counter + 1).

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**Grayscale Data input cycle combined with Grayscale PWM cycle**

- **Data input must be complete before GSCLK_Counter reaches 4096.**
  - Use the following equations to verify that the data input cycle will be completed before the PWM cycle is completed:
    - \( f_{SCLK} \) = minimum serial data frequency
    - \( f_{PWM} \) = frequency of complete Grayscale cycle
    - \( n \) = number of TLC5940 in series

\[
\text{for } f_{SCLK} = 1 \text{ or } \frac{1}{f_{PWM \_cycle}} \text{ use: } \frac{1}{192} \times \frac{1}{n} \\
\text{for } f_{SCLK} = 2 \text{ or } \frac{1}{f_{PWM \_cycle}} \text{ use: } \frac{1}{192} \times \frac{1}{n} \times \frac{1}{2}
\]

- **Is GSCLK_Counter > n*192-1?**
  - **YES**: Set BLANK = High.
  - **NO**: Set VPRG = Low, Set FirstCycleFlag = 1.

- **Pulse SCLK.**

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**LOD Check**

- **Set Data_Counter = 0.**

- **Is Data_Counter > n*192-1?**
  - **YES**: Set XLAT = High.
  - **NO**: Set BLANK = Low.

- **Increment Data.Counter (Data.Counter + 1).**

- **Pulse GSCLK.**

- **Set BLANK = High.**

---

**Check LOD Function?**

- **No**
  - **Set DCPRG = Low.**
  - **Set SCLK = Low.**
  - **Set VPRG = High.**
  - **Set XLAT = Low.**
  - **Set BLANK = High.**

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**After LOD Check Function the Status Information Data packet is available in the TLC5940 Shift Register. It may be read from the SOUT pin (of the last device in series) during the following GS input cycle.**

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**Data input must be complete before GSCLK_Counter reaches 4096.**

**Use the following equations to verify that the data input cycle will be completed before the PWM cycle is completed:**

\[
f_{SCLK} = \frac{1}{f_{PWM \_cycle}} \times \frac{1}{192} \times \frac{1}{n}
\]

- **n** = number of TLC5940 in series

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**Check LOD Function?**

- **Yes**

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**Use DC EEPROM data?**

- **YES**: Set DCPRG = Low.
- **NO**: Set DCPRG = Low.
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