In the previous post in this series, an equation was derived to describe the ratio of the Nth $R_{SET}$ resistor in Figure 1 below.

That equation, again, is as follows:

$$M_{RN} = M_{IN} \times \left[ \left( 1 - \sqrt{M_{IN}} \right) \times \left( 1 + \frac{V_{REF}}{K_n \times R_{SET1}} \right) + \sqrt{M_{IN}} \right]^{-1}$$

So, what can be said about Equation 1? First of all, for an $M_{IN}$ ratio of 1, the corresponding $M_{RN}$ ratio will also be 1, as would be expected. Second, for values of $M_{IN}$ greater than 1, notice that the two terms of the denominator of Equation 1 take on different signs. This means that depending on certain physical quantities involved ($K_n$, $R_{SET1}$, $V_{REF}$), $M_{RN}$ can become arbitrarily large. Thus, this region should be avoided, instead favoring the $M_{IN} \leq 1$ region; that is, by ensuring that $I_{SINKN}$ is less than or equal to $I_{SINK1}$ for all N.

Notice that allowing the denominator of the root term in Equation 1 (the $K_n$, $R_{SET1}$, $V_{REF}$ product) to become large results in a 1:1 linear relationship between $M_{RN}$ and $M_{IN}$ in the limit. Ultimately, the range of usable values that $V_{REF}$ and $R_{SET1}$ can take on to increase this product are going to be limited by the headroom required for the sink; though it is worth noting that for a fixed $I_{SINK1}$ value, increasing $V_{REF}$ requires an increase in $R_{SET1}$ as well. The final variable in the product, $K_n$, is the process transconductance of the MOSFET and can be maximized through device selection. The effect of $K_n$ on the linearity of the $M_{RN}$, $M_{IN}$ relationship (across five decades of $K_n$ values) is illustrated in Figure 2 below.
The process transconductance is so named due to its dependence on carrier mobility, oxide permittivity, and oxide thickness ($\mu$, $\varepsilon_{\text{ox}}$, $t_{\text{ox}}$)—all material and process properties:

$$K_n = k_n \frac{W}{L} = \mu_n x C_{\text{ox}} x \frac{W}{L} = \mu_n x \varepsilon_{\text{ox}} x \frac{W}{L}$$ \hspace{1cm} (2)

However, it is also dependent on the W/L ratio of the device, so in general larger devices will result in increasingly linear behavior in Equation 1. While most datasheets will not include $K_n$, it can be calculated from a common datasheet parameter, the forward transconductance, often listed as $g_m$ or $g_{FS}$:

$$g_m = g_{FS} = \frac{\partial I_{Dn}}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}} \left( \frac{1}{2} \times K_n x (V_{GS} - V_T)^2 \right) = K_n x (V_{GS} - V_T)$$ \hspace{1cm} (3)

Recall that the drain current equation for an NMOS operating in the saturation region is:

$$I_{Dn} = \frac{1}{2} x K_n x (V_{GS} - V_T)^2 x (1 + \lambda x V_{DS})$$ \hspace{1cm} (4)

Neglecting channel length modulation and rewriting the terms of Equation 4:

$$V_{GS} - V_T = \sqrt{\frac{2 x I_{Dn}}{K_n}}$$ \hspace{1cm} (5)

This result can be substituted into Equation 3 and ultimately solved for $K_n$:

$$g_m = K_n x \sqrt{\frac{2 x I_{Dn}}{K_n}} = \sqrt{2 x I_{Dn} x K_n}$$ \hspace{1cm} (6)

$$K_n = \frac{g_m^2}{2 x I_{Dn}}$$ \hspace{1cm} (7)
Thus, using Equation 7 it is possible to select optimal MOSFET devices for the bias network. Further, having obtained this value, it can be utilized in Equation 1 to calculate (more accurately) required $R_{\text{SETN}}$ resistor values to produce desired $I_{\text{SINKN}}$ currents.

It is important to note that Equation 1 tends to overestimate the $R_{\text{SETN}}$ resistance in the $M_{\text{IN}} \leq 1$ region; that is, it results in currents that are lower than the desired value. However, the ideal transistor case ($M_{\text{IN}}=M_{\text{RN}}$) will always underestimate the $R_{\text{SETN}}$ resistance in this region. Thus, calculating these two values will ultimately bound the exact value required. Consider two randomly chosen NFETs, N-channel MOSFET A and N-channel MOSFET B, as represented in Table 1, which have listed $g_{\text{FS}}$ values of 5.5A/V$^2$ (at $I_D=9A$) and 15A/V$^2$ (at $I_D=31A$), respectively. Suppose these are used to implement an $M_{\text{IN}}$ ratio of $\frac{1}{4}$; the corrected $R_{\text{SETN}}$ and $M_{\text{RN}}$ ratios are calculated using Equation 1 (along with some straightforward design values) in Table 1 below.

<table>
<thead>
<tr>
<th></th>
<th>$g_{\text{FS}}$ (S)</th>
<th>$I_D$ (A)</th>
<th>$K_N$ (A/V$^2$)</th>
<th>$V_{\text{REF}}$ (V)</th>
<th>$I_{\text{SINKI}}$ (A)</th>
<th>$I_{\text{SINKN}}$ (A)</th>
<th>$M_{\text{IN}}$</th>
<th>$R_{\text{SETI}}$ (Ω)</th>
<th>$R_{\text{SETN}}$ (Ω)</th>
<th>$M_{\text{RN}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-channel MOSFET A</td>
<td>5.5</td>
<td>9.0</td>
<td>1.68</td>
<td>1.25</td>
<td>1.0</td>
<td>0.25</td>
<td>0.25</td>
<td>1.25</td>
<td>7.18</td>
<td>0.174</td>
</tr>
<tr>
<td>N-channel MOSFET B</td>
<td>15.0</td>
<td>31.0</td>
<td>3.63</td>
<td>1.25</td>
<td>1.0</td>
<td>0.25</td>
<td>0.25</td>
<td>1.25</td>
<td>6.48</td>
<td>0.193</td>
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</table>

Using the conditions listed above for the N-channel MOSFET B, Figure 3 displays the results of a TINA-TI simulation of the circuit in Figure 1 implemented with $R_{\text{SETN}}$ values calculated from the ideal case (5Ω under these conditions), the corrected case (Equation 1), and the average of these two.

**Figure 3. Sink Current vs. Drain Voltage for Ideal, Corrected, and Average $R_{\text{SETN}}$ Values**

The results for simulations using both the N-channel MOSFET A and N-channel MOSFET B with the three $R_{\text{SETN}}$ values (as described above) are summarized along with corresponding percent error calculations in Table 2 below.
Ultimately a single feedback device can be used to derive a bias network of arbitrary values so long as certain conditions are met: particularly that the current in the primary feedback driven leg is the largest in the network, and the proper headroom is maintained in each leg. Thus, from a single voltage reference, a bias network is established.

<table>
<thead>
<tr>
<th></th>
<th>Ideal</th>
<th>Corrected</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R_{SETN}$ ($\Omega$)</td>
<td>$I_{SINKN}$ (A)</td>
<td>Error (%)</td>
</tr>
<tr>
<td>N-channel MOSFET A</td>
<td>5.0</td>
<td>0.304</td>
<td>21.6</td>
</tr>
<tr>
<td>N-channel MOSFET B</td>
<td>5.0</td>
<td>0.283</td>
<td>13.2</td>
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</table>
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