TEXAS INSTRUMENTS

User's Guide
DLPU100–May 2020

DLP3021-Q1 FPGA User's Guide

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1 Introduction

1.1 Purpose and Scope

This document defines the interfaces and functionality of the DLP® Automotive Dynamic Ground Projection FPGA design implemented for the Spartan 7 (XA7S15-1CPGA196Q). Some specifications are based on the Spartan 7 hardware blocks and non-design-specific constraints. In these cases, Xilinx Spartan 7 documentation should be considered the more accurate source of information if there are conflicting values.

In this application, the FPGA reads video data directly from a flash memory to display on the DMD. The FPGA also coordinates the illumination timing to coordinate with the displayed video content.

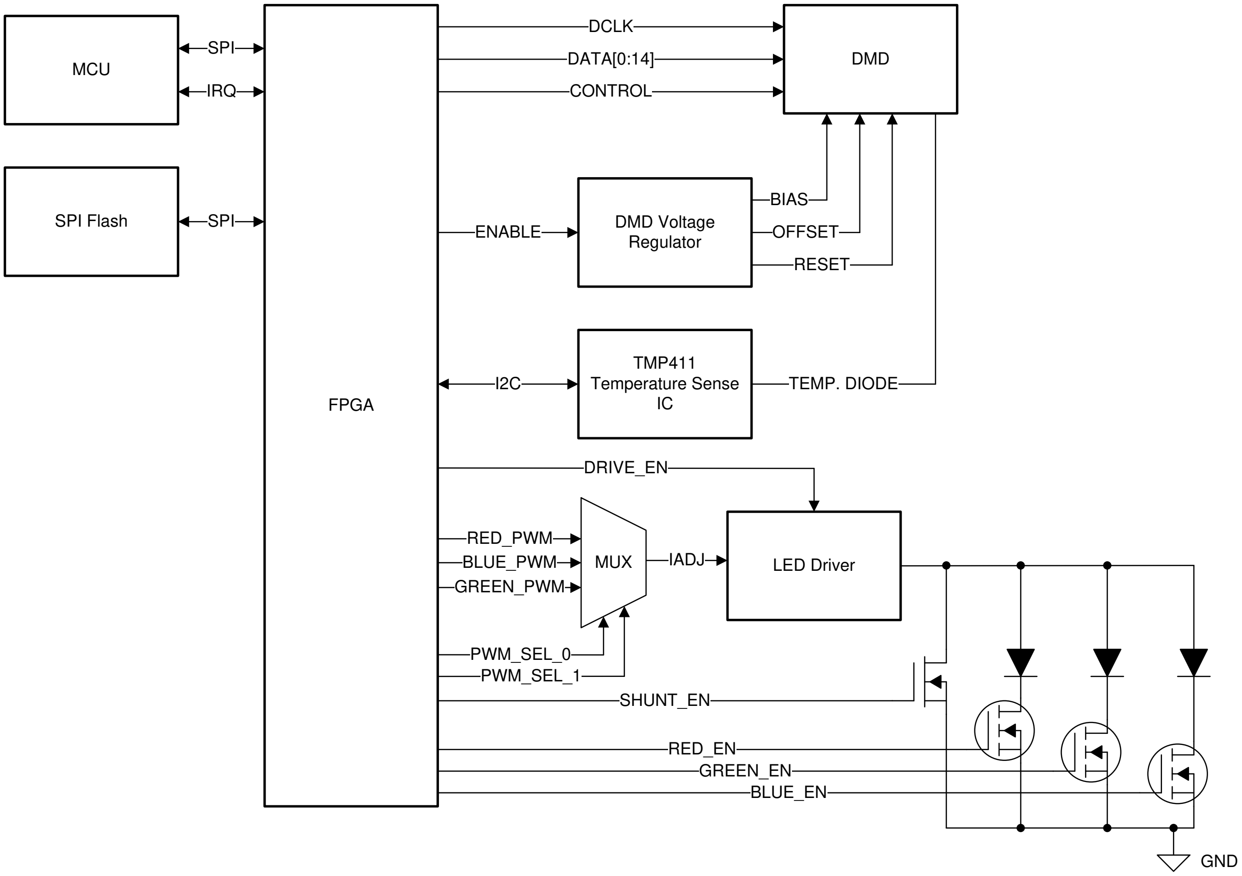

Figure 1. Dynamic Ground Projection Electronics Block Diagram

2 FPGA Pin Configuration and Functions

This section details the pin configuration of the FPGA and describes the function and I/O type of each pin.

2.1 DMD Interface

Table 1. DMD Interface Pin Descriptions

PIN		I/O		DESCRIPTION
NAME	NUMBER	POWER	TYPE	
D0	L14	1.8 V	O	DMD data pins
D1	L13	1.8 V	O	
D2	J14	1.8 V	O	
D3	K12	1.8 V	O	
D4	H12	1.8 V	O	
D5	K13	1.8 V	O	
D6	G14	1.8 V	O	
D7	H14	1.8 V	O	
D8	H13	1.8 V	O	
D9	G12	1.8 V	O	
D10	F14	1.8 V	O	
D11	E12	1.8 V	O	
D12	E13	1.8 V	O	
D13	F13	1.8 V	O	
D14	D14	1.8 V	O	
DCLK	B14	1.8 V	O	DMD data clock (DDR)
TRC	C14	1.8 V	O	DMD data toggle rate control
LOADB	C13	1.8 V	O	DMD data load signal (active low)
SAC BUS	M14	1.8 V	O	DMD SAC bus data
SAC CLK	N13	1.8 V	O	DMD SAC bus clock
DAD BUS	N14	1.8 V	O	DMD DAD bus data
DMD TDO	P12	1.8 V	I	DMD interface test data input. Signal connected to DMD JTAG interface to allow the verification of the interface. This signal connects to the DMD JTAG TDO. Includes an internal pullup resister. DMD JTAG functionality is not implemented in the FPGA design. This pin can be left disconnected.
DMD TDI	P10	1.8 V	O	DMD interface test data output. Signal connected to DMD JTAG interface to allow the verification of the interface. This signal connects to the DMD JTAG TDI. DMD JTAG functionality is not implemented in the FPGA design. This pin can be left disconnected.
DMD TCK	P11	1.8 V	O	DMD interface test data input. Signal connected to DMD JTAG interface to allow the verification of the interface. This signal connects to the DMD JTAG TDO. DMD JTAG functionality is not implemented in the FPGA design. This pin can be left disconnected.
DMD TMS	M10	1.8 V	O	DMD interface test mode. Signal connected to DMD JTAG interface to allow the verification of the interface. DMD JTAG functionality is not implemented in the FPGA design. This pin can be left disconnected.
RESET OEZ	P13	1.8 V	O	DMD DAD output enable (active low). A pullup to the 1.8-V rail for the DMD interface is needed to keep this signal inactive when tri-stated.
SCTRL	A13	1.8 V	O	DMD data serial control signal
RESET STROBE	M12	1.8 V	O	DMD DAD bus strobe

2.2 Light Control

Table 2. Light Control Pin Descriptions

PIN		I/O		DESCRIPTION
NAME	NUMBER	POWER	TYPE	
S_EN	A2	3.3 V	O	Shunt enable for illumination driver
R_EN	A3	3.3 V	O	Red select for illumination driver
G_EN	A4	3.3 V	O	Green select for illumination driver
B_EN	A5	3.3 V	O	Blue select for illumination driver
LED_EN	B6	3.3 V	O	Enable to illumination driver
PWM0	N2	3.3 V	O	Red PWM output
PWM1	N3	3.3 V	O	Green PWM output
PWM2	P3	3.3 V	O	Blue PWM output
PWM_SEL0	P4	3.3 V	O	Encoded PWM select
PWM_SEL1	N4	3.3 V	O	Encoded PWM select

2.3 Communication

Table 3. Communication Pin Descriptions

PIN		I/O		DESCRIPTION
NAME	NUMBER	POWER	TYPE	
HOST CLK	H3	3.3 V	I	SPI port (Slave) clock
HOST MOSI	H1	3.3 V	I	SPI port (Slave) data input
HOST MISO	J1	3.3 V	O	SPI port (Slave) data output
HOST CS	M1	3.3 V	I	SPI port (Slave) chip select
HOST IRQ	N1	3.3 V	O	Host interrupt
Temp SDA	L2	3.3 V	B	I^{2}C Port (Master) data An external pullup is required. Typical use of this I^{2}C port is communication with a temperature sensing device.
Temp SCL	K3	3.3 V	O	I2C Port (Master) clock An external pullup is required. Typical use of this I^{2}C port is communication with a temperature sensing device.
Flash DQ0	C10, F12	1.8 V	B	SPI port (Master) Control interface to flash device, transmit and receive data.
Flash DQ1	C11, E11	1.8 V	B	SPI port (Master) Control interface to flash device, transmit and receive data.
Flash DQ2	B11	1.8 V	B	SPI port (Master) Control interface to flash device, transmit and receive data.
Flash DQ3	A12	1.8 V	B	SPI port (Master) Control interface to flash device, transmit and receive data.
Flash DQ4	B12	1.8 V	B	SPI port (Master) Control interface to flash device, transmit and receive data.
Flash DQ5	A10	1.8 V	B	SPI port (Master) Control interface to flash device, transmit and receive data.

Table 3. Communication Pin Descriptions (continued)

Flash DQ6	A9	1.8 V	B	SPI port (Master) Control interface to flash device, transmit and receive data.
Flash DQ7	D11	1.8 V	B	SPI port (Master) Control interface to flash device, transmit and receive data.
Flash CS	C12, D13	1.8 V	O	SPI port (Master) Control interface to flash device, transmit and receive data. An external pullup resistor (<= 10 kΩ) is required.
Flash DQS	H11	1.8 V	I	Flash data strobe
Flash Clk	B9, A7	1.8 V	O	Flash clock

2.4 Support

Table 4. Support Pin Descriptions

PIN		I/O		DESCRIPTION
NAME	NUMBER	POWER	TYPE	
TSTPT_0	B1	3.3 V	O	Reserved for test outputs. These I/O should be left open or unconnected for normal operation in final product design.
TSTPT_1	B2	3.3 V	O	
TSTPT_2	C1	3.3 V	O	
TSTPT_3	C2	3.3 V	O	
TSTPT_4	D1	3.3 V	O	
TSTPT_5	D3	3.3 V	O	
TSTPT_6	E1	3.3 V	O	
TSTPT_7	E2	3.3 V	O	
Osc Input	G2	3.3 V	I	Reference clock input
Brownout Detect	F2	1.8 V	I (HSTL)	Brownout Detect
DMD Discharge En	M5	3.3 V	O	DMD Discharge enable
Clock Loopback	J11, J13			Reserved

2.5 FPGA Dedicated Pins

The following pins are hardware-dedicated on Spartan 7 FPGA. Refer to Xilinx documentation for primary guidelines. Descriptions in this table are recommendations for application-specific consideration.

Table 5. FPGA Dedicated Pin Descriptions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
PUDC	B10	I	Pullup during configuration Tie either directly (or through a 1-KΩ or less resistor) to GND. This will enable pullups on pins during configuration.
PROGRAMZ	N8	I	Asynchronous reset to configuration logic (active low)
INITZ	N7	B (open drain)	Indicates initialization of configuration memory (active low)
DONE	M9	B	Indicates successful completion of configuration (active high)
CFGBVS_0	N9	I	Tie to ground
DXN_0	J7	N/A	Temperature-sensing diode pin for FPGA. Tie to ground if not used.

Table 5. FPGA Dedicated Pin Descriptions (continued)

DXP_0	J8	N/A	Temperature-sensing diode pin for FPGA. Tie to ground if not used.
M0_0	L10	I	Configuration mode select Tie to 1.8 V.
M1_0	L8	I	Configuration mode select Tie to ground.
M2_0	L9	I	Configuration mode select Tie to ground.
HSTL VREF	C4, L3	REF	Voltage reference for HSTL 1.8-V input
TDO	M6	I	JTAG data output
TDI	M7	I	JTAG data input
TCK	A8	O	JTAG clock
TMS	L7	I	JTAG mode select

2.6 Power and Ground

Table 6. Power and Ground Pin Descriptions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
VCCAUX	D6, D8, D10	PWR	1.8-V power supply pins for auxiliary circuits
VCCBRAM	C7, C9	PWR	1.0-V power supply pins for the FPGA logic block RAM
VCCINT	E7, E9, F6, G9, H6, J9, K6, K8	PWR	0.9-V/1.0-V power supply pins for the internal core logic
VCCO_0	N6, P8	PWR	Power supply pins for bank 0
VCCO_14	F10, H10, K10	PWR	Power supply pins for bank 14
VCCO_34	E5, G5, J5	PWR	Power supply pins for bank 34
GND	A1, H5, H9, J2, J6, J10, J12, K4, K5, K7, K9, K14, L1, L5, L6, L11, M3, M8, M13, N5, N10, P1, P5, P6, P7, P9, P14, A6, A11, A14, B3, B8, B13, C6, C8, D2, D5, D7, D9, D12, E4, E6, E8, E10, E14, F1, F5, F9, F11, G3, G6, G10, G11, G13	RTN	Ground

2.7 Unused Pins

All NC pins have internal pullups and should be left unconnected in the schematic design.

Table 7. Unused Pins

PIN		TYPE
NAME	NUMBER	
IO_L2P_T0_34	B4	NC
IO_L3N_T0_DQS_34	B5	NC
IO_L3P_T0_DQS_34	C5	NC
IO_L5N_T0_34	B1	NC
IO_L5P_T0_34	B2	NC

Table 7. Unused Pins (continued)

PIN		TYPE
NAME	NUMBER	
IO_L6P_T0_34	D4	NC
IO_L7N_T1_34	C1	NC
IO_L7P_T1_34	C2	NC
IO_L8N_T1_34	D3	NC
IO_L8P_T1_34	E3	NC
IO_L9N_T1_DQS_34	D1	NC
IO_L9P_T1_DQS_34	E1	NC
IO_L10N_T1_34	E2	NC
IO_L11N_T1_SRCC_34	F3	NC
IO_L11P_T1_SRCC_34	F4	NC
IO_L12N_T1_MRCC_34	G1	NC
IO_L13N_T2_MRCC_34	G4	NC
IO_L13P_T2_MRCC_34	H4	NC
IO_L14N_T2_SRCC_34	H2	NC
IO_L16N_T2_34	J3	NC
IO_L16P_T2_34	J4	NC
IO_L17N_T2_34	K1	NC
IO_L18N_T2_34	K2	NC
IO_L19P_T3_34	L4	NC
IO_L20P_T3_34	M2	NC
IO_L23N_T3_34	P2	NC
IO_0_34	C3	NC
IO_L16P_T2_CSI_14	K11	NC
IO_L18P_T2_D28_14	L12	NC
IO_L23P_T3_D19_14	N11	NC
IO_L23N_T3_D18_14	N12	NC
IO_L24N_T3_D16_14	M11	NC
TCK_0	A8	NC
TDI_0	M7	NC
TDO_0	M6	NC
TMS_0	L7	NC
NC1	B7	NC
NC2	F7	NC
NC3	F8	NC
NC4	G7	NC
NC5	G8	NC
NC6	H7	NC
NC7	H8	NC

3 Specifications

3.1 Recommended Operating Conditions

Table 8. Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
VCCO_0	1.71	1.8	1.89	V
VCCO_14	1.71	1.8	1.89	V
VCCO_34	3.14	3.3	3.46	V
VCCAUX[1]	1.71	1.80	1.89	V
VCCBRAM[1]	0.95	1.00	1.05	V
VCCINT[1]	0.95	1.00	1.05	V

[1] Values are based on FPGA documentation available at the time of writing. Refer to the FPGA data sheet as the primary source specification.

3.2 FPGA Power Consumption

Table 9. FPGA Power Consumption Specification

COMPONENT	MIN	NOM	MAX	UNIT
1.0 volt rail			127	mW
1.8 volt rail			308	mW
3.3 volt rail			45	mW
FPGA total power		363	480	mW

3.3 Host SPI Interface Timing

Table 10. Host SPI Interface Timing

	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, HOST CLK (50% reference points)		5	MHz
t_{su}	Setup time – HOST MOSI valid before HOST CLK capture edge (50% reference points)	0		ns
t_h	Hold time – HOST MOSI valid before HOST CLK capture edge (50% reference points)	20		ns
t_{out}	Clock to data out – HOST MISO from HOST CLK transition edge (50% reference points)	40	60	ns

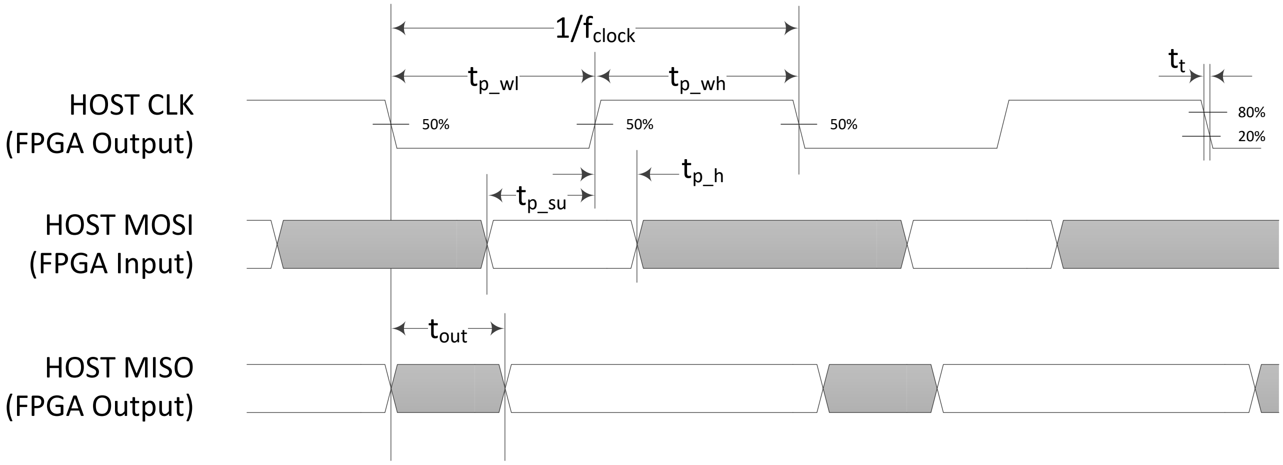

Figure 2. Host SPI Interface Timing Diagram

3.4 Power Supply and Reset Timing

3.4.1 Power-Up Timing

Table 11 specifies the configuration and initialization timing during FPGA start-up. After Host_irq gets set high, the FPGA is configured and ready to receive commands on the SPI interface. However, the first commands will not be executed for an additional 10 ms.

Table 11. Power-up Timing Specifications

		MIN	NOM	MAX	UNIT
t_{init} [1]	FPGA configuration initialization. 1.8-V power to DONE rising edge		230 ms		ms
t_{oez}	DONE rising edge to DMD RESET OEZ low		8.5		ms
t_{irq} [2]	RESET OEZ low to HOST IRQ high		1.15		ms
t_{ramp} [3]	Ramp time for each power supply: 1.0 V, 1.8 V, and 3.3 V (GND to 90% reference points)	0.2		50	ms

[1] INITZ should be pulled up to 1.8 V for shortest start-up time. If INITZ rising edge is delayed then the configuration will be delayed.

[2] HOST IRQ ready bit will indicate that the FPGA is ready for SPI communication from a host. This bit must be set in the interrupt enable mask in order for this condition to set HOST IRQ high at startup. The interrupt enable mask can be automatically configured on startup from the default configuration.

[3] Value is based on FPGA documentation available at the time of writing. Refer to FPGA data sheet as primary source specification.

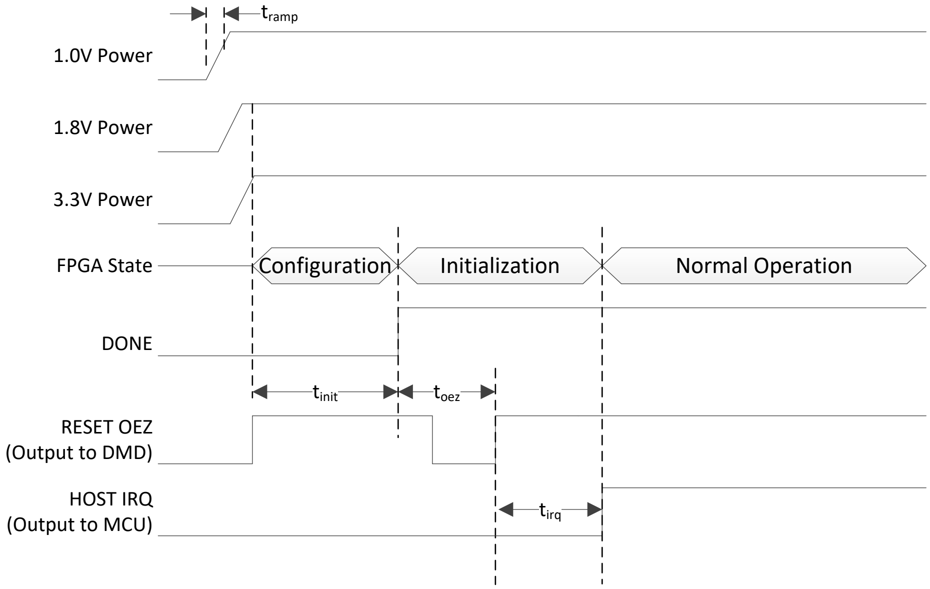

Figure 3. Power-up Timing Diagram

3.4.2 Power-Down Timing

Table 12. Power-down Timing Specifications

		MIN	NOM	MAX	UNIT
t_{park}	Time required for DMD to properly park[1]			500	µs
$t_{debounce}$	Time required for input voltage to remain below brownout detection threshold before park sequence begins.	100			µs

[1] DMD voltages (2.5 V, 1.8 V, 8.5 V, 16 V, –10 V) must remain valid until parked.

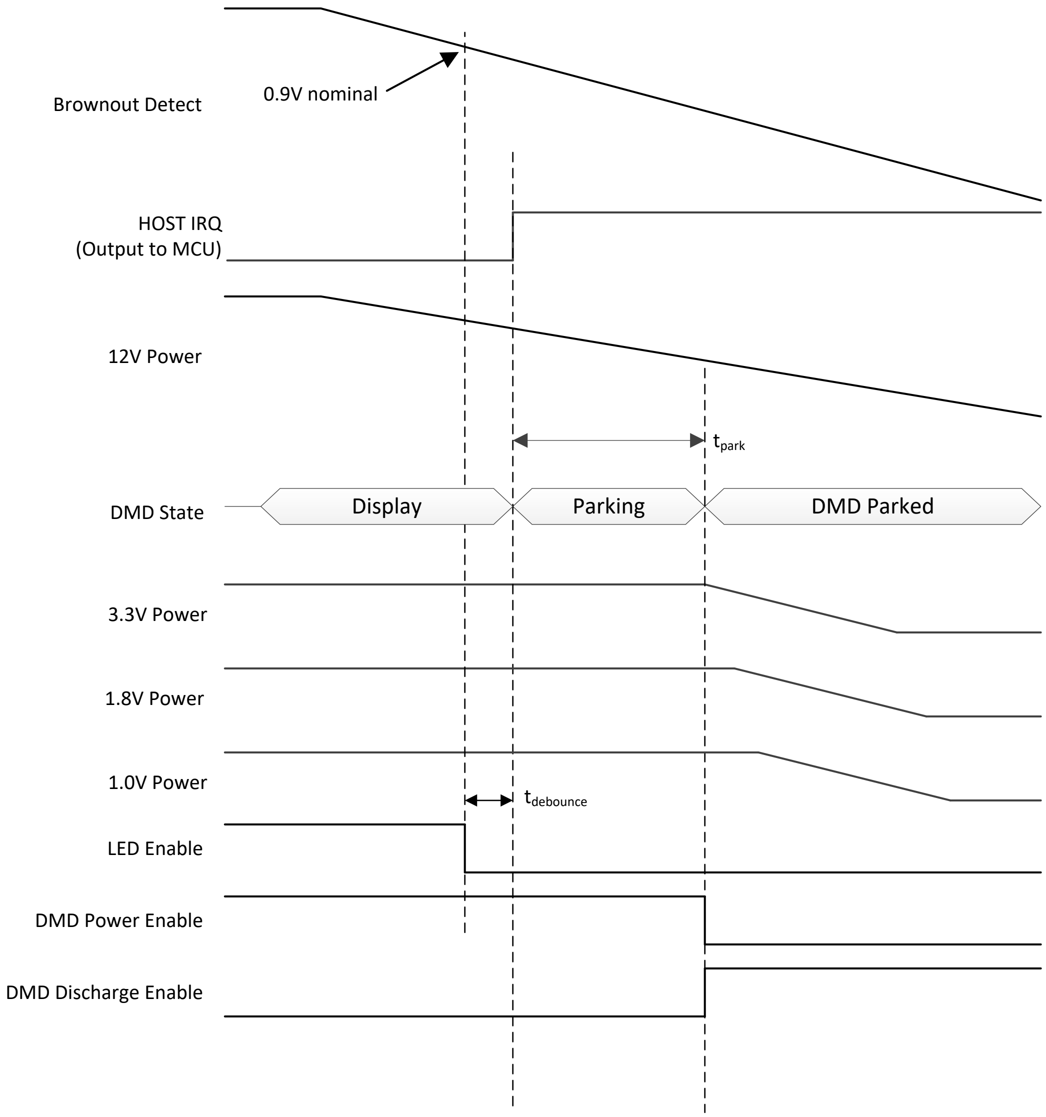

Figure 4. Power-down Timing Diagram

3.4.3 Brownout Detection

The DLP3021-Q1 FPGA configuration includes a brownout detection function to alert and properly shut down the system when the input voltage begins to fall. FPGA pin F2 is configured as the brownout detect pin. This pin is configured as a digital input that will trigger a brownout interrupt on a high-to-low transition. The input voltage should be divided down as an input to this pin so that the nominal voltage to the pin will not exceed 1.8 V. The brownout condition will occur when the input falls below a nominal voltage of 0.9 V. Once the brownout condition is triggered and the input voltage remains below the brownout voltage threshold for a 100-µs debounce period, the FPGA will automatically begin to park the DMD for proper power-down sequencing. After the brownout detection has parked the DMD, the system must be fully powered down before restarting, ensuring proper power-up sequencing upon restart.

Table 13. Brownout Detection Specifications

		MIN	NOM	MAX	UNIT
$V_{Brownout}$	Input voltage that triggers the brownout condition	0.8[1]	0.9[1]	1.0[1]	V

[1] Voltage valid for V_{REF} = 0.9 V.

3.5 DMD Interface Timing

Table 14. DMD Interface Timing Specifications

		MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, DCLK and SAC CLK		80	82	MHz
t_{wh}	Pulse width high, DCLK and SAC CLK (50% reference points)	5			ns
t_{wl}	Pulse width low, DCLK and SAC CLK (50% reference points)	5			ns
t_t	Transition time, all signals (20% to 80% reference points)	0.5		2.5	ns
t_{su}	Output setup time – D(14:0), SCTRL, LOADB and TRC relative to rising and falling edges of DCLK (50% reference points)	1.5			ns
t_h	Output hold time – D(14:0), SCTRL, LOADB and TRC relative to rising and falling edges of DCLK (50% reference points)	1.5			ns
t_{clkdat}	Clock to data output delay	–1.5		1.5	ns

3.6 Flash Memory Interface Timing

Table 15. Flash Memory Interface Timing

		MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency		130		MHz
t_{su}	Setup time	0.5			ns
t_{hd}	Hold time	0.6			ns
t_{out}	Output data valid time, relative to flash clock edge	–0.6		0.6	ns

3.7 Reference Clock Timing

This design utilizes MMCM blocks within the FPGA.

Table 16. Reference Clock Timing Specifications

		MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, Osc Input	39.5	40	40.5	MHz
t_{wh}	Pulse duration, Osc Input high[1]	25% of f_clock			
t_{wl}	Pulse duration, Osc Input low[1]	25% of f_clock			
t_{clkjit}	Clock period jitter, Osc Input[1]			50	ps

[1] Values are based on FPGA documentation available at the time of writing. Refer to the FPGA data sheet as primary source for MMCM specifications.

3.8 I²C Interface Timing

Table 17. I²C Interface Timing[1]

	Description	MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency		51		kHz

[1] Meets all I²C timing as specified by the I²C bus specification.

4 Feature Descriptions

4.1 Video Control

The FPGA is capable of reading video data from external flash memory and displaying it on the DMD. The video data must be converted and compressed by the DLP Composer tool before it is stored in flash memory. When the flash binary is generated, DLP Composer will specify the address locations of the video content within memory.

There are two sets of registers for two video configurations. This allows a seamless transition between two videos if desired. More than two videos can also be displayed seamlessly, but intervention is required from a host controller during playback to do so. One configuration can be modified while the other configuration is playing. A configuration is latched in when the video configuration begins playing. Interrupt signals can be used to notify a host controller when one configuration completes so that its values can be modified to another desired video while the next configuration plays.

During operation, the following registers can be used to configure the FPGA to display video content from flash memory:

- Video Frame Rate
- Video Start Address 1
- Video Configuration 1
- Video Start Address 2
- Video Configuration 2
- Video Control
- Video Status

The steps to display video are:

- **Write Video Frame Rate** – Set frame rate to match the DMD sequence.
- **Write Start Address X** – Set start address of the desired video in flash.
- **Write Configuration X** – Set number of frames in the video, and number of times to loop the video.
- **(Optional) Write Start Address Y** – Set start address of the second desired video in flash.
- **(Optional) Write Configuration Y** – Set number of frames in the next video, and number of times to loop the video.
- **Write Video Control** – Select playback options, and play video.

4.1.1 Video Options

The Video Control register is used to set up which video configuration is used and how to transition between the two video configurations.

Table 18. Video Control Register Configuration

VIDEO CONTROL REGISTER			RESULT
LOOP CONFIGURATIONS (BIT 4)	TOGGLE CONFIGURATIONS (BIT 5)	CONFIGURATION POINTER (BIT 3)	
0	0	0	Play config 1 once
0	0	1	Play config 2 once

Table 18. Video Control Register Configuration (continued)

0	1	0	Play (config 1, then config 2) once
0	1	1	Play (config 2, then config 1) once
1	0	0	Repeat config 1 continuously
1	0	1	Repeat config 2 continuously
1	1	0	Repeat (config 1, then config 2) continuously
1	1	1	Repeat (config 2, then config 1) continuously

If “Loop configurations” = 0, the end action is determined by “Auto-stop” (bit 2). The Auto-stop bit allows you to either fully turn off the video (1), or freeze on the last image in the video (0). If “Loop configurations” = 1, there is no end action because the video or videos will loop until stopped by command.

4.1.2 Example 1: Display a Static Image

The following steps can be used to display a single image on the DMD.

1. Write Video Frame Rate register.
   a. The clock count should match the length of the DMD sequence that is used.
2. Write Video Start Address 1 register.
   a. The start address should match the location of the image in flash memory. This can be found in the build log output from the DLP Composer™ tool.
3. Write Video Configuration 1 register.
   a. Frame count = 1
   b. Loop count = 1
4. Write Video Control register.
   a. Loop configurations = 1
   b. Toggle configurations = 0
   c. Configuration pointer = 0
   d. Play = 1
   e. Stop = 0

This configuration will display the image forever, or until the “stop” bit is set. Since the “loop configurations” bit is set, it will continually execute this configuration each time it completes.

4.1.3 Example 2: Display 1 Video Repeatedly

The following steps can be used to display a single video on the DMD repeatedly.

1. Write Video Frame Rate register.
   a. The clock count should match the length of the DMD sequence that is used.
2. Write Video Start Address 1 register.
   a. The start address should match the location of the video in flash memory. This can be found in the build log output from the DLP Composer™ tool.
3. Write Video Configuration 1 register.
   a. Frame count = number of frames in the video
   b. Loop count = 1
4. Write Video Control register.
   a. Loop configurations = 1
   b. Toggle configurations = 0
   c. Configurations pointer = 0
   d. Play = 1
   e. Stop = 0

This configuration will play the video and then continue to repeat it until the “stop” bit is set. Since the “loop configurations” bit is set, it will continue to execute this configuration each time it completes.

4.1.4 Example 3: Display Two Videos Then Stop

The following steps can be used to display two videos in a row and then stop displaying.

1. Write Video Frame Rate register.
   a. The clock count should match the length of the DMD sequence that is used.
2. Write Video Start Address 1 register.
   a. Start address should match the location of the video in flash memory.
3. Write Video Configuration 1 register.
   a. Frame count = number of frames in the video
   b. Loop count = 1
4. Write Video Start Address 2 register.
   a. The start address should match the location of the video in flash memory. This can be found in the build log output from the DLP Composer™ tool.
5. Write Video Configuration 2 register.
   a. Frame count = number of frames in the video
   b. Loop count = 1
6. Write Video Control register.
   a. Loop configurations = 0
   b. Toggle configurations = 1
   c. Configurations pointer = 0
   d. Play = 1
   e. Stop = 0
   f. Auto-stop = 1

This configuration will begin with Configuration 1 due to “configuration pointer” = 0. It will play one loop of this video, and then toggle to Configuration 2. After one loop of this second video, the display will auto-stop. This means that light will turn off and no image will be displayed.

4.1.5 Example 4: Display a vVdeo Once and Then Display an Image Forever

The following steps can be used to display a video followed by a static image.

1. Write Video Frame Rate register.
   a. The clock count should match the length of the DMD sequence that is used.
2. Write Video Start Address 1 register.
   a. The start address should match the location of the video in flash memory. This can be found in the build log output from the DLP Composer™ tool.
3. Write Video Configuration 1 register.
   a. Frame count = number of frames in the video
   b. Loop count = 1
4. 4. Write Video Start Address 2 register.
   a. The tart address should match the location of the video in flash memory. This can be found in the build log output from the DLP Composer™ tool.
5. Write Video Configuration 2 register.
   a. Frame count = 1
   b. Loop count = 1
6. Write Video Control register.
   a. Loop configurations = 0

   b. Toggle configurations = 1
   c. Configurations pointer = 0
   d. Play = 1
   e. Stop = 0
   f. Auto-stop = 0

This configuration will begin with Configuration 1 due to “configuration pointer” = 0. It will play one loop of the desired video, and then toggle to Configuration 2. In this case, configuration 2 is set to one frame (image). Because auto-stop is set to 0, the display will repeat the last frame of Configuration 2 instead of stopping. Configuration 2 is set to one frame for the desired image, and therefore, this image is displayed repeatedly until commanded to stop.

4.1.6 Example 5: Display 3+ Videos/Images Seamlessly

Displaying more than two videos without pause requires host intervention since there are only two sets of configuration registers. The HOST IRQ signal includes interrupt events that can help seamlessly transition to additional video content.

1. Write FPGA Interrupt Enable register “Video configuration complete” bit.
2. Read FPGA Interrupt Set register and Write FPGA Interrupt Clear register.
   a. Write 1 to the FPGA Interrupt Clear register to clear any active interrupts that can be holding the HOST IRQ signal high.
3. Write Video Frame Rate register.
   a. The clock count should match the length of the DMD sequence that is used.
4. Write Video Start Address 1 register.
   a. Start address should match the location of the first video in flash memory. This can be found in the build log output from the DLP Composer™ tool.
5. Write Video Configuration 1 register.
   a. Frame count = number of frames in the video
   b. Loop count = 1
6. Write Video Start Address 2 register.
   a. Start address should match the location of the second video in flash memory. This can be found in the build log output from the DLP Composer™ tool.
7. Write Video Configuration 2 register.
   a. Frame count = number of frames in the video
   b. Loop count = 1
8. Write Video Control register.
   a. Loop configurations = 0
   b. Toggle configurations = 1
   c. Configurations pointer = 0
   d. Play = 1
   e. Stop = 0
   f. Auto-stop = 0
9. Wait for HOST IRQ signal to interrupt host MCU and read FPGA Interrupt Set register to confirm that “video configuration complete” is a source of the interrupt.
10. Write Video Start Address 1 register.
    a. Start address should match the location of the **third** video in flash memory
11. Write Video Configuration 1 register.
    a. Frame count = number of frames in the video
    b. Loop count = 1
12. 12. Wait for HOST IRQ signal to interrupt host MCU and read FPGA Interrupt Set register to confirm

that “video configuration complete” is a source of the interrupt.

13. Write Video Control register.
    a. Loop configurations = 0
    b. Toggle configurations = 1
    c. Configurations pointer = 0
    d. Play = 1
    e. Stop = 0
    f. Auto-stop = 0

The first two videos are set up in Video Configuration 1 and 2. Then, the host MCU should wait until the “video configuration complete” interrupt triggers to indicate that the FPGA has swapped to displaying Configuration 2. After this occurs, the host MCU can modify Configuration 1 without affecting the displayed video content. It should then store the settings of the third video in Configuration1 before video 2 completes. After video 2 completes, the FPGA will loop back to configuration 1, which should now be set up to display video 3. This process can be repeated for any desired number of videos or images. After HOST IRQ interrupts to switch to the final video configuration, the Video Control register can be set to auto-stop after completion. When this register is written, do not set the play bit. If the play bit is set at this time, the video configuration would restart at the specified configuration pointer on the next video frame instead of waiting for the current configuration to complete.

4.2 Temperature Measurements

The FPGA can optionally read temperature measurements from an external TMP411 temperature sensor connected through I^2C. This allows reading the TMP411 local temperature and DMD remote temperature using a diode built into the DMD.

The FPGA reads the two temperatures from the TMP411 at approximately 8 Hz and stores the latest values in registers that can be read back by the host controller.

The temperature values in the FPGA are returned in the TMP411 12-bit format. The eight MSbs are an integer portion. The four LSBs are the fractional portion, which should be divided by 16 and added to the integer portion.

4.3 PWM Outputs

The FPGA has three PWM outputs which typically correspond to red, green, and blue illumination colors. The PWM duty cycles can be adjusted to set a reference voltage to an external illumination driver circuit as needed to balance colors and adjust output brightness.

A typical PWM circuit is shown in Figure 5. In this example, each PWM is low-pass filtered and the outputs connect to a 4:1 analog multiplexer. An optional resistor is shown in parallel with the capacitor for each filter to act as a voltage divider if needed to match the required illumination driver reference voltage range. The PWM output frequency is 40 kHz at maximum duty cycle.

The PWM_SELx signals can be used to select which output PWM is multiplexed to the illumination driver while the DMD sequence is executing. Table 19 describes the expected relationship between the PWM_SELx outputs and the multiplexer output.

Table 19. PWM Selection Configuration

PWM_SEL0	PWM_SEL1	MULTIPLEXER OUTPUT	TYPICAL SEQUENCE COLOR
0	0	None	None
0	1	PWM1	Red
1	0	PWM2	Green
1	1	PWM3	Blue

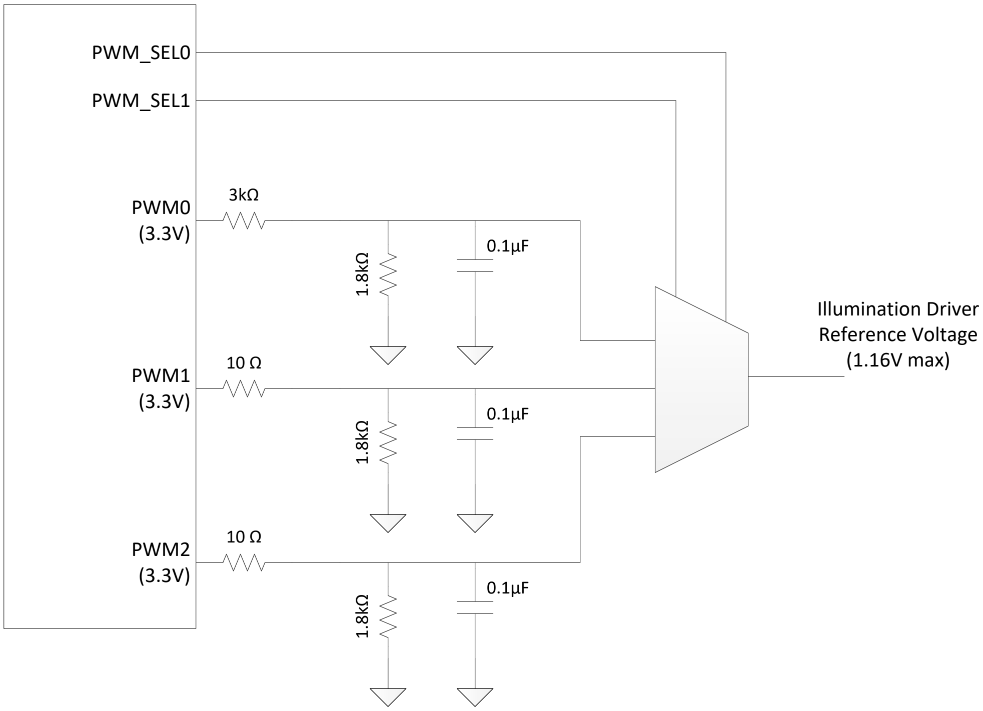

Figure 5. Typical PWM Circuit

4.4 Host IRQ Interrupt Signal

HOST IRQ is a level interrupt output from the FPGA. Multiple internal interrupt sources can trigger the external interrupt signal. If the signal is low, all of the enabled interrupt sources are cleared. If the signal is high, one of the sources is enabled and has been triggered. Three registers are used for handling the interrupt sources:

- FPGA Interrupt Enable
- FPGA Interrupt Set
- FPGA Interrupt Clear

FPGA Interrupt Enable is used to mask which interrupt sources will trigger the external HOST IRQ signal. For example, if the “video loop complete” enable bit is set to 1, then this source will set HOST IRQ high when triggered. If it is set to 0, then HOST IRQ will not be set high due to this source.

FPGA Interrupt Set is used to read back the currently set interrupts. Once an internal interrupt source is set, it will remain set until it is cleared by writing to the FPGA Interrupt Clear register.

FPGA Interrupt Clear is used to clear interrupt sources once handled. Typically, the FPGA Interrupt Set register can be directly written to the FPGA Interrupt Clear register in order to clear all currently active interrupts. Then, the host MCU can determine what action to take based on the interrupts that were set.

HOST IRQ will remain high if multiple enabled interrupt sources trigger.

4.5 Video and Image Compression

Videos and images stored in flash will be automatically compressed by the DLP Composer tool when the flash binary is built. These video frames and images will be formatted for display on the DLP3021-Q1 and compressed using a simplified run length encoding (RLE) for lossless compression. The maximum compression ratio is 16:1 for all black or all white images, but typical image compressibility is around 2:1 compression. The compression ratio will depend on the content, so the total number of images or length of video that can be stored will depend on the video content and size of the flash chip chosen. Typical storage capabilities are listed in Table 20.

Table 20. Typical Storage Capabilities

FLASH SIZE	APPROX. NUMBER OF IMAGES / FRAMES[1]	VIDEO LENGTH (s) 25-Hz Video
512 Mb	150	6
1 Gb	300	12
2 Gb	600	24

[1] Number of frames stored in flash will depend on compressibility of video and image data. Actual number of frames will depend on individual content.

5 Layout

For new board designs, ensure proper trace length matching of the FPGA to flash memory interface and DMD interface.

- DMD clock and data
  - This consists of the signals between the FPGA and the DMD synchronous with DCLK, including D0-D14, LOADB, SCTRL, RESET_STROBE, and TRC. The trace length matching requirement for these signals is ±50 mm.
  - DAD_BUS and SAC_BUS are syrchronous to SAC_CLK. These signals should be matched within 20 mm of each other but do not have matching requirements to the previous set of signals.
  - DMD_TMS, DMD_TDO, DMD_TDI are synchronous to DMD_TCK and should be matched within 20 mm of each other but do not have matching requirements to the previous set of signals.
- Flash clock and data
  - This consists of the eight data signals, clock, chip select, and data strobe between the FPGA and the flash memory. The trace length matching requirement for these signals is ±15 mm.

For FPGA specific layout guidelines, see the Xilinx *7 Series FPGAs PCB Design Guide*.

6 Host Command Protocol

6.1 SPI Specifications

Table 21. SPI Specifications

PARAMETER	VALUE
Clock Frequency	5 MHz
Mode (Clock Phase and Polarity)	0 (Data captured on rising edge, transitions on falling edge. Clock idle low.)
Bit order	Most significant bit first within a byte
Byte order	Least significant byte first
Chip select polarity	Active low

6.2 SPI Write Command

MOSI (master output, slave input):

Table 22. SPI MOSI Write Command Information

DATA	DESCRIPTION
CMD	Command byte. 0 for write
Address	2-byte register address
Data	4-byte register data
Checksum	Sum of all transmitted bytes including command, address, data. Discard overflow if sum exceeds 255.

MISO (Master input, slave output):

Table 23. SPI MISO Write Command Information

DATA	DESCRIPTION
CMD (ACK)	Echo of the received command from the master
Address (ACK)	Echo of the received address
Data	Echo of the received data

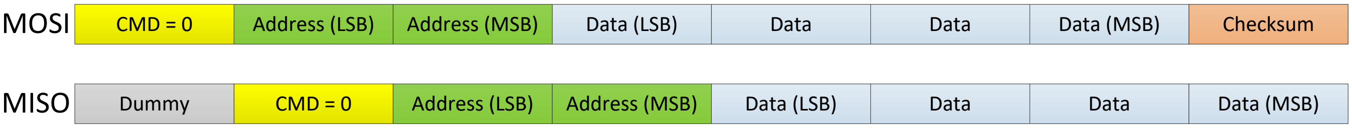

Figure 6. SPI Write Command Format

6.3 SPI Read Command

MOSI (Master output, slave input):

Table 24. SPI MOSI Read Command Information

DATA	DESCRIPTION
CMD	Command byte. 1 for read
Address	2-byte register address

MISO (Master input, slave output):

Table 25. SPI MISO Read Command Information

DATA	DESCRIPTION
CMD (ACK)	Echo of the received command from the master
Address (ACK)	Echo of the received address
Data	Data from requested register
Checksum	Sum of command, address, and data bytes. Does not include dummy byte.

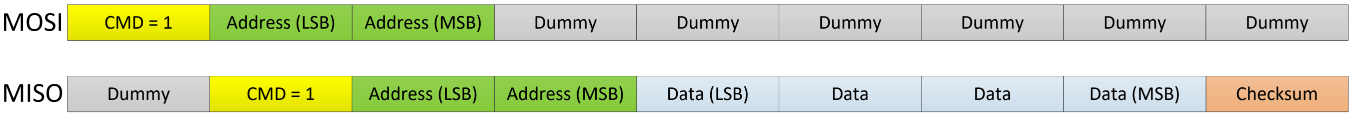

Figure 7. SPI Read Command Format

7 FPGA Register Definitions

This section defines the FPGA registers that can be accessed over SPI.

Table 26 lists the memory-mapped registers for the device registers. All register offset addresses not listed in Table 26 should be considered as reserved locations and the register contents should not be modified.

Table 26. FPGA SPI Registers

ADDRESS	ACRONYM	REGISTER NAME	SECTION
0x0	FPGA_INTERRUPT_CLEAR	FPA Interrupt Clear	Go
0x4	FPGA_INTERRUPT_SET	FPGA Interrupt set	Go
0x8	FPGA_INTERRUPT_ENABLE	FPGA Interrupt enable	Go
0xC	FPGA_MAIN_STATUS	TI internal use. Read/Write behavior is not defined.	

Table 26. FPGA SPI Registers (continued)

ADDRESS	ACRONYM	REGISTER NAME	SECTION
0x10	FPGA_VERSION	FPGA Version	Go
0x14	FPGA_CONTROL	TI internal use. Read/Write behavior is not defined.	
0x20	FMT_FLIP	Format flip	Go
0x24	FMT_CONTROL	TI internal use. Read/Write behavior is not defined.	
0x28	FMT_CMB_STATUS.	TI internal use. Read/Write behavior is not defined.	
0x2C	FMT_FRB_STATUS	TI internal use. Read/Write behavior is not defined.	
0x30	RSC_SW_DMD_UNPARK	TI internal use. Read/Write behavior is not defined.	
0x34	RSC_PARK_WAVEFORM_CTRL	TI internal use. Read/Write behavior is not defined.	
0x38	RSC_UNUSED	TI internal use. Read/Write behavior is not defined.	
0x3C	RSC_MISC_CONTROL	TI internal use. Read/Write behavior is not defined.	
0x40	RSC_SEQ_CONTROL	TI internal use. Read/Write behavior is not defined.	
0x44	RSC_SEQBUF_SELECT	Sequence Buffer Select	Go
0x50	PWM_CONTROL	PWM Control	Go
0x60	VCM_FRAME_RATE	Frame Rate	Go
0x64	VCM_START_ADDR1	Video 1 start address	Go
0x68	VCM_CONFIG1	Video configuration 1	Go
0x6C	VCM_START_ADDR2	Video 2 start address	Go
0x70	VCM_CONFIG2	Video configuration 2	Go
0x74	VCM_CONTROL	Video control	Go
0x78	VCM_STATUS	Video Status	Go
0x7C	VCM_SEQABORT	TI internal use. Read/Write behavior is not defined.	
0x80	VCM_TMSEL	TI internal use. Read/Write behavior is not defined.	
0x90	TMP_CTRL	Temperature control	Go
0x94	TMP_STATUS	Temperature Status	Go
0x98	TMP_REMOTE_TEMP	Remote Temperature Measurement	Go
0x9C	TMP_LOCAL_TEMP	Local Temperature Measurement	Go
0xDC	DESTOP_TIMEOUT_DEBUG_INFO_REG	TI internal use. Read/Write behavior is not defined.	
0xE0	DESTOP_MBOX0_SAPTR_REG	TI internal use. Read/Write behavior is not defined.	
0xE4	DESTOP_MBOX0_CTRL_REG	TI internal use. Read/Write behavior is not defined.	
0xF0	DESTOP_MBOX0_DATA_REG	TI internal use. Read/Write behavior is not defined.	
0x100	DESTOP_MBOX1_SAPTR_REG	TI internal use. Read/Write behavior is not defined.	
0x104	DESTOP_MBOX1_CTRL_REG	TI internal use. Read/Write behavior is not defined.	
0x110	DESTOP_MBOX1_DATA_REG	TI internal use. Read/Write behavior is not defined.	

Complex bit access types are encoded to fit into small table cells. Table 27 shows the codes that are used for access types in this section.

Table 27. Device Access Type Codes

ACCESS TYPE	CODE	DESCRIPTION
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1 FPGA_INTERRUPT_CLEAR Register (Address = 0x0) [reset = 0x0]

FPGA_INTERRUPT_CLEAR is shown in Table 28.

Return to Summary Table.

Write 1 to any bit to clear the interrupt event.

Table 28. FPGA_INTERRUPT_CLEAR Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-5	RESERVED	R	0x0	Reserved
4	VID_CONFIG_COMP_IRQ	R/W	0x0	Video configuration completed including all requested loops. This triggers once after all loops of a video complete. If both video configurations are requested to be used, it will trigger after each configuration completes.
3	VID_LOOP_COMP_IRQ	R/W	0x0	Video loop completed. If multiple loops of a video are requested, this interrupt triggers after each completed loop.
2	BROWNOUT_IRQ	R/W	0x0	Brownout detected
1	INIT_DONE_IRQ	R/W	0x0	Initialization done
0	RESERVED	R	0x0	Reserved

7.2 FPGA_INTERRUPT_SET Register (Address = 0x4) [reset = 0x0]

FPGA_INTERRUPT_SET is shown in Table 29.

Return to Summary Table.

Read the status of interrupt events.

Table 29. FPGA_INTERRUPT_SET Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-5	RESERVED	R	0x0	Reserved
4	VID_CONFIG_COMP_IRQ	R/W	0x0	Video configuration completed including all requested loops. This triggers once after all loops of a video complete. If both video configurations are requested to be used, it will trigger after each configuration completes.
3	VID_LOOP_COMP_IRQ	R/W	0x0	Video loop completed. If multiple loops of a video are requested, this interrupt triggers after each completed loop.
2	BROWNOUT_IRQ	R/W	0x0	Brownout detected
1	INIT_DONE_IRQ	R/W	0x0	Initialization done
0	RESERVED	R	0x0	Reserved

7.3 FPGA_INTERRUPT_ENABLE Register (Address = 0x8) [reset = 0x0]

FPGA_INTERRUPT_ENABLE is shown in Table 30.

Return to Summary Table.

Interrupt event mask. Write 1 to any bit to enable that interrupt event to set HOST IRQ high.

Table 30. FPGA_INTERRUPT_ENABLE Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-5	RESERVED	R	0x0	Reserved
4	VID_CONFIG_COMP_IRQ	R/W	0x0	Video configuration completed including all requested loops. This triggers once after all loops of a video complete. If both video configurations are requested to be used, it will trigger after each configuration completes.
3	VID_LOOP_COMP_IRQ	R/W	0x0	Video loop completed. If multiple loops of a video are requested, this interrupt triggers after each completed loop.
2	BROWNOUT_IRQ	R/W	0x0	Brownout detected

Table 30. FPGA_INTERRUPT_ENABLE Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
1	INIT_DONE_IRQ	R/W	0x0	Initialization done
0	RESERVED	R	0x0	Reserved

7.4 FPGA_VERSION Register (Address = 0x10) [reset = 0x10000000]

FPGA_VERSION is shown in Table 31.

Return to Summary Table.

FPGA Bitstream Version

Table 31. FPGA_VERSION Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-28	FPGA_BUILD_LEVEL	R	0x1	FPGA bitsream build level 0x0 = Debug release, not reproducible 0x1+ = Versioned release, can be reproduced
27-20	FPGA_VERSION_MINOR	R	0x0	FPGA Bitsream Minor Revision
19-12	FPGA_VERSION_MAJOR	R	0x0	FPGA Bitsream Major Revision
11-0	FPGA_BUILD_NUMBER	R	0x0	FPGA Bitstream build number

7.5 FMT_FLIP Register (Address = 0x20) [reset = 0x0]

FMT_FLIP is shown in Table 32.

Return to Summary Table.

DMD Flip control register

Table 32. FMT_FLIP Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-5	RESERVED	R	0x0	Reserved
4	FMT_CTL_DMDLFLIP	R/W	0x0	DMD Long Side Flip 0x0 = no long side flip 0x1 = Enable Image flip along DMD long side
3-1	RESERVED	R	0x0	Reserved
0	FMT_CTL_DMDSFLIP	R/W	0x0	DMD Short Side Flip 0x0 = no short side flip 0x1 = Enable Image flip along DMD short side

7.6 RSC_SEQBUF_SELECT Register (Address = 0x44) [reset = 0x0]

RSC_SEQBUF_SELECT is shown in Table 33.

Return to Summary Table.

Sequence Buffer Select

Table 33. RSC_SEQBUF_SELECT Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-1	RESERVED	R	0x0	Reserved
0	RSC_SEQBUF_SELECT	R/W	0x0	Sequence Buffer Select 0x0 = Select sequencer buffer 0 0x1 = Select sequencer buffer 1

7.7 PWM_CONTROL Register (Address = 0x50) [reset = 0x46419064]

PWM_CONTROL is shown in Table 34.

Return to Summary Table.

PWM Control Register

Table 34. PWM_CONTROL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31	RESERVED	R	0x0	Reserved
30	PWM_EN	R/W	0x1	PWM Enable
29-20	PWM_BPWM_DC	R/W	0x64	Blue PWM Duty Cycle
19-10	PWM_GPWM_DC	R/W	0x64	Green PWM Duty Cycle
9-0	PWM_RPWM_DC	R/W	0x64	Red PWM Duty Cycle

7.8 VCM_FRAME_RATE Register (Address = 0x60) [reset = 0x00186A00]

VCM_FRAME_RATE is shown in Table 35.

Return to Summary Table.

Frame Rate Selection

Table 35. VCM_FRAME_RATE Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-24	RESERVED	R	0x0	Reserved
23-0	VCM_FRAME_RATE	R/W	0x00186A00	Video frame time in 40-MHz clock counts. Value should match sequence time 25 Hz = 1600000 60 Hz = 666666

7.9 VCM_START_ADDR1 Register (Address = 0x64) [reset = 0x0]

VCM_START_ADDR1 is shown in Table 36.

Return to Summary Table.

Video 1 start address

Table 36. VCM_START_ADDR1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-0	START_ADDR1	R/W	0x0	Video 1 start address in flash

7.10 VCM_CONFIG1 Register (Address = 0x68) [reset = 0x1001]

VCM_CONFIG1 is shown in Table 37.

Return to Summary Table.

Video configuration 1

Table 37. VCM_CONFIG1 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-24	RESERVED	R	0x0	Reserved
23-12	LOOP_CNT1	R/W	0x1	Number of times to loop video 1 0x0 = invalid 0x1 = 1 loop 0x2 = 2 loop

Table 37. VCM_CONFIG1 Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
11-0	FRAME_CNT1	R/W	0x1	Number of frames in video 1 0x0 = invalid 0x1 = 1 frame 0x2 = 2 frames

7.11 VCM_START_ADDR2 Register (Address = 0x6C) [reset = 0x0]

VCM_START_ADDR2 is shown in Table 38.

Return to Summary Table.

Video 2 start address

Table 38. VCM_START_ADDR2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-0	START_ADDR2	R/W	0x0	Video 2 start address in flash

7.12 VCM_CONFIG2 Register (Address = 0x70) [reset = 0x1001]

VCM_CONFIG2 is shown in Table 39.

Return to Summary Table.

Video configuration 2

Table 39. VCM_CONFIG2 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-24	RESERVED	R	0x0	Reserved
23-12	LOOP_CNT2	R/W	0x1	Number of times to loop video 2 0x0 = invalid 0x1 = 1 loop 0x2 = 2 loop
11-0	FRAME_CNT2	R/W	0x1	Number of frames in video 2 0x0 = invalid 0x1 = 1 frame 0x2 = 2 frames

7.13 VCM_CONTROL Register (Address = 0x74) [reset = 0x10]

VCM_CONTROL is shown in Table 40.

Return to Summary Table.

Table 40. VCM_CONTROL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-6	RESERVED	R	0x0	Reserved
5	VCM_TOGGLE_CONFIGS	R/W	0x0	Video buffer toggle selection 0x0 = Playback will only use the selected buffer 0x1 = Playback will use both buffers
4	VCM_LOOP_CONFIGS	R/W	0x1	Loop configuration 0x1 = Repeat configuration
3	VCM_BUF_PTR	R/W	0x0	Video Configuration pointer 0x0 = Play Video 1 0x1 = Play Video 2

Table 40. VCM_CONTROL Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
2	VCM_AUTOSTOP	R/W	0x0	Auto-stop after playback 0x0 = Repeat last frame of video playback until commanded otherwise 0x1 = Stop and park the DMD after video(s) complete
1	VCM_STOP	R/W	0x0	Stop Video / Park DMD 0x0 = Allow Video Play 0x1 = Stop video playback and park DMD. Must be set to 0 to play video
0	VCM_PLAY	R/W	0x0	Play video. Self-clearing

7.14 VCM_STATUS Register (Address = 0x78) [reset = 0x0]

VCM_STATUS is shown in Table 41.

Return to Summary Table.

Video Status Register

Table 41. VCM_STATUS Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-3	RESERVED	R	0x0	Reserved
2	VCM_SEQABORT_ERR	R	0x0	Sequence abort error Clears on video play
1	VCM_CURR_CONFIG_PTR	R	0x0	Current video configuration pointer
0	VCM_VID_IN_PROGRESS	R	0x0	Video in progress when set

7.15 TMP_CTRL Register (Address = 0x90) [reset = 0x00010003]

TMP_CTRL is shown in Table 42.

Return to Summary Table.

Temperature control register

Table 42. TMP_CTRL Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-17	RESERVED	R	0x0	Reserved
16	TMP_CTRLEN	R/W	0x1	Temperature function enable 0x0 = Disable 0x1 = Enable
15-8	TMP_I2CSLADDR	R/W	0x0	TMP411 I^{2}C slave address (see TMP411 datasheet for details)
7-0	TMP_NFACTOR	R/W	0x3	N factor to compensate TMP411 measurement (see TMP411 datasheet for details)

7.16 TMP_STATUS Register (Address = 0x94) [reset = 0x0]

TMP_STATUS is shown in Table 43.

Return to Summary Table.

Temperature Status Register

Table 43. TMP_STATUS Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-2	RESERVED	R	0x0	Reserved
1	TMP_VALID	R	0x0	Temperature Status Valid 0x0 = I^{2}C temperature read failed or not yet completed 0x1 = I^{2}C temp read succeded
0	TMP_PASS	R	0x0	Temperature Status Pass 0x0 = Select sequencer buffer 0 0x1 = Select sequencer buffer 1

7.17 TMP_REMOTE_TEMP Register (Address = 0x98) [reset = 0x0]

TMP_REMOTE_TEMP is shown in Table 44.

Return to Summary Table.

DMD Temperature Measurement

Table 44. TMP_REMOTE_TEMP Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-28	RESERVED	R	0x0	Reserved
27-16	TMP_REMOTE_FILTERED	R	0x0	TMP411 Remote temperature filtered measurement DMD temperature measurement after filtering
15-12	RESERVED	R	0x0	Reserved
11-0	TMP_REMOTE_RAW	R	0x0	TMP411 Remote temperature raw measurement Single DMD temperature measurement

7.18 TMP_LOCAL_TEMP Register (Address = 0x9C) [reset = 0x0]

TMP_LOCAL_TEMP is shown in Table 45.

Return to Summary Table.

TMP411 Temperature Measurement

Table 45. TMP_LOCAL_TEMP Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
31-28	RESERVED	R	0x0	Reserved
27-16	TMP_LOCAL_FILTERED	R	0x0	TMP411 Local temperature filtered measurement TMP411 temperature measurement after filtering
15-12	RESERVED	R	0x0	Reserved
11-0	TMP_LOCAL_RAW	R	0x0	TMP411 Local temperature raw measurement Single temperature measurement

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265